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Thermal Driven Test Access Routing in Hyper-interconnected Three-Dimensional System-on-Chip

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Abstract

The rapid emergence of three dimensional integration using a "Through-Silicon-Via" (TSV) process calls for research activities on testing and design for testability. Compared to the traditional 2D designs, the 3D-SoC poses great challenges in testing, such as three dimensional placement of cores and test resources, severe chip overheating due to the nonuniform distribution of power density in 3D, and 3D test access routing. In this work, we propose an effective and efficient test access routing and resource partitioning scheme to tackle the 3D-SoC test challenges. We develop a simple and scalable 3D-SoC test thermal model for thermal compatibility analysis. We construct a 3-D test access architecture for efficient test access routing, and partition the limited test resources to facilitate a thermal-aware test schedule while minimizing the overall test time. The promising results are demonstrated by extensive simulation on ITC'02 benchmark SoCs.

Keywords

Test access architecture design; thermal-aware testing; through-silicon via; 3D-SoC modular test; test optimization.

I. Introduction

Three dimensional circuit structure using a "Through-Silicon-Via" (TSV) process is rapidly emerging recently, which enables the integration of logics, memory, processors, radio frequency/ photonic devices and microelectromechanical systems on a single chip, namely 3D-SoC. 3D integration is characterized by bonding and very high density vertical inter-chip wiring of stacked thinned device substrates with freely positioned TSVs by using standard silicon wafer processes [1]. In particular, the TSV technology interconnects stacked devices on wafer or die level for high-performance communication, namely hyper interconnection. An example schematic of a 3D IC is shown in Figure 1 [2], where TSVs provide hyper interconnection for three tiers integration. The TSV technology has various potential benefits. Firstly, the short vertical connection (tens of μm) significantly reduces the average wire length of block-to-block interconnects by stacking functional cores vertically. Second, high density vertical connection ($10^4 - 10^6$ per cm^2) allow implanting complex multi-chip system entirely within silicon. Thus, the 3D-SoC delivers higher density, faster interconnection and heterogeneous integration.

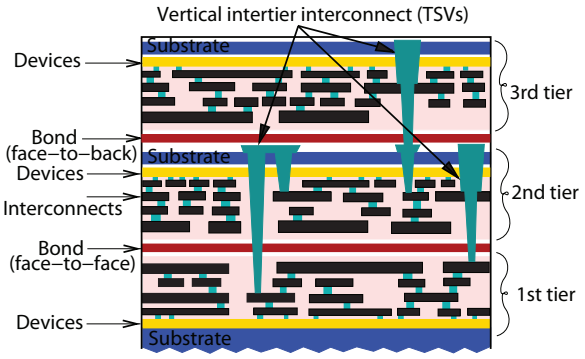

Figure 1. Schematic illustration of TSV.

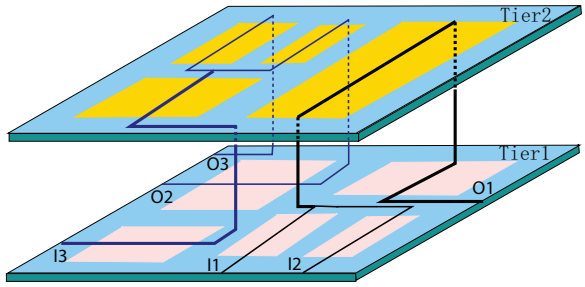

Figure 2. The illustration of a test access architecture for 3D-SoC.

With significant research carried out in 3D integration, 3D designers face three major challenges, namely, thermal management, test and design for testability, and EDA enablement. Among them, the research on 3D SoC testing is still in its infancy. Wu et al. have made the initial attempts in scan chain ordering and TAM design for testing 3D ICs by taking into account the 3D TSV effects (such as the length of TSVs and the number of TSVs) and 3D core placement for earlier 3D technologies [3], [4]. With the rapid advance in 3D integration technologies, adequate research need to be carried out

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to define and tackle the 3D testing challenges and to incorporate 3D integration characteristics (specified by bonding and stacking) into testing process. It becomes essential to study the tools and methodologies to facilitate cost effective 3D-SoC testing.

Modularity based 3D integration facilitates design reuse. And intuitively, modular test approach is attractive with the support of an efficient test access architecture which isolates the embedded modules while providing test access to them. Under the specially designed DFT structure, the test access mechanism (TAM) transports test stimuli from test data source to the core-under-test (CUT) and test responses from CUT to test data sink. The test wrappers interface the CUT to the TAM wires and switch a core between functional mode and test modes. The TAM design and wrapper configuration have great impact on concurrent testing of embedded modules and consequently the overall SoC testing time under various test constraints. Extensive research has been carried out in TAM design and wrapper configuration for planar (2D) SoC testing with the consideration of various constraints such as pin count, power and thermal limit [5], [6], [7], [8], [9], [10], [11].

In 3D-SoC, a three dimensional test access architecture need to be constructed where the test access paths can be routed vertically by using TSVs. A hyperthetical 3D test access architecture is illustrated in Figure 2. Parallel flexible width test buses are routed from input pins to output pins to form the TAMs. A bus may connects several modular cores spanning on multiple tiers. The cores on the same bus are tested in sequence while the cores on different buses are tested in parallel. Buses can merge and fork to provide the best sharing of the TAMs and to accommodate the flexible wrapper interfacing. Compared to the 2D designs, the 3D-SoC poses great challenges in testing: (1) Extremely limited test resources such as pin count, TSV density, and routing area, are shared among more and more cores in three dimensional placement. Specially, the pins are only located at the bottom tier, and the test access to the upper tiers are through the TSVs. (2) Thermal management becomes even more critical due to the increased power density and the nonuniform distribution of power density in 3D. It's a key design issue to prevent chip-wide overheating during the test mode. The spatial and temporal non-uniform thermal behavior of the cores during testing should be properly modeled and utilized during concurrent test scheduling. (3) As the cores are deeply embedded and spread among multiple tiers, the three dimensional test access architecture faces a more complex and comprehensive configuration environment.

In this work, we propose an effective and efficient test access routing and resource partitioning scheme to tackle the above 3D-SoC test challenges. The solution is delivered in a way that constructs a thermal-safe test access architecture for efficient test access routing and partitions the limited test resources to facilitate an efficient test schedule while minimizing the test cost in terms of test time, routing cost and test bandwidth. In particular, we prevent the creation of hotspots during testing by embedding thermal compatibility into test scheduling. We develop a simple and scalable thermal model based on the spatial allocation of the cores to preliminarily derive the thermal compatibility information which is used to orient the scheduling of concurrent tests in temporal domain. In this way we could limit the time-consuming thermal simulation to the minimum without sacrificing test concurrency.

The rest of the paper is organized as follows. In Sec. II, we discuss the related work on SoC testing and the motivation behind our work. The thermal aware 3D-SoC testing problem is formulated in Sec. III and our proposed approach is presented in Sec. IV. Extensive simulation results are provided in Sec. V to demonstrate the effectiveness and efficiency of the proposed heuristic algorithm. Finally we conclude this paper.

II. Prior Work

Core wrapper design, TAM design and test scheduling have been very active areas of planar SoC testing research. Goel et. al presented a genetic algorithm based heuristic for optimal wire allocation and core assignment with test-rail/ test-bus based TAMs [5]. A wrapper/TAM co-optimization method was described in [7] for efficient test planning. A graph-theoretical approach for power constrained test scheduling was discussed in [8]. More work focused on minimizing the SoC testing time under the total TAM width and maximum power constraints, can be found in the literature. Recently, chip overheating during testing has drawn great attention and several research efforts have been conducted to prevent hotspots during testing. In [10], the authors proved that test scheduling under maximum power constraints doesn't prevent chip overheating and proposed a thermal resistance based model to reduce thermal simulations. The idea of combining thermal compatibility information derived using clique identification in test scheduling was presented in [17]. A test set partitioning and interleaving method was proposed in [16] where cooling periods was introduced if the temperature of a core under test exceeds a specified limit. Yu et. al proposed a TAM/ wrapper co-design methodology that targets both test time minimization and prevention of hotspots [12].

There are very limited work on 3D-SoC testing. The first work on TAM design for 3D-SoC was presented in [4]. An integer linear programming (ILP) model was designed to divide the total TAM wires into several test buses with fixed width and to assign modular cores to test buses so as to minimize the overall test time under the constraint of TSV count utilized by TAMs. The recent advance in 3D process integration reveals the potential of high TSV interconnection density in the

range of 10^4 to 10^6 per square centimeter [13]. As a result, TSV count becomes a very loose constraint for TAM routing. Meanwhile, the test concurrency is restricted by the fixed width test bus architecture used for parallel test data transportation. More importantly, this work does not account for the possibility of hotspot creation during concurrent testing which however becomes even more severe due to nonuniform distribution of power density in 3D-SoC. High computation complexity of ILP based method also motivates the development of efficient heuristics to resolve the testing problem for large and complex 3D-SoC devices.

A flexible TAM architecture is designed in this paper which maximizes test concurrency by efficiently utilizing high density vertical interconnection while tackling thermal safety issue by incorporating thermal compatibility into scheduling.

III. Problem Formulation

The problem of 3D-SoC test framework design under thermal constraints (P_{3DTF}) can be described as follows. Given a three dimensional System-on-Chip with core test profile (including input/ output terminals, the number of scan chains and their lengths, test pattern count, test power dissipation, temperature constraint, and core placement) and tier details (such as the maximum number of TAM wires allowed on each tier restricted by area cost, a list of cores placed on each tier, and the vertical distance between each tier), determine (1) the test wrapper design for each core, (2) the routing of TAM across and through the tiers, and (3) a thermal safe test schedule for concurrent modular testing such that the overall testing time is minimized and the core temperature never exceeds the specified limit at any point during testing.

Table I
Test parameters for benchmark *3*DSoC_Test01

num	N_{in}	N_{out}	L_{sc_j}	$Test\_pattern\_count$	$Test\_power(\mu W)$	$Center\_point$
1	62	152	150 150 150 150 38	236	150	(200, 390)
2	77	150	150 150 150 84	126	150	(600, 362)
3	35	320	864 864	16	320	(400, 790)
4	28	106	150 150 150 150 150 150 150 150 150 150 136	99	850	(1200, 915)
5	38	304	150 150 150 150 150 150 150 150 150 76	136	864	(1150, 562)
6	62	152	150 150 150 150 38	236	150	(200, 390)
7	35	320	864 864	16	320	(1000, 400)
8	38	304	150 150 150 150 150 150 150 150 150 76	136	854	(350, 962)

Thermal become a more critical issue to 3D-SoC due to its nonuniform spatial and temporal power distribution. Concurrent testing of cores spanning across multiple vertically stacked tiers has a great impact on power density variation. Such a largely varied power density could easily lead to chip overheating. In order to study the impact of vertical stacking on power distribution and consequently the chip temperature variation, we experiment on a simple ITC'02 benchmark d695. Without loss of generality, we create two SoC configurations under two dimensional and three dimensional integration respectively, and generate several test schedules under certain power constraint. The maximum temperatures for the 2D and 3D chips are measured using HotSpot simulator. Assuming the test power dissipations for the same core in both configurations are identical. The total test power and the maximum temperature of these schedules are shown in Figure 3. As we can see that the maximum temperature is not solely dependent on the power dissipation, but rather the power distribution. Even when the total power dissipation is the same for running the same schedule under the two configurations, the maximum temperature of a 3D-SoC is much higher than that of a 2D-SoC. This is caused by higher power density and lesser thermal conductivity of heat dissipation paths. Ignoring these effects can simply lead to chip overheating during concurrent testing of cores. Thus, it is essential to investigate thermal-safe test scheduling under 3D integration scenario.

In order to efficiently avoid hot spots without sacrificing test concurrency, we need to validate the generated test schedule through thermal simulation. In order to efficiently study the concurrent testing problem under thermal constraint, we introduce thermal compatibility here. If two cores can be tested in parallel without violating the thermal limit, we say these two cores are *thermal compatible*. The frequency of a core's thermal compatibility with any other cores is named as the *thermal compatibility level*. The higher the frequency, the higher the compatibility level, and consequently the higher the scheduling flexibility. However, the analysis of thermal compatibility by running thermal simulation based on HotSpot [14] is very time consuming. Hence, thermal simulation should be performed only when the concurrently scheduled cores being checked are very likely thermal compatible. Simple models should be set up to preliminarily study the thermal compatibility before running the thermal simulation. Based on the observation that the temperature of a core is dependent on its own test power dissipation and that of its neighboring cores. Hotspots may be created if multiple power sources appear in the close vicinity. In this work, we develop a simple thermal model based on inter-core distance to gain a preliminary understanding of thermal compatibility.

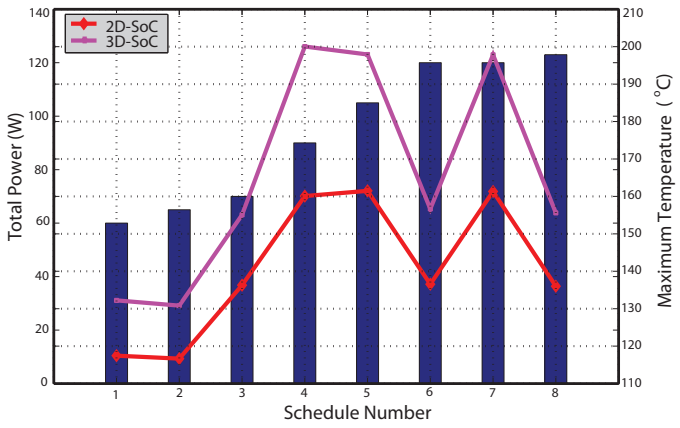

Figure 3. Maximum temperature vs. power dissipation for 2D and 3D configurations of d695.

For illustration, we use a SoC benchmark, **3DSoC_Test01**, as a running example throughout this paper. For simplicity, we assume that the benchmark has two tiers with 5 cores on tier 1 and 3 cores on tier 2. The related test parameters are given in Table I. The column of center point denotes the cartesian co-ordinates of the center points of the cores when the left-most corner of the tier is considered the origin. All distances are marked in nanometers. The temperature constraint of each core is assumed to be 60^oC. Cores 1-5 are placed on the first tier and cores 6-8 are placed on the second tier. We assume the distance between tier 1 and tier 2 is 100μm.

IV. Proposed 3D-SoC Thermal Aware Test Scheduling Algorithm: *3DTATS*

We propose an efficient heuristic to resolve the problem of P_{3DTF} and establish the test framework for 3D-SoCs. The proposed algorithm, namely *thermal-aware test scheduling for three-dimensional System-on-Chip (3DTATS)*, consists of a pre-processing step followed by two design stages. In the pre-processing step, we run the wrapper design algorithm employed from [8] for each core and obtain a set of wrapper configuration candidates and their associated testing times. The wrapper candidates list provides us the flexibility to choose the most suitable wrapper design during the concurrent test scheduling. Next, we find the maximum possible TAM width for each core which is determined either by (1) the available number of input pins if the core is allocated on the bottom tier, or (2) the number of TSVs dedicated to carry the test stimuli to the top tier where the core is placed. We use this maximum possible TAM width to find the least possible testing time of all cores. The cores are then sorted in descending order of their least testing times.

Algorithm 1: Pre-processing

```
for (each core C_i, i ∈ (1...N_c)) do
    run Design_Wrapper (C_i);
    record R_i[k] := {w_k, t_k};
end
for (each core C_i, i ∈ (1...N_c)) do
    Find the maximum TAM width possible (MaxTam_i);
    Find the minimum testing time possible (MinCycles_i);
end
Sort C_i in the descending order of MinCycles_i;
L_1 := {C_i | i ∈ 1...N_c};
```

After preprocessing, we get a list of cores for benchmark **3DSoC_Test01** $L_1 = \{C_1, C_6, C_8, C_5, C_2, C_4, C_3\}$, given the number of external TAM of 20 and number of TSVs of 16.

A. Stage 1: Thermal Compatibility Speculation

In the first stage of *3DTATS*, we perform a new ordering of cores by speculating on thermal compatibility among cores. This stage generates a "Compatibility Order" of the cores in terms of their compatibility level that will be used in the

second stage. Thermal compatibility analysis (e.g., using clique identification, a well known NP-complete problem) is time consuming and can adversely affect running time of thermal aware test scheduling algorithms. Thus, we develop a simple inter-core distance based thermal model for initial study. The basic idea is to keep simultaneous power dissipation sources as distant from each other as possible so as to avoid hotspots. In other words, if two cores are highly apart from each other, they are more likely thermal compatible and thus can be schedule in parallel. The pseudocode is given below.

Algorithm 2: Compatibility Speculation

```
1  Find Candidate in L_1 such that MinCycles_Candidate := max{MinCycles_i};
2  CompatibilityOrder[1] := Candidate;
3  Compcount := 1;
4  while (Compcount < N_c) do
5      Comp_Func := 0;
6      for (each core C_i, i ∈ (1...N_c) && C_i ∉ CompatibilityOrder) do
7          Find horiz_dist (Candidate, C_i);
8          Find vert_dist (Candidate, C_i);
9          Weighed_Dist := horiz_dist × α + vert_dist × β;
10         Comp_func[Candidate][C_i] := Weighed_Dist × MinCycles_i;
11         if (Comp_func[Candidate][C_i] > Comp_Func) then
12             next_candidate := C_i;
13             Comp_Func := Comp_func[Candidate][C_i];
14         end
15     end
16     Candidate := next_candidate;
17     Compcount ++;
18     CompatibilityOrder[Compcount] := Candidate;
19 end
```

Initially, we pick the first core following the order in list L_1. As this core might take the longest time in testing, we start thermal compatibility analysis from it. As long as there are cores not included in the compatibility order, we repeat the steps 13-24 to find a new "candidate" core in each iteration. At beginning, a candidate is the latest addition to the "Compatible Order". For all other cores which are currently excluded in the compatibility order, we calculate their horizontal and vertical distances from the candidate. The horizontal distance is approximated by calculating the distance between the centers of the two cores as if they are mapped onto the same tier. Vertical distance is the distance between two tiers on which the two cores are placed. The effects from both horizontal and vertical distances are justified by multiplying with user-defined weights (i.e., the horiz_objective α and the vert_objective β, and horiz_objective + vert_objective = 1). The weighed horizontal and vertical distances are added together to get Weighed_Dist. This value is multiplied with the least possible testing time of the core under consideration to compute Comp_func which represents the compatibility level between the two cores. Bigger the value of Comp_func, higher the compatibility level. The core with the largest value in Comp_func (the highest compatibility with the candidate) is chosen to be the next candidate and is added to the compatibility order.

We pick the horizontal and vertical objectives as α = 0.15 and β = 0.85 and run experiments on benchmark **3DSoC_Test01**. The obtained compatibility order is $L_2 = \{C_1, C_4, C_6, C_7, C_8, C_2, C_5, C_3\}$ which will be utilized in the second stage for thermal-aware test scheduling.

B. Stage 2: Speculative Scheduling

We use the rectangle-packing based formulation to model the scheduling problem. The cores are represented as rectangles with the height denoting the number of TAM wires assigned to the core and the width denoting the test time in terms of the number of clock cycles. Following the sequence in compatibility order (list L_2), we start scheduling with the first core which is allocated with its least test time. Without exceeding the total TAM limit, we try to allocate more cores in parallel with it in time dimension. Generally speaking, whenever there are idle TAM wires available at a possible start time, we consider the first unscheduled core from L_2. This core has to satisfy two conditions before being scheduled at the start time.

First is to ensure that the test time of the chosen core is reasonably close to its least test time calculated in the pre-processing step. The basic idea is to divide the cores in list L_2 into two groups based on the least time. The selected core belonging to the first (or second) group will be scheduled at the start time only if its test time can be configured

Algorithm 3: Speculative Scheduling

```
1  Cur_Sched := CompatibilityOrder[1];
2  Num_Sched := 1;
3  TAM_Width[Cur_Sched] := MaxTam_{Cur_Sched};
4  while (Num_Sched < N_c) do
5      Find the least start time where a core can be scheduled;
6      Find TAM_Ava at the start time;
7      for each unscheduled core C_i, i ∈ (1...N_c) do
8          Find Test_Cycles_i of C_i with TAM_Ava;
9          if (C_i belongs to the 1st group) then
10             if (Test_Cycles_i ≤ first_limit×MinCycles_i) then
11                 run_hotspot := 1;
12             end
13             else
14                 run_hotspot := 0;
15             end
16         end
17         else
18             if (Test_Cycles_i ≤ second_limit×MinCycles_i) then
19                 run_hotspot := 1;
20             end
21             else
22                 run_hotspot := 0;
23             end
24         end
25         if (run_hotspot == 1) then
26             Run HotSpot thermal simulation;
27         end
28         if (temperature of all cores are within the limit) then
29             Cur_Sched := C_i;
30             Num_Sched ++;
31             Update TAM_Ava at the start time;
32         end
33     end
34 end
```

within $first\_limit \times MinCycles_{selected\_core}$ (or $second\_limit \times MinCycles_{selected\_core}$). The user defined variables ($first\_limit$ and $second\_limit$) determine the ratio of the final test time of a core to its least possible test time. The cores in the first group are usually "big" cores (in terms of the core rectangle area, i.e., maximum TAM width $\times$ least test time), and thus the ratio should be set as close to unity as possible. It's simply because the overall test time is dominated by the test time of "big" cores. It may lead to a very high overall test time if a "big" core is configured to fit in the idle space at the start time with very less idle TAM width. The "small" cores in the second group have a higher flexibility in core rectangle configuration so as to fit in the idle space by setting a higher ratio.

The second condition is to incorporate thermal compatibility into scheduling. The compatibility order provides us a starting point to consider thermal compatibility during scheduling. When allocating each core, the thermal constraints are checked to avoid hotspots at any time. We use the HotSpot simulator [14] to perform thermal simulation. If the selected core violates the thermal constraint, the next core in L_2 is picked and is checked with the two conditions again. Otherwise, it is scheduled at the start time and the available TAM width is updated. Once the idle space at the start time can no longer accommodate any unscheduled cores, it is marked invalid, the available TAM width is updated and we try to schedule cores at the next start time. The pseudocode of the scheduling heuristic is given below.

For the running example of *3DSoC_Test01*, we group the cores into two sets comprising 6 and 2 cores respectively by setting first_limit = 1.25 and second_limit = 2.25. The final scheduling result is shown in Figure 4 and the resulted TAM

routing is illustrated in Figure 5.

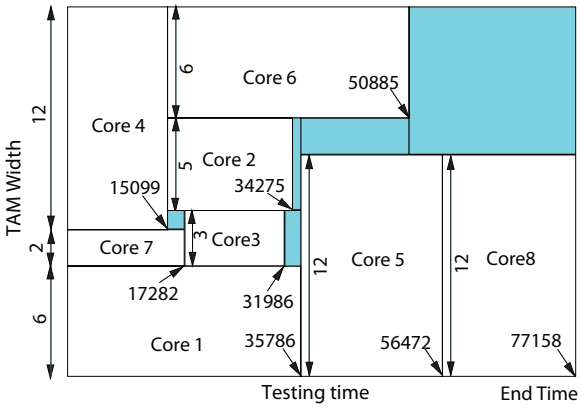

Figure 4. Illustration of the final schedule for *3DSoC_Test01*.

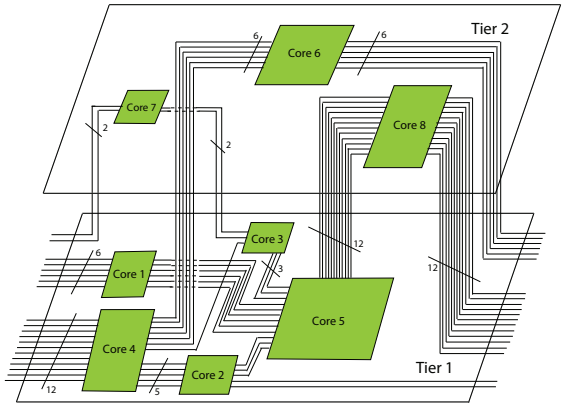

Figure 5. Illustration of the test access architecture for *3DSoC_Test01*.

V. Experimental results

We run extensive simulations using ITC'02 benchmarks, d695, P22810 and P93791 and construct 3D SoC models considering different number of tiers and core placement, variation in TSV density and total TAM limit. The comparison to the approach in [4] cannot be performed because their approach doesn't consider thermal constraints in test scheduling and the core placement information is not provided.

In simulation scenario 1, we build four 3D-SoC models with different number of tiers and core placement by replicating the cores of benchmark d695. The four models are described as S1 (10 cores, 5 cores per tier for two tiers), S2 (20 cores, 10 cores per tier for two tiers), S3 (30 cores, 10 cores per tier for three tiers), and S4 (40 cores, 10 cores per tier for four tiers). For each tier, the maximum number of TSVs for test data transfer is specified. The temperature limit of each core is set to a conservative value at 63^oC. The results are given in tables II-V. The total test application time (TAT) in clock cycles is provided for each TAM width - TSV limit combination. It can be seen that the test application time reduces when the number of TAM wires or the number of TSVs is increased. The CPU running time (including thermal simulations) varies between 3-30 minutes according to the complexity of the SoC and the available TAM width and TSV count, and is dominated by the thermal driven test configuration.

Table II
Test application time for S1

W	TSV = W/8	TSV = W/4	TSV = W/2	TSV $\geq$ W
16	210477	117835	67032	44027
24	141867	72495	49972	32542
32	111849	61046	34594	23016
40	85223	50155	31555	19646
48	72495	40460	25439	18837
56	63960	39536	21750	15237
64	54840	30047	17927	12974

Table III
Test application time for S2

W	TSV = W/8	TSV = W/4	TSV = W/2	TSV $\geq$ W
16	354127	203193	124032	86179
24	224874	115644	85478	65024
32	177199	98126	55844	49616
40	135201	76874	46631	39906
48	115644	61500	41589	37674
56	101298	59616	32510	27239
64	88057	44492	30798	25781

Table IV
TEST APPLICATION TIME FOR S3

W	TSV = W/8	TSV = W/4	TSV = W/2	TSV $\geq$ W
16	360148	203025	136659	130325
24	227239	134693	101954	99906
32	177119	98126	71182	75037
40	147478	82259	55241	57871
48	116544	67818	50902	47245
56	99758	64668	41547	45600
64	86881	46410	41228	39699

Table V
TEST APPLICATION TIME FOR S4

W	TSV = W/8	TSV = W/4	TSV = W/2	TSV $\geq$ W
16	364781	206330	180516	171069
24	249178	146044	129557	134227
32	178535	112465	96168	99656
40	143019	89266	77210	75243
48	115354	77194	69683	70968
56	100199	66287	54419	63441
64	86932	58991	50489	47560

In simulation scenario 2, we run experiments on three ITC'02 benchmarks, d695, p22810 and p93791 with TSV width of 80. The three 3D-SoC models are set up as d695 with two tiers (5 cores on each tier), p22810 with three tiers (10 cores each on tier 1 and tier 2 and 8 cores on tier 3), and p93791 with four tiers (8 cores on each tier). The temperature constraint of each core is estimated by taking the average of temperature variations of the core obtained from the temperature trace file of HotSpot. The results of the total test application time are provided in table VI. Further, we run test scheduling without thermal compatibility speculation. The comparison results are given in table VII for d695, where TAT_1 and RT_1 are referred to as the overall 3D-SoC testing time and the CPU running time with compatibility speculation while TAT_2 and RT_2 without compatibility speculation. Here, the running time is reported in seconds. We can observe that both the TAT and RT are lesser when the thermal compatibility speculation is built into the heuristic.

Table VI
TEST APPLICATION TIME (TSV WIDTH = 80)

W	d695_TAT (CC)	p22810_TAT (CC)	p93971_TAT (CC)
16	44027	469487	1864872
24	32542	376819	1257312
32	24133	270592	1185928
40	19718	240542	1107394
48	18837	179755	987669
56	15237	157402	701307
64	13816	146630	659045

Table VII
TEST APPLICATION TIME AND HEURISTIC RUN-TIME FOR D695

W	TAT_1	TAT_2	$\delta TAT(\%)$	RT_1	RT_2	$\delta RT(\%)$
16	44027	44995	-2.2	426	599	-40.61
24	32542	32474	0.21	506	1864	-268.38
32	24133	24597	-1.92	561	1977	-252.41
40	19718	20629	-4.62	613	1951	-218.27
48	18837	19391	-2.94	653	1991	-204.9
56	15237	18400	-20.76	687	2072	-201.6
64	13816	13025	5.73	719	2064	-187.07

VI. CONCLUSION

We have addressed the problem of 3D-SoC test framework design under thermal constraints. With three dimensional core placement and test resource allocation, we proposed an efficient test scheduling algorithm for 3D test access routing by

utilizing TSV interconnection. We considered the more severe chip overheating problem in 3D-SoC concurrent testing. As thermal simulation can be quite time consuming and becomes the bottleneck during run-time, we developed a simple thermal modeling to provide fast and preliminary thermal compatibility analysis and incorporate the thermal compatibility into test configuration and test scheduling with the objective of minimizing the overall test time.

REFERENCES

[1] P. Ramm, A. Klumpp, R. Merkel, J. Weber, and R. Wieland, *"Vertical System Integration By Using Inter-Chip Vias And Solid-Liquid-Interdiffusion Bonding"*, in Japanese Journal of Applied Physics, Vol. 43, No. 7A, pp. 829-830, 2004.

[2] Daniel Regun, *"Tomorrow's Chips to Stack Cores Vertically"*, in Hot Hardware News, http://hothardware.com/News/Tomorrows-Chips-To-Stack-Cores-Vertically.

[3] X. Wu, P. Falkenstern, and Y. Xie, *"Scan Chain Design for Three-Dimensional Integrated Circuits"*, in Proc. of IEEE International Conference on Computer Design, pp. 208-214, 2007.

[4] X. Wu, Y. Chen, K. Chakrabarty, and Y. Xie, *"Test access mechanism optimization for core-based three-dimensional SOCs"*, in Proc. of IEEE International Conference on Computer Design, pp. 212-218, 2008.

[5] S. Goel, and E. Marinissen, *"Effective and Efficient Test Architecture Design for SoCs"*, in Proc. of IEEE International Test Conference, pp. 529-538, 2002.

[6] Y. Huang et al., *"Optimal Core Wrapper Width Selection and SoC Test Scheduling Based on 3-D Bin Packing Algorithm"*, in Proc. of IEEE International Test Conference, pp. 74-82, 2002.

[7] V. Iyengar, K. Chakrabarty, and E. Marinissen, *"Co-Optimization of Test Wrapper and Test Access Architecture for Embedded Cores"*, Journal of Electronic Testing: Theory and Applications, Vol. 18, No. 2, pp. 213-230, 2002.

[8] D. Zhao, and S. Upadhyaya, *"Power Constrained Test Scheduling with Dynamically Varied TAM"*, in Proc. of IEEE VLSI Test Symposium, pp. 273-278, 2003.

[9] D. Zhao, U. Chandran, and H. Fujiwara, *"Shelf Packing to the Design and Optimization of A Power-Aware Multi-Frequency Wrapper Architecture for Modular IP cores"*, in Proc. of IEEE Asia and South Pacific Design Automation Conference, 2007.

[10] P. Rosinger, B. Al-Hashimi, and K. Chakrabarty, *"Rapid Generation of Thermal-Safe Test Schedules"*, in Proc. of IEEE Design Automation and Test in Europe, pp. 840-845, 2005.

[11] Z. He, Z. Peng, and P. Eles, *"A Heuristic For Thermal-Safe SoC Test Scheduling"*, in Proc. of IEEE International Test Conference, pp. 1-10, 2007.

[12] T. E. Yu, T. Yoneda, K. Chakrabarty, and H. Fujiwara, *"Thermal-Safe Test Access Mechanism And Wrapper Co-optimization For System-on-Chip"*, in Proc. of IEEE Asian Test symposium, pp. 187-192, 2007.

[13] P. Garrou, C. Bower, and P. Ramm, *"3D Integration: Technology and Applications"*, by John Wiley & Sons, Inc., 2008.

[14] W. Huang, S. Ghosh, K. Sankaranarayanan, K. Skadron, and M. R. Stan, *"HotSpot: Thermal Modeling for CMOS VLSI Systems"*, IEEE Trans. on Component Packaging and Manufacturing Technology, 2005.

[15] Y. Huang,et.al ,*"Optimal core wrapper width selection and SOC test scheduling based on 3-D bin packing algorithm "* Proc. IEEE International Test Conference 2002, pp. 7482.

[16] Z. He, Z. Peng, P. Eles, P. Rosinger, and B. M. Al-Hashimi,*"Thermal-aware SoC test scheduling with test set partitioning and interleaving"*, J. Electronic Testing: Theory and Applications, Vol. 24, No. 1-3, pp. 247-257, June 2008.

[17] P. Rosinger, B.M. Al-Hashimi, and K. Chakrabarty, *"Thermal Safe Test Scheduling for Core-Based System-on-Chip Integrated Circuits"*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 25, No. 11, pp. 2502-2512, Nov. 2006.