Technology for Three Dimensional Integrated System-on-a-Chip

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Abstract

We have proposed a wafer stacking technology to integrate various kinds of devices into three-dimensional (3D) SoC[1-6]. In 3D SoC, each circuit layer is stacked and electrically connected vertically using a huge number of vertical interconnection. Hence, we can dramatically increase the wiring connectivity, reduce the number of long wiring and integrate various kinds of devices with different fabrication process sequences into one chip. In this paper, we describe a 3D microprocessor test chip consisting of three circuit layers and demonstrate the basic operation of the 3D microprocessor.

Introduction

System-on-a Chip (SoC) is very useful to increase the system performance and to reduce the power and size of system. However, it is not easy to integrate various kinds of devices with different fabrication process sequences into one chip. We propose a new wafer stacking technology to integrate various kinds of devices into three-dimensional (3D) SoC.

Figure 1 shows the cross-sectional structure of 3D SoC. Several circuit layers with different functions are stacked into one chip in 3D SoC. For example, the first layer consists of DRAM array, the second layer is SRAM array, the third layer is MPU and so on. Each circuit layer is stacked and electrically connected vertically using a huge number of vertical interconnection: buried interconnections and micro bumps. Hence, we can dramatically increase the wiring connectivity and reduce the number of long wiring. As a result, we can realize the high performance SoC using three dimensional integration technology.

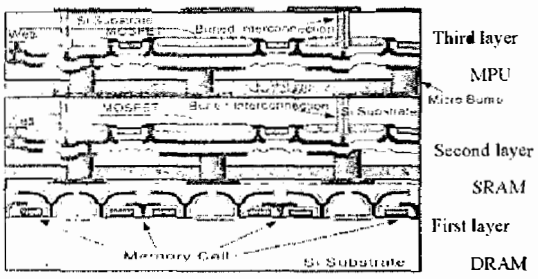

Fig.1 Conceptual viewgraph of 3D SoC.

Wire Length Distribution

The vertical interconnection plays important role in 3D SoC. The wire length distribution in 3D SoC is theoretically evaluated with Rent's rule as shown in Fig.2[7-10]. This figure clearly shows that the number of long wiring dramatically decreases with increasing the number of stacking layers. Hence, high speed and low power consumption can be realized in 3D SoC.

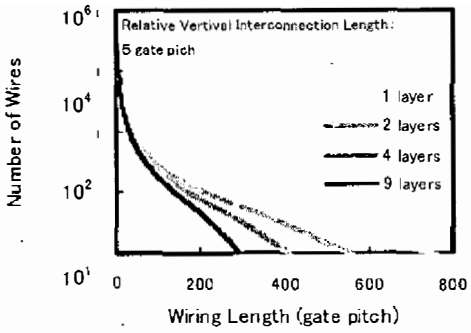

Fig.2 Wiring length distribution.

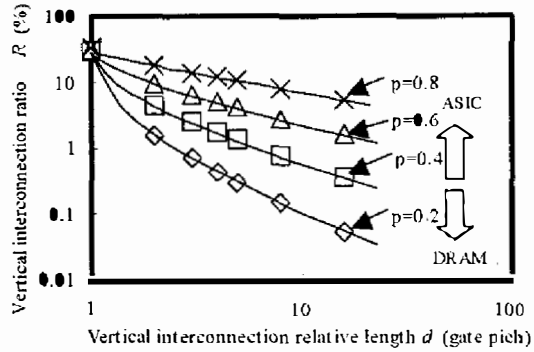

Fig.3 Vertical interconnection ratio in all of wires depends on the length and Rent's constant.

Figure 3 shows the dependence of the ratio of vertical interconnection to all wiring on relative vertical interconnection length with changing Rent's constant p. It is clearly observed that vertical interconnection density strongly depends on them. It means that many vertical interconnections are effectively utilized in chips

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with high Rent's constant p, such as MPUs, and ASICs. Therefore, SoC is a suitable application of three dimensional integration technology.

3D Integration Process

The fabrication sequence of the 3D SoC is illustrated in Fig.4. After the formation of devices and buried interconnections, In-Au micro bumps are formed on the top surface of each device wafer. The second wafer is face-down bonded to the first device wafer. A special 3D wafer aligner is used to align two wafers before wafer bonding. The alignment tolerance is less than ±1μm. The liquid epoxy adhesive is injected into the gap between two wafers in a vacuum chamber after the temporary bonding using the micro bumps. After wafer bonding, the upper device wafer is thinned to around 30μm from the back side. In-Au micro bumps are formed again on the back surface of the second device wafer. Then, the third device wafer is again face-down bonded to the stacked wafers and thinned from the back side. By repeating this sequence, the 3D stacked wafer is obtained.

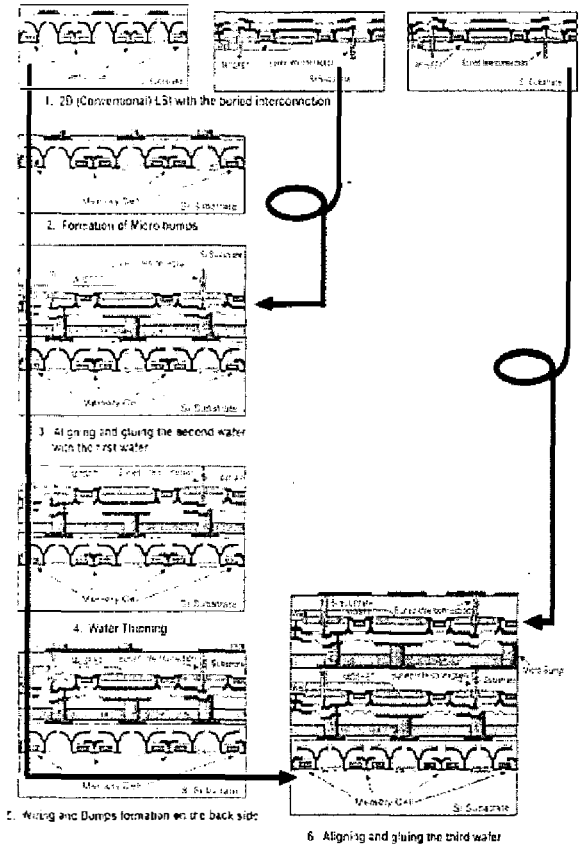


Fig.4 Fabrication sequence of the 3D SoC.

In our wafer stacking technology, it is required to form the deep Si trench in order to form the buried interconnection. Then, Si trench with diameter of 2μm and depth of 50 to 60μm is formed using plasma etching (ICP). This Si trench is oxidized and filled with n^+ poly-Si (0.4mΩ-cm). Figure5 shows SEM cross section of buried interconnection after filling with poly-Si. It is clear that trench is completely filled with poly-Si. Figure6 shows electrical characteristic of the vertical interconnection chain with 144-bumps and 144-buried interconnections. From these characteristics, we obtain the values of around 9Ω for the resistance of buried interconnection and around 10mΩ for the contact resistance of micro-bumps.

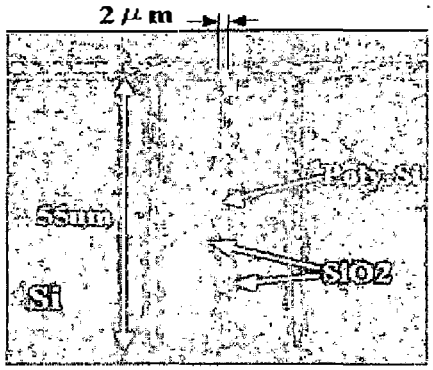


Fig.5 SEM cross section of buried interconnection filled with poly-Si.

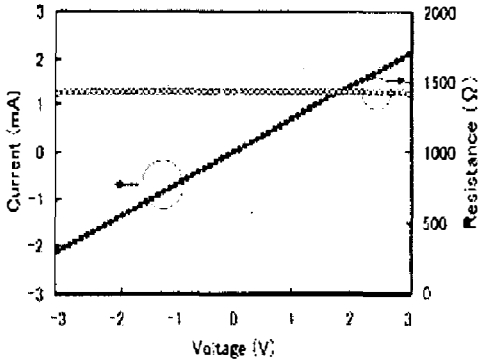
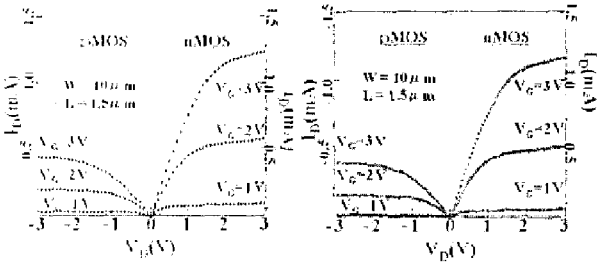


Fig.6 Electrical characteristic of the vertical interconnection chain in 3D SoC chip.

We evaluated the I-V characteristics of MOSFET after 3D integration as shown in Fig.6. Excellent characteristics of MOSFET formed in the first layer are measured through vertical interconnections at bonding pads in the third layer



(a) Before (b) After 3D integration

Fig.6 *I-V* characteristics of MOSFET before/after 3D integration.

3D Microprocessor Test Chip

We have proposed 3D microprocessor as a typical example of 3D SoCs. In 3D microprocessor, DRAM and SRAM are stacked on processor and closely connected each other as shown in Fig.7. We fabricated 3D microprocessor test chip using the wafer stacking technology to confirm the basic operation of this 3D microprocessor. The configuration of 3D microprocessor test chip is shown in Fig.8. The 3D microprocessor test chip consists of SRAM layer, level-converter layer and processor layer. SRAM layer is composed of high-Vth MOSFET and is operated at higher supply voltage to obtain the large static noise margin and the fast access time. The processor layer is composed of low-Vth MOSFET and is operated at lower supply voltage to reduce the propagation delay and power consumption.

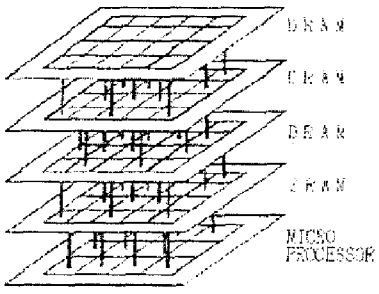


Fig.7 Configuration of 3D microprocessor.

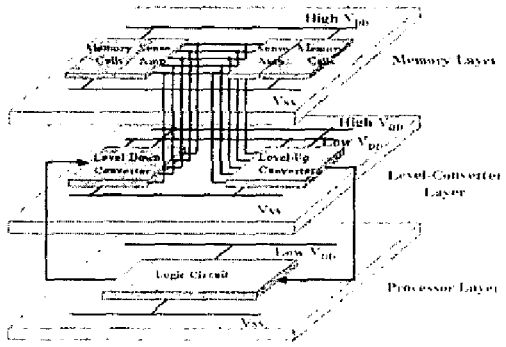


Fig.8 Configuration of 3D microprocessor test chip.

Figure 9 shows SEM cross section of fabricated 3D microprocessor test chip. It is clearly observed that three layers are well aligned and uniformly bonded through the microbumps and insulating epoxy adhesive. Waveforms measured in 3D microprocessor test chip are shown in Fig.10.

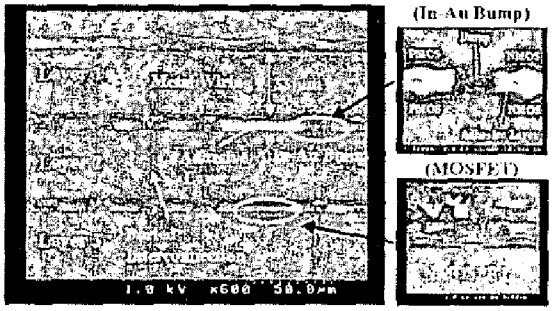


Fig.9 SEM cross section of 3D microprocessor test chip.

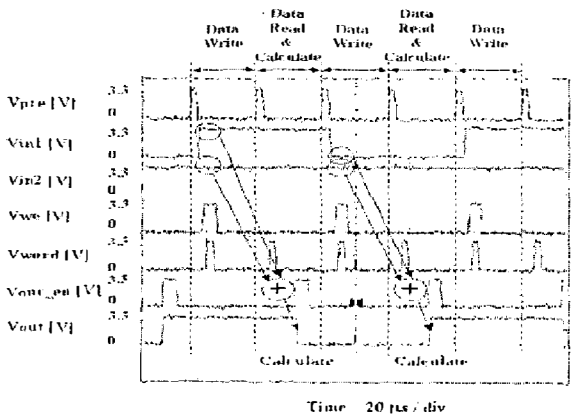


Fig.10 Measured waveforms of 3D microprocessor test chip.

It is successfully demonstrated that the signal data read out of SRAM are transferred to the processor layer after they are converted to lower voltage swing and then "add" operation is executed in the processor layer.

Conclusions

We have proposed a new wafer stacking technology to integrate various kinds of devices into three-dimensional (3D)SoC in this paper. We evaluate the *I-V* characteristics of MOSFET in 3D test chip. Excellent characteristics of MOSFET are obtained. Therefore we confirm that our 3D integration technology do not cause any degradations for MOSFETs. Then we fabricate 3D microprocessor test chip consisting of three circuit layers and successfully demonstrate the basic operation of 3D microprocessor.

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