A Structured and Scalable Test Access Architecture for TSV-Based 3D Stacked ICs

Erik Jan Marinissen[1]
[1] IMEC
SSET/DC
Kapeldreef 75
3001 Leuven, Belgium
erik.jan.marinissen@imec.be

Jouke Verbree[2]
[2] Delft University of Technology
Department of Computer Engineering
Mekelweg 4
2628CD Delft, The Netherlands
j.verbree@student.tudelft.nl

Mario Konijnenburg[3]
[3] Holst Centre/IMEC
SSET/WATS
High Tech Campus 31
5656AE Eindhoven, The Netherlands
mario.konijnenburg@imec-nl.nl

Abstract

New process technology developments enable the creation of three-dimensional stacked ICs (3D-SICs) interconnected by means of Through-Silicon Vias (TSVs). This paper presents a DfT test access architecture for such 3D-SICs that allows for both pre-bond die testing and post-bond stack testing. The DfT architecture is based on a modular test approach, in which the various dies, their embedded IP cores, the inter-die TSV-based interconnects, and the external I/Os can be tested as separate units to allow optimization of the 3D-SIC test flow. The architecture builds on and reuses existing DfT hardware at the core, die, and product level. It adds a die-level wrapper, which is based on IEEE 1500, with the following novel features: (1) *dedicated probe pads* on the non-bottom dies to facilitate pre-bond die testing, (2) *TestElevators* that transport test control and data signals up and down during post-bond stack testing, and (3) a *hierarchical* Wrapper Instruction Register (WIR) chain. The paper also hints at opportunities for optimization and standardization of this architecture.

1 Introduction

The semiconductor industry is preparing itself for 3D-SICs based on TSVs [1–3]. TSVs are conducting nails which extend out of the back-side of a thinned-down die and enable the vertical interconnect to another die [4, 5]. TSVs are high-density, low-capacity interconnects compared to traditional wire-bonds, and hence allow for many more interconnections between stacked dies, while operating at higher speeds and consuming less power [6]. TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities [7, 8]. Combined with their smaller form factor and lower overall manufacturing cost, 3D-SICs have many compelling benefits, and hence their technology is quickly gaining ground.

Like all micro-electronics, TSV-based die stacks have a manufacturing process that is sensitive to defects, and hence 3D-SICs need to undergo electrical testing to ensure product quality. While the process and design technology is getting to maturity, testing 3D-SICs for manufacturing defects is considered by many as a major, still largely unresolved obstacle to make these devices a product reality. Next to all basic and most advanced test technology issues, 3D-SICs have some unique new test challenges of their own [9, 10]. These challenges include (1) development of new fault models and corresponding tests for TSV-based interconnects and new 3D-induced intra-die defects, (2) wafer probing on small and numerous micro-bumps and/or TSV tips and pads under stringent damage requirements, (3) handling of and probing on wafers with thinned-die stacks, (4) the design, partitioning, and optimization of DfT architectures that span across multiple dies, and (5) optimization of the test flow for maximum effectiveness and lowest cost.

In this paper, we focus on the design of a structured and scalable test access architecture. The architecture supports pre-bond die testing, post-bond stack testing, and final packaged-product testing. It allows for modular testing [11] of intra-die circuitry and inter-die TSV-based interconnects, and hence supports stacks of possibly heterogeneous and/or black-boxed dies, flexible test flow creation during the various maturity stages of a 3D-SIC product, and easy diagnosis. The architecture reuses commonly encountered design-for-test structures within the various dies as much as possible. It leverages two existing design-for-test standards, viz. IEEE 1149.1 [12, 13] for chips on a Printed Circuit Board (PCB) and IEEE 1500 [14, 15] for embedded cores within an System-On-Chip (SOC). The test access architecture initially targets 3D-SICs consisting of scan-testable digital logic and memory dies, but can be extended to include other types of dies as well.

The remainder of this paper is organized as follows. Section 2 describes related prior work in test access architectures for 3D-SICs. Section 3 provides an overview of test access architecture standards for PCBs and 2D-SOCs, which, like 3D-SICs, are also built from interconnected smaller components. The test requirements and constraints which are unique to 3D-SICs are discussed in Section 4. Our proposed 3D-SIC test access architecture is presented in Section 5. Section 6 concludes this paper.

2 Related Prior Work

The first paper dedicated to testability of 3D-SICs was [16]. It focuses on pre-bond die testing, required to achieve acceptable compound stack yields. Testing incomplete products as formed by the various stack tiers is identified as a potential problem. In our opinion, this does *not* have to pose a problem really, provided that (1) structural, not functional tests are applied, (2) a modular test strategy is followed, and (3) the infrastructure (power/ground, clocks) can be made operational per die. [16] proposes a 'scan island' approach, which is essentially the wrapper technology from IEEE 1149.1 [12, 13] and IEEE 1500 [11, 14, 15] under a different name.

Most other papers on 3D-SIC testing implicitly propose a test access architecture, while focusing on optimizing the design parameters of that ar-

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chitecture to minimize the resulting test length and/or the associated wire length. Wu et al. [17] describe three scan chain optimization approaches for 3D-SICs. Implicitly, this paper assumes that a single logic test unit is partitioned over multiple tiers, which seems rather unrealistic. Therefore, in [18], Wu et al. propose a core-based design and test approach (as common for 2D-SOCs) in which each core resides on a single tier. The paper proposes an ILP-based Test Access Mechanism (TAM) optimization approach, which tries to minimize the resulting test length under a constraint for the number of additional 'test TSVs'. Both papers [17, 18] focus exclusively on post-bond stack testing, and ignore the requirements for pre-bond die testing.

Jiang et al. [19] describe a TAM optimization approach based on simulated annealing that minimizes test length and TAM wire length with a user-defined cost weight factor. They assume a modular core-based 3D-SIC test approach and take both pre-bond and post-bond test lengths into account. The paper lacks realistic constraints on wafer and packaged stack test access, due to which it unrealistically allows TAMs to start and end at any stack tier. Successor paper [20] remedies this partly, by working with pre-bond tests that are applied through dedicated probe pads at the die in question, for which a maximum count is assumed. The paper proposes heuristics that determine a post-bond stack test architecture, from which segments are reused as much as possible to build additional die-level test architectures for the pre-bond tests, while meeting the maximum probe pad count constraint and minimizing test length and TAM wire length.

In contrast to the prior work by others, our paper starts out by identifying realistic constraints and requirements set forward by, among others, wafer probe technology and test flow set-ups. Subsequently, we focus on the design of a generic and structured test access architecture. The architecture is scalable in the sense that its design parameters can be optimized for varying core, die, and stack parameters, but the focus of our paper is *not* on those optimization procedures. The prior work published until now has focused on testing the cores in the various dies constituting the 3D-SIC, but has ignored testing the circuitry within a die in between the cores, as well as it has ignored testing the (TSV-based) inter-die interconnects. The prior work also did not identify how existing DfT standards and test access architectures can be leveraged. Finally, test control and instructions were ignored in the prior work. We address all the above issues.

3 Related Test Access Standards

3.1 Test Access Architecture for PCBs

The commonly-used test access architecture for PCBs is based on IEEE Std. 1149.1, Boundary Scan (a.k.a. 'JTAG') [12, 13]. In order for chips to be compliant to IEEE 1149.1, a small hardware wrapper is added to them. IEEE 1149.1 works through a narrow single-bit interface, as every JTAG terminal requires an additional chip pin and these are considered expensive. Fortunately, the prime focus of IEEE 1149.1 is PCB interconnect testing, and that requires only a small number of test patterns [21]. The single-bit interface pins are called TDI and TDO, and they transport both instructions and test data. The control interface consists of the pins TCK, TMS (and optionally TRSTN). For an example PCB containing three chips, a common JTAG-based test access architecture is depicted in Figure 1. The control signals are broadcast to all chips, while the TDI-TDO pins are concatenated through the chips. The broadcast control signals can configure the TAP Controller finite state machine in a mode in which it is willing to receive instructions, which are subsequently scanned into the Instruction Register (IR) via the daisychained TDI-TDO interface. Note that this allows for different instructions for different chips; for example, Chip B can be configured in INTEST mode, while Chips A and C are configured in BYPASS mode. Then, the chips are brought into their instructed test modes via the broadcast control signals and test data is scanned in and out again via the daisychained TDI-TDO interface. The selected test data register (e.g., the bypass register, a Boundary Scan Register (BSR), or a chip-internal scan chain) depends on the instruction, and can be different for different chips; in any case, it is a single shift register, as shown in Figure 1.

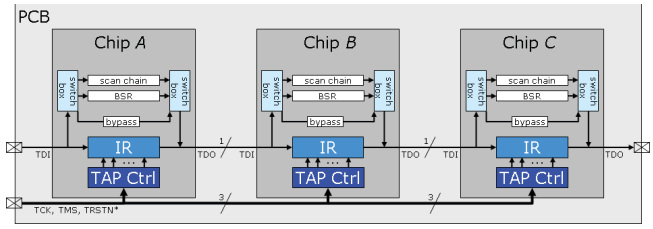

Figure 1: Board-level test access architecture for chips based on IEEE 1149.1.

3.2 Test Access Architecture for 2D-SOCs

The commonly-used test access architecture for (two-dimensional) SOCs containing embedded IP cores is based on IEEE Std. 1500 [11, 14, 15]. Like IEEE 1149.1, IEEE 1500 adds a small hardware wrapper around the module-under-test. As shown in Figure 2, the test access architecture for an IEEE 1500-based SOC shows similarities to IEEE 1149.1-based PCBs. Control signals are broadcast to all cores. Once configured in the appropriate mode, instructions are shifted into the Wrapper Instruction Register (WIR) via the daisychained WSI-WSO interface. That same instruction interface also doubles as single-bit test data interface. However, next to the similarities, there are also significant differences between IEEE 1149.1- and IEEE 1500-based test access architectures. Below, we list the most important ones.

- Unlike IEEE 1149.1, the focus of IEEE 1500 is not (only) on testing wiring interconnects between cores. First of all, the interconnect circuitry in between IP cores typically does not consist only of wires, but is often formed by deep sequential logic [22]. In addition, IEEE 1500 is meant to support also the testing of the cores themselves, and IP cores are often significantly-sized and complex design entities. Therefore, the test data volumes involved are typically quite large, and a single-bit test data interface would not suffice. Hence, IEEE 1500 has an optional n-bit ('parallel') test data interface (named WPI and WPO), where n can be scaled by the user to match the test data volume needs of the IP core in question.
- Adding wider interfaces to embedded IP cores does not add chip pins as in IEEE 1149.1, but only core terminals; and they are considered to be significantly less expensive than chip pins.
- IEEE 1149.1 has two (or three) standardized control pins, which are expanded within the chip by the TAP Controller. IEEE 1500 has no TAP Controller, but receives it control signals directly. These are six (or seven) signals: WRCK, WRSTN, SELECTWIR, SHIFTWR, CAPTUREWR, UPDATEWR (and optionally TRANSFERDR) [11, 14, 15].

Figure 2 also features a parallel wrapper bypass. This bypass is not mandated by IEEE 1500, but often implemented to shorten the test access path

to other cores in the same TAM [23]. It is the task of the *switch boxes* in Figure 2 to make an effective mapping between the active WIR instruction mode and the TAM-to-chain connections.

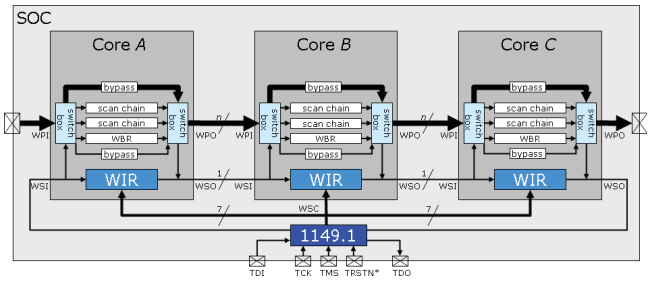

Figure 2: SOC-level test access architecture for cores based on IEEE 1500.

IEEE 1500 only standardizes the core-level test wrapper, and *not* the SOC-level test access architecture of the optional parallel TAMs. At the SOC-level, optimizations can be made w.r.t. TAM type [24, 25], TAM architecture [23], and corresponding test schedule. In a tyical implementation, as shown in Figure 2, the SOC itself is equipped with an IEEE 1149.1 wrapper to facilitate board-level testing. The IEEE 1500 serial interface (WSC, WSI, and WSO) is multiplexed onto the IEEE 1149.1 Test Access Port [15] to save otherwise additional test pins. The IEEE 1500 parallel interface (WPI and WPO) can be multiplexed onto the functional external pins, as is common for regular scan chains; this saves otherwise additional test pins.

4 Requirements and Constraints

We consider three types of 3D-SICs; examples of these types (in this case for stacks of three tiers) are depicted in Figure 3. The three types differ in their connections to the external world (*'pins'*): (a) wire-bond from the top die, (b) wire-bond from the bottom die, and (c) flip-chip connections from the bottom die. All three types have in common that only one side of one of the extreme tiers (top or bottom) holds all external connections. In the remainder of this paper we assume all external connections are in the *bottom* die. This assumption is without loss of generality, as we can always swap the references to top and bottom die.

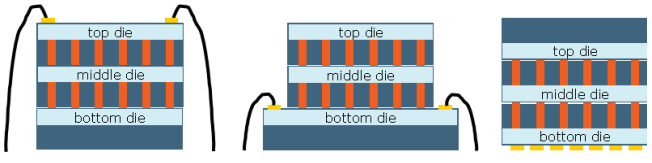

Figure 3: Three options for 3D-SIC external connections: (a) wire-bond from top die, (b) wire-bond from bottom die, and (c) flip-chip from bottom die.

A 3D-SIC test flow consists of (1) *pre-bond die tests* and (2) *post-bond stack tests* [10]. The pre-bond die tests are wafer tests; the post-bond stack tests can be carried out on both unpackaged as well as packaged stacks. A test of a stack might consist of (re-)tests of the various dies, as well as tests of the TSV-based interconnects between the dies. A 3D-SIC test access architecture should support all these tests. While testing unpackaged stacks, it should be possible not only to test the complete stack, but also to test partial stacks. Furthermore the test access architecture should also support external interconnect testing, once the 3D-SIC is mounted on a board.

We want the 3D-SIC test to be a *modular* test [11, 23], as opposed to a test in which the entire stack is tested as one monolithic entity. A modular test considers the various dies and TSV-based interconnect layers as separate test units; for complex dies, it is very well possible that they are further sub-divided in multiple finer-grain test modules, e.g., embedded cores. Modular testing for 3D-SICs comes with the same benefits as it brings to 2D-SOCs [11]: (1) different tests for various modules of heterogeneous products, (2) test of black-boxed IP, (3) divide-and-conquer test generation and application, and (4) test reuse. Modular testing provides two more benefits specific to 3D-SICs: (5) flexibility in optimizing the test set per step of the test flow ("how often do we re-test a module?"), and (6) first-order diagnosis ("which module of the stack contains the fault?"). The latter is all the more important given the likelihood that multiple companies contribute to the manufacturing of a single 3D-SIC. Modular testing requires DfT in the form of *wrappers* that provide controllability and observability at the boundary of the module-under-test and *Test Access Mechanisms (TAMs)* that transport the test data from the chip's probe pads or pins to the module-under-test and vice versa [11, 25].

We assume a 3D-SIC of which the constituting dies are *scan testable*; for example, this can include scan-tested digital logic, BIST-ed embedded memories, or even scan-enabled analog cores. Furthermore, we assume it is a requirement for board-level interconnect testing that the overall product is IEEE 1149.1 compliant on its external pins. We assume that additional external test pins beyond IEEE 1149.1 are expensive and hence should be avoided. In contrast, we assume that some additional TSV-based interconnects between tiers for the purpose of test are relatively affordable; e.g., IMEC's *via-middle* TSVs are made at a 10μm minimum pitch [4, 5].

The test access architecture should be able to provide a trade-off between additional area cost for DfT, test generation effort, and test length. To minimize silicon area, we want to re-use the existing intra-die DfT infrastructure as much as possible: internal scan chains, test control, test data compression circuitry, built-in self-test, etc. To minimize the test generation effort, we prefer to base our die-level wrapper on the existing IEEE Std. 1500, given its scalable TAM width and flexible WIR. The test access architecture should allow for flexible test scheduling to minimize the test length. It is also a requirement that the test access architecture itself is testable. It is desirable that this can be done without depending on the correct functionality of the existing DfT inside the local dies and embedded IP cores.

The bottom die can be probed on the wire-bond or flip-chip pads for its external connections; that is 'business-as-usual'. For their pre-bond die test, the other (non-bottom) dies need to be probed as well. Today's probe technology is insufficient to provide probe access on TSV tips and TSV landing pads [10]; they are too small and too fragile. Hence, for all non-bottom dies, it is a requirement to provide dedicated *probe pads* for pre-bond wafer test access [10, 16, 20].

For the post-bond stack tests, test access is only possible via the bottom die. This implies that signals for test control and test data exclusively come from and go to the bottom die, and hence have a 'u-turn' type of shape; we refer to these as *TestTurns*. Also, in order to reach dies higher up in the stack, all test signals have to be transported up and down through a new type of DfT hardware that includes TSVs and which we refer to as *TestElevators*.

2D-SOCs allow us to design DfT features in the SOC circuitry around (i.e., outside) the embedded cores. This is not the case for 3D-SICs; all DfT needs to be in the various dies. The only thing that exists outside the dies are vertical interconnects, and even those need to be pre-designed in terms of die-level features, such as TSVs and TSV landing pads. This im-

plies that wrappers, TAMs, and their control signaling all needs to be predesigned in the die; not only for *that* die, but also for the dies above it in the stack. Hence, we assume that for all tiers, the DfT is designed in adherence to a pre-defined test access architecture, or that we have the freedom to modify the DfT circuitry; it cannot be added as an after-thought.

We require the test access architecture to be *scalable*, in the sense that it works for an undetermined number of stack tiers. Also, the architecture should not predestine a die to a certain tier level, such that dies that adhere to the architecture can function at any level in the stack hierarchy. Exceptions to this requirement are formed by the bottom die, which with its external connections is obviously predestined as bottom, and possibly the top die.

5 3D-SIC Test Access Architecture

5.1 Die-Level Wrapper

The test access architecture we propose for 3D-SICs is based on a die-level wrapper, which is an extended version of IEEE 1500. The die-level wrapper provides a consistent external interface to other dies in the stack, while internally within the die, it connects up to the existing functional circuitry and regular intra-die DfT. The architecture uses a limited, scalable number of dedicated TSV-based interconnections between dies in addition to the already existing functional interconnects.

Figure 4 shows a schematic overview of the DfT features and additional interconnects for an arbitrary Die x in the middle of a stack. The figure abstracts from the functional circuitry and interconnects. It shows two internal scan chains, which are representative for the possible die-internal DfT, such as any number of scan chains for a monolithic design, TAMs for a core-based SOC design, and/or BIST-ed logic or memory. Die x is equipped with an IEEE 1500-like wrapper that is normally encountered with embedded IP cores. The figure shows the conventional IEEE 1500 features of that die-level wrapper: a seven-bit Wrapper Serial Control (WSC), a Wrapper Instruction Register (WIR), a Wrapper Boundary Register (WBR), a serial WSI-WSO interface for instructions and low-bandwidth test data, and parallel WPI-WPO interface for test data. Note that it is mandatory that the entire IEEE 1500 interface is situated at the bottom side of the die.

Our die-level wrapper has three 3D-SIC-specific features (Items 1 and 2 are highlighted in orange in Figure 4):

1. All control and data signals of IEEE 1500 (WSC, WSI, WSO, WPI, and WPO) not only enter or exit Die x via TSV-based interconnects from/to the die below Die x for post-bond stack testing, but are also equipped with dedicated probe pads for pre-bond die testing. In Figure 4, for easy figure layout, these probe pads are drawn on the bottom side; however, that does not imply that these probe pads need to be physically located at the bottom side of the die. Note that the width of the parallel interface WPI-WPO might be chosen differently for the TSV interconnects (n) and probe pads (m).
2. All control and data signals of IEEE 1500 can be transferred to a die above Die x via a set of signals with identical names, post-fixed with the letter 's' (for 'stack'): WSCs, WSIs, WSOs, WPIs, and WPOs. These signals are called TestElevators, and are all situated on the top side of the die.
3. To prevent unbridled lengthy WIR chains, we propose hierarchical WIR chains. This is further described in Section 5.2 and depicted in Figure 7.

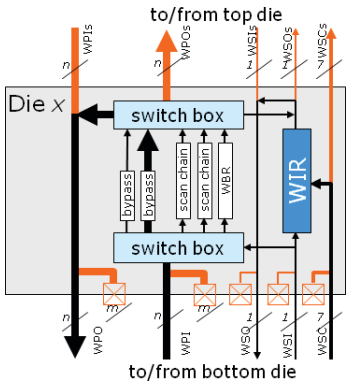

Figure 4: Schematic view of the die-level wrapper based on IEEE 1500.

The DfT in a bottom die differs from a middle die in the following aspects.

- Dedicated pre-bond probe pads are not required. Instead, the functional external I/O pads can be used for probe access.
- The bottom die is equipped with IEEE 1149.1 to facilitate board-level testing and provide a board-level test and debug port. The JTAG boundary scan chain includes all external I/Os of the 3D-SIC product.
- The serial IEEE 1500 interface (WSC, WSI, and WSO) can be multiplexed onto the IEEE 1149.1 Test Access Port (TAP), similar to what is common in 2D-SOCs [15]. This saves otherwise dedicated pads, and makes the 3D test access architecture accessible even when the 3D-SIC is soldered onto a PCB.
- The parallel IEEE 1500 interface (WPI and WPO) is multiplexed onto the functional external I/O pads, similar to what is common for scan chains and parallel TAMs in 2D-SOCs. This saves otherwise dedicated pads, but restricts the TestElevator width to the available functional I/O.

The DfT in a top die differs from a middle die in the following aspect.

- The die does not have TSV-based interconnects to an even higher-level die, as it is the top die. Hence, the top-side TestElevators WSCs, WSIs, WSOs, WPIs, and WPOs are absent.

Figure 5 depicts the test access architecture for an example 3D-SIC containing three dies; Dies 1, 2, and 3 are respectively the bottom, middle, and top die of the stack. To show the similarities and differences with test access architectures for PCBs and 2D-SOCs, the dies are shown next to each other, instead of as a vertical stack.

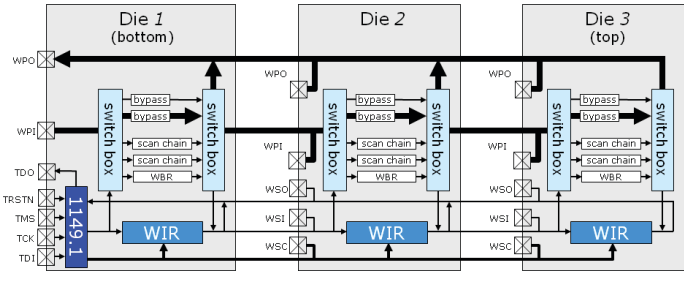

Figure 5: 3D-SIC test access architecture for dies based on IEEE 1500.

This test access architecture requires $7 + 2 + 2m$ dedicated probe pads at each (non-bottom) die in the stack. As the parallel TAM is optional in IEEE 1500, note that m can be zero. This number of dedicated probe pads needs to be extended by all required infrastructural pads for power, ground, clocks, etc.; these are not shown in Figure 4, although their presence is obviously essential.

IEEE 1500 allows various types of wrapper cells in its WBR. Embedded cores in 2D-SOCs commonly use the cell depicted in Figure 6(a); it consists of only a single flip-flop and hence occupies little silicon area. For the WBR chain of our proposed 3D-SIC die-level wrapper, we prefer to use the (also IEEE 1500-compliant) double flip-flop wrapper cell shown in Figure 6(b). At the expense of an extra flip-flop, this wrapper cell provides ripple-protection during shift mode, which seems appropriate especially if the various dies come from different sources, and ripple-during-shift might result in unwanted signal combinations at the inter-die interfaces.

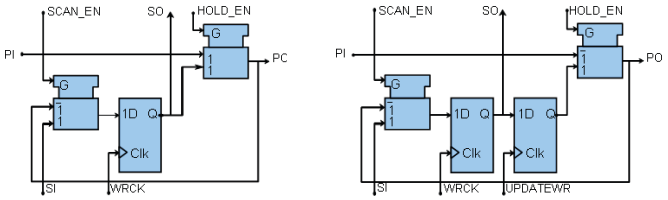

Figure 6: IEEE 1500-compliant WBR cells, (a) commonly used for embedded cores in 2D-SOCs, and (b) proposed for stacked dies in 3D-SICs.

5.2 Operating Modes

The test architecture has a number of test modes, which define the following settings.

- *Functional* / *Serial* / *Parallel* – non-test vs. test modes, resp. via serial or parallel test interface
- *Prebond* / *Postbond* – usage of dedicated test pads or TestElevators
- *Bypass* / *Intest* / *Extest* – selected test data register: bypass, all chains, or only the WBR chain
- *Turn* / *Elevator* – test responses from this die are fed via the TestTurn directly towards the bottom die or, via TestElevators, test responses from this die are transported up and responses from a higher-level die are transported down.

This leads to the following operating modes: *Functional*; *SerialPrebondBypassTurn*, *SerialPrebondIntestTurn*, *SerialPostbondBypassTurn*, *SerialPostbondIntestTurn*, *SerialPostbondExtestTurn*, *SerialPostbondBypassElevator*, *SerialPostbondIntestElevator*, *SerialPostbondExtestElevator*; *ParallelPrebondBypassTurn*, *ParallelPrebondIntestTurn*, *ParallelPostbondBypassTurn*, *ParallelPostbondIntestTurn*, *ParallelPostbondExtestTurn*, *ParallelPostbondBypassElevator*, *ParallelPostbondIntestElevator*, *ParallelPostbondExtestElevator*. A bottom die does not implement the pre-bond operating modes, as a bottom die does not have dedicated test pads.

Combining instructions for the various dies in a stack allows us to test one, multiple, or all dies simultaneously, as well as test one, multiple, or all layers of TSV-based interconnects simultaneously. This gives the same test scheduling options as the single daisychain TAM for 2D-SOCs [26].

Loading instructions into a WIR of a die-level wrapper is similar to what is known from IEEE 1500-compliant cores in 2D-SOCs. While a new instruction is shifted into the WIR, the previous instruction remains valid; only once fully arrived in place, the new instruction is activated by pulsing the UPDATEWR signal. In IEEE 1500, the WIRs of multiple IP cores are to be concatenated in a single WIR chain, which allows different cores to be loaded with different instructions. For 3D-SICs, a single concatenated WIR chain might become very lengthy, especially in case the individual dies are core-based SOCs [27] with their own concatenated WIR chain segments. Hence, we propose an hierarchical WIR mechanism, which opens up as needed, similar to a harmonica. Initially, the WIR chain only consists of the die-level WIRs. Once loaded with die-level instructions, the core-level WIR chain segments are included in the overall WIR chain for only those dies for which one of the *InTest* instructions was given; subsequently, further core-level WIR instructions can be loaded. Figure 7 schematically shows this concept by means of an example. The orange arrows highlight the active WIR chain. In this example, Dies 2 and 3 are in an *InTest* mode and hence, the WIR chain also includes the WIRs of their cores, resp. WIRC + WIRD and WIRE + WIRF. The benefit of this hierarchical WIR mechanism is that we prevent an unbridled growth of the WIR chain length; at any moment, the WIR is as long as needed. The cost is the requirement for the user to keep track of the current WIR chain length and a more complex procedure for loading instructions.

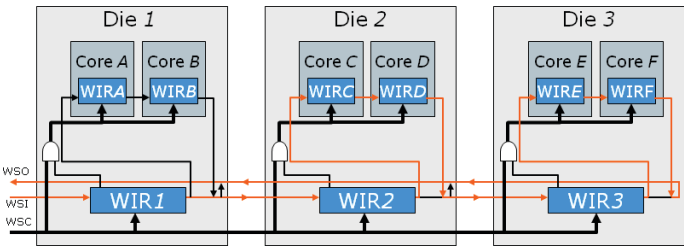

Figure 7: Hierarchical WIR chain, which has opened up for Dies 2 and 3, which are in one of their *Intest* modes.

Figures 8 and 9 show two examples of a 3D-SIC in which neighboring dies are in different operating modes. In Figure 8, Die $(x-1)$ is in its *ParallelPostbondBypassElevator* mode, while Die x is in its *ParallelPostbondIntestTurn* mode. This means that Die x is currently being tested, while the test data passes up and down in the stack through Die $(x-1)$. The orange arrows in the figure highlight the test data flow.

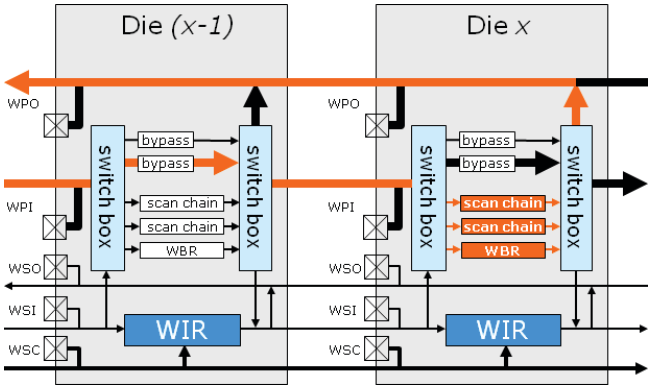

Figure 8: Example in which Die x is being tested; Die $(x-1)$ is in *ParallelPostbondBypassElevator* mode and Die x is in *ParallelPostbondIntestTurn* mode.

In Figure 9, Die $(x-1)$ is in its *ParallelPostbondExtestElevator* mode, while Die x is in its *ParallelPostbondExtestTurn* mode. This means that the TSV-based interconnects between Dies $(x-1)$ and x are currently

being tested. The orange arrows in the figure highlight the test data flow.

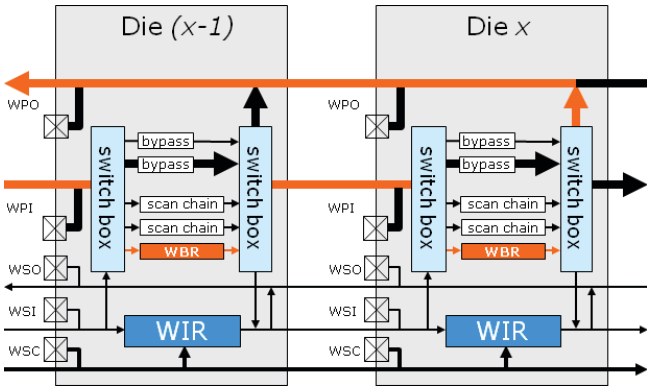

Figure 9: Example in which the TSV-based interconnects between Dies $(x-1)$ and x are being tested; Die $(x-1)$ is in *ParallelPostbond-ExtestElevator* mode and Die x is in *ParallelPostbondExtestTurn* mode.

6 Conclusion

In this paper, we presented a generic test access architecture for TSV-based 3D-SICs. The architecture supports a modular test approach, in which dies and their embedded cores, as well as inter-die interconnects, can be tested separately. The architecture leverages (1) existing intra-die DfT features such as internal scan, test data compression, built-in self-test, and core-based wrappers and TAMs, as well as (2) boundary scan at the 3D-SIC's PCB interface.

A main component of the 3D-SIC test access architecture is a die-level wrapper. This wrapper is based on IEEE 1500, extended with three novel features: (1) dedicated probe pads for all IEEE 1500 test control and data signals on non-bottom dies, to facilitate pre-bond die testing; (2) TestElevators that transport the IEEE 1500 test control and data signals up and down during post-bond stack testing; and (3) a hierarchical WIR chain to prevent unbridled growth of its length.

The proposed architecture is *structured*, as it provides a common DfT template that meets all 3D-SIC test access requirements. The proposed architecture is also *scalable*, in the sense that it works for all stacks heights and provides user-defined test access bandwidth; the latter provides a trade-off opportunity between silicon area and test length. Future work is to automate the EDA tool flow for DfT insertion and test expansion, and to exploit the optimization opportunities that are offered, by careful parameter selection for the switch box in the die-level wrappers.

Given that it is likely that multiple companies contribute to the manufacturing of a single 3D-SIC, standardization of the die-level test access features makes sense. The proposed test access architecture serves as an excellent starting point for standardization: "IEEE 1500.3D". It is based on the already existing standard IEEE 1500, and only requires a few specific extensions of that standard. Standardization might require to fix the parameters n and m to standardized values, such as 16, 32, or 64. For real plug-and-play test interoperability between dies from different sources, it is required that the inter-die test interconnections are defined not only electrically, but also with respect to their x, y layout locations. If a single DfT standard is to serve 3D-SICs of different footprint size, it seems beneficial to concentrate the TestElevators in the center of their layout. A 3D-SIC DfT standard should also be accompanied by a description format for transfer of DfT and test 'knowledge' like the IEEE 1149.1 Boundary Scan Description Language (BSDL) [12, 13] and/or IEEE 1450.6 Core Test Language (CTL) [28, 29].

This paper focused on a digital test access architecture for factory production tests. Future work includes extension of the architecture to support debug and diagnosis, making embedded test instruments available to system-level 3D-SIC users, and inclusion of analog tests.

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