SOC Test Architecture and Method for 3-D ICs

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***Abstract*—3-D integration provides another way to put more devices in a smaller footprint. However, it also introduces new challenges in testing. Flexible test architecture named test access control system for 3-D integrated circuits (TACS-3D) is proposed for 3-D integrated circuits (IC) testing. Integration of heterogeneous design-for-testability methods for logic, memory, and through-silicon via (TSV) testing further reduces the usage of test pins and TSVs. To highly reuse pre-bond test circuits in post-bond test, an innovative linking mechanism shares TSVs and test pins of the 3-D IC. No matter how many layers are there in the 3-D IC, a large portion of TSVs and test pins is reserved for data application. Therefore, smaller post-bond test time is expected. A test chip composed of a network security processor platform is taken as an example. Less than 0.4% test overhead increases in area and time between 2-D and 3-D cases. Compared with the instinctively direct access, TACS-3D reveals up to 54% test time improvement under the same TSV usage.**

***Index Terms*—3-D IC test, system-on-chip (SOC) test, test architecture, test integration.**

I. Introduction

Until recently, the semiconductor industry has to face the bottleneck of complementary metal oxide semiconductor (CMOS) technology scaling and soaring system-on-chip (SOC) development cost. The delay and power consumption issues of global interconnects become the main barriers of further performance progress under allowable cost [1]. By stacking dies vertically and connecting them with through-silicon vias (TSVs), 3-D integration solves this problem effectively. However, there are still obstacles to its commercial application. Tools and methodologies for 3-D integrated circuit (IC) testing are regarded as the number-one challenge [2].

Both pre-bond and post-bond tests [3] avoid dispensable loss during 3-D IC construction. Pre-bond test provides known-good-dies (KGDs) to be stacked, while post-bond test filters out the defects newly introduced in the bonding processes. However, 3-D IC testing faces more difficulties in test access [2] and higher demands in efficiency of test inputs/outputs (IOs) and TSVs. Since different layers are connected through TSVs instead of wire-bonding, extra pads dedicated to find KGDs are required in wafer probing. Furthermore, most cores are accessible only through TSVs when dies are bonded. The congestion of test pins and TSVs is aggravated especially when the layers of the 3-D IC increase. Therefore, the efficiency of TSVs and IO pins should be emphasized in both pre-bond and post-bond tests.

Research on 3-D IC testing is emerging recently. Lewis and Lee [3] propose scan-island based test architecture which focuses on functional blocks crossing multiple layers of the 3-D IC. For 3-D SOCs with entire cores in the same layer, test reuse is more attractive. Wu *et al.* [4] propose test access mechanism (TAM) optimization for core-based 3-D SOCs under the non-trivial constraints related to the number of TSVs and the thermal limits. They highlight the post-bond test time minimization, therefore the pre-bond test is not discussed in their test architecture and the context. When the layers increase, applying post-bond test only can lead to the exponential decay in the yield of the final product [3]. Jiang *et al.* [5] optimize the summation of pre-bond and post-bond test time of 3-D ICs. However, they neglect the required TSVs in their scheduling results, claiming that the size of TSVs can be reduced to μm^2 range. To maximize the advantages of 3-D integration, the tradeoff between total test time and the cost due to required TSVs needs careful consideration. Furthermore, both [4] and [5] consider the IOs and the TSVs for applying test data only. They do not discuss the controller and its complexity. However, it is not easy to operate multiple TestRails [6] or Test Buses [7] arbitrarily with a single controller in 2-D SOC. The situation becomes worse when they cross multiple layers of the 3-D IC. Therefore, the IO pins and TSVs for control signals cannot be neglected when the number of TestRails or Test Buses increases in 3-D IC testing.

In this paper, we propose a test architecture for pre-bond and post-bond tests in core-based 3-D ICs. Both control signals and TAM are optimized in test pins and TSVs for 3-D IC testing. For pre-bond test, test access control system for 3-D ICs (TACS-3D) reuses TACS [8] for SOC test, with all the cores in the same layer. This is similar to 2-D SOC testing. Since TACS has optimized the test pin usage, TACS-3D can minimize the extra pads dedicated for finding KGDs. To highly reuse pre-bond test circuits in the post-bond test, an innovative linking mechanism is proposed for sharing TSVs and test pins between embedded cores in multiple layers. No matter how many layers are there in the 3-D IC, only 5-bit signals are sufficient for test control. A large portion of TSVs and test pins can be reserved for data application, therefore smaller total test time is expected. In addition, integration of heterogeneous design-for-testability (DFT) methods for logic, memory, and TSV testing further alleviates the congestion of test pins and TSVs for post-bond test. A test chip composed of a network security processor (NSP) platform is taken as an example. Less than 0.4% test overhead increases in both area and time between 2-D and 3-D cases. Compared with the instinctively direct access, TACS-3D also reveals up to 54% test time improvement under the same TSV usage.

II. Preliminaries and Motivation

Fig. 1(a) shows a typical flow considering the yield of final product for 3-D ICs. Before the dies are bonded together to construct 3-D ICs, pre-bond test is applied to find KGDs. After KGDs are obtained, they are bonded layer by layer based on the die-to-die, die-to-wafer, or wafer-to-wafer bonding technologies. Every time a KGD is bonded on the top layer of the stacked chips, TSV testing is performed between any two layers. It can verify the vertical connection of the stacked chips. As long as its thermal limit is not violated, we prefer

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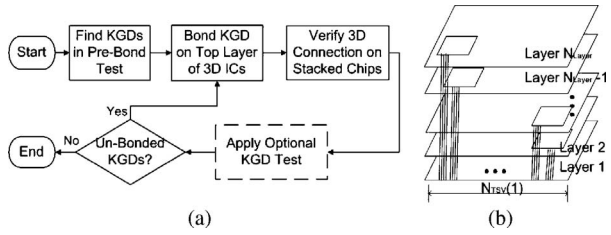

Fig. 1. (a) Typical flow considering the yield of final product for 3-D ICs. (b) Directly access the test architecture of different layers through TSVs.

to test all the TSVs concurrently for smaller total test time. If necessary, we also perform optional KGD tests for currently stacked chips. Once the faulty components are found, we apply related remedies immediately or abandon them to prevent the further loss. Since this flow is performed iteratively during 3-D IC construction, flexible test architecture and cost-effective test scheme are urgent to pursue competitive 3-D ICs.

We assume that the access of the stacked chips during post-bond test is through the bottom layer of the 3-D IC [4]. Without special arrangement for reusing pre-bond test circuits in its post-bond test, people use TSVs to access test ports in each layer instinctively like Fig. 1(b). There are total N_{Layer} layers in the stacked chips, while W_{Ctrl_j} and W_{TAM_j} stand for the control signals and TAM width dedicated for layer j. According to Fig. 1(b), the total number of TSVs required for the control signals and TAM width through layer i is

$$N_{\text{TSV}}(i) = \sum_{j=i+1}^{N_{\text{Layer}}} W_{Ctrl\_j} + 2 \times \sum_{j=i+1}^{N_{\text{Layer}}} W_{TAM\_j}. \quad (1)$$

The total number of TSVs required in 3-D ICs is

$$N_{\text{TSV}} = \sum_{i=1}^{N_{\text{Layer}}-1} N_{\text{TSV}}(i). \quad (2)$$

In this case, the bottom layer suffers the most congestion of TSVs (and also test pins) regardless of the test architecture. The total number of TSVs through the bottom layer is $N_{\text{TSV}}(1) = \sum_{j=2}^{N_{\text{Layer}}} W_{Ctrl\_j} + 2 \times \sum_{j=2}^{N_{\text{Layer}}} W_{TAM\_j}$. Therefore, we urge for a scalable test architecture and a linking mechanism with cost-effective usage of TSVs and IO pins in 3-D IC testing. Both control signals and TAM need optimization to reduce the test cost in the iterative flow like Fig. 1(a).

III. TACS-3D and Proposed Test Configurations

A. TACS-3D—Test Integration of 3-D SOC

Our previous work—TACS [8] has optimized IO pins to test embedded cores based on IEEE 1500 [9] Test Wrapper in 2-D SOCs. To reduce TSVs and IO pins in 3-D IC testing, TACS-3D inherits an extended JTAG/IEEE 1149.1 [10] TAP Controller and multiplexer-based TAM buses. Built-in self-test (BIST)-based methods and TSV testing are also integrated in this paper for the same purpose. Fig. 2 shows the block diagram of TACS-3D. Only five pins (TCK, TRST, TMS, TDI, and TDO [8]) are sufficient to control the test operations before and after the bonding processes. Other ports,

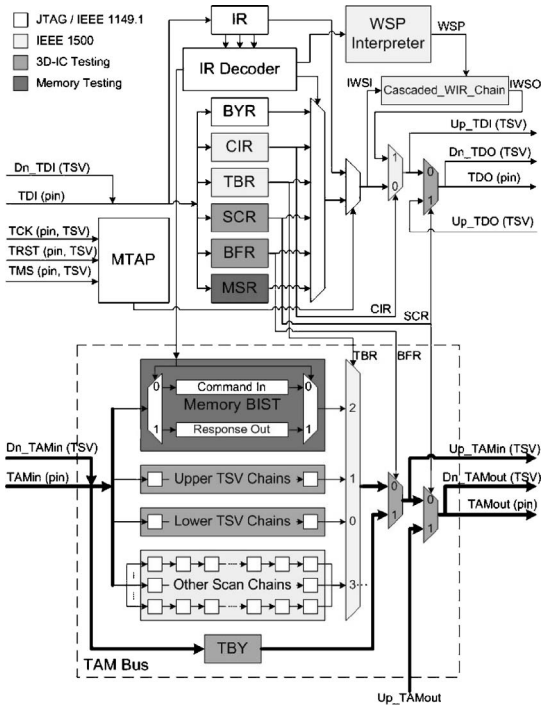

Fig. 2. Block diagram of TACS-3D.

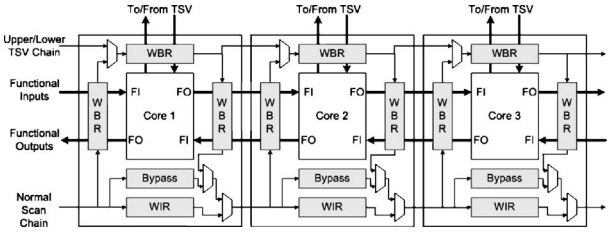

Fig. 3. Reused IEEE 1500 Test Wrapper for TSV testing.

such as Up/Dn_TDI, Up/Dn_TDO, Up/Dn_TAMin, and Up/Dn_TAMout, are used for post-bond test access between the neighboring layers.

For logic testing, TACS-3D obtains the robustness of TACS that features the IEEE 1500 Wrapper Control, hierarchical test control, at-speed test (for transition faults), functional and scan test, heterogeneous test protocols, and so on [8]. A finite state machine having the same state diagram of JTAG TAP controller is named MTAP. According to the MTAP state and instruction register, wrapper serial port (WSP) interpreter generates WSP signals for 1500 Test Wrapper. Core identity register connects the TDI–TDO path to directly access the wrapper instruction registers (WIRs) of all the embedded cores, while TAM bus register (TBR) arbitrates TAM buses for test switching. The Cascaded_WIR_Chain stands for the cascade of all WIRs in the current layer. Single/cascade register (SCR) and bypass flag register (BFR) decide the connection of TDI–TDO path and TAM buses between neighboring layers. Memory built-in self-test (MBIST) is taken as an example to support BIST-based methods in TACS-3D. MBIST start register (MSR) triggers the operations of MBIST, while the CommandIn and ResponseOut store the programmable commands and corresponding responses.

TACS-3D also reuses 1500 Test Wrapper to do TSV testing, and Fig. 3 shows its detailed configuration. The upper TSV chains only connect all the wrapper boundary register cells whose corresponded inputs (outputs) are from (to) the upper layer through TSVs. In a similar way, the lower TSV chains only connect all of them related to lower layer through TSVs. These two types of scan chains are only configured during the TSV testing. All the above techniques contribute to the reduction of TSVs and test pins.

B. Configuration of TACS-3D in Pre-/Post-Bond Test

Fig. 4(a) shows the configuration of TACS-3D in pre-bond test. Since test circuits are completely implemented in every layer of 3-D ICs, KGD test is applied as 2-D SOC testing [8]. Before pre-bond test, both SCR and BFR are reset to 0 by setting asynchronous TRST = 0 or TMS = 1 for five cycles [10].

By taking parallel TSV testing as an example, Fig. 4(b) shows the configuration of TACS-3D to activate the tests in all three layers during post-bond test. TCK, TRST, and TMS are broadcast to its test controllers in three layers, while TDI, TDO, TAMin, and TAMout are connected to the neighboring layers through Up/Dn_TDI, Up/Dn_TDO, Up/Dn_TAMin, and Up/Dn_TAMout. All the SCRs are set to 1 (except the top-most layer) and then we have the cascade of TDI–TDO paths across all three layers of the 3-D IC. In a similar way, all the BFRs are set to 0 for applying test data through the vertical TAM buses. This configuration greatly reduces the required TSVs for control signals and TAM, and the TSVs required for TACS-3D through layer i are

$$N_{\mathrm{TSV}}(i) = 5 + 2 \times \max_{i+1 \le j \le N_{\mathrm{Layer}}} W_{TAM\_j}. \tag{3}$$

The TSVs required in the bottom layer of TACS-3D are $N_{\mathrm{TSV}}(1) = 5 + 2 \times \max_{2 \le j \le N_{\mathrm{Layer}}} W_{TAM\_j}$.

Fig. 4(c) shows an example of applying optional KGD test to the top layer of the stacked chips. For those idle layers during post-bond test, BFRs are set to 1 and their TDI–TDO paths are connected to 1-bit bypass registers (BYR) [10]. Therefore, TACS-3D can reduce the redundant cycles in post-bond test. In this case, TACS-3D can reuse pre-bond test circuits in post-bond test by testing different layers sequentially. In addition, TACS-3D supports a test architecture for sharing available TSVs and test pins during post-bond test. Its configuration can be any combination of Fig. 4(b) and (c) by specifying SCRs, BFRs, and TBRs. SCRs and BFRs select the layers to be accessed, while the TBRs select the detailed allocation and arbitration of TAM buses for embedded cores. The cascade of TDI-TDO paths and the vertical TAM buses apply control signals and test data for embedded cores in multiple layers. Although TACS-3D allows sharing of TSVs and test pins in post-bond test, we cannot test multiple layers in parallel with the maximum TAM width for every layer. The summation of the required TAM widths for embedded cores does not exceed the total TAM width in its bottom layer. Compared with (1) and (3) under the same TSV and test-pin usage, TACS-3D reserves more width for data application especially when the

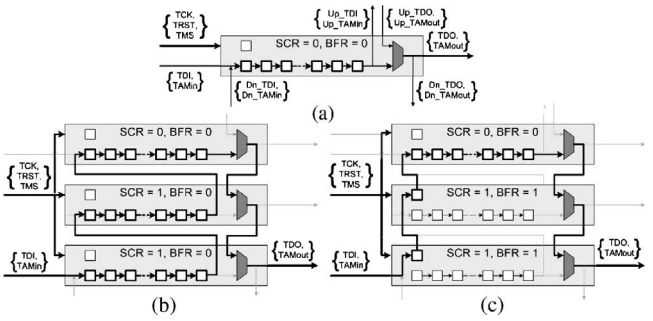

Fig. 4. Examples of TACS-3D configuration. (a) Find KGD in pre-bond test. (b) Apply parallel TSV testing between the neighboring dies. (c) Apply optional KGD test in the top-most die.

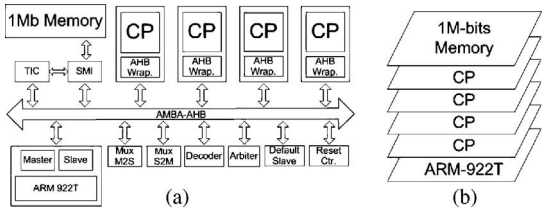

Fig. 5. NSP platform with four CPs. (a) Block diagram. (b) Way of 3-D stacking.

layers of the 3-D IC increase. Therefore, the smaller test time is expected.

If post-bond test time is the major concern [4], all embedded cores of the 3-D IC are scheduled together with available test pins in the bottom layer. By adopting the hybrid configuration of Fig. 4(b) and (c), we use the cascade of the TDI-TDO paths and the vertical TAM buses to do test control and data application. Therefore, the required TSVs in an individual layer of the 3-D IC are also limited to the available unassigned test pins. In this case, the scheduling algorithm of [11] for traditional 2-D SOCs can be transformed for 3-D IC testing just by further considering its thermal limitation. The scheduling results always limit the required TSVs in an individual layer to the number of available test pins. In pre-bond test, we do only on-chip scheduling with the available pins for pre-bond test in an individual layer. In order to reuse pre-bond test circuits during post-bond test, the required TSVs (or test pins) of TACS-3D through layer i is $N_{\mathrm{TSV}}(i)$ in (3).

IV. Experimental Result

A test chip composed of our NSP platform [12] with four crypto processors (CPs) is used for TACS-3D and the proposed test scheme. Fig. 5(a) shows its block diagram including an ARM-922T host processor, four CPs, a 1M-bit DRAM, a test interface controller (TIC), a static memory interface and the basic components of an advanced microcontroller bus architecture (AMBA) advance high-performance bus (AHB). Fig. 5(b) shows its 3-D architecture.

The proposed test scheme for the target system is described as follows. The ARM-922T is a legacy core which is tested with the authorized test patterns through its JTAG ports; every CP layer that includes two advanced encryption standard (AES) cores, two keyed-hash message authentication code (HMAC) cores, and one RSA core is tested with IEEE 1500

TABLE I
TEST INFORMATION OF EMBEDDED CORES IN CP

Core	FI	FO	Scan Cells	Test Patterns	TSVs
AES × 2	49	37	2807	210	88
HMAC × 2	46	37	1688	312	83
RSA	53	36	6156	172	91

Test Wrapper and the logic testing flow of TACS-3D; the 1M-bit memory layer combined with MBIST is tested with the memory testing flow of TACS-3D during post-bond test; the AMBA-AHB components distributed in four CP layers are tested with scan patterns as glue logics; the functional TSVs of the stacked chips are tested in the way of Fig. 3. Table I shows the information of embedded cores in CP layer. The first column is the core name and its amount. The second and third columns show the number of functional inputs (FI) and outputs (FO). The fourth column shows the number of scan cells, while the fifth column lists the number of test patterns. The last column shows the number of TSVs tested with Fig. 3. Additionally, each core has a functional clock, a scan enable, and an asynchronous reset signal.

A. Analysis of Test Architecture for 2-D and 3-D SOCs

Table II shows the analysis of test architecture for 2-D and 3-D SOCs. Our previous work TACS and the proposed TACS-3D are compared in the domain of area overhead, test time, and test pin usage among logic and memory testing.

For logic test, we equalize the available test pins for these two test cases. Then, we check its test time, test pin usage, and the related area overhead for applying test. The area information of embedded cores for traditional 2-D SOC testing (i.e., using TACS) and TACS-3D is revealed in the first part of Table II. The original design and the test wrapper for these embedded cores are listed in column 2 to column 4. The related test controller and the TAM buses are shown in columns 5 and 6, respectively. Finally, column 7 shows the sum of columns 2–6. By taking AESx8 as an example, their test wrappers increase 24 032 − 23 204 = 828 gates from TACS to TACS-3D. Since we reuse 1500 Test Wrapper for TSV testing, extra two multiplexers are required per core for every 1-bit TAM to switch between upper/lower TSV chains and normal scan chains. In this example of AESx8, the total width of TAM is 16. Therefore, we need 2 × 8 × 16 = 256 multiplexers. In addition, the 1500 Test Wrapper requires further extension to support TSV testing configuration. Thus, this technique increases the area overhead in TACS-3D. However, the percentage of area overhead has just 0.1% to 0.27% increase in test wrapper for different cores.

When we mention the increase in test architecture involving test controller and the TAM buses, the area overhead for TACS-3D is almost three times of that in 2-D SOC test scheme. The area overhead of test controller and the TAM buses in TACS is 388 + 1141 = 1529 gates, while that in TACS-3D is 1618 + 2876 = 4494 gates. This is resulted from implementing TACS-3D to all the layers of 3-D ICs. But the overall area increase of the test architecture is just 3.81 − 3.50 = 0.31%. Under the constraint of the same test-pin usage in these two test architecture, they almost have the same performance. The test time of TACS is 869 258 cycles, while that of TACS-3D is 868 947 cycles. This information is listed in column 2 of the third part of Table II. Although these two test schemes use the same number of test pins, TACS-3D requires additional (5+2×16)×4 = 148 test TSVs in four-layer CPs.

TABLE II
COMPARISON BETWEEN 2-D AND 3-D TEST ARCHITECTURE

Area Overhead in Logic Test

	AESx8	HMACx8	RSAx4	Ctrler	TAM	Total
Orig.	777 360	351 832	581 384	–	–	1 710 576
Traditional 2-D SOC Test (TACS)						
Wrap.	23 204	22 693	12 376	388	1141	59 865
(%)	2.99	6.45	2.13	–	–	3.50
SOC Test Flow of Logic on 3-D ICs (TACS-3D)						
Wrap.	24 032	23 464	13 144	1618	2876	65 134
(%)	3.09	6.72	2.26	–	–	3.81

Area Overhead in Memory Test

	1Mb Memory	Ctrler	TAM	Total
Original	609 100	–	–	609 100
MBIST in 2-D SOCs				
MBIST	5876	0	0	5876
(%)	0.96	–	–	0.96
SOC Test Flow of Memory on 3-D ICs (TACS-3D)				
MBIST+adap.	6793	387	429	7609
(%)	1.12	–	–	1.25

Test Time and Test Pin Usage

	Logic Test		Memory Test	
	Time (Cycles)	Pin (#)	Time (Cycles)	Pin (#)
TACS or MBIST	869 258	37	303 532	8
TACS-3D	868 947	37	304 669	0
Overhead (%)	−0.04	0	0.37	–

For memory test, we analyze the overhead of translating MBIST to post-bond memory test flow of TACS-3D. The second part of Table II shows the area overhead in memory test. Its second column shows the area of the original memory, MBIST, and the MBIST+adapter (CommandIn and ResponseOut). The area of test controller and the TAM buses are shown in columns 3 and 4, respectively. The area overhead of "adapter+test controller+TAM buses" contributes to total 7609 − 5876 = 1733 gates increase and 1.25 − 0.96 = 0.29% of its original area. The related test time is shown in column 4 of the third part in Table II. The test time of TACS-3D has 304 669−303 532 = 1137 cycles increase. This is resulted from applying six times MBIST commands in this test example. Among this extra timing overhead, Adapter uses 282 cycles and the application of TACS-3D uses 855 cycles. However, the test pin usage of applying MBIST with TACS-3D is reduced to 0 due to the integration.

B. Analysis of Test Interface Configuration in Post-Bond Test

In this section, we analyze the efficiency of TSVs and test pins for TACS-3D in post-bond test of 3-D ICs. As we mentioned in the second paragraph of Section IV (before Section IV-A), ARM-922T is tested with the authorized test patterns through its JTAG ports. Therefore, post-bond test for the stacked CP layers is through the IOs of the bottom layer—

TABLE III
TEST TIME COMPARISON CONSIDERING TSVS FOR DATA APPLICATION AND RELATED CONTROL SIGNALS

Available test TSV	32	48	64	80	96	112	128
Scan Chain Number = 16							
Proposed scheme	1 184 968	726 444	544 608	431 044	396 880	296 240	296 240
Direct control	2 291 678	1 345 472	669 169	602 814	399 283	399 283	301 512
Time impr. (%)	48.29	46.00	18.61	28.49	0.60	25.81	1.75
Scan Chain Number = 32							
Proposed scheme	1 082 968	693 992	532 528	399 972	344 980	296 240	265 420
Direct control	2 291 678	1 156 943	652 893	592 498	383 141	366 240	269 180
Time impr. (%)	52.74	40.02	18.44	32.49	9.96	19.11	1.40
Scan Chain Number = 64							
Proposed scheme	1 044 604	692 384	500 052	399 048	322 124	272 928	264 168
Direct control	2 276 776	1 028 585	625 484	498 637	383 141	366 240	269 180
Time impr. (%)	54.12	32.69	20.05	19.97	15.93	25.48	1.86
Dynamically Configuring Scan Chains with Available W_{TAM}							
Proposed scheme	1 033 676	644 208	466 536	367 140	304 692	254 292	223 220
Direct control	2 237 416	959 436	614 504	451 688	357 844	295 956	250 548
Time impr. (%)	53.80	32.86	24.07	18.72	14.85	14.07	10.91

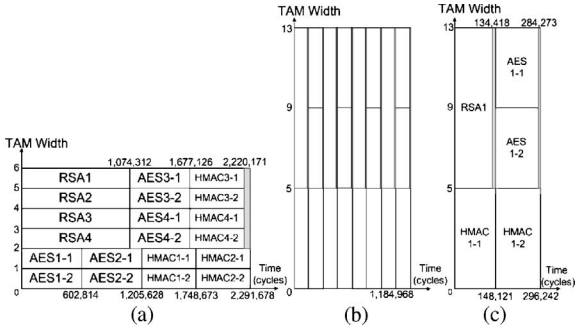

Fig. 6. Experimental result (SC = 16, TSV = 32). (a) Direct control. (b) Proposed TACS-3D. (c) Detailed result of (b).

ARM-922T. In this test case, the efficiency of available TSVs in the bottom layer can be regarded as that of the available test pins. Both TAM and control signals are considered between the direct access scheme [shown in Fig. 1(b)] and our proposed configuration of TACS-3D. Fig. 6 shows a result of using 32 test TSVs (or test pins) in the bottom layer of 3-D ICs, and all the embedded cores of CPs are configured to 16 scan chains (SC = 16) in this example.

For direct access, the control signals for every layer of 3-D ICs must be reserved to concurrently activate tests in multiple layers. Since there are total four CP layers in the example of Fig. 5(b), its maximum available TAM width is $(32-5\times4)/2 = 6$ by using JTAG-based test controller. Its best scheduling result is 2 291 678 cycles and the detailed information is shown in Fig. 6(a). For the same TSVs in its bottom layer (or test pins) using TACS-3D, the maximum TAM width is $\lfloor(32-5)/2\rfloor = 13$. Therefore, it has much shorter time of 1 184 968 cycles in post-bond test and 48.29% improvement. The details of scheduling result are also shown in Fig. 6(b) and (c). Other scheduling results considering the combination of scan-chain number in embedded cores and the TSVs in its bottom layer are listed in Table III. The available TSVs range from 32 to 128, while the scan chains of embedded cores are configured to 16, 32, 64, and the maximum available TAM width. According to (1) and (3), TACS-3D can reserve more TSVs or test pins for data application. Therefore, it can have much shorter post-bond test time.

V. CONCLUSION

We have proposed a scalable and flexible test architecture—TACS-3D for 3-D IC testing. The usage of TSVs and test pins for control signals and TAM is optimized by the linking mechanism shown in Fig. 4, while tests of embedded cores are applied through the cascade of TDI–TDO paths and the vertical TAM buses. Only a small constant of control signals is sufficient, and major portion of TSVs and test pins is reserved for data application. From the experimental results in Section IV, less than 0.4% overhead increases in both area and time between 2-D and 3-D test cases. Up to 54% of test time improvement is shown in the comparison between TACS-3D configuration and instinctively direct access. In addition, heterogeneous DFT methods for logic, memory, and TSV testing are also integrated to further reduce test pins and TSVs during 3-D IC testing. A TSV testing method that reuses 1500 Test Wrapper was also proposed.

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