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Optimum Test Schedule for SoC with Specified Clock Frequencies and Supply Voltages

Vijay Sheshadri, Vishwani D. Agrawal and Prathima Agrawal
Department of Electrical and Computer Engineering
Auburn University
Auburn, AL 36849, USA
Email: {vijay, agrawvd, agrawpr}@auburn.edu

***Abstract*—Testing of a system-on-chip (SoC) consists of a schedule of test sessions. In each session, a subset of cores of the SoC is tested such that the peak power consumption of each core as well as that of the entire SoC remain under specified limits. Traditional methods assume fixed test frequency and supply voltage (V_{DD}) and group core tests into sessions such that the overall time of the schedule is minimized. In this work, we assume that each test session can be assigned its own clock frequency and V_{DD}, which are related through the critical path delay constraint and together determine the power consumption. Integer linear programming (ILP) is used to find optimal test schedules with lower test time than was possible before. We show that the test time of ASIC Z, for which the best previously published time is 300 time units, is reduced to 155 units by optimally selecting the clock frequency and V_{DD} for each session.**

***Keywords*-SoC testing; Test scheduling; Integer Linear Programming;**

I. Introduction

A system-on-chip (SoC) may contain an entire system integrated onto a single chip. Such an SoC is often implemented by embedding reusable blocks called cores. The cores can be a variety of intellectual property blocks, such as digital logic, processor, memory, and analog or mixed signal circuit. As technology advances, a larger number of cores can be accommodated on an SoC device [2]. The resulting increase in the complexity of SoC devices has led to high volumes of test data and long test times. Reducing test time has become a major objective in SoC testing research.

The SoC testing problem can be divided into three parts: test access mechanism (TAM) design/optimization, core wrapper design/optimization and test scheduling [22]. TAM is an on-chip structure that provides test access to the cores and is responsible for transporting test data to and from cores. TAM design involves trade-offs between the transport capacity of the mechanism and the test application cost incurred in terms of test time, area overhead, etc. An optimized TAM leads to a more efficient on-chip test data transport. A flexible TAM architecture is often assumed, in order to achieve better optimization. Some of the earlier work formulates the test time as a function of TAM width and optimizes TAM allocation among cores, to achieve test time minimization [7], [10], [11], [20]. The core wrapper forms the interface between the TAM and cores. The wrapper may also perform serial-parallel or parallel-serial conversion to provide width adaptation in case of a mismatch between the available TAM width and the core input/output terminals. IEEE P1500 [1] defines a standardized, scalable and configurable core wrapper for efficient test isolation and ease of test access. Several wrapper optimization techniques [9], [13] as well as wrapper-TAM co-optimization approaches [7] have been proposed.

Test scheduling is a process of selecting sets of time-compatible tests of a system, for execution. The tests that can be applied concurrently are referred to as time-compatible tests [4]. The concurrent execution of a set of tests is possible only if there are no resource conflicts among them. Such compatible tests are scheduled into test sessions; the time taken by the session to complete execution is referred to as test length whereas the power dissipated during the test session is called the test power. The test scheduling problem must find an optimal test schedule for a given set of tests and their resources, such that the total test time is minimized while satisfying the resource constraints of each test.

The power dissipation during the test mode is often higher than that in the system mode because a larger number of signals switch during test. Therefore, care must be taken while testing multiple cores concurrently so that the combined test power does not exceed the maximum power limit of the SoC. Power-aware test strategies have been developed in order to efficiently test an SoC under a given power limit [5]. One of these strategies is power-constrained test scheduling, where multiple tests are scheduled to run simultaneously in sessions in such a way that the test time is minimized while considering test power constraints and test resource conflicts [4], [6], [11], [14], [20]. A power budget is often specified for the SoC under test. This defines the maximum power that can be dissipated at any time during the test. The problem of power-constrained test scheduling has been tackled, in the past, using various optimization methods [7], [22]; integer linear programming (ILP) is one such method. ILP models have been developed to describe the non-partitioned test scheduling problem and obtain optimized test

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schedules for given power and resource constraints [3]. In [18], it is shown that test time minimization can be achieved, under a given power constraint, by adopting variable clock frequencies for each test session in the SoC test schedule. For this, test time and test power are expressed as functions of the test clock frequency. The ILP model for the nominal clock rate test-scheduling problem is modified to incorporate a term that corresponds to the operating frequency of each session. Several papers [8], [17] have examined similar problems. While the work in [17] is focused, specifically, towards multi-channel ATE, our method can be applied to single-channel ATE as well. Also, the work presented in this paper is directed toward a single-V_{DD} design whereas [8] addresses multiple-V_{DD} voltage islands.

In this paper, we invoke the concept of customizable test clock rates and find an optimal V_{DD} value at which a better test time minimization can be obtained. Since the operating voltage influences the power dissipation in the circuit as well as the circuit delay, this voltage can be manipulated to obtain a reasonable compromise between the power and delay of cores in the SoC and allow the tests for the cores to execute at a faster clock rate, hence reducing the total test time. The authors in [19] also show similar trends in their experiments on ISCAS benchmark circuits. The rest of the paper is organized as follows: Section II begins with a list of symbols used throughout the paper and then provides an integer linear programming (ILP) model for optimization of test schedules. Section III discusses applications of the method and gives experimental results. Section IV concludes the paper.

II. ILP Formulation

The terms and symbols used in this paper are listed in Table I. In this section, we describe an integer linear programming (ILP) model for optimizing the test time under power constrain. We define the power budget for an SoC, P_{max}, as the maximum allowable power dissipation during the testing of SoC. Let there be n cores, $C_1, \cdots, C_n$ in the SoC and let the test corresponding to core C_i be t_i, where $i \in 1, 2, \cdots, n$. Each test is associated with test time (referred to as test length throughout this paper) and test power. Let L_{t_i} and P_{t_i} be the length and power of the test t_i. Let the tests, $t_1, \cdots, t_n$, be distributed among k sessions, $S_1, \cdots, S_k$ such that each session, S_j contains one or more tests. The test length of a session S_j, given by $L_{S_j} = \max(L_{t_i} | \forall t_i \in S_j)$ and the power dissipated during session S_j is given by $P_{S_j} = \sum(P_{t_i}), \forall t_i \in S_j$.

The classic test scheduling problem can be formulated as an ILP model (we will refer to this ILP model as $M1$):

Objective: Minimize $\sum_{j=1}^{k} L_{S_j} \cdot x_j$, where

$$x_j = \begin{cases} 1, & \text{if } S_j \text{ is scheduled} \\ 0, & \text{otherwise} \end{cases}$$

Table I
Symbols and their description.

Symbol	Description
t_i	i^{th} test of an SoC
S_j	j^{th} test session
L_{S_j}	test length(time) of session S_j
P_{S_j}	test power of session S_j
F_j	Frequency factor of session S_j
P_{max}	power budget of the SoC
P_{core}	maximum power limit of the core
$f(S_j)$	clock frequency of session S_j
$f(t_i)$	clock frequency of test t_i
V_{DD}	supply voltage
V_{TH}	threshold voltage
f_s	structurally constrained frequency limit of a core
f_p	power constrained frequency limit of a core
f_{s_j}	structural constraint on clock rate of session S_j
f_{p_j}	power constraint on clock rate of session S_j

Subject to: 1) Power constraint, $P_{S_j} \cdot x_j \leq P_{max}$, where P_{max} is the power budget for the SoC, and 2) Test completeness constraint that each test $t_i, i \in \{1, 2, \cdots, n\}$, is executed at least once.

It is assumed here that the test clock frequency throughout the entire testing process is constant and is decided by the maximum scan frequency of the slowest core. However, it has been shown that employing a variable clock frequency for testing of SoCs achieves a much better optimization [8], [17], [18]. Since frequency is directly proportional to the power consumed during test and inversely proportional to the test time, increasing the frequency of the test clock, in turn, increases the test power and lowers the test time. On the other hand, decreasing the frequency results in a reduction in the power and an increase in the test time for individual tests. However, due to reduced power, more tests can be scheduled in a single session thereby decreasing the total test time. Thus, a proper choice of clock frequency for a test session can reduce the overall test time and also maintain the test power under the power budget. In [18], the ILP model $M1$ is modified to include a new term, called *frequency factor*, that corresponds to the clock frequency of a test session. That ILP model (say, $M2$) is as follows:

Objective: Minimize $\sum_{j=1}^{k} (L_{S_j}/F_j) \cdot x_j$, where

$$x_j = \begin{cases} 1, & \text{if } S_j \text{ is scheduled} \\ 0, & \text{otherwise} \end{cases}$$

and F_j = frequency factor for session S_j
Subject to: 1) Power constraint, $P_{S_j} \cdot F_j \cdot x_j \leq P_{max}$, where

P_{S_j} is the test power of the session and P_{max} is the power budget for the SoC, and 2) Test completeness constraint, i.e., each test $t_i, i \in \{1, \cdots, n\}$, is executed at least once.

In both ILP formulations ($M1$ and $M2$) and in the present work, it is assumed that the SoC design for testability (DFT) infrastructure is already in place and that the TAM assignment and the wrapper design have been optimized. TAM resources, along with other test resources, may be shared among the core tests and as a result concurrent execution of tests may be hampered due to resource conflicts. As done previously by Chou *et al.* [4] and Sheshadri *et al.* [18], we make use of a test compatibility graph (TCG) to resolve the problem of test concurrency and resource conflicts. A TCG consists of nodes, representing tests, connected by edges; an edge indicates compatibility of the connected nodes (tests) and implies that both tests can be scheduled in the same session for a concurrent execution. The cliques and sub-cliques of the TCG form the possible test sessions; a subset of these sessions is selected as the test schedule, such that the total test time is optimized while satisfying the constraints mentioned in the ILP models $M1$ and $M2$. Further details on the mathematical formulation of the test schedule optimization can be found in [18].

The frequency factor F_j for a session is defined as the ratio of the clock frequency for the session to that of the slowest core, i.e., $F_j = \frac{f(S_j)}{f_0}$, where $f(S_j)$ is the frequency of operation of session, S_j and f_0 is the frequency of the slowest core in the SoC. A frequency factor greater than 1 for a session implies that the test clock frequency is being increased for that session, while a frequency factor less than 1 implies that the that the test clock frequency is being decreased for that session.

The frequency factor has two constraints: 1) $0 \leq F_j \leq \frac{P_{max}}{P_{S_j}}$. This limitation is derived, directly, from the power constraint of the ILP formulation. Hence, $\max\{F_j\} = \frac{P_{max}}{P_{S_j}}$. 2) Maximum clock rate of the slowest core tested in the session, i.e., $f(S_j) \leq \min\{f(t_i) | \forall t_i \in S_j\}$. The maximum frequency of every core is limited by a structural constraint (critical path) and a power constraint (maximum power dissipation limit of the core). Consequently, the maximum clock frequency of a session is decided by the maximum clock frequency of the slowest core in that session. Thus, $\max\{F_j\} = \min[\frac{\max\{f(t_i)\}}{f_0} | \forall t_i \in S_j]$.

The structural and power constraints that limit a core's maximum frequency are also influenced by the supply voltage. The power consumed varies with supply voltage and clock frequency as,

$$P \propto V_{DD}^2 \cdot f \tag{1}$$

This implies that power consumption can be reduced by lowering the operating voltage. As a result, the clock rate can be increased without exceeding the power constraint of the core. However, the delay of a circuit also varies with the voltage, as described by the α-power law [15], [16]:

$$delay \propto \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}} \tag{2}$$

The value of α is 2.0 for long-channel MOSFET and is approximately 1.3 for the present day short-channel MOSFET devices [15]. As seen from expression (2), reducing the voltage causes the delay to increase, which in turn, slows down the execution speed and hence results in a longer test time. Thus, as we reduce V_{DD}, on one hand, the lowered power consumption allows higher clock rates thereby shrinking the total test time, while on the other hand, the increased circuit delay results in a slower clock rate and longer test time.

Let f_p and f_s be the frequency limits corresponding to the power and structural constraints of a core, respectively. Expressions (1) and (2) can now be written as:

$$P_{core} \propto V_{DD}^2 \cdot f_p \tag{3}$$

where P_{core} and f_p are the power rating and the power constrained frequency limit for a core, respectively. Since the power rating for a core is a constant, the relationship between f_p and V_{DD} is expressed as:

$$f_p \propto 1/V_{DD}^2 \tag{4}$$

This relationship can also be expressed using the alpha power law, as

$$f_s \propto \frac{(V_{DD} - V_{TH})}{V_{DD}} \tag{5}$$

From these expressions it can be noted that as V_{DD} is decreased, f_p increases allowing higher clock rates. At the same time, f_s decreases with decreasing V_{DD}. If it is assumed that initially all cores are executing at their power constrained maximum frequency, f_p, and that $f_s > f_p$, then as we decrease V_{DD}, the clock rates of the cores transition from being power constrained to become structurally constrained. Now, the clock frequency of a session is given by $f(S_j) \leq \min\{f_p(t_i), f_s(t_i) | \forall t_i \in S_j\}$ and since the frequency factor of a session, $F_j = \frac{f(S_j)}{f_0}$, its maximum value is given by,

$$\max\{F_j\} = \min[\frac{\min\{f_p(t_i), f_s(t_i)\}}{f_0}, \frac{P_{max}}{P_{S_j}} | \forall t_i \in S_j] \tag{6}$$

III. Experimental Procedure and Results

We demonstrate the effects of voltage manipulation on optimal test time for two benchmark systems, ASIC Z and System L.

Table II
THE COMPONENTS OF ASIC Z WITH THEIR TEST TIME (IN ARBITRARY UNITS) AND POWER (IN MILLIWATTS).

Block	Test time	Test power
RAM1	69	282
RAM2	61	241
RAM3	38	213
RAM4	23	96
ROM1	102	279
ROM2	102	279
RL1 [a]	134	295
RL2	160	352
RF [b]	95	10

[a]RL = Random logic block
[b]RF = Register file

Table III
TEST TIMES PREVIOUSLY REPORTED FOR ASIC Z.

Chou *et al.* [4]		Larsson and Peng [12]	
Test time	**Blocks**	**Test time**	**Blocks**
69	RAM1,RAM3, RAM4,RF	160	RL2,RL1,RAM2
160	RL1,RL2	102	RAM1,ROM1, ROM2
102	ROM1,ROM2, RAM2	38	RAM3,RAM4,RF
331		300	

A. ASIC Z

The system ASIC Z was introduced by Zorian [21] and consists of RAM, ROM and other blocks. These blocks along with their test time and power are listed in Table II. In the past, the optimal test time for the ASIC Z, for a power budget (P_{max}) of 900mW, was determined by Chou *et al.* [4] as 330 units whereas Larrson and Peng [12] came up with a solution of 300 units. Their test schedules are shown in Table III.

By using the ILP model $M2$, the total test time can be further reduced to 268.74 units, as demonstrated in [18]. The resulting optimal test schedule is given in Table IV. In this case, the test sessions in the schedule are operating at their maximum frequencies which means that clock rates cannot be further stepped up to reduce test time. To account for limits on the frequency of individual cores, maximum clock rates are set for each component, as shown in Table V. These limits were assigned based on the test length and test power of the blocks and normalized with respect to the slowest core/block.

Let us assume that the frequency limits listed in Table V for the blocks of ASIC Z are purely power constrained, i.e. an increase in the frequency will cause the test power to exceed the power limit of the core but will not cause any timing violations. Thus, the blocks in the test sessions of the schedule shown in Table IV, can be said to be executing at f_p. For simplicity, we shall assume the following: nominal $V_{DD} = 1$V, $V_{TH} = 0.5$V, $\alpha = 1$ and that $f_s = 2f_p$ (i.e., the structurally constrained maximum frequency is twice that of the power constrained value).

Table IV
OPTIMAL TEST SCHEDULE FOR ASIC Z, OBTAINED BY THE INCLUSION OF FREQUENCY FACTOR [18].

Session	Block	Frequency factor	Test length
1	RAM1,ROM2	1.5	68
2	RAM2,RAM3	1.98	30.77
3	RAM4,RF	4.71	4.88
4	ROM1,RL1,RL2	0.97	164.624
		Total test time =	268.274

Table V
NORMALIZED MAXIMUM FREQUENCY VALUES FOR COMPONENTS OF ASIC Z.

Block	Norm. max. frequency
RAM1	1.75
RAM2	2
RAM3	3
RAM4	5
ROM1	1.5
ROM2	1.5
RL1	1.2
RL2	1
RF	8

From (4) and (5), it can be noted that as V_{DD} is reduced, f_s decreases whereas f_p increases. Since the frequency limit is the minimum of the two quantities, at lower V_{DD}, the structural constraint (f_s) dominates the power constraint (f_p). That is to say, as V_{DD} decreases, the clock rate of the cores and, in turn, their scheduled test sessions execute at a structurally constrained clock rate. The plot of the total test time as a function of V_{DD} is shown in Figure 1.

In Figure 1, it should be noted that the value of the total test time reduced from 268.3 time units at $V_{DD} = 1$V to 155 time units at $V_{DD} = 0.75$V. By reducing V_{DD} beyond this point, the test time increases as the operational frequency of more blocks becomes structure constrained. At $V_{DD} = 0.6$V, all blocks of ASIC Z are operating at clock frequencies determined from structural constraints (critical path delays).

For illustration, we assumed that the structurally constrained maximum frequency for all the blocks is twice the power constrained frequency limit, i.e., $f_s = 2f_p$. The plot in Figure 2 examines the behavior of the total test time

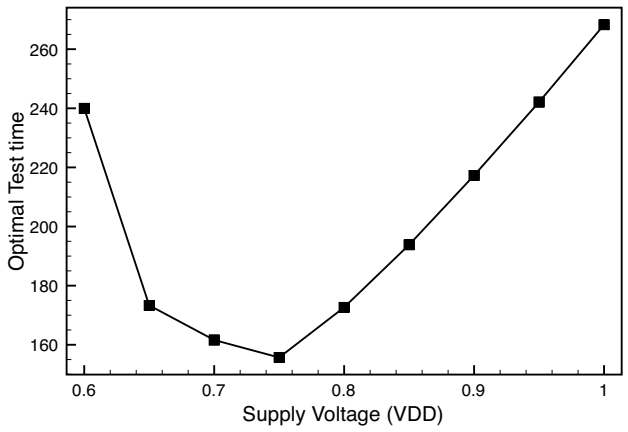

Figure 1. Optimal test time versus V_{DD} for ASIC Z.

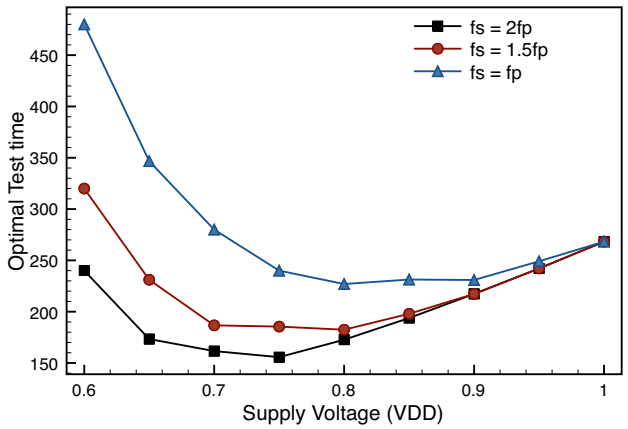

Figure 2. Effect of varying the proximity of structural and power constraints on optimal test time of ASIC Z.

as the operation becomes controlled by one or the other constraint. As the constraints come closer to each other, the scope for increasing the test clock rate by lowering V_{DD} decreases. Consequentially, the effectiveness of this technique in improving the test time is hindered. The test time minimization is not only affected by difference between the structural and power constraints but also by the number of cores that have a lower power constraint than their structural constraint. Better test time minimization is achieved when many cores in the SoC have power constrained frequency limits that are much lower than their structurally constrained frequency limits.

B. System L

System L is an industrial design consisting of 14 cores and 17 tests, as shown in the Table VI [10]. Tests A through M are block-level tests and tests N through Q are top-level tests. Cores D, G and H are tested as parts of other top-level

Table VI
DESCRIPTION OF SYSTEM L.

Block	Test	Test time	Test power	Test port
A	Test A	515	379	scan
B	Test B	160	205	test-bus
C	Test C	110	23	test-bus
E	Test E	61	57	test-bus
F	Test F	38	27	test-bus
I	Test I	29	120	test-bus
J	Test J	6	13	test-bus
K	Test K	3	9	test-bus
L	Test L	3	9	test-bus
M	Test M	218	5	test-bus
A	Test N	232	379	functional pins
N	Test O	41	50	functional pins
B	Test P	72	205	functional pins
D	Test Q	104	39	functional pins

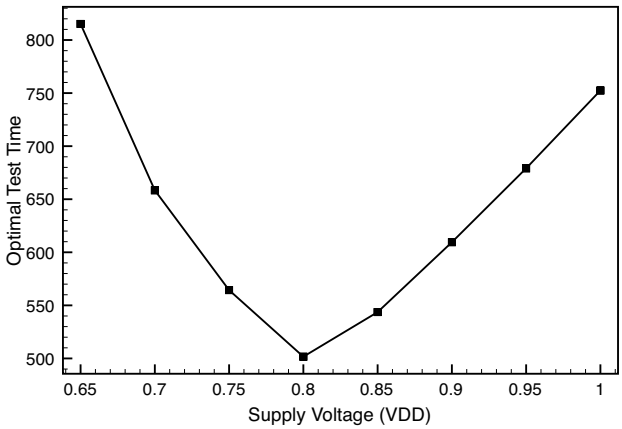

Figure 3. Optimal test time versus V_{DD} for System L.

tests. Block-level tests and top-level tests cannot be executed, concurrently. Also, concurrent execution among top-level tests and block-level tests using the test-bus is not possible. The total test time of System L for a constant test clock is 1374 units whereas, for a variable test clock, the total test time is 752.5 units. Here again, the cores were assigned maximum clock frequencies based on their test length and power. As in the case of ASIC Z, we assume that the test clock rates of the sessions in the test schedule are at their power constrained value (f_p). Now, as we reduce V_{DD}, the total test time initially decreases, but as clock frequencies of more cores near their structurally constrained value (f_s) any further reduction in V_{DD} only leads to an increase in the total test time. The plot in Figure 4 shows the behavior of the total test time for different ratios of f_s and f_p.

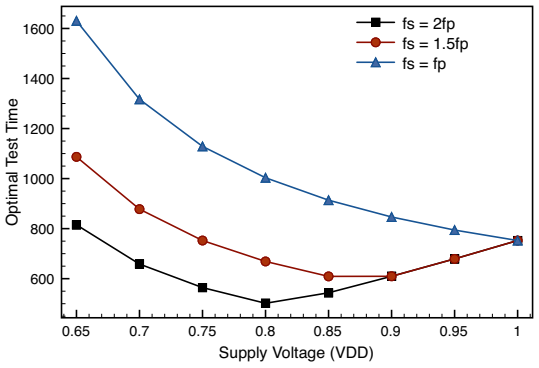

Figure 4. Effect of varying the proximity of structural and power constraints on optimal test time of System L.

IV. Conclusion

We have demonstrated that the test time of SoC devices, for a given power budget, can be minimized by optimizing the supply voltage and customizing the clock rates for each test session. Voltage can be reduced to lower the power and increase the clock frequency without exceeding the power limit of the core. As a result, test time is minimized. However, in accordance with the alpha-power law, further reduction in the voltage causes the gate delay to increase which, in turn, leads to the increase of test time. For illustration when we assume that, for all cores, the structural constraint for the clock frequency is twice that of the power constraint, we find that the test time of ASIC Z, a frequently used benchmark SoC, is as low as 155 time units, which is an improvement of 48.1% over the existing best solution of 300 time units. We also show that varying this assumption alters the optimal V_{DD} value and the total test time. For another benchmark, System L, the test time of 1374 units for a constant test clock was lowered to 501 units using the proposed method.

In the work presented in this paper, we assumed that initially all core tests are specified at the power constrained frequency limit and that the difference between the structural constraint and the power constraint is same across all cores. However, in reality, these may differ from core to core, resulting in non-identical optimal V_{DD} values for cores. Also, the operating voltages of cores may be different from each other. Hence, a multiple voltage assignment is desirable in order to assign optimal V_{DD} to each core and thus accomplish the best test time minimization.

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