Test-Access Solutions for Three-Dimensional SOCs

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Abstract

We present a design technique for providing test access to 3D core-based SOCs under constraints on the number of TSVs and the TAM bitwidth. The associated optimization method is based on a combination of integer linear programming, LP-relaxation, and randomized rounding. Simulation results are presented for the ITC 02 SOC Test Benchmarks and the test times are compared to that obtained when methods developed earlier for two-dimensional ICs are applied to 3D ICs.

1. Introduction

A test-access architecture, also referred to as a test-access mechanism (TAM), provides the means for on-chip test data transport. Test-wrapper design and TAM optimization are vital for modular testing, because they directly affect SOC testing time, and therefore the test cost. Prior work has been limited to traditional two-dimensional (2D) integrated circuits (ICs) [1]. However, with the emergence of three-dimensional (3D) ICs and the increasing likelihood of core-based design being the design style of choice for 3D ICs, there is a need to develop modular testing methods for 3D ICs [2].

The reduction of interconnect delays and power consumption are of paramount importance for deep-submicron designs. 3D ICs have recently emerged as a promising means to mitigate these problems. Among several 3D integration technologies, the through-silicon-via (TSV) is especially promising. 3D ICs offer a number of advantages over traditional two-dimensional (2D) design: higher performance, lower interconnect power consumption, higher packing density and smaller footprint, and support for the implementation of mixed-technology chips [2]. In this work, we address TAM optimization for 3D SOCs based on TSVs.

2. Discussion

The general problem of 3D SOC test planning includes the design/optimization of a test-access architecture, optimization of core wrappers, and test scheduling. The goal is to minimize the testing time under limits on the number of TSVs and the SOC-level TAM width. Additional constraints are also imposed by thermal considerations that are of paramount importance in 3D integration. The placement of cores on different layers is also an important issue. The TAM optimization problem that we address in this work is as follows. Given the test set parameters (number of test patterns, number of I/Os, and scan chains, and scan-chain lengths) for the embedded cores in the SOC, the total TAM width, 3D-technology constraints (maximum number of TSVs, thermal limits, etc.), and the 3D placement for each core, determine the partition of the total TAM width among the TAM partitions, an optimal assignment of cores to each TAM partition, and an optimal wrapper design for each core, such that the overall SOC testing time is minimized.

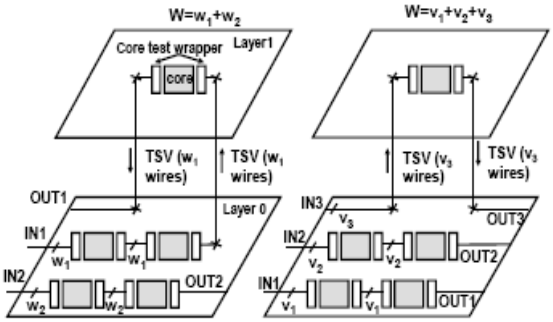

Fig.1 Two solutions for a TAM optimization in a 3D IC

Fig. 1 shows an example to illustrate the motivation of our research. A total of five (wrapped) cores are shown in a 3D IC. Four cores are placed in Layer 0, while the fifth core is placed on Layer 1. Suppose that a total of 2W channels (TAM wires) are available from the tester to access the cores, out of which W channels must be used for transporting test stimuli and the remaining W channels must be used for collecting the test responses. Fig. 1 shows two possible TAM designs for the same 3D SOC design: (1) two TAMs of width w1 and w2 (w1 + w2 = W). A total of 2·w1 TSVs are needed; (2) three TAMs are used (v1 + v2 + v3 = W) and total of 2·v3 TSVs are needed. Both 2·w1 and 2·v3 are no more than the limit on the number of TSVs. It is not obvious to the designers which approach is better in terms of test time. Therefore, optimization methods and design tools are needed to determine a test-access architecture that leads to the minimum test time under constraints on the number of TSVs.

We have formulated thermal-aware and layout-oriented optimization problems and developed integer linear programming (ILP) models for them. The optimization problems have been shown to be NP-hard in [1]. Therefore, we also develop a heuristic technique based on a combination of ILP modeling, LP-relaxation, and randomized rounding to efficiently obtain near-optimal results.

We have carried simulations for four ITC'02 SOC test benchmarks by considering thermal-aware placement on a 3D substrate. Simulation results show that the proposed method leads to lower test times compared to a baseline method that applies 2D TAM optimization to each layer of the 3D SOC. In addition, we have examined the dependence of test time on different 3D placements, the number of layers, and upper limits on the number of TSVs.

3. References

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