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Reducing Test Time of Power Constrained Test by Optimal Selection of Supply Voltage

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***Abstract*—As supply voltage is reduced, a power constrained test clock can be sped up in spite of the increased delay of the circuit. However, a large reduction in voltage makes the operation structurally constrained, requiring the clock to slow down. We determine an optimum supply voltage that allows fastest clock speed for a given power limit. Examples show that the test time can be reduced by as much as 63% from the nominal voltage test time. In a typical application, this technique can reduce the cost of wafer sort.**

***Keywords*-Reduced voltage test, Test time reduction, Scan based test, DFT.**

I. Introduction

Total power dissipation in CMOS circuits consists of static (leakage), short circuit, and dynamic power dissipation. Dynamic power dissipation occurs due to signal transitions at the gate output and contributes to most of the power dissipation in digital circuits. In low power design, combinational and sequential circuit synthesis algorithms often encode states such that the source and destination states of frequent state transitions have fewer bit changes. This reduces the number of transitions in flip-flops and combinational logic, thereby reducing power dissipation during the functional operation of the circuit. During test the correlation between consecutive test patterns generated by an automated test pattern generator (ATPG) is minimum [22] and this causes high switching activity in the circuit under test (CUT) [27]. High test power dissipation is also possible in designs that employ power management blocks. This prevents simultaneous operation of two or more memory blocks consuming high power during functional mode [16]. However, it is a common practice to test multiple blocks simultaneously in an effort to minimize test application time, resulting in high power dissipation during test.

In power constrained testing various methods have been proposed to minimize the power dissipated during testing. These methods can be categorized as either test set dependent or test set independent approach. A test set dependent approach minimizes the switching activity in the pattern by replacing the don't care bits with bits that cause low transitions, or by improving correlation between two patterns. Either method increases the test time while reducing the power dissipation. On the other hand, a test set independent approach involves reducing the test power by decreasing the frequency of operation or by inserting blocking gates to prevent the scan register transitions from affecting the combinational logic. Once again, neither method improves the test time but focuses on the power reduction. Power dissipation can be reduced by down-scaling the power supply voltage [11]. Techniques have been proposed [6], [14] to dynamically vary the supply voltage on the fly to reduce power dissipation during functional operation but this approach decreases the operational frequency. Any reduction of the clock frequency during test, however, increases the test time, which directly translates into increased cost of the chip [7]. Therefore, for complex devices test time and power dissipation during test are serious concerns.

II. Prior Work

Shanmugasundaram and Agrawal [25], [26] recently proposed a method to reduce test application time by monitoring the activity during scan and increasing the test frequency for clock cycles with low activity. They demonstrated test time reduction possibility of 20-50% with some area overhead. Hashempour *et al.* [13] suggested a switch over technique, which combines the advantages of built-in self-test (BIST) and automatic test equipment (ATE). In this work BIST is used initially to detect "easy to detect" faults and the ATE is then used to detect the rest of undetected or "hard to detect" faults. The limitation of this method lies in the effectiveness of BIST. Lai *et al.* [15] suggested selective scanning and reusable scan chains that eliminate unwanted scan operations during scan shifting, thus reducing the test application time. However, reduction in test time depends on the availability and identification of test patterns that closely resemble the previous test pattern.

Devanathan *et al.* [10] proposed an adaptive voltage regulator for scan circuits to vary the voltage during test and thereby reduce test power dissipation. Their paper also shows that the test frequency can be increased when the voltage is reduced. The work considers the delay between two flip-flops in the scan chain and considers the critical path through the combinational logic as false path during the scan shifting operation. Though this is agreeable during scan shift, care must be taken during the capture cycle where

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the delay of the critical path is of concern. This will also produce unwanted switching in the combinational circuit in the absence of gating logic to isolate the combinational part during scan shift.

In this work we propose a test set independent approach to reduce the test time. We make use of the quadratic effect on power observed due to supply voltage scaling. The method proposed in our work can be used in tandem with any of the power constrained test methods described above. Since the work proposed considers the critical path delay of the combinational circuit, correct operation of the circuit during test response capture is guaranteed.

III. Low-Voltage Testing

Testing at low voltage has several advantages. Hao and McCluskey [12] have shown that manufacturing defects such as interconnect bridging and gate-oxide shorts become more visible (testable) at reduced voltage. Such defects are the main cause for early life failures and reliability issues in circuits but they often escape the test at nominal voltage [8], [9], [12]. When the voltage is reduced, the resistance of the short does not change and the voltage drop across these resistive shorts becomes high. According to Chang and McCluskey, [8], [9] the voltage at which these defects are detected lies between $2V_{TH}$ to $2.5V_{TH}$. Roehr [21] indicates that for a reasonable yield, the voltage is obtained through statistical analysis of min-VDD tests on a large sample of chips. A cited disadvantage of reduced voltage testing is the possible change in critical paths, [8], which can force an increase in the test clock period. Qian *et al.* [18] have suggested novel timing tests as an alternative solution to the conventional logic tests to identify gate oxide defects at reduced power supply. In our work we present a methodology to identify the shortest test application time possible using reduced power supply while staying within the peak power limit of the circuit. We also show that it is possible to test the circuit in reduced time without being affected by the change in critical paths.

In the following section we describe a method to determine the minimum voltage that can speed up the test for a given peak power without compromising the functionality of the CUT. We describe two constraints that limit the test speed of the CUT at any voltage and then demonstrate with experimental results how those constraints can be used to advantage.

IV. Optimized Test Time Reduction by Varying Voltage

A. Power Constrained Test

In power constrained testing, the maximum power dissipated by the circuit during scan test, $P_{MAX(test)}$, is limited by the maximum allowable power dissipated during functional operation, $P_{MAX(func)}$, at the rated clock frequency of CUT. In other words, $P_{MAX(test)} = P_{MAX(func)}$. The shortest permissible test clock period, T, for power constrained test is defined as the ratio of maximum energy dissipated per clock cycle during test to the maximum allowable power. Quantitatively, it is written as,

$$T = \frac{E_{MAX(test)}}{P_{MAX(func)}} \tag{1}$$

where

$T =$ Test clock period.

$E_{MAX(test)} =$ Maximum energy dissipated during a vector period by test using ATPG vectors.

$P_{MAX(func)} =$ Maximum allowable power obtained from functional simulation assuming that the circuit is designed to operate correctly in the presence of power supply noise effects (ground bounce, voltage droop, thermal anomalies, etc.) due to this amount of power dissipation.

We conducted an experiment on s298 benchmark circuit synthesized using TSMC 0.18μ technology that has a nominal supply voltage of 1.8V. Full scan was implemented with a single scan chain and tests were generated by Mentor's Fastscan [1]. Using static timing analysis (STA) [4], the maximum rated clock frequency was found as 500MHz. Thus, the clock period for this circuit cannot be shorter than 2ns. We obtained the maximum power dissipated by the CUT during normal operation by simulating it for 100 random vectors (assumed to represent the functional operation of the circuit) at the rated frequency and measuring the power per clock cycle using Nanosim Spice simulator [2]. The maximum power during any cycle was 1.2mW.

The maximum energy dissipated by the CUT during a test clock cycle is independent of the clock frequency and is proportional to the maximum switching activity in the CUT. Hence it is possible to find the maximum energy at any supply voltage using a fixed arbitrary (slow) clock frequency. Of course, we are neglecting the leakage, which should be taken into account for 90nm and finer technologies. Once the maximum energy per clock cycle is obtained, the clock period necessary for power constrained test is found using equation (1). For the CUT in this experiment (s298 implemented in 0.18μ CMOS technology), the test clock period was calculated as 5.38ns at 1.8V, which is more than the functional clock period of 2ns. Thus, a test at the nominal supply voltage of 1.8V must run at a 2.69 times slower speed than the functional speed of the circuit.

The total scan test time for any CUT can be written as $TT = N \times T$ [7], where $N = [(n_{comb}+2) \times n_{sff} + n_{comb} + 4]$ is the number of test clock cycles. Here, n_{comb} is number of combinational ATPG vectors, n_{sff} is number scan flip-flops, T is test clock period and TT is the total test time. We must, however, use the power-constrained test clock of equation (1). We thus obtain,

$$TT_{power} = N \times \frac{E_{MAX(test)}}{P_{MAX(func)}} \tag{2}$$

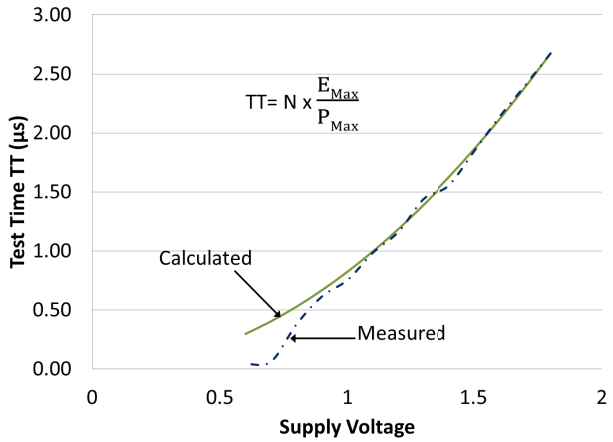

Figure 1. Measured and calculated test time plots of s298 benchmark circuit for power constrained clock period.

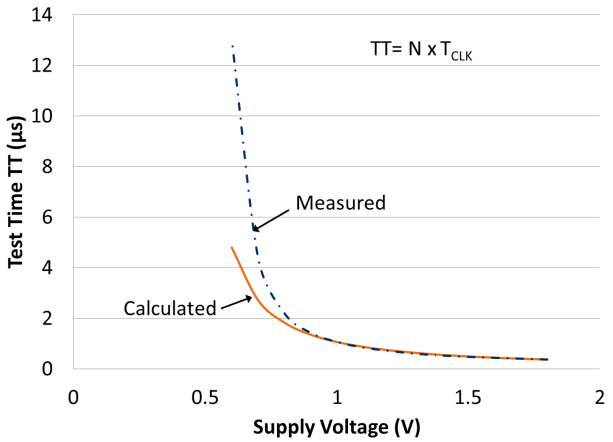

Figure 2. Measured and calculated test time for s298 benchmark circuit for structure constrained clock period.

This equation gives the total test time for any power constrained test. It shows that the total test time is directly proportional to the maximum energy dissipated during any test cycle. Hence the test time can be reduced by reducing the maximum energy for the specified peak power for the circuit.

Because energy has a quadratic dependence on the supply voltage, by reducing the supply voltage to half, the energy and hence power, are reduced four times. As mentioned earlier, the power must be kept within the allowable peak power limit. Therefore, as the voltage is reduced it is now possible to increase the test clock frequency such that the power dissipated by the circuit remains constant.

The test clock frequency increase is possible because the testing speed, as we found earlier, was power constrained and not structure (critical path) constrained.

Figure 1 shows the test time for the power constrained scan testing of s298 sequential benchmark circuit. The test time was calculated using equation (2), where $N = 14$ and $P_{MAX(func)} = 1.2mW$. For the curve labeled 'calculated' the energy $E_{MAX(test)}$ is calculated using the energy equation $E = C_{eff} \times V_{DD}^2$ [19] for each supply voltage, where C_{eff} is the maximum switched capacitance for the test cycle with maximum switching activity. The test time plot labeled 'measured' is really simulated data and is obtained using the energy computed by Nanosim Spice simulation [2]. The clock frequency at each supply voltage is obtained from equation (1) using the energy measured. The graph serves as a proof of correctness for equation (2) that finds the test time using the energy dissipated by the circuit for various voltages. The difference in the calculated and measured plots at low voltages is due to the device becoming structure constrained (explained in the following section). Owing to the increased gate delays at low voltages the clock period ends before the circuit attains steady state. As a result, some transitions spill over to the next clock period and merge with transitions there. The simulator, which is merely integrating power over a clock period, thus underestimates the energy, E_{Max}. Hence the test clock period calculated using equation (1) is smaller and so is test time. We observe that equation (2) for test time does not hold when the device becomes structure constrained.

B. Structure Constrained Test

In digital logic circuits, the operational speed is limited by the circuits critical path delay. The total sum of propagation delay of each gate in the path from one register to the next constitutes the total delay in that path. The maximum delay among all the paths in the circuit identifies the critical path. The propagation delay of a gate relates to the charging or didcharging of the output load capacitance. During switching the circuit enters the saturation mode of operation and hence the drain current is directly proportional to the square of the difference in gate-source voltage and the threshold voltage. Sakurai and Newton [24] show that in the region of saturation the drain current I_D is directly proportional to $(V_{GS} - V_{TH})^{\alpha}$, where α is the velocity saturation index. The relation of gate delay and voltage is also shown quantitatively in [17], [24]. A more simplified equation that shows the proportionality between the propagation delay and supply voltage is as follows [23]:

$$delay \propto \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

where V_{DD} is the supply voltage, V_{TH} is the threshold voltage and α is velocity saturation index.

Methods to obtain the value of alpha are specified in [5], [23], [24]. Bowman *et al.* [5] find the value of α to be 1.86 for 0.18μ and Sakurai [23] mentions that the value of α can be approximated to 1.3 for short channel devices. In our

experiment we found the value of α to be near 2 and used the same for all calculations. However, the experiment can be conducted using any value for α, based on the available technology data and the proposed methodology will remain valid.

The equation specified above can be re-written as follows

$$t_{pd} = K \times \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}} \tag{3}$$

where t_{pd} is the propagation delay, and K is a proportionality constant.

For a given value of α and threshold voltage, it is possible to find the propagation delay for the circuit at different voltages. In the structure constrained experiment we use equation (3) to calculate the CUT's critical path delay at different voltages. In this experiment we initially find a vector that can activate (propagate a transition through) the critical path of the circuit. The critical path was obtained by STA during synthesis of the CUT using Leonardo Spectrum [4]. Once the critical path and its source and destination registers are known, Fastscan ATPG [1] is used to determine a path delay pattern for any path between those registers, if none can be found for the critical path. For s298, the ATPG was able to find a non-robust path delay test pattern set for a path that has 6 of the 7 logic gates from the critical path. We use this pattern to observe and measure the effect of critical path delay with respect to the voltage variations. The circuit was simulated using Nanosim's Spice simulator [2] and the waveform was viewed in ezwave waveform viewer [3]. The structural clock period (T_{CLK}) is the sum of the critical path delay and the setup time of the register. Hence the total structure-constrained test time can be written as,

$$TT_{structure} = N \times T_{CLK} \tag{4}$$

Figure 2 shows the total test time for the scan test sequences of s298 using the structure onstrained clock at various voltages from 1.8V to 0.6V. The curve labeled "calculated" is obtained using the critical path delay at each voltage using $\alpha = 2$ and $K = 0.85$. This value of K was derived by substituting for t_{pd} in equation (3) the delay obtained from the simulation of critical path at 1.8V supply. The plot labeled "measured" denotes simulation results from Nanosim Spice Simulator [2]. Clearly, the two plots match for voltage above 0.8V, verifying the validity of equation (3) in that range. The difference becomes more drastic as we reduce the voltage below 0.8V. This is because as the voltage is reduced the critical path delay increases and hence for proper operation of the circuit the clock period must be increased. That was not done since the present application would not require lower voltages, where due to structure constraint the test time begins to increase.

C. Optimum Voltage

In this section we aim to find the best voltage at which a power constrained test can run in minimum test time without exceeding the peak power or violating the critical path delay constrain of the circuit. As mentioned in the previous sections the test time can be reduced while limiting the power by reducing the supply voltage. However, there exists a point where the voltage will not be enough to charge the output load capacitance within the right amount of time. Thus the value at the output will be wrong. At this point the circuit is considered structure constrained and the test time is now dependent on the critical path delay of the circuit. Hence using the equations (2) and (4) the total test time can be written as,

$$TT = max(TT_{power},\ TT_{structure}) \tag{5}$$

The optimum voltage at which a power constrained test will run with the fastest clock and in least overall test time will be the voltage at which both TT_{power} and $TT_{structure}$ are equal.

Application of the theory proposed here is illustrated with an experiment performed on s298 sequential benchmark circuit, used for demonstration throughout this paper. In order to observe the peak power dissipated by the circuit during test as well as the critical path delay, scan vectors generated by the ATPG for stuck at fault tests were combined with the vectors generated to trigger the critical path. Simulations were performed using Nanosim SPICE simulator [2] tool by varying the voltage from 1.8V down to 0.6V in steps of 0.1V. The peak energy dissipated and the critical path delay were measured at each voltage points. Using equations (2) and (4), the values for test times were calculated and the maximum of the two values is the total time as given by equation (5).

V. Results

Figure 3 shows the graph for the simulation result and calculated results to find the optimum voltage points. The point labeled minimum V_{DD} is the cross point at which the power-constrained test clock period and the critical path delay of the circuit are approximately the same. Reducing the voltage beyond this point increases the test time as the critical path delay increases above the power-constrained clock period. Hence, the test must slow down. The dotted line, labeled "measured", shows the result from simulation. The best voltage is 1.04V with a total test time of approximately 1μs and a test clock frequency of 500MHz is the same as the functional frequency. The minimum of the "measured" curve exactly coincides with the cross-over point of the two calculated curves from equations (2) and (4). This validates the calculation of the best supply voltage for minimum test time as is obtained from equation (5). Thus, Spice simulation, which is expensive for a large circuit, is not required for many voltages. Once E_{Max} and t_{pd} have been

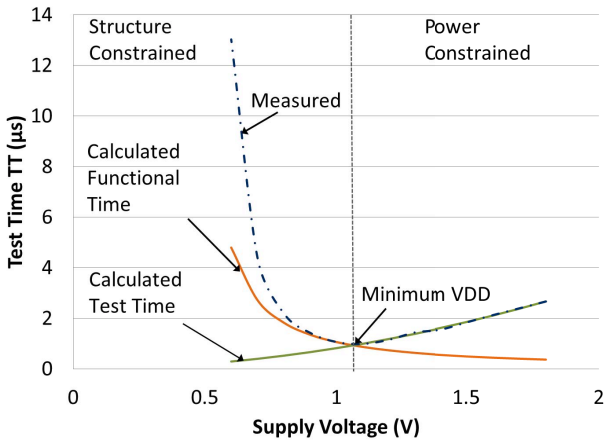

Figure 3. Simulation and experimental test time plots to find the optimum voltage for s298 benchmark circuit.

Table I
OPTIMUM V_{DD} FOR REDUCED TEST TIME OF ISCAS'89 BENCHMARK CIRCUITS.

Circuit name	Combinational ATPG vectors	Total scan test cycles	Peak per cycle power (W)	Nominal voltage (1.8V) test		Optimum voltage test			Test time reduction (%)
				Test frequency (MHz)	Test time (μs)	Supply voltage (Volts)	Test frequency (MHz)	Test time (μs)	
s298	33	498	0.0012	187	2.66	1.04	500	0.996	62.5
s382	31	704	0.0029	300	2.34	1.35	563	1.25	46.5
s713	44	809	0.0027	136	5.89	1.45	263	3.07	48.0
s1423	62	4649	0.0045	141	33.00	1.70	158	29.42	11.0
s13207	121	41266	0.0213	110	375.00	1.45	165	250.00	40.3
s15850	125	67624	0.1781	182	371.56	1.65	222	304.61	18.0
s38417	123	181536	0.0737	121.8	1491.90	1.50	175	1036.10	30.5
s38584	144	186159	0.1106	129	1443.09	1.30	187	995.50	31.0

obtained at one voltage (say, nominal voltage or 1.8V in our example), both equations (2) and (4) can be characterized.

Experiments of the proposed methodology were performed on ISCAS'89 sequential benchmark circuits synthesized using TSMC 0.18μ technology. Simulations were carried out using Nanosim Spice simulator [2]. Fastscan ATPG [1] was used to generate vectors for stuck-at fault tests with 100% test coverage.

Table I shows the results for the circuits used in our experiments. The column labeled "peak power" denotes the maximum allowable power during functional operation. Columns 5 and 6 give the power constrained test clock frequency and the total test time for nominal voltage of 1.8V. Column 7 shows the optimum voltage at which maximum reduction in test time is achievable without exceeding the peak power limit or critical path delay. The test frequency and test time for optimum voltage obtained using the method described in section IV-C are given in Columns 8 and 9. Finally, column 10 gives the percentage reduction achieved through the proposed method.

The values for voltages are based on the critical path delay obtained through STA and are pessimistic. This is because the critical path may not be activated by any vector during test or even in the functional mode. It may even be a false path. From Table I it is seen that using our methodology it is possible to achieve a reduction more than 25% in most of the circuits with a maximum of 62.5% seen in s298 benchmark circuit.

It was observed that if the difference in energy dissipated during functional operation and during test is not large, then the reduction in test time is not high either. This is because the circuit can be operated close to the functional speed and the voltage cannot be reduced without making the operation structure constrained. On the other hand, for circuits with significantly high energy dissipation during test it is possible to achieve high reduction in test time. For example, in s1423 and s15850 benchmark circuits the difference in the energy dissipated during functional operation and during test was only 0.5-2 units. But for all other cases the difference was in the range of 5-8 units. Hence, a test that dissipates higher power than the allowable power is more likely to have a larger reduction through our method. This is true for many circuits used today, which are known to consume up to *four* times the normal power during testing [20].

VI. Conclusion

We propose a novel test time reduction method by optimally selecting the supply voltage during test application. The test clock frequency is chosen to be fastest to allow signal propagation through critical paths as well as not exceed the given peak power dissipation. The method, as presented is suitable for wafer sort where the basic pass-fail test is of interest and test cost is a serious concern. Future exploration of the proposed method includes test for non-classical faults and for sub-nanometer technologies. First, the test for non-classical faults where the proposed method is directly applied to scan in and scan out operations, may require closer examination during the normal mode cycles in which various delay test modes are exercised. Second, we developed the analysis assuming that dynamic power was the major component of dissipation. For nanometer technologies, leakage may modify some details of the analysis. Third, also for nanometer technologies, the nominal supply voltage may be closer to the threshold voltage and the delay would increase more rapidly as we get closer to the threshold voltage. However, potential applications of the proposed method may be possible in all these cases.

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