Wrapper Chain Design for Testing TSVs Minimization in Circuit-Partitioned 3D SoC

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***Abstract*—Three dimensional (3D) System-on-Chips (SoCs) that typically employ through-silicon vias (TSVs) as vertical interconnects, emerge as a promising solution to continue Moore's law. Whereas, it also brings challenging problems, one of which is the test wrapper chain design and optimization, especially for circuit-partitioned 3D SoCs in which scan chains can cross among layers. Test time is the primary goal for wrapper chain design, both for 2D and 3D SoCs. The 3D SoC wrapper chain design problem can be converted into the well-studied 2D one by projecting wrapper chain components of all layers to one virtual layer. Thereafter, we can leverage 2D optimization algorithms to determine the composition of wrapper chains and thus guarantee minimal testing time for 3D SoCs. One specific thing for circuit-partitioned 3D SoCs is that TSVs are needed to connect cross-layer wrapper structures to form the wrapper chains. As TSVs occupy planar chip area and will aggravate the routing congestion problem, it is necessary to reduce TSVs for test purpose as much as possible. In this work, we observe that by varying the connection orders of wrapper chain components, e.g., scan chains and I/O cells, the TSVs consumed vary significantly. Based on the above, we formulate this problem and propose novel heuristic to tackle it. Experimental results show that the proposed solution can save on average 33.2% amount of TSVs when compared to a prior intuitive method.**

I. Introduction

As semiconductor feature size shrinks continuously, global interconnects that cross a large part of a chip become the major performance bottleneck for current System-on-Chip (SoC) designs. 3D integration technology that stacks active device layers thus efficiently reduces global long wires is considered to be one of the most promising solutions to tackle the above problem. 3D technique benefits the integrated circuits (ICs) in many aspects, such as diverse technology integration, device density, bandwidth, etc.

Although 3D SoC has many advantages, there are still many road-blocks need to be cleared before it prevails. Among others, testing of 3D ICs is viewed as a key challenge [1]. Several 3D SoC testing schemes have been proposed for different partition styles, i.e. technology-level, architecture-level and circuit-level partitions [2]–[5]. The former two can best reuse existing design efforts whereas the third one can better exploit 3D stacking benefits. Testing of circuit-partitioned 3D SoCs is more challenging. 3D SoCs demand both pre-bond and post-bond testing to combine known good dies to achieve satisfactory manufacturing yield. In this paper, we focus on the wrapper scan chain optimization for the circuit-partitioned 3D SoCs.

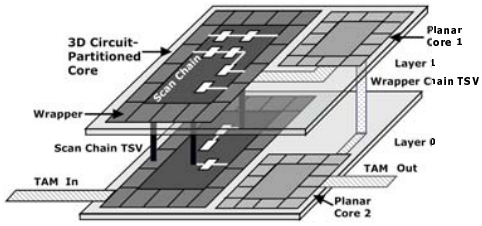

Fig. 1. Test Wrapper Chain in the Circuit-Partitioned 3D SoC

For both 2D and 3D SoCs, testing time is of the primary importance as it directly impacts test cost [6], [7]. There exists extensive research work on 2D SoC wrapper chain design to minimize the time for testing [8]–[10]. We can convert the 3D SoC wrapper chain design problem to the well-studied 2D one by projection of wrapper chain components of all layers to one virtual layer. Thereafter, we can leverage 2D optimization algorithms to guarantee minimal testing time for 3D SoCs. One thing specific for circuit-partitioned 3D SoCs is that vertical interconnects, i.e., TSVs are needed to connect cross-layer wrapper structures to form the wrapper chains. Fig.1 illustrates a conceptual test wrapper chain structure of 3D SoC. In this figure, the SoC consists of one 3D IP core and two planar IP cores. Every IP core is embraced by its test wrapper, which can be connected together to form the wrapper chain.

Prior 2D wrapper chain construction solutions generally balance the length of different wrapper chains within an IP core according to the bandwidth of test access mechanism (TAM) to achieve both parallelism and minimal test time. However, in this work we observe that different wrapper chain design can achieve the same minimal test time while the number of TSVs consumed for testing purpose varied significantly. Note that TSVs generally introduce bonding pads in the planar layers and occupy chip areas. This will be a great burden for place and route which can not be ignored [11]–[15]. Therefore, it motivates us to reduce testing TSVs as much as possible while keep testing time minimal.

In this work, we firstly convert the 3D wrapper optimization problem to its corresponding 2D one and adopt existing

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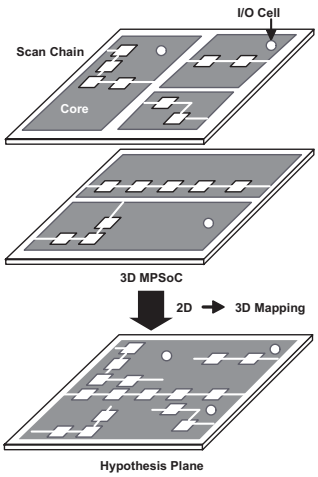

Fig. 2. Mapping of 3D SoC Wrapper Components to the Hypothesis Plane

research efforts to tackle it. Based on this, we propose novel algorithms to determine how these wrapper chain components are connected to minimize the amount of TSVs. This problem can be formulated as finding the shortest Hamilton path in a complete diagraph. Extensive experimental results show that we can reduce test time by 8.7% on average while the TSV count can be reduced as much as 33.2% in comparison with an intuitive method proposed in [16].

The rest of this paper is organized as follows: In section II, we briefly describe the related work and motivate our work through an illustrative example. Subsequently, the TSV optimization problem is formulated in section III. The proposed heuristic is also detailed in this section. Experimental results and analysis are presented in section IV and section V concludes this paper.

II. Related Work & Motivation

A. Related Work

Test and DFT research in 3D realm can be classified in three categories corresponding to three design styles, i.e. technology-level deign, architecture-level design and circuit-partitioned level design [3]. At each level, the test procedure can be divided into pre-bond and post-bond test further. At architecture level, Lewis et al. exploited the pre-bonding test problem and proposed scan-island design method in [17]. The test length optimization, however, is not touched. For the post-bond design, Marinissen et al. proposed a test framework similar to the IEEE 1500 style design to tackle the 3D SoC test issue [4]. Then, the author proposed an improved test framework to facilitate both pre-bonding and post-bonding test reusing already existing test resources as much as possible [18], [19]. Unfortunately, the tradeoff between test length and test TSV resources is not deeply exploited. Wu et al. proposed a novel scan chain design method for 3D integrated circuits [5] and optimized TAM structure for 3D SoCs [7]. Jiang et al. optimized the test structure for 3D SoC considering the congestion [20]. They also exploited the test optimization

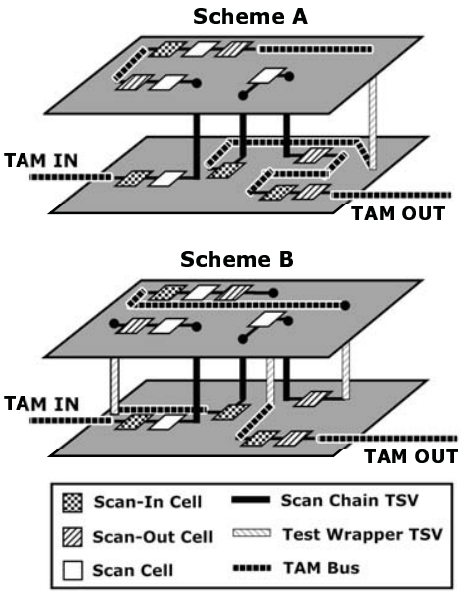

Fig. 3. Test TSV Count Comparison Between Different Wrapper Chain Designs

under the test pin count constraint [21]. Lo et al. proposed an IEEE 1500 compatible 3D IC test framework to optimize the test time and TSV usage [22]. All these work, however, only considered the architecture level testing, which assumes the core under test to reside on a single layer.

To exploit the potentials of 3D ICs to extreme, circuit-level partitioning method would be adopted, which means that a single core may cross several layers. For circuit-partitioned 3D ICs, Lewis et al. explored the design for testability technique in [2]. Zhao et al. attacked the clock network design problem for pre-bonding test in 3D ICs [23]. However, the test time optimization isn't touched in these papers. Noia. et al. optimized the test time of circuit-partitioned 3D SoC with the constraint of TSV count [16]. Unfortunately, due to TSV limits, the test time can not be guaranteed global optimal. Roy et al. optimized the TSV count based on the work of [16] but they only consider the scenario that each scan chain only resides on one particular layer. Different from the above work, we believe that test time is of the primary importance in 3D test and should be optimized superior to TSV reductions. In addition, each scan chain may cross several layers which is more meaningful for the circuit-partitioned 3D IC.

B. Motivation

There are already extensive research work for wrapper chain design to optimize test time for the planar SoC design [8], [9]. Without any other constrains, we can convert the 3D SoC wrapper chain design problem to a 2D one by projecting the whole 3D structure to a single hypothesis plane. For the ease of representation, we use wrapper component for presentation instead of scan chain and I/O cell in the rest of this paper. As shown in Fig.2, the wrapper components of a two-layer 3D SoC can be mapped onto a single plane. Consequently, our

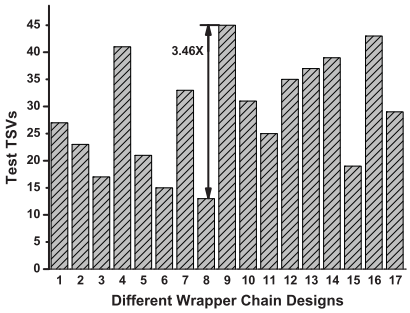

Fig. 4. Test TSV Count Comparisons Among Different Wrapper Chain Structures for Core 13 of p93791 Benchmark

problem is translated to test time optimization for the planar design.

Through above procedure, we can determine the composition of each wrapper chain with the optimal test time. However, the connection order of the wrapper components within the same wrapper chain can impact the number of TSVs significantly. To illustrate the potential optimization space of test TSV count, we use a synthetic example and connect wrapper components within the same wrapper chain in different ways for comparison. The experimental 3D SoC is implemented with two layers and a single wrapper chain is designated to test it. Two different wrapper design strategies are depicted in Fig. 3. Although scheme A and B are treated as the same from the planar optimal test wrapper design perspective, however, in 3D scenario, B consumes two additional test TSVs in comparison with A (i.e. 1 for A and 3 for B).

To further demonstrate the optimization space, we choose core 13 of p93791 from the ITC'02 SoC benchmark and divide the circuit in two layers. We first determine the wrapper chain components, and then enumerate all possible connection orders within a wrapper chain exhaustively. The resulting test TSV counts are plotted in Fig.4. From the figure, it can be seen that different test wrapper configurations with the same test time can introduce as large as 3.46 times difference on the test TSV consumptions. In the following sections, we formulate this problem and propose a novel heuristic to attack it.

III. Problem Formulation & Proposed Heuristic

A. Problem Formulation

Based on the above description, our optimal wrapper chain design problem can be formulated as follows:

Given: The number of wrapper chains $\mathcal{M}$ designated to test the target 3D SoC; the location information of wrapper components (e.g. as for the scan chain, the information includes the start layer $\mathcal{S}_i$, the end layer $\mathcal{E}_i$ and the scan chain length $\mathcal{L}_i$). The components within a wrapper chain have been determined via certain 2D wrapper chain design algorithms.

The goal of our optimization is to determine the connect order of the wrapper components such that TSV count is

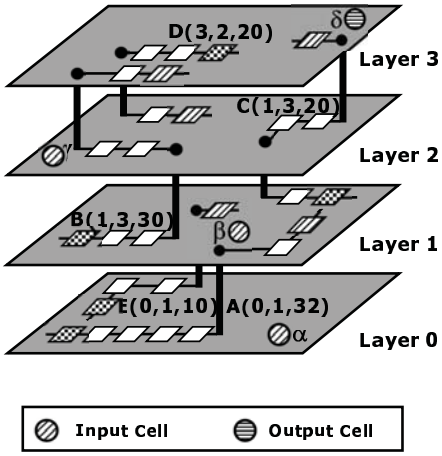

Fig. 5. Wrapper Component Distributions within the 3D SoC

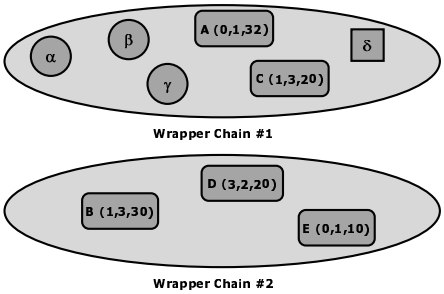

Fig. 6. Wrapper Chain Composition with Minimal Test Time

minimized, i.e.

$$\textit{Minimize:} \quad (\sum_{i=1}^{\mathcal{M}} \text{TSV}_{\text{wrapper\_chain}}(i)) \tag{1}$$

where $\text{TSV}_{\text{wrapper\_chain}}(i)$ denotes the number of TSVs used by the i^{th} test wrapper chain. Furthermore, $\text{TSV}_{\text{wrapper\_chain}}(i)$ can be calculated via the following expression:

$$\begin{aligned} &\text{TSV}_{\text{wrapper\_chain}}(i) = max\{I_{i,j}|1 \le j \le w\} \\ + \quad &|SI_{i,1} - I_{i,w}| + \sum_{k=1}^{u-1} |SI_{i,k+1} - SO_{i,k}| \\ + \quad &|O_{i,1} - SO_{i,u}| + max\{O_{i,l}|1 \le l \le v\} \end{aligned} \tag{2}$$

In above formula, w, u, v denote the number of input cells, scan chains and output cells on the i^{th} wrapper chain respectively. I and O denote the layer of input cell and output cell respectively. SI and SO represent the scan-in and scan-out layer of the scan chain. In the rest of this section, we will propose an intuitive method and a heuristic algorithm to attack this problem in sequence based on an illustrative example.

As shown in Fig.5, assume that the 3D SoC is designed as four strata and it contains five scan chains, three input cells and one output cell. In the figure, Layer 0 denotes the bottom layer where test pins locate. The layers of input cells are 0, 1, and 2 respectively. The output cell lies on layer 3. The

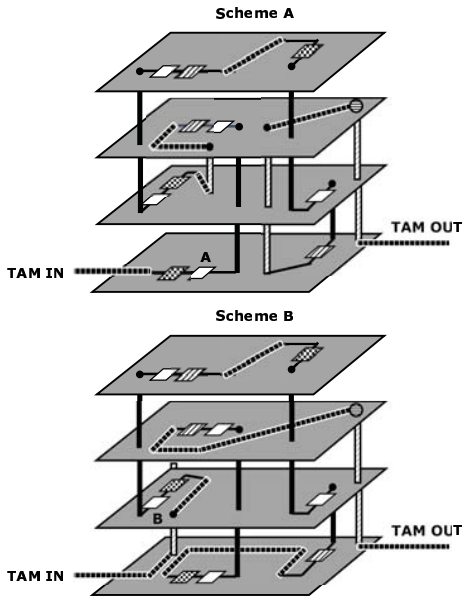

Fig. 7. A Counterexample of the Intuitive Method

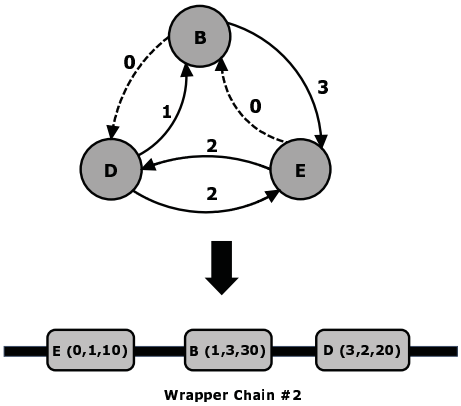

Fig. 8. Reorder of Wrapper Components on Wrapper Chain #2 for Test TSV Minimization

information of each scan chain is represented by the triple (x, y, z), where x represents the scan-in layer, y represents the scan-out layer and z denotes its length. For this example, they are as the following: A(0,1,32), B(1,3,30), C(1,3,20), D(3,2,20) and E(0,1,10). Two test wrapper chains are assumed to be designated to test the chip. From [24], we know that the test time of the 3D SoC can be expressed as follows:

$$T = (1 + max(S_i, S_o)) \times p + min(S_i, S_o) \qquad (3)$$

where S_i, S_o denote the scan-in length and the scan-out length of the wrapper chain respectively and p is the number of test patterns. Eq. (3) indicates that test time is minimized when the maximum scan-in and scan-out length are balanced. As stated in the motivation, we convert this problem to a 2D wrapper chain design problem and use the algorithm proposed in [24] to solve it. The composition of each wrapper chain derived is shown in Fig.6. In the figure, wrapper chain # 1 is composed of scan chain (A and C), input cells (α, β, γ) and output cells (δ). Wrapper chain # 2 is composed of only scan chains (B, D and E). Note that the input cells should be connected firstly, then scan chains are connected and output cells are considered lastly according to [24]. Next, it is time for us to consider how to connect these components in the specific order to reduce TSV overheads as much as possible.

B. Proposed Heuristic Algorithm for TSV Reduction

When the composition of each wrapper chain is determined, it is intuitive to connect them in such a fashion that the starting layer of the successive wrapper component is the same as the end layer of the former one to avoid using TSVs. This intuitive method is derived from the No-Look Ahead method proposed in [16]. For the example shown in Fig.5, the connection order of the wrapper chain #1 should be α, β, γ, C, A, δ while that of #2 should be E, B, D. We will use this method as a baseline for comparison with our proposed heuristic algorithm below.

The intuitive algorithm is simple but not effective. A counterexample is shown in Fig.7. In this figure, there are three scan chains and one output cell distributed among the four layers and these wrapper components are connected to form a wrapper chain. The connection order derived using the intuitive method is illustrated as Scheme A, which connect scan chain A firstly because it lies in the same layer as the test pin. However, if we use the scheme B shown in Fig.7, the TSV count can be reduced from 5 to 3. This phenomenon is due to the fact that the intuitive method only finds the local optimal solution in each connection step without considering the problem globally. In the following, we will propose an efficient and effective heuristic to tackle the problem.

To find the optimal design, we first represent the wrapper chain structure by a complete digraph. Nodes in the graph represent the scan chains on the wrapper chain and the edge between the two adjacent node denotes the test TSV count if the source node is connected with the sink node. Thus, the TSV optimization problem can be formulated as to find the shortest Hamilton path in this graph. We propose a greedy-based heuristic to tackle it. Firstly, a complete digraph is constructed and vertices denote wrapper components on the wrapper chain. Secondly, edges of the constructed complete digraph are sorted in the descendant order regarding to their length. Then, the shortest edge is selected and two vertices of this edge are marked so as not to be considered again in the following steps. Above selection scheme is continued until all vertices have been marked once and only once. Thus, the shortest Hamilton path is obtained. Fig.8 shows the complete digraph for wrapper chain #2. The shortest Hamilton path is depicted in dashed line in the figure. The final solution of the above example derived by our 3D Wrapper Chain Design (3D-WCD) algorithm is illustrated in Fig.9.

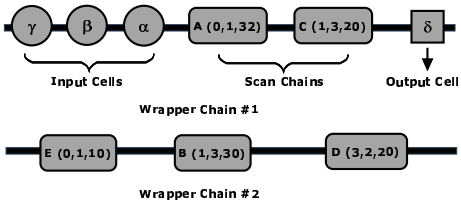

Fig. 9. The Final Wrapper Chain Structure of the Illustrative Example

IV. Experimental Results

A. Experiment Setup

To verify the effectiveness of our algorithm, several ITC'02 SoC benchmarks are chosen for our experiments, including core7 of d281, core13 of p93791 and core 26 of p22810. Since ITC'02 SoC benchmarks only contain 2D structure specifications without layer information, every wrapper component (i.e. the scan chain or the I/O cell) is added with layer information in our experiments. Layers where input cells, output cells, scan-in cells and scan-out cells located are assigned randomly for the general sense. Test time is computed using the formula stated in Eq.(3). Our proposed algorithm is written in C++ and run on the platform configured with Pentium Dual-Core E5300 2.6GHz CPU and 2GB memory.

B. Optimal Test Time Validation

Test time optimization is of the first priority in the test wrapper chain design. To validate the effect of our proposed mapping method, we compare the test time of our design with that of the methods proposed by [16], i.e., no look-ahead and look-ahead solutions. However, the input of [16]'s algorithm is the test TSV limitation and then output the minimum test time under this limitation. For the fair comparison, we firstly apply mapping method and 3D-WCD algorithm to obtain the TSV requirement for the optimal test time. Then, the TSV count is fed to [16]'s algorithm to derive its shortest test time inversely. In this experiment, we take core 7 of d281, core 13 of p93791 and core 26 of p22810 as our benchmarks for comparisons. The former two cores are implemented using four layers and the last one is designed with six layers. The number of designated wrapper chains is assumed to be 2, 4, 6 and 8 for d281 and p93791 while 2,4,8 and 12 for p88210 respectively. The results of comparisons are plotted in Fig.10. In the figure, vertical axis denotes test time and horizontal axis denotes the different wrapper chain count. The figure indicates that the test time of the 3D SoC using our method is always shorter than those proposed by [16]. The test time can be reduced by 8.7% on average (10% for d281, 7% for p93791 and 9.1% for p22810).

C. Test TSV Optimization Evaluation

In the experiments, random algorithm, which connects wrapper components randomly, and the baseline intuitive algorithm, which mentioned in the Section III, are compared with our proposed method to validate the effectiveness of our algorithm. The benchmarks used are the same as above. The comparison results are illustrated in Fig.11. On average, both the intuitive method and 3D-WCD perform much better than the random one and 3D-WCD performs best among the three. On average, the TSV count can be reduced by 55.9% and 33.2% for 3D-WCD in comparison with the random and the intuitive methods, respectively. In addition, as the number of designated wrapper chains increases, TSVs consumed by both random and intuitive method also increase. However, 3D-WCD algorithm exhibits a relative flat trend, which validates its efficiency and effectiveness.

V. Conclusion

As 3D technology is introduced for SoC designs, testing challenge is becoming more severe than ever before, which requires new DFT mechanism. In this paper, a 3D wrapper chain construction solution is proposed to guide the designer to achieve minimal test time while optimize the number of TSVs. First, we map the 3D wrapper chain design problem to 2D problem by projecting all wrapper components onto one layer. Then, a heuristic algorithm is proposed to determine how to connect the components within a wrapper chain to reduce the number of TSVs for testing. From experimental results, it is shown that the test wrapper structure designed by this flow can minimize the test time in comparison with the algorithms proposed by [16] (8.7% on average). Moreover, the number of test wrapper TSVs needed for the test time optimal design is also optimized dramatically (as much as 55.9% reductions in comparison with random method and 33.2% in comparison with intuitive method).

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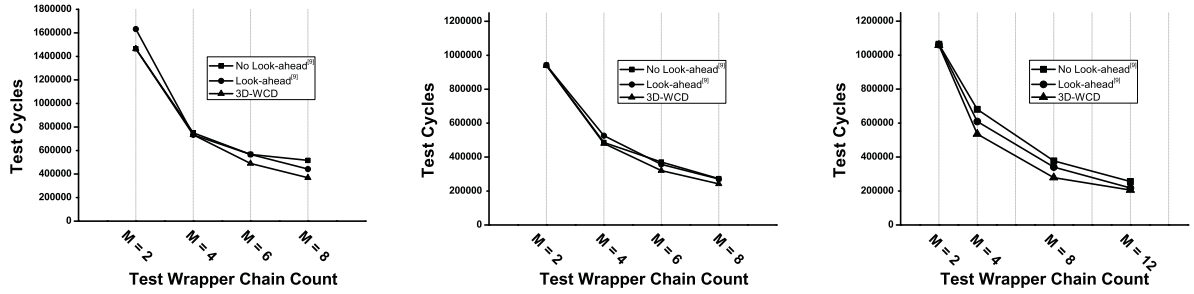
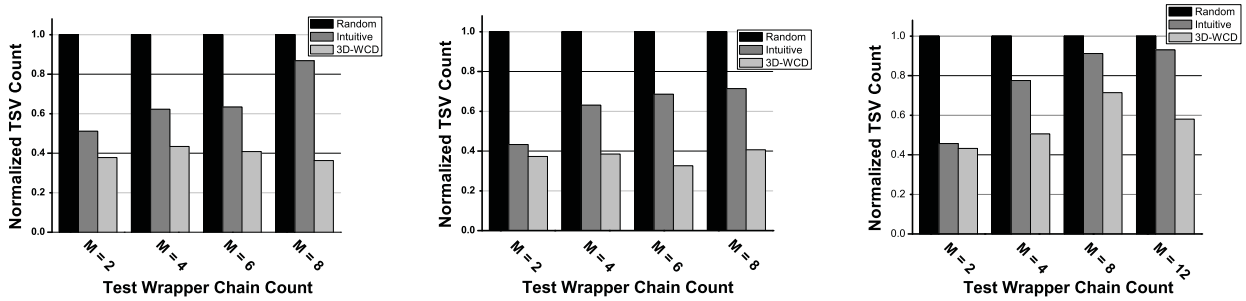


(a) (b) (c)

Fig. 10. Test Time Comparisons for the Three Algorithms on (a) Core 7 of d281 (b) Core 13 of p93791 and (c) Core 26 of p22810 SoC Benchmarks



(a) (b) (c)

Fig. 11. Test TSV Count Comparisons Among Three Algorithms for (a) Core 7 of d281, (b) Core 13 of p93791 and (c) Core 26 of p22810 Benchmarks

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