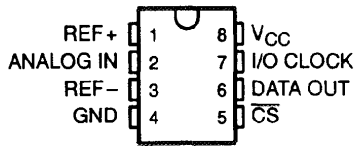
17 1026

TLC548C, TLC548I, TLC549C, TLC549I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067A – NOVEMBER 1983 – REVISED MARCH 1995

- Microprocessor Perlpherai or Stand-Aione Operation
- 8-Bit Resolution A/D Converter
- Differential Reference Input Voitages
- Conversion Time . . . 17 µs Max
- Total Access and Conversion Cycies Per Second
  - TLC548 . . . up to 45,500
  - TLC549 . . . up to 40,000
- On-Chip Software-Controiiabie Sample-and-Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- 4-MHz Typicai internai System Ciock
- Wide Suppiy Range . . . 3 V to 6 V
- Low Power Consumption . . . 15 mW Max
- ideal for Cost-Effective, High-Performance Appiications inciuding Battery-Operated Portable instrumentation
- Pinout and Controi Signals Compatibie With the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit ND Converter
- CMOS Technoiogy

D OR P PACKAGE
(TOP VIEW)



iescription

The TLC548 and TLC549 are CMOS analog-todigital converter integrated circuits buiit around an 8-b switched-capacitor successive-approximation ADC. They are designed for seriat-interface with a micrc processor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use onl the input/output clock (I/O CLOCK) input aiong with the chip select (CS) input for data controi. The maximur I/O CLOCK input frequency of the TLC548 is 2.048 MHz. and the I/O CLOCK input frequency of the TLC54 is specified up to 1.1 MHz. Detaiied information on interfacing to most popular microprocessors is readil availabie from the factory.

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC54 devices; however, the TLC548 and TLC549 provide an on-chip system ciock that operates typically at 4 MH and requires no external components. The on-chip system clock allows internal device Operation to procee independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desire for a wide range of Software and hardware requirements. The I/O CLOCK together with the internal system cloc allow high-speed data transfer and conversion rates of 45,500 conversions per second for the TLC548, ar 40,000 conversions per second for the TLC549.

AVAILABLE OPTIONS

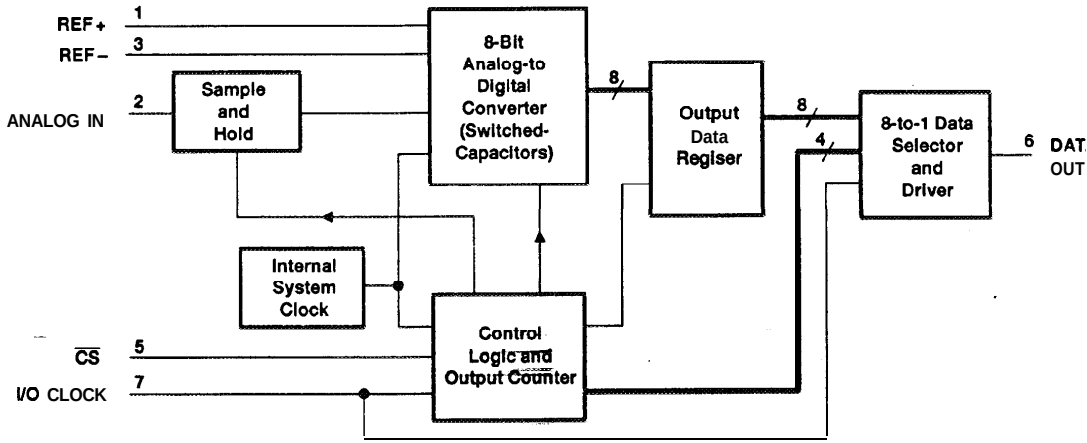
T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TLC548CD TLC549CD	TLC548CP TLC549CP
–40°C to 85°C	TLC548ID TLC549ID	TLC548IP TLC549IP

description (Continued)

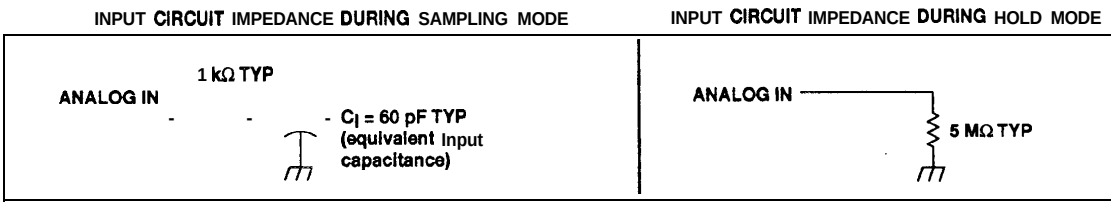
Additional TLC548 and TLC549 features include versatile control logic, an on-chip Sample-and-hold circuit tha can operate automatically or under microprocessor control, and a high-speed converter with differenti high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation fro logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circu allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 µs.

The TLC548C and TLC549C are characterized for Operation from 0°C to 70°C. The TLC548I and TLC549I ar characterized for Operation from –40°C to 85°C.

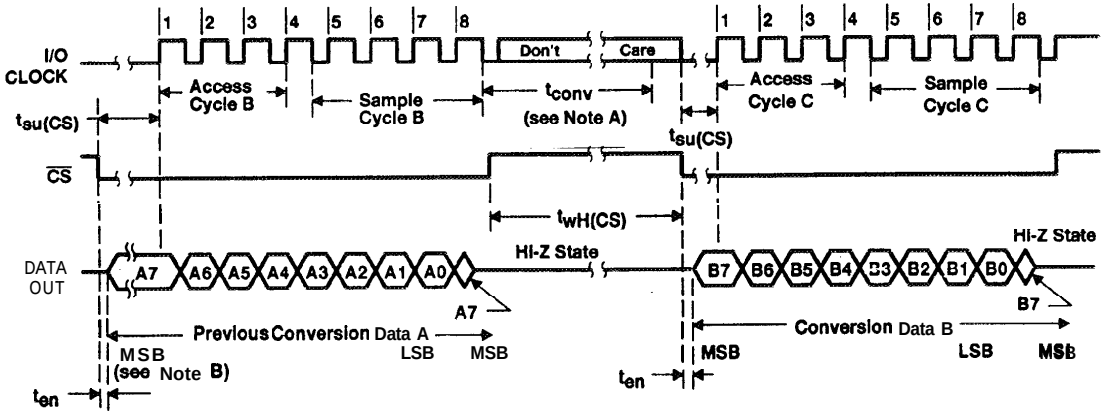
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 µs maximum), is initiated with the eighth I/O clock puls trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bi (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bi (A6–A0) will be clocked out on the first seven I/O clock falling edges. B7–B0 will follow in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 6.5
Input voltage range at any input . . . . . –0.3 V to V_{CC} + 0.3
Output voltage fange . . . . . -0.3 V to V_{CC} + 0.3
P±10 input current range (any input) . . . . . m
Peak total input current range (all inputs) . . . . . m
Operating free-air temperature range, T_A (see Note 2): TLC548C, TLC549C . . . . . 0°C to 70"
TLC548I, TLC549I . . . . . -40°C to 85"
Storage temperature range, T_{stg} . . . . . –65°C to 150°
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260"

NOTES: 1. All voltage values are with respect to the network ground terminal with the REF- and GND terminals connected together, unle otherwise noted.

2. The D package is not recommended below -40°C.

recommended operating conditions

		TLC548			TLC549			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{ref+} (see Note 3)		2.5	V_{CC}	V_{CC}+0.1	2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-} (see Note 3)		–0.1	0	2.5	–0.1	0	2.5	V
Differential reference voltage, V_{ref+}, V_{ref-} (see Note 3)		1	V_{CC}	V_{CC}+0.2	1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 V to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 V to 5.5 V)				0.8			0.8	V
Input/output clock frequency, $f_{clock(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock transition time, $t_{t(I/O)}$ (see Note 4) (for V_{CC} = 4.75 V to 5.5 V)				100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for V_{CC} = 4.75 V to 5.5 V)		17			17			µs
Setup time, $\overline{CS}$ low before first I/O CLOCK, $t_{su(CS)}$ (for V_{CC} = 4.75 V to 5.5 V) (see Note 5)		1.4			1.4			µs
Operating free-air temperature, T_A	TLC548C, TLC549C	0		70	0		70	°C
	TLC548I, TLC549I	–40		85	–40		85	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111). while input voltages less than that applied to REF- convert to all zeros (00000000). Forproperoperation, the positive reference voltage V_{ref+}, must be at least 1 V greater than the negative reference voltage V_{ref-}. In addition, unadjusted errors rnay increase as the differential reference voltage $V_{ref+} - V_{ref-}$ falls below 4.75 V.

4. This is the time required for the input/output clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.

5. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. This $\overline{CS}$ set-up time is given by the ten and $t_{su(CS)}$ specifications.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V,	I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current, control inputs		V_I = V_{CC}			0.005	2.5	µA
I_{IL}	Low-level input current, control inputs		V_I = 0			-0.005	-2.5	µA
$I_{I(on)}$	Analog channel on-state input current during sample cycle		Analog input at V_{CC}			0.4	1	µA
			Analog input at 0 V			−0.4	−1	
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.8	2.5	mA
I_{CC} + I_{ref}	Supply and reference current		V_{ref+} = V_{CC}			1.9	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

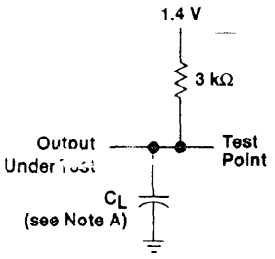
operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC548			TLC549			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
E_L	Linearity error	See Note 6			±0.5			±0.5	LSB
E_{ZS}	Zero-scale error	See Note 7			±0.5			±0.5	LSB
E_{FS}	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
t_{conv}	Conversion time	See Operating Sequence		8	17		12	17	µs
	Total access and conversion time	See Operating Sequence		12	22		19	25	µs
ta	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓		10			10			ns
t_d	Delay time to data output valid	I/O CLOCK↓			2000			400	ns
t_{en}	Output enable time	See Parameter Measurement Information			1.4			1.4	µs
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

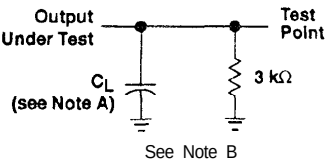
† All typicals are at V_{CC} = 5 V, TA = 25°C.

NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the differenc between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.

PARAMETER MEASUREMENT INFORMATION

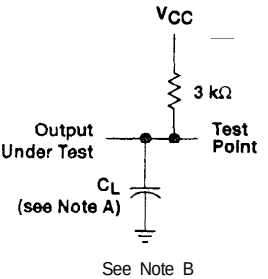


LOAD CIRCUIT FOR t_d, t_r, AND t_f



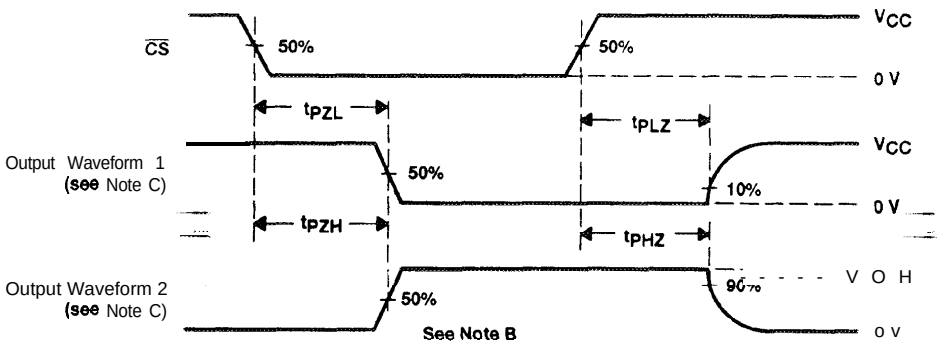
See Note B

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

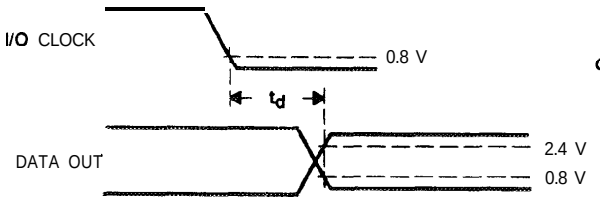


See Note B

LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND **DISABLE** TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME

VOLTAGE WAVEFORMS **FOR** RISE AND FALL **TIMES**

NOTES: A. CL = 50 pF for TLC548 and 100 pF for TLC549; CL includes jig capacitance.
B. ten = t_{PZH} or t_{PZL}, **bis** = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to VS with 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C(1/2\ \text{LSB}) = VS - (V_S/512) \quad (2)$$

Equating equaticn 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = VS\ (1 - e^{-t_c/R_t C_i}) \quad (3)$$

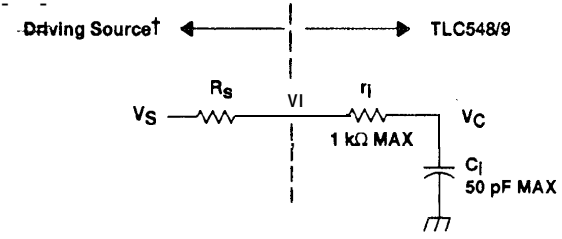
and

$$t_c(1/2\ \text{LSB}) = Rt \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c(1/2\ \text{LSB}) = (R, + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at ANALOG IN
VS = Extemal Driving Source Voltage
R_s = Source Resistsnce
r_i = Input Resistance
C_I = Input Capacltance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an intern system clock, sample and hold, 8-bit A/D converter, data register, and control iogic circuitry. For flexibility and acces speed, there are two controi inputs: I/O CLOCK and chip select ($\overline{CS}$). These control inputs and a TTL-compatib 3-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can t completed in 17 µs or less, while complete input-conversion-output cycles can be repeated in 22 µs for the TLC54 and in 25 µs for the TLC549.

The internal system clock and I/O CLOCK are used independently and do not require any special speed or phas relationships between them. This ındependence simplifies the hardware and Software control tasks for the devic Due to this independence and the internal generation of the system clock, the control hardware and Software nee oniy be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. this manner, the internal system clock drives the "conversion crunching" circuitry so that the control hardware an software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a high-impedance condition and I/O CLOCK is disabled. This $\overline{CS}$ control functio allows I/O GLOCK to share the same control logic point with its counterpart terminal when additional TLC548 an TLC549 devices are used. This also serves to minimize the required control logic terminals when using multipl TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtai the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for two rising edge and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. Howeve upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even thoug the rest of the integrated circuitry will not recognize the transition until the $t_{su(CS)}$ specification has elapsed This technique is used to protect the device against noise when used in a noisy environment. The mos significant bit (MSB) of the previous conversion result will initially appear on DATA OUT when $\overline{CS}$ goes lov
2. The falling edges of the first four I/O CLOCK cycles shift out the second, third, fourth, and fifth most significar bits of the previous conversion result. The on-chip sample and hold begins sampling the analog input after th fourth high-to-low transition of I/O CLOCK. The sampling Operation basically involves the charging of intern; capacitors to the level of the analog input voltage.
3. Three more I/O CLOCK cycles are then applied to the I/O CLOCK terminal and the sixth, seventh, and eight conversion bits are shifted out on the falling edges of these clock cycles.
4. The final, (the eighth), clock cycle is applied to I/O CLOCK. The on-chip sample and hold begins the hol function upon the high-to-low transition of this clock cycle. The hold function will continue for the next fou internal system clock cycles, after which the holding function terminates and the conversion is performe during the next 32 system clock cycles, giving a total of 36 cycles. After the eighth I/O CLOCK cycle, $\overline{CS}$ mus go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completio of the hold and conversion functions. $\overline{CS}$ can be kept low during periods of multipie conversion. When keepin $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on th I/O CLOCK line. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller an the device will lose synchronization. If $\overline{CS}$ is taken high, it must remain high until the end of conversion Otherwise, a valid high-to-low transition of $\overline{CS}$ will cause a reset condition, which will abort the conversion i progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previou conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in timt This device will accommodate these applications. Although the on-chip sample and hold begins sampling upon th high-to-low transition of the fourth I/O CLOCK cycle, the hold function does not begin until the high-to-low transitio of the eighth I/O CLOCK cycle, which should occur at the moment when the analog signal must be converted. Th TLC548 and TLC549 will continue sampling the analog input until the high-to-low transition of the 8th I/O CLOC pulse. The control circuitry or Software will then immediately lower I/O CLOCK and start the holding function to hol the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to the most popular microprocessor is readily available from Texas Instrument: