Solutions for IE1205 2022-01-17 exam

Problem 1

Let A be Alice goes, B Ben goes, and so on.

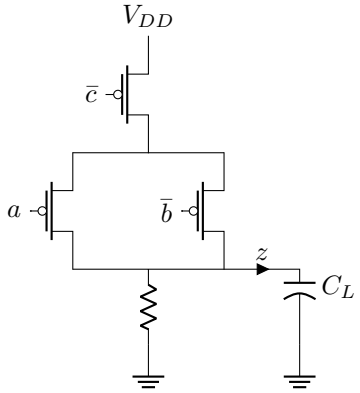
- Ben goes, unless both Elena and Carlos skips. So Ben goes if either Elena or Carlos goes; $B = C + E$.
- Carlos goes if two more go. So if Alice and Ben goes Carlos goes, or, if Alice and David goes Carlos goes, and so on; $C = AB + AD + AE + BD + BE + DE$.
- David goes if Ben goes or if at most three people go. So if one person other than Ben skips or if Ben goes, David goes; $D = \bar{A} + B + \bar{C} + \bar{E}$.
- Elena goes if everybody else go; $E = ABCD$.

Problem 2

If $A = 0$ the top transistors are off and the bottom ones on (conducting) and $F = B$. If $A = 1$ it is the opposite and $F = \bar{B}$. Thus, $F = \bar{A}B + A\bar{B} = A \oplus B$.

Problem 3

z implemented in PMOS using one serial and one parallel primitive:



The change will charge the capacitor because when $abc = 110$ the capacitor is connected to ground and when $abc = 011$ it is connected to V_{dd}. The answer is F since the charge rises rapidly.

Problem 4

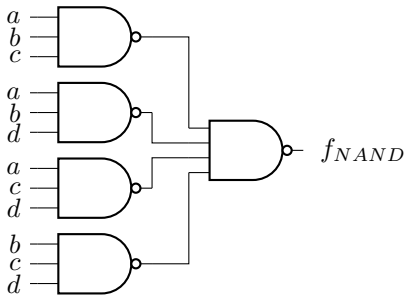
The four-input majority function has the truth table:

a	b	c	d	f
0	0	–	–	0
0	1	0	–	0
0	1	1	0	0
0	1	1	1	1
1	0	0	–	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	–	1

Function's boolean expressions derived using Karnaugh maps:

$$
\begin{aligned}
f_{SOP} &= abc + abd + acd + bcd \\
f_{POS} &= (a+b)(a+c)(a+d)(b+c)(b+d)(c+d) \\
f_{NAND} &= \overline{\overline{abc} \cdot \overline{abd} \cdot \overline{acd} \cdot \overline{bcd}}
\end{aligned}
$$

Circuit implementing f_{NAND}:



Problem 5

Division of $36_{10} = 100100_2$ with $3_{10} = 11_2$:

```
          0  0  1  1  0  0
        +-----------------
1  1  |  1  0  0  1  0  0
      -  0
      ----
         1  0
      -     0
      -------
         1  0  0
      -     1  1
      ----------
               1  1
      -        1  1
      -------------
                  0  0
      -              0
      ----------------
                     0  0
      -              0
      ----------------------
                        0
```

Multiplication of $-0.25 = 1.11_2$ and $-0.5 = 1.10_2$ in Q1.2 format by sign extending both numbers to six bits:

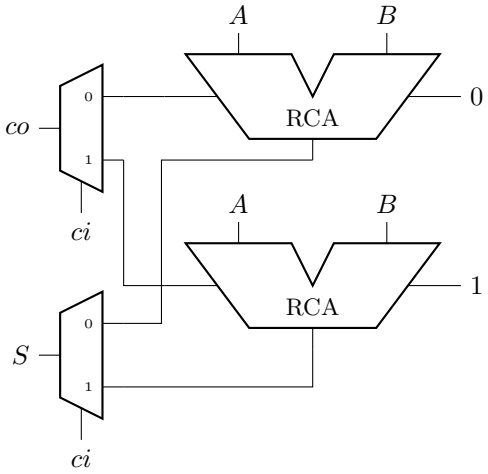
```
          1  1  1  1  1  1
      *   1  1  1  1  1  0
      ------------------
          0  0  0  0  0  0
          1  1  1  1  1  x
          1  1  1  1  x  x
          1  1  1  x  x  x
          1  1  x  x  x  x
      +   1  x  x  x  x  x
      ------------------
          0  0  0  0  1  0
```

Result is $00.0010_2 = 0.125 = 1/8$. Equivalent solution that two-complements the last double-negative term:

```
                   1  1  1
      *            1  1  0
      ------------------
          0  0  0  0  0  0
          1  1  1  1  1  x
      +   0  0  0  1  x  x
      ------------------
          0  0  0  0  1  0
```

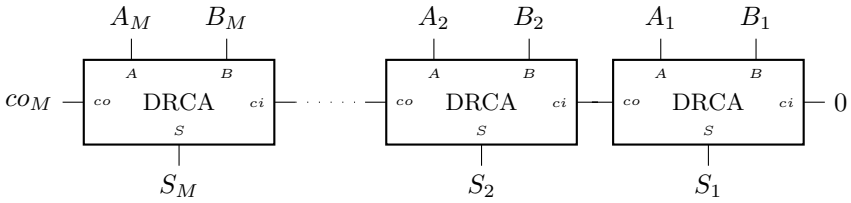
Problem 6

Let DRCA be the following circuit:



The circuit takes two N-bit numbers and a carry in bit as inputs; A, B, and ci. It outputs the sum of the numbers an a carry out bit; S and co. The RCAs compute the sum and carry out for $ci = 0$ and $ci = 1$. The muxes select the output based on ci.

The MxN CLA chains M DRCA circuits:



The carry out of every DRCA is connected to the carry in of the next. Except for the last one, whose carry out is disconnected and the first one, whose carry in is 0. The numbers given as input to each DRCA are two N-bit slices of the numbers to add so that the first DRCA is given the N least significant bits, the next DRCA the next N least significant bits, and so on. The full addition is the concatenation of all N-bit sum slices outputted by the DRCAs.

The critical path through the MxN CLA is from one of the first bit slices to the last carry out – A_1 (or B_1) to co_M. Let $\mathrm{D}[ci \to co]$ and $\mathrm{D}[A \to co]$ be the DRCA's path delays to carry out and $\mathrm{D}[i \to o]$ and $\mathrm{D}[(s \to o)]$ the muxes' path delays, then:

$$\begin{aligned}\mathrm{D}[A_1 \to co_M] &= \mathrm{D}[A \to co] + (M-1)\mathrm{D}[ci \to co] \\ &= \mathrm{D}[RCA] + \mathrm{D}[(i \to o)] + (M-1)\mathrm{D}[s \to o] \\ &= 4 + 2N + 2 + (M-1)3 = 2N + 3M + 3\end{aligned}$$

If the first DRCA is replaced with an RCA the path delay shrinks to $2N+3M+1$. Both solutions are acceptable.

Problem 7

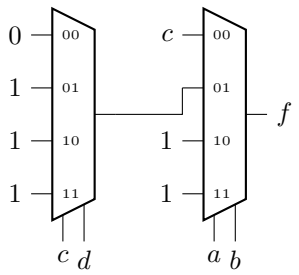
$f = ab + a\bar{c} + b\bar{c}d + c$ simplifies to $f = a + bd + c$. Decomposition with respect to a and b:

a	b	$a + bd + c$
0	0	c
0	1	$c + d$
1	–	1

Decomposition of the second row:

c	d	$c + d$
0	0	0
–	1	1
1	–	1

Implementation of expression $\bar{a}\bar{b} \cdot c + \bar{a}b \cdot (c + d) + a\bar{b} \cdot 1 + ab \cdot 1$ using two 4-to-1 muxes:



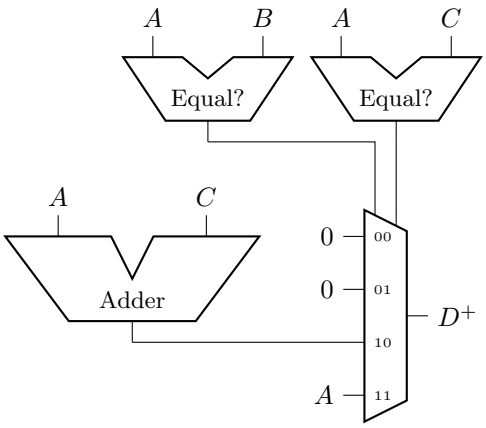
Alternative decomposition: $\bar{a}\bar{c} \cdot bd + \bar{a}c \cdot 1 + a\bar{c} \cdot 1 + ac \cdot 1$ (implementation not shown).

Problem 8

Let D^+ denote the value to assign to D for the cases $A = B$ and $A = C$:

$A = B$	$A = C$	D^+
0	0	0
0	1	0
1	0	$A + C$
1	1	A

Note that 0 as a value for D is an 8-bit number and not a single bit. The following circuit implements the design:



The Equal? circuit signals 1 if the two input numbers are equal. This is accomplished by connecting a NOR gate to the *lt* and *gt* signals of a comparator. The width of all wires is 8 except for the wires from the Equal? circuits to the mux which are single bits. The circuit can also be implemented using two 2-to-1 muxes instead of one 4-to-1 mux.

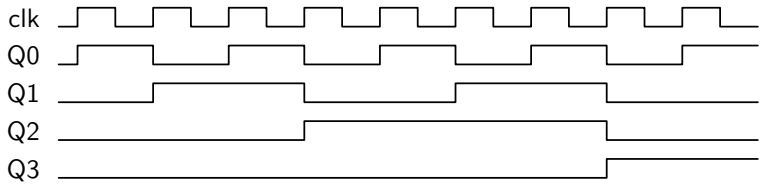
Problem 9

s_2	s_1	s_0	Op	Description
0	0	-	OP_0	No operation
0	1	0	OP_1	Not used
0	1	1	OP_2	Same as OP_1
1	0	0	OP_3	Left shift
1	0	1	OP_4	Left rotate
1	1	1	OP_5	Right shift
1	1	1	OP_6	Right rotate

The shifts are logical because the sign bit is not preserved.

$X = \text{AB}_{16} = 10101011_2$. X left shifted is $01010110_2 = 56_{16}$ and right rotated is $11010101_2 = \text{D5}_{16}$.

Problem 10

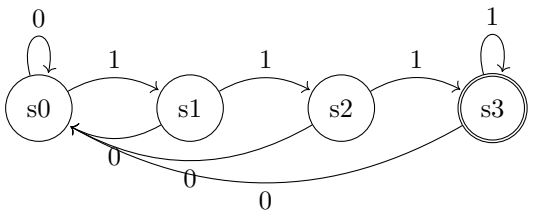


Problem 11

A setup violation occurs if $T_{\text{clk}} < T_{\text{setup}} + T_{\text{clk}-2-\text{Q}} + T_{\text{cp}} - T_{\text{skew}}$. Solving for T_{skew} reveals that the skew needs to be at least 3 ns. A hold violation occurs as

$T_{\text{clk}-2-\text{Q}} + T_{\text{sp}} < T_{\text{skew}} + T_{\text{hold}}$, which is the case by 0.1 ns. Increasing T_{sp} by 0.1 ns avoids the hold violation.

Problem 12



The FSM emits 1 in state s3 and 0 elsewhere.

X	-	1	0	1	1	1	0	1	1	0	0	1	1	1	1	0	1	0	0
Z	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0
Curr_state	s0	s0	s1	s0	s1	s2	s3	s0	s1	s2	s0	s0	s1	s2	s3	s3	s0	s1	s0
Next_state	s0	s1	s0	s1	s2	s3	s0	s1	s2	s0	s0	s1	s2	s3	s3	s0	s1	s0	s0

Problem 13

Truth table and boolean equations for counter. $D_1^+, \ldots, D_4^+$ denotes the next state variables and $T_1, \ldots, T_4$ the T flip-flop inputs.

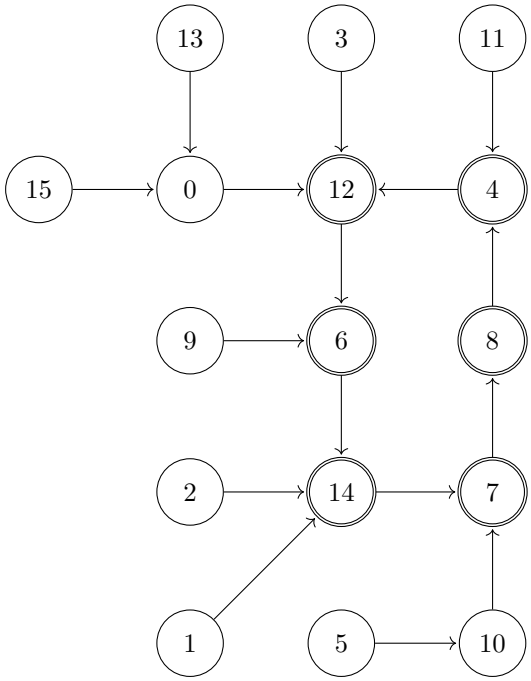
#	D_1	D_2	D_3	D_4	D_1^+	D_2^+	D_3^+	D_4^+	T_1	T_2	T_3	T_4
0	0	0	0	0	–	–	–	–	–	–	–	–
1	0	0	0	1	–	–	–	–	–	–	–	–
2	0	0	1	0	–	–	–	–	–	–	–	–
3	0	0	1	1	–	–	–	–	–	–	–	–
4	0	1	0	0	1	1	0	0	1	0	0	0
5	0	1	0	1	–	–	–	–	–	–	–	–
6	0	1	1	0	1	1	1	0	1	0	0	0
7	0	1	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	1	0	0	1	1	0	0
9	1	0	0	1	–	–	–	–	–	–	–	–
10	1	0	1	0	–	–	–	–	–	–	–	–
11	1	0	1	1	–	–	–	–	–	–	–	–
12	1	1	0	0	0	1	1	0	1	0	1	0
13	1	1	0	1	–	–	–	–	–	–	–	–
14	1	1	1	0	0	1	1	1	1	0	0	1
15	1	1	1	1	–	–	–	–	–	–	–	–

$$
\begin{aligned}
T_1 &= 1 \\
T_2 &= \overline{D_2} + D_4 \\
T_3 &= D_1 D_2 \overline{D_3} + D_4 \\
T_4 &= D_1 D_3 + D_4
\end{aligned}
$$

The ten illegal states and their next states are (T flip-flops inputs shown for clarity):

D_1	D_2	D_3	D_4	D_1^+	D_2^+	D_3^+	D_4^+	T_1	T_2	T_3	T_4
0	0	0	0	1	1	0	0	1	1	0	0
0	0	0	1	1	1	1	0	1	1	1	1
0	0	1	0	1	1	1	0	1	1	0	0
0	0	1	1	1	1	0	0	1	1	1	1
0	1	0	1	1	0	1	0	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1	0	1
1	0	1	1	0	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0	1	1	0	1
1	1	1	1	0	0	0	0	1	1	1	1

This diagram illustrates the transitions between the six legal states (double-circled) and ten illegal states (single-circled). The numbers represent $D_1D_2D_3D_4$ interpreted as decimal numbers:



Problem 14

The next state expressions are $A^+ = XA + XB$ and $B^+ = XA + X\bar{B}$. State transition table including the output of the FSM ($Y = \overline{AB}$):

A	B	X	A^+	B^+	Y
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	0