2.

a.

According to given values, duty cycle (D) range is 0.25 - 0.6875. This range is found using the equation AA. The converter should be operating in CCM operation between this duty range.

AA

And using the given constant output voltage and rated output power in equation BB, the output current is found to be 1A.

BB

In order to find **minimum** inductance that would keep de converter operating in CCM operation, the output current should be equal to output boundary current value (equation. It cannot directly found from the maximum boundary current value (equation X2) since all values in D range (0.25 – 0.6875) should be ensured but in equation X2, D = 1/3.

X1

X2

The possible L range with respect to found data is 1.79 – 3.95 µH. If 1.79 µH (i.e. minimum value of the possible inductor range) is chosen, the converter cannot operate in CCM operation mode when duty cycle is below 0.6875. In order to converter operate in CCM operation mode under given all circumstances, **L should be chosen as 3.9** µH, considering all the values in D range**.**

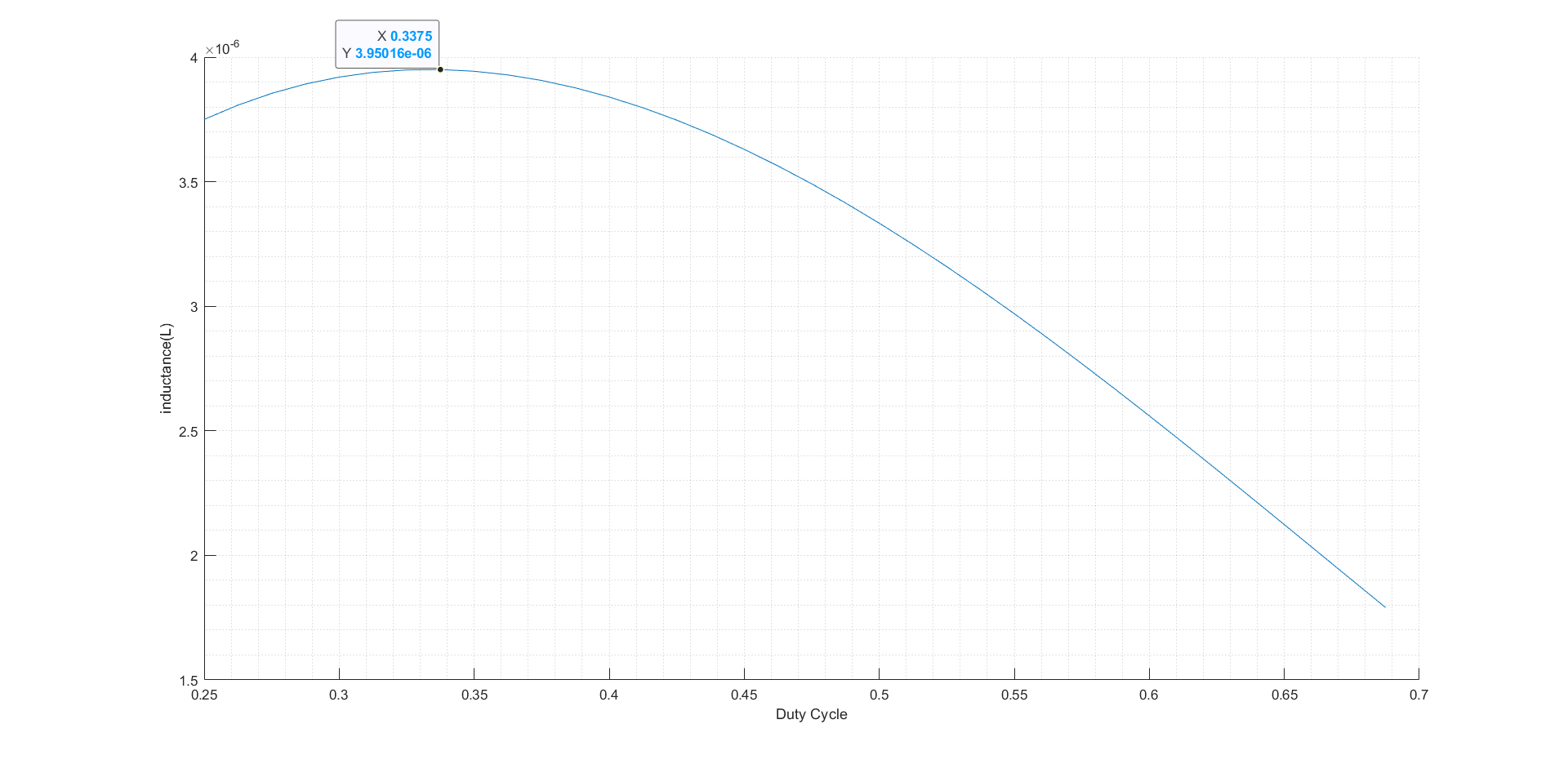
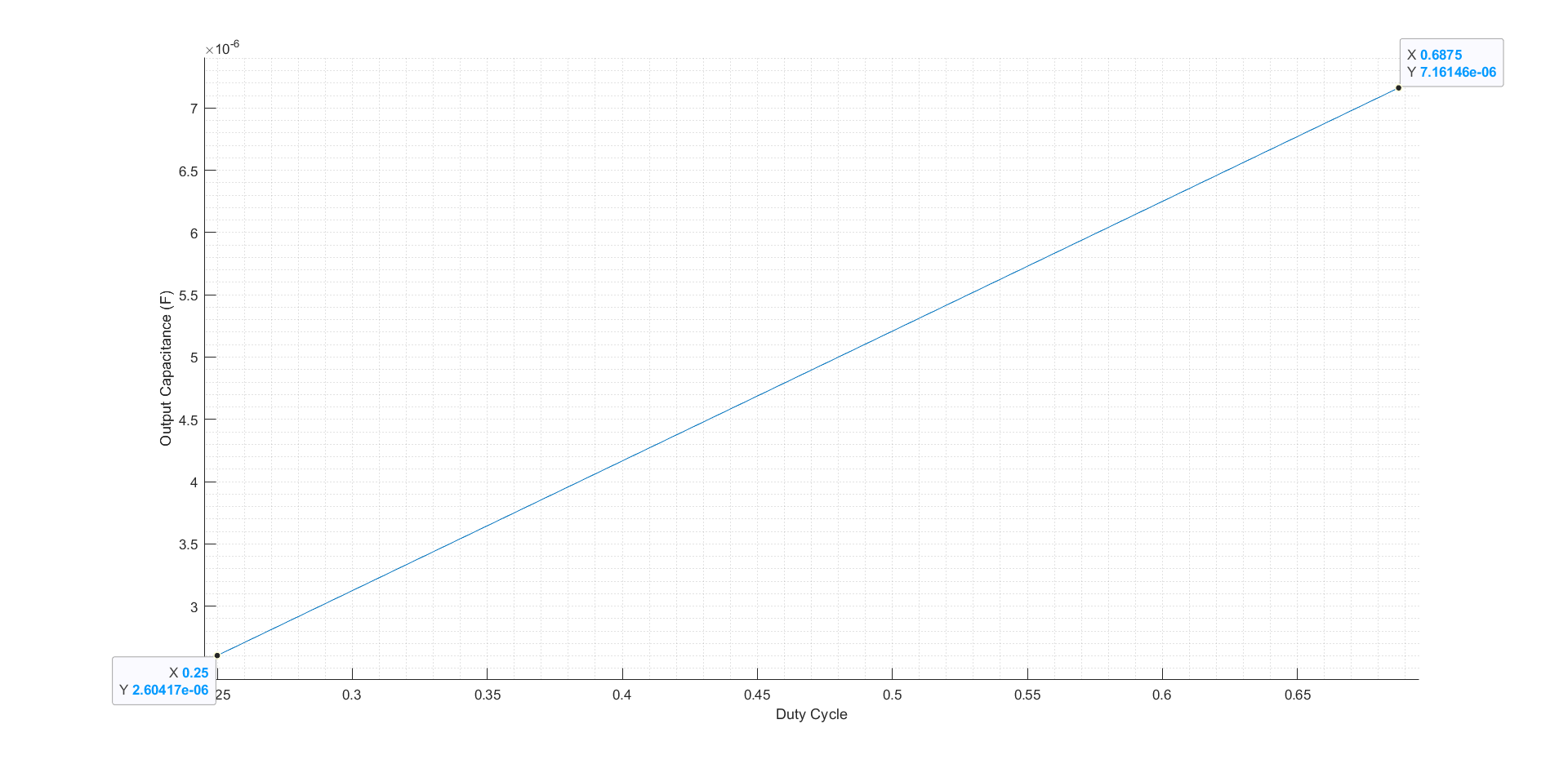


Figure X. Duty cycle vs Inductance

b.

Output capacitance for peak-to-peak voltage ripple less than 2% can be calculated by using the equation YY where and .

The connection between duty cycle and output capacitance can be observed in figure X. Output capacitance should be chosen as 7.16146 µF for voltage ripple smaller than 2% for all values of duty cycle.



*Figure X. Duty Cycle vs Output Capacitance*

c.

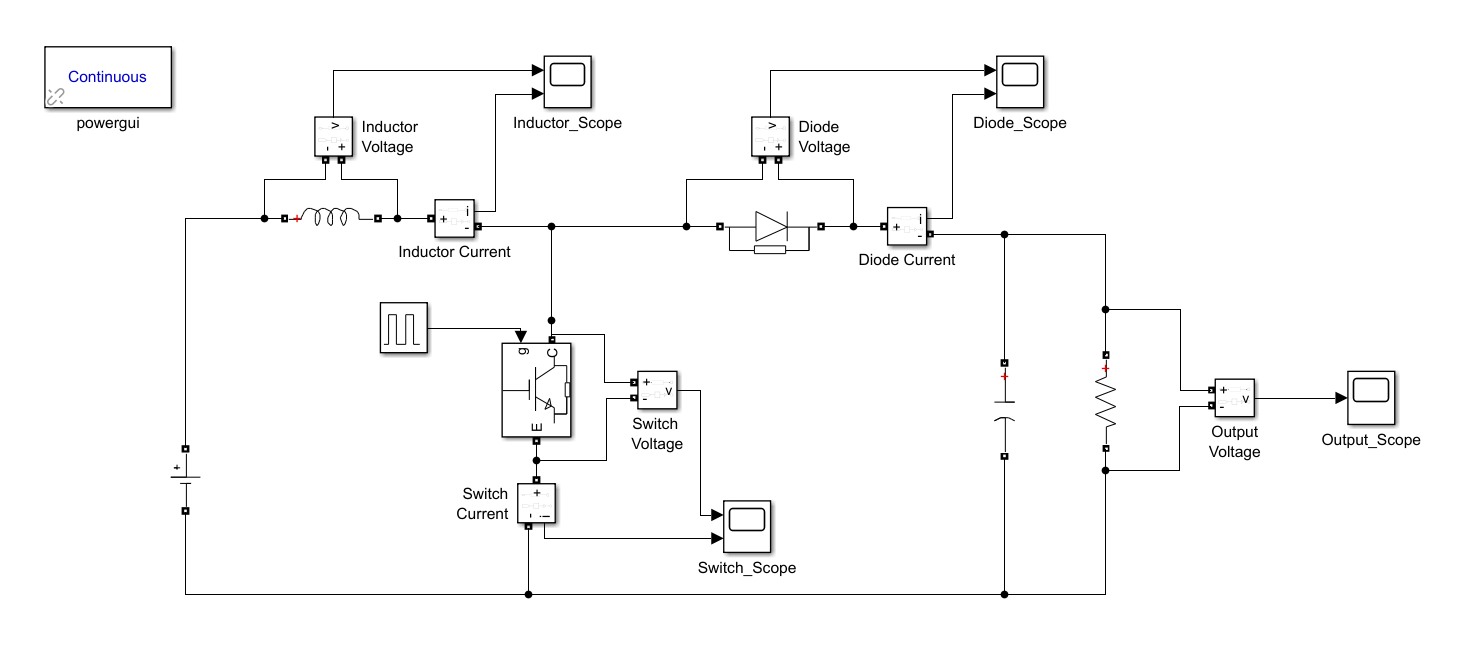
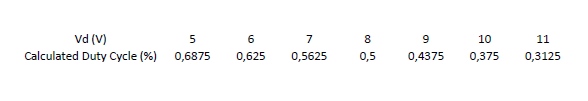


Figure XX. Boost Converter Circuit Design for Part 2.c

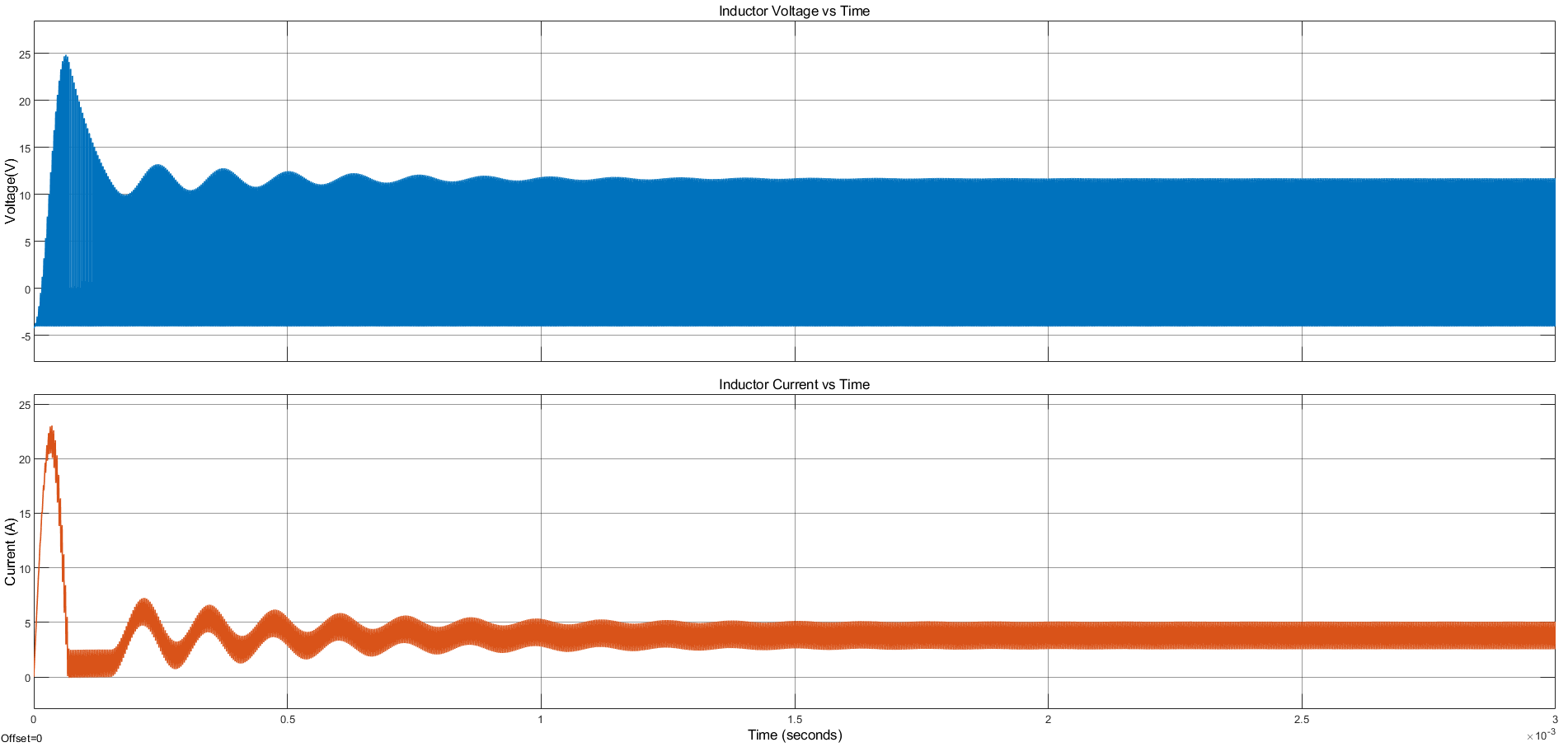
Considering the constant output and varying input voltage, a duty cycle range is calculated using the equation AA. The results can be seen in figure ZZ.



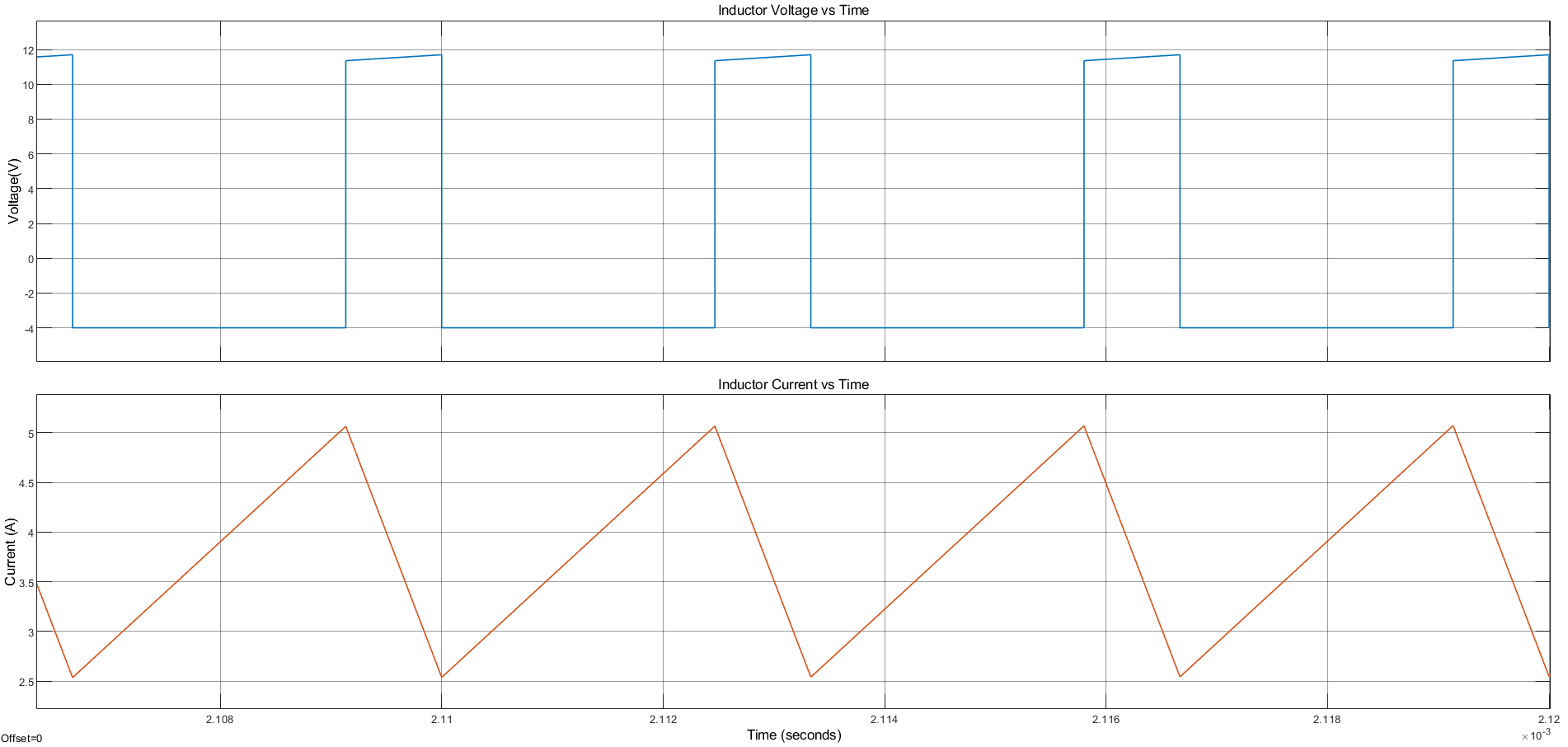
*Figure ZZ.* *Varying Input Voltages and Respective Duty Cycles*

But those calculations are made under the assumption that components are ideal. Even though simulation is designed to converge to ideal, there are still some non-idealities that causes approximately 5% duty cycle deflection (they should be increased approximately 5% to get Vo = 16V).

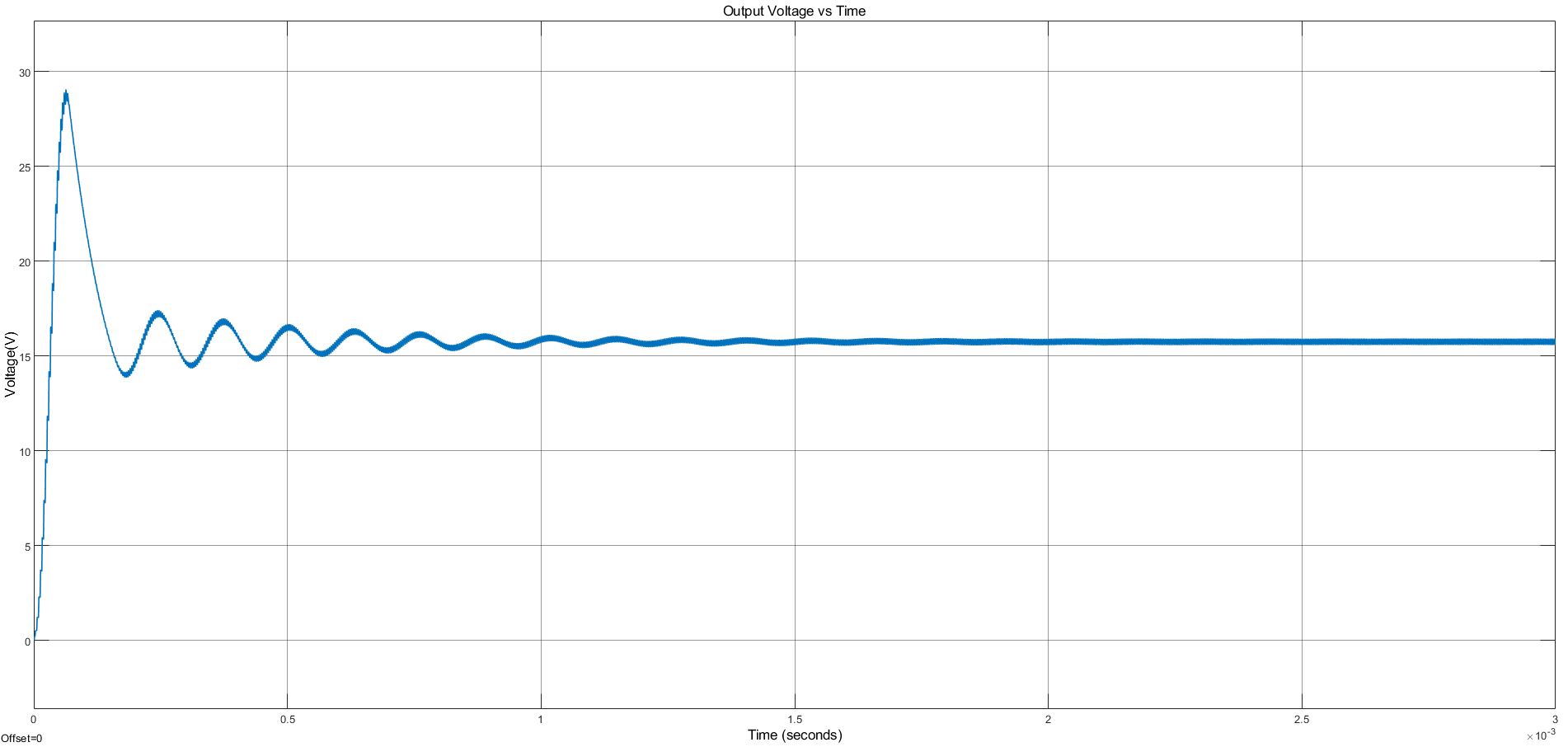
In order to analyze the waveforms properly they first observed on a large scale then small scale.There are high fluctuations in the beginning of the simulations, which can be explained by capacitor not being pre-charged.



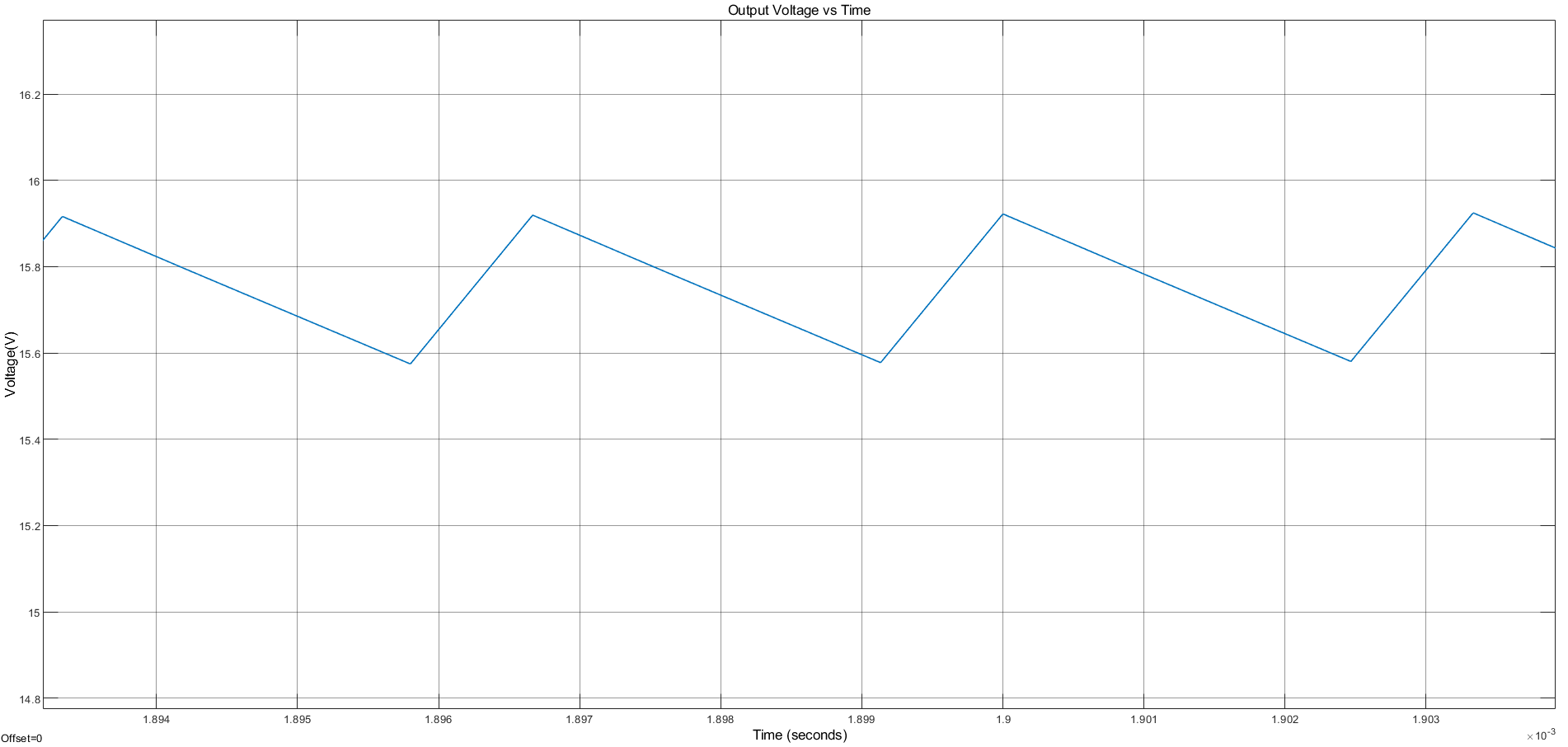
*Figure X. Inductor Voltage & Current vs Time for Input Voltage = 5V and D = 74%*



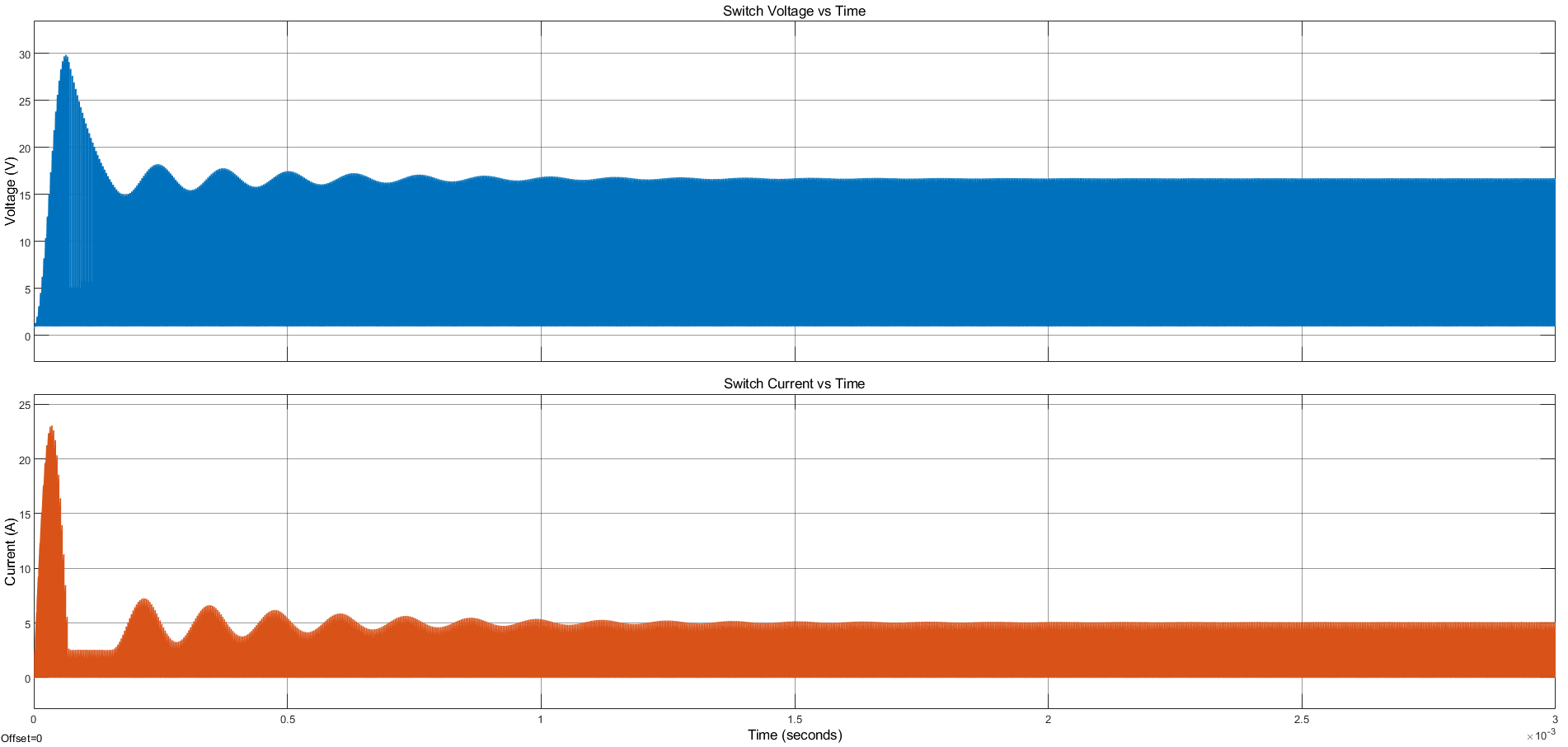
*Figure X. Inductor Voltage & Current vs Time for Input Voltage = 5V and D = 74%*



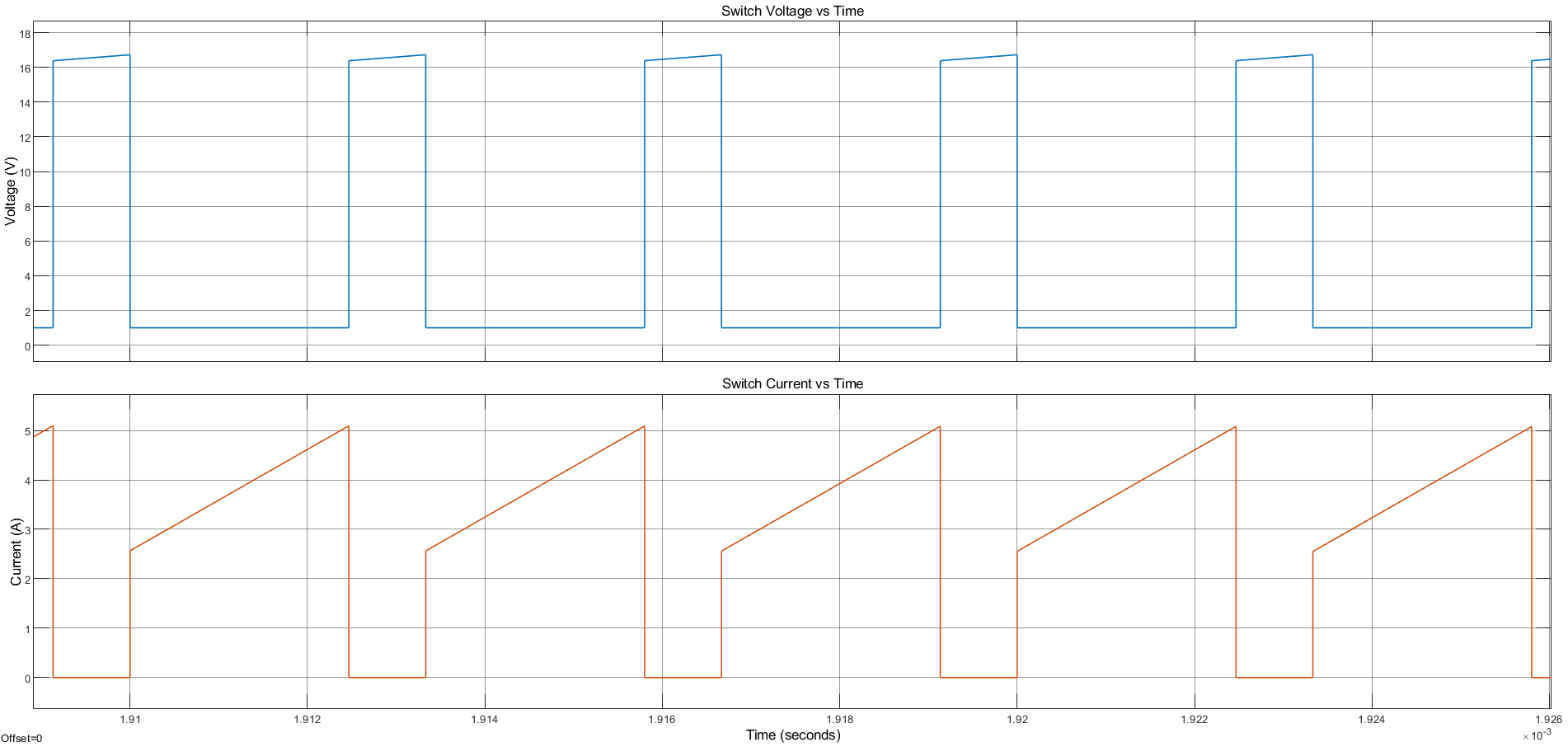
*Figure X. Output Voltage vs Time for Input Voltage = 5V and D = 74%*



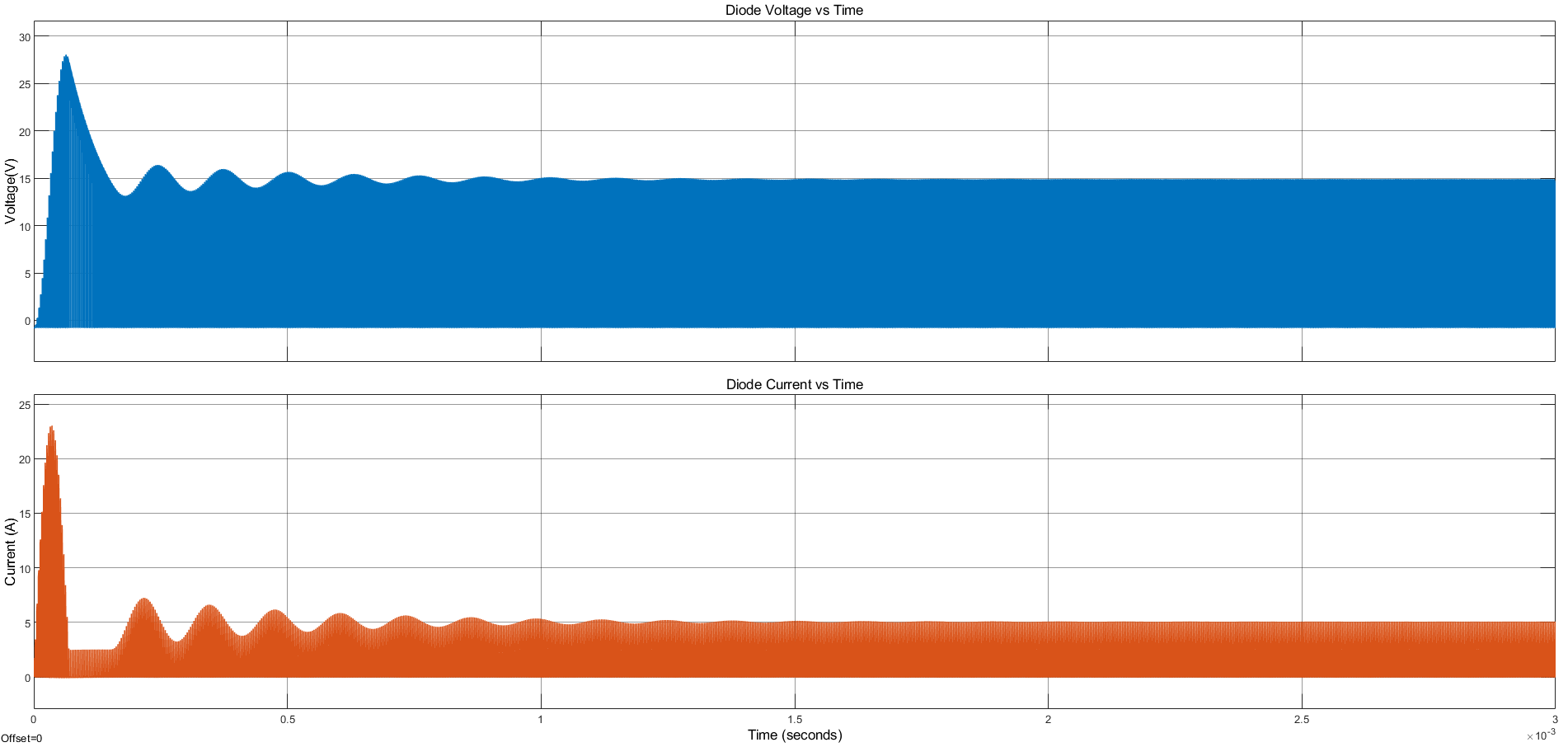
*Figure X.Output Voltage vs Time for Input Voltage = 5V and D = 74%*



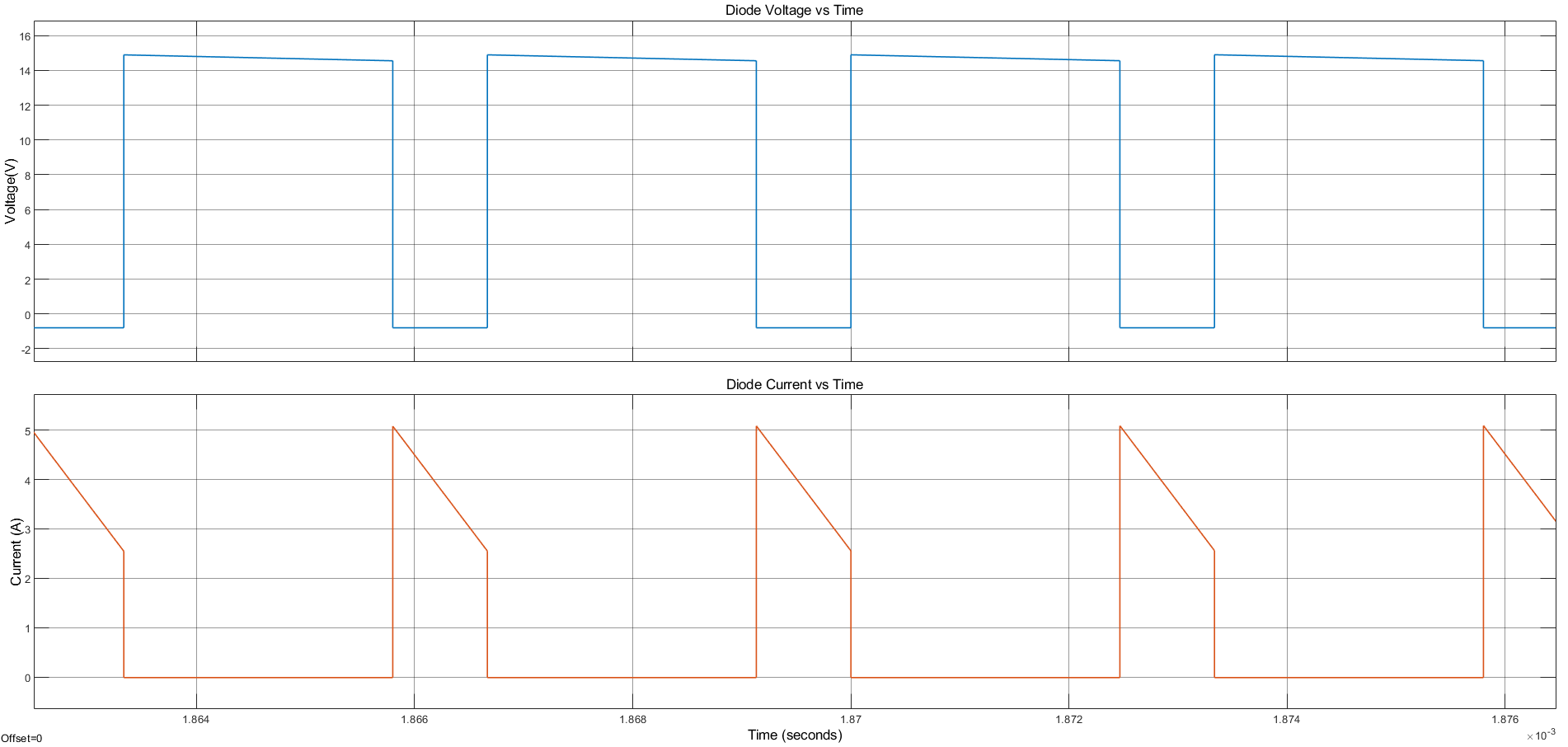
*Figure X. Switch Voltage & Current vs Time for Input Voltage = 5V and D = 74%*



*Figure X. Switch Voltage & Current vs Time for Input Voltage = 5V and D = 74%*



*Figure X. Diode Voltage & Current vs Time for Input Voltage = 5V and D = 74%*



*Figure X. Diode Voltage & Current vs Time for Input Voltage = 5V and D = 74%*

d.

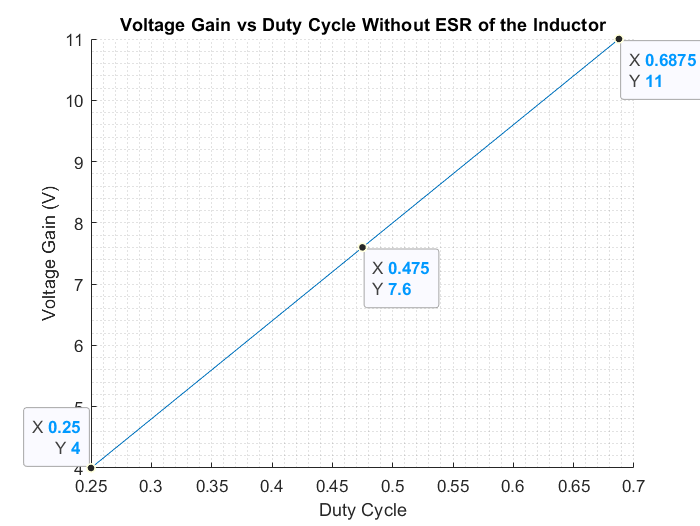
without ESR (at steady state):

(D0)

(D011)

Using D0 in D011:

(D1)

****

*Figure X.* *Voltage Gain vs Duty Cycle Without ESR of the Inductor*

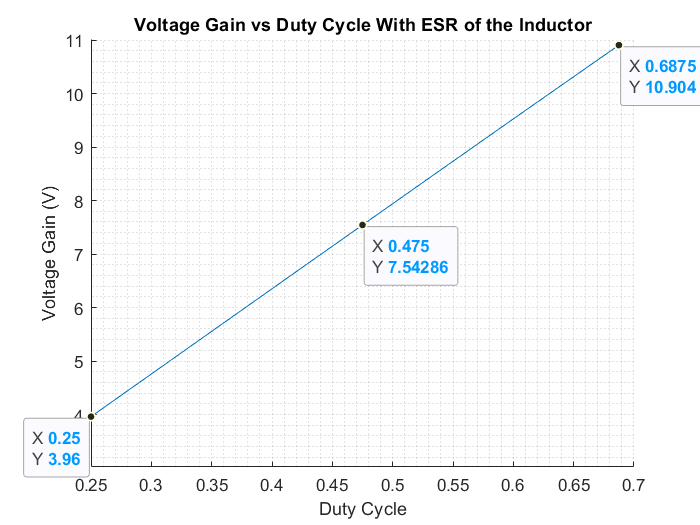
(D2)

With ESR = 0.03Ω;

Using the inductor current found in D2:

(D3)

Then, using equation D3 in D011:



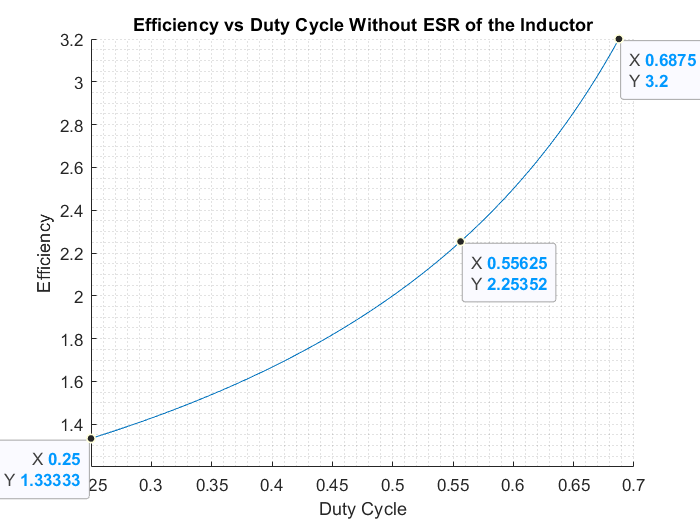
*Figure X.* *Voltage Gain vs Duty Cycle With ESR of the Inductor*

As it can be observed from the plots, there is a slight decrease in voltage gain when the equivalent series resistance of the inductance is also considered. The importance of decrease depends on the ESR: sincec ESR is only 0.04Ω for this question, decrease is not very much.

e.

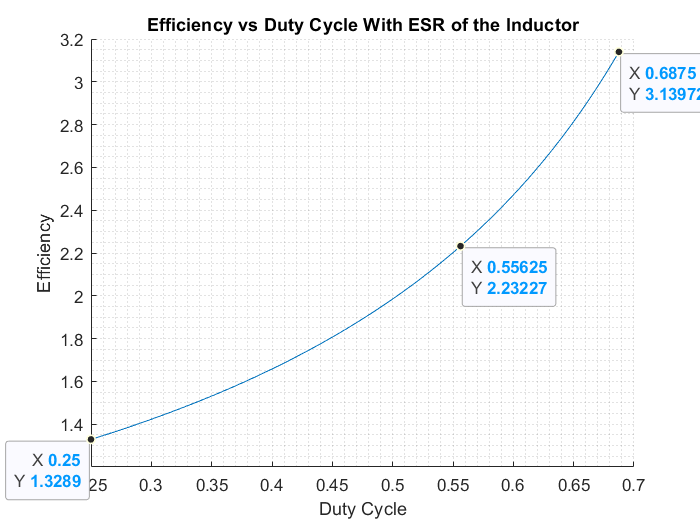
(E0)

Using equation D0 in E1:

****

*Figure X. Efficiency vs Duty Cycle Without ESR of the Inductor*

Using equation D3 in E1:



*Figure X. Efficiency vs Duty Cycle With ESR of the Inductor*

The efficiency of the converter decreased when the ESR is considered. The reasons are same with the change in voltage drop (part 2.d). So efficiency decreases with increasing ESR.