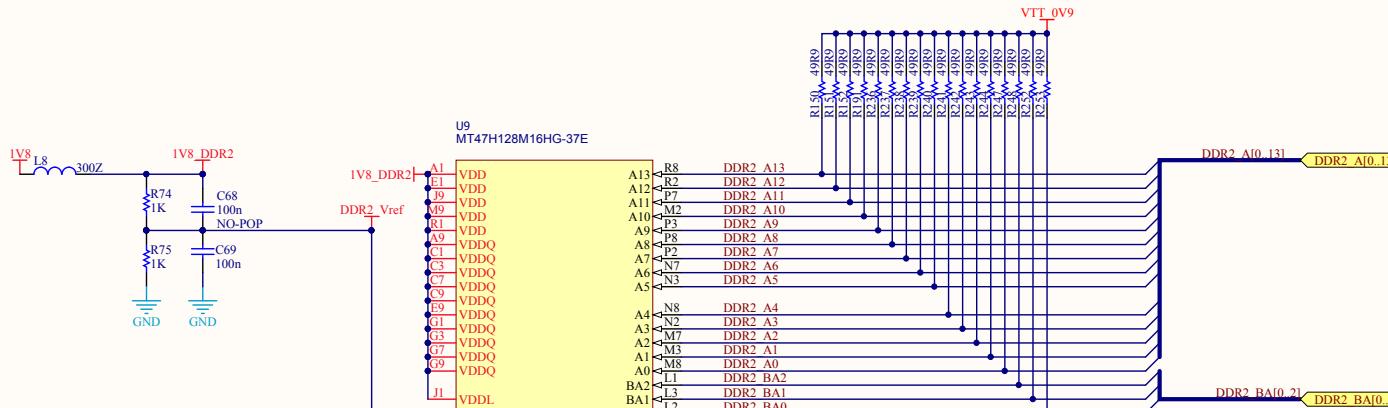
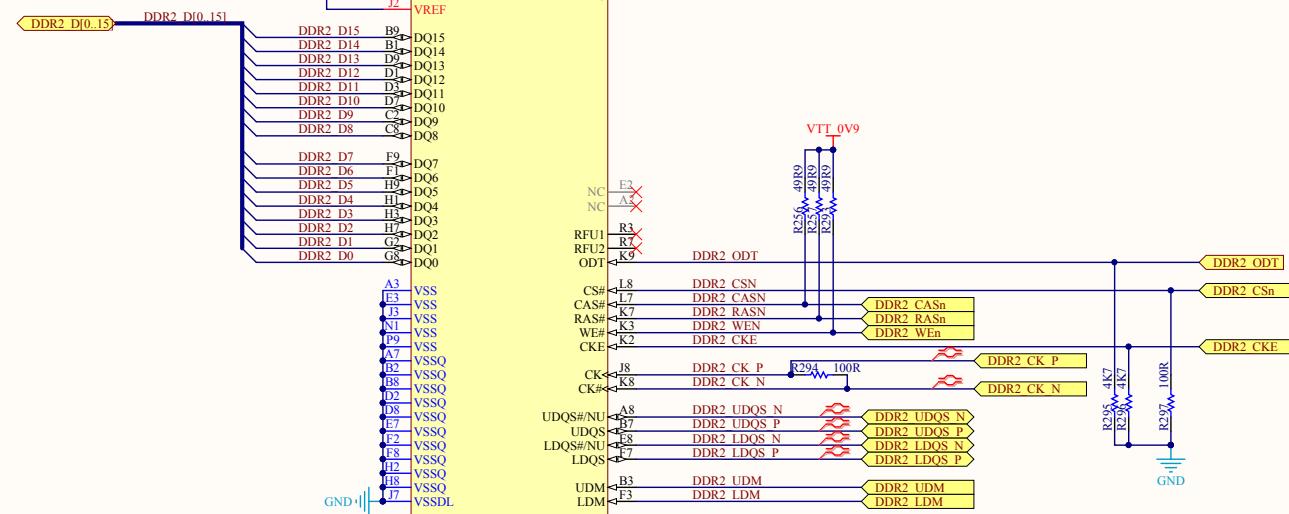


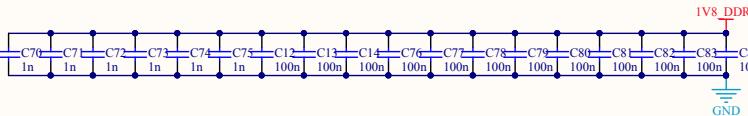
A



B



C



A

A

B

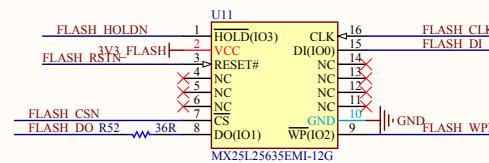
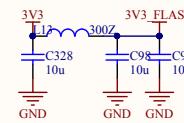
B

C

C

D

D



A

A

B

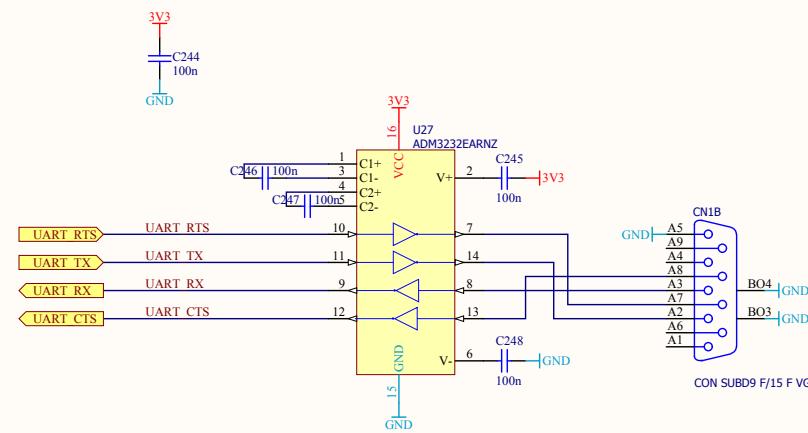
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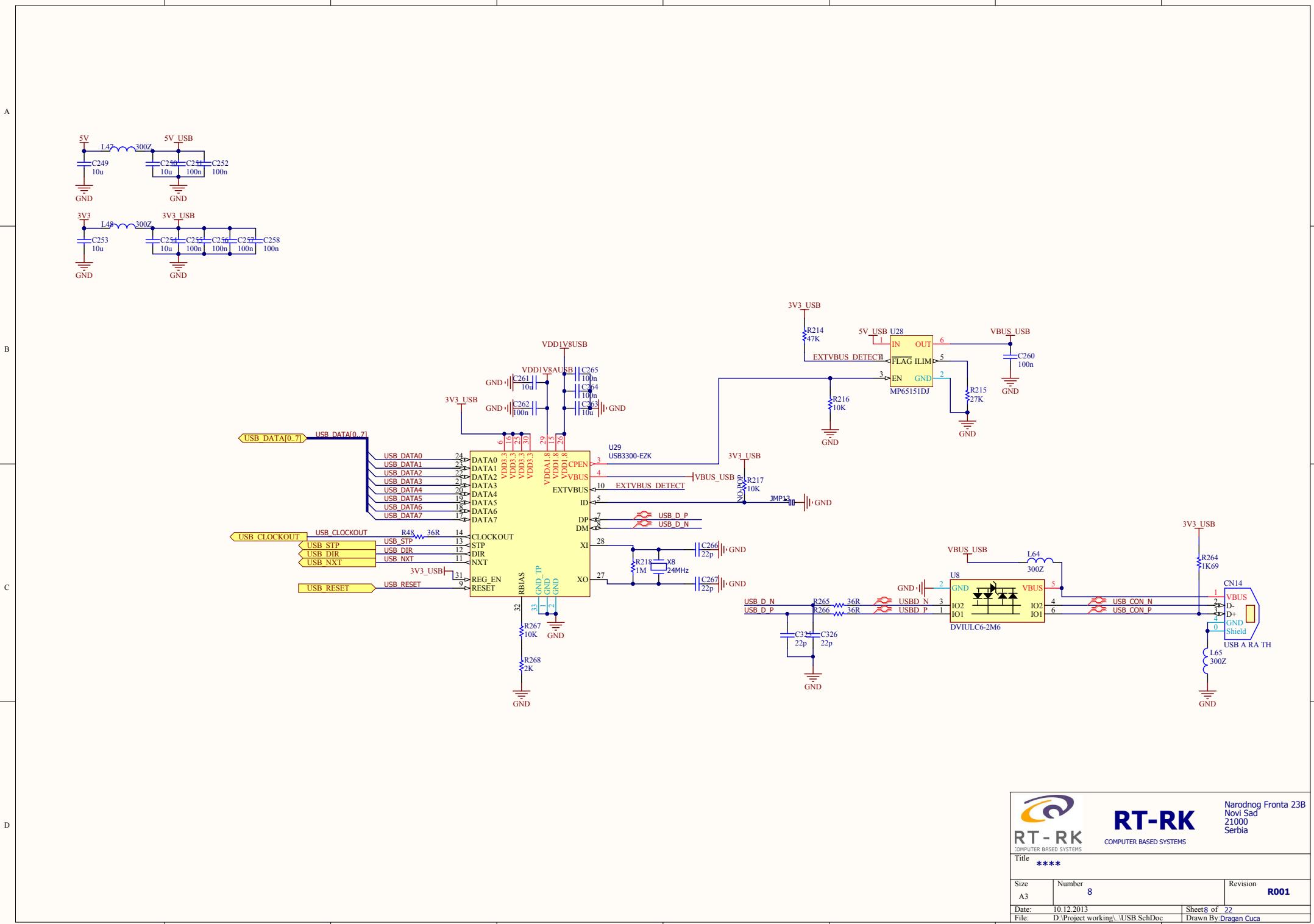
C

C

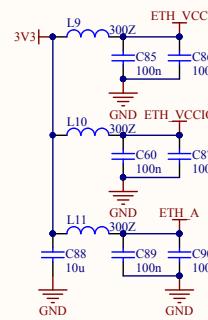
D

D



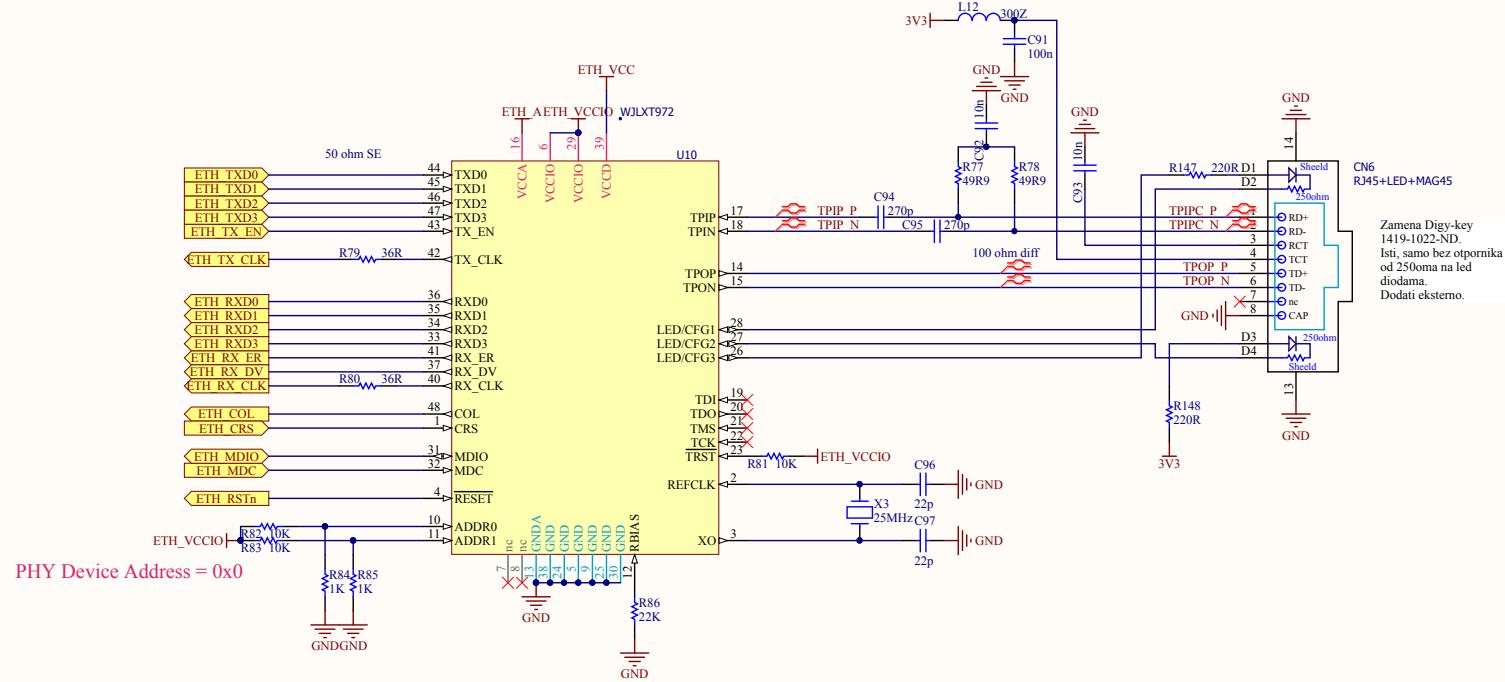


A



A

B



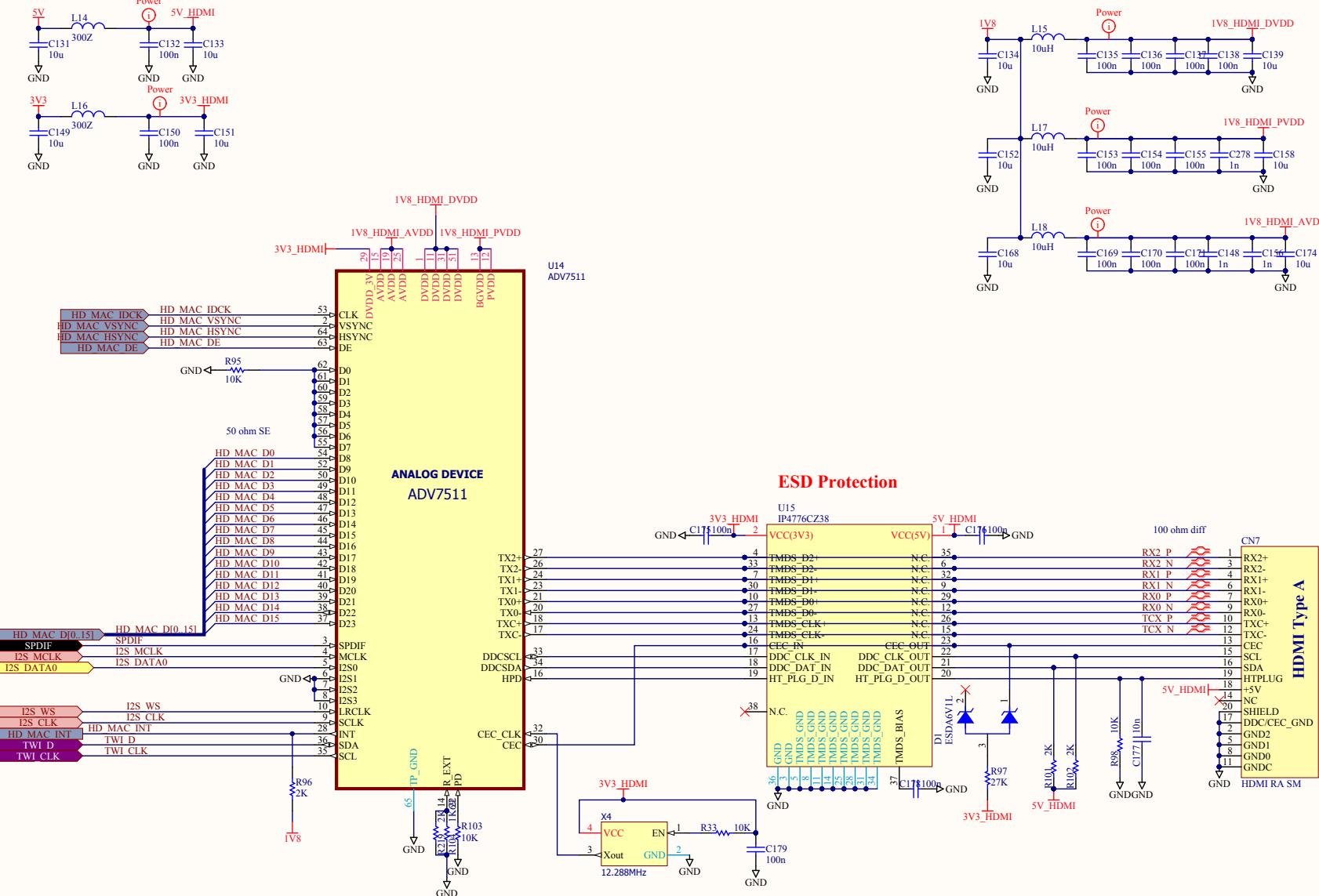
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C

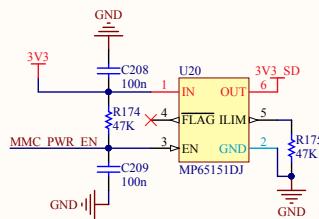
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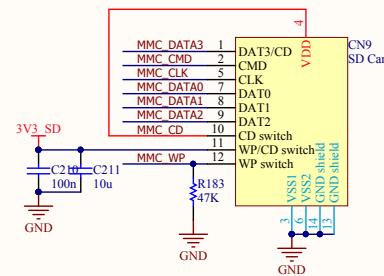
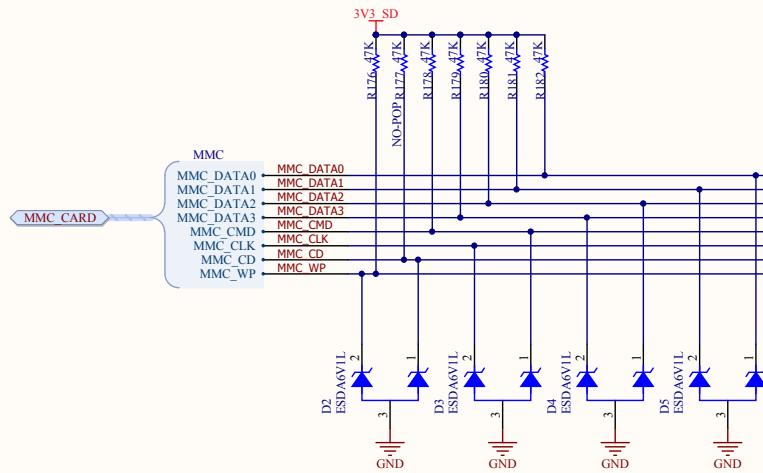
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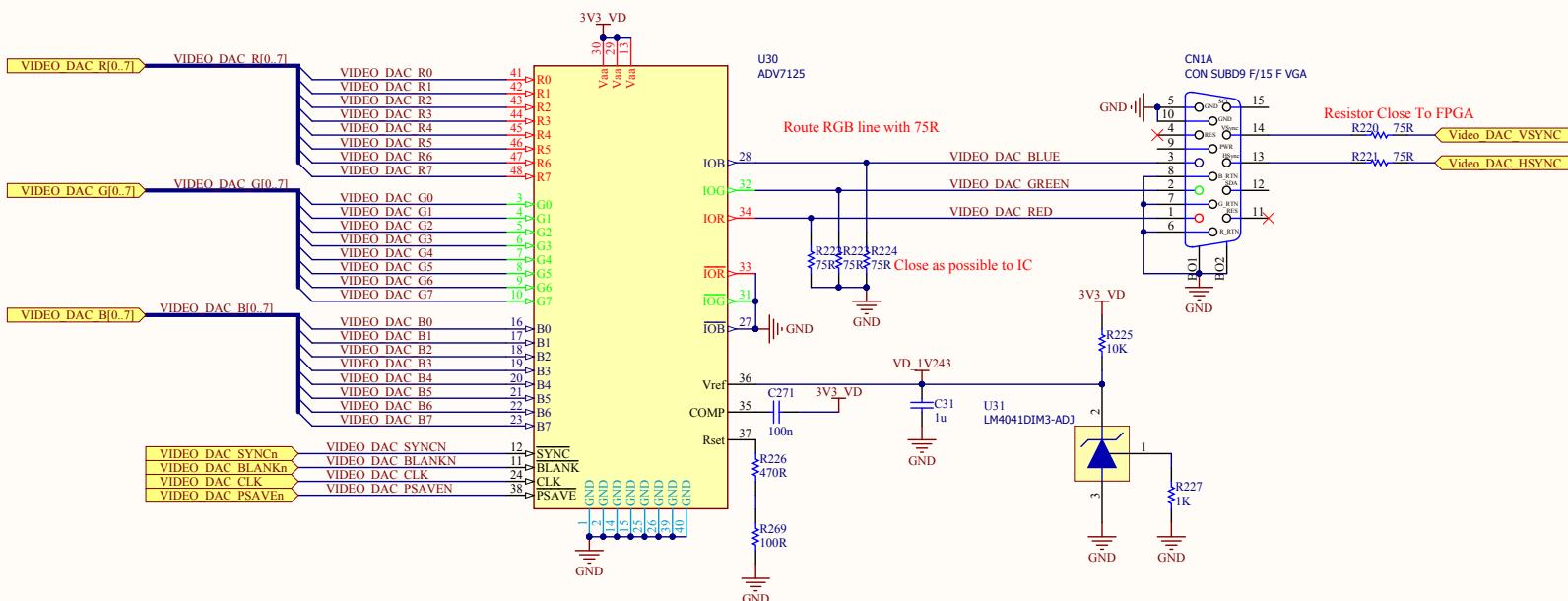
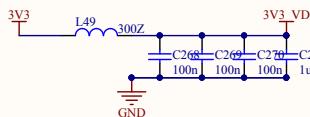
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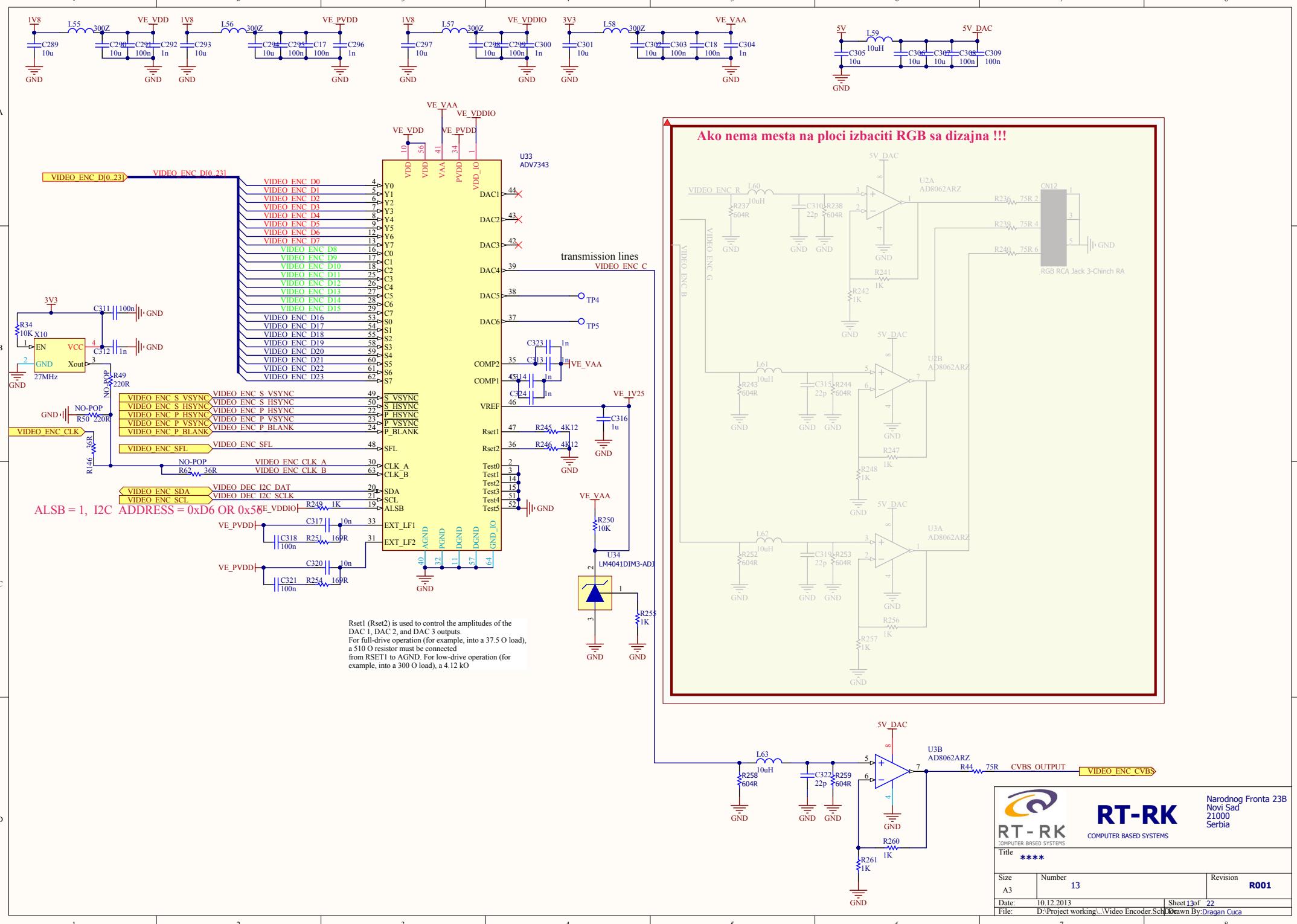


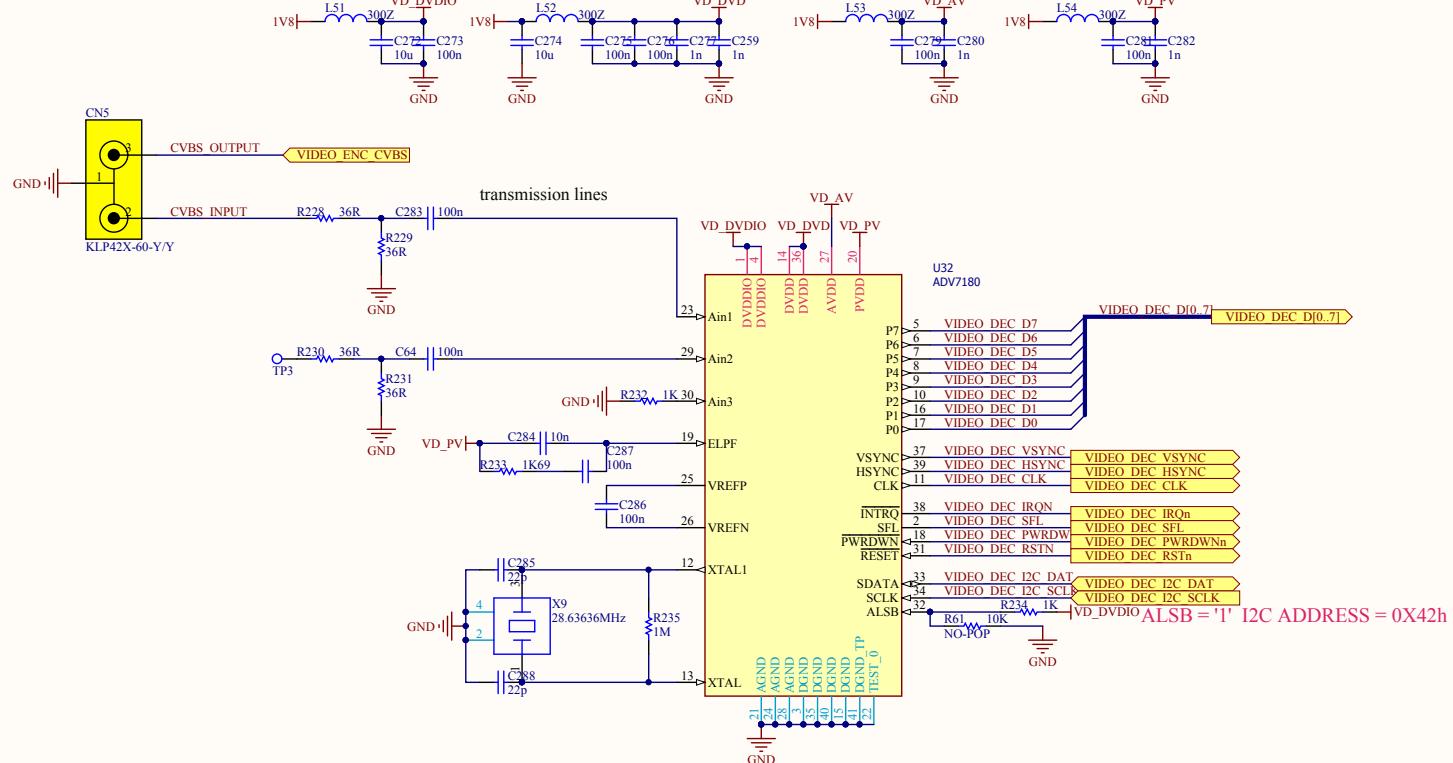
B



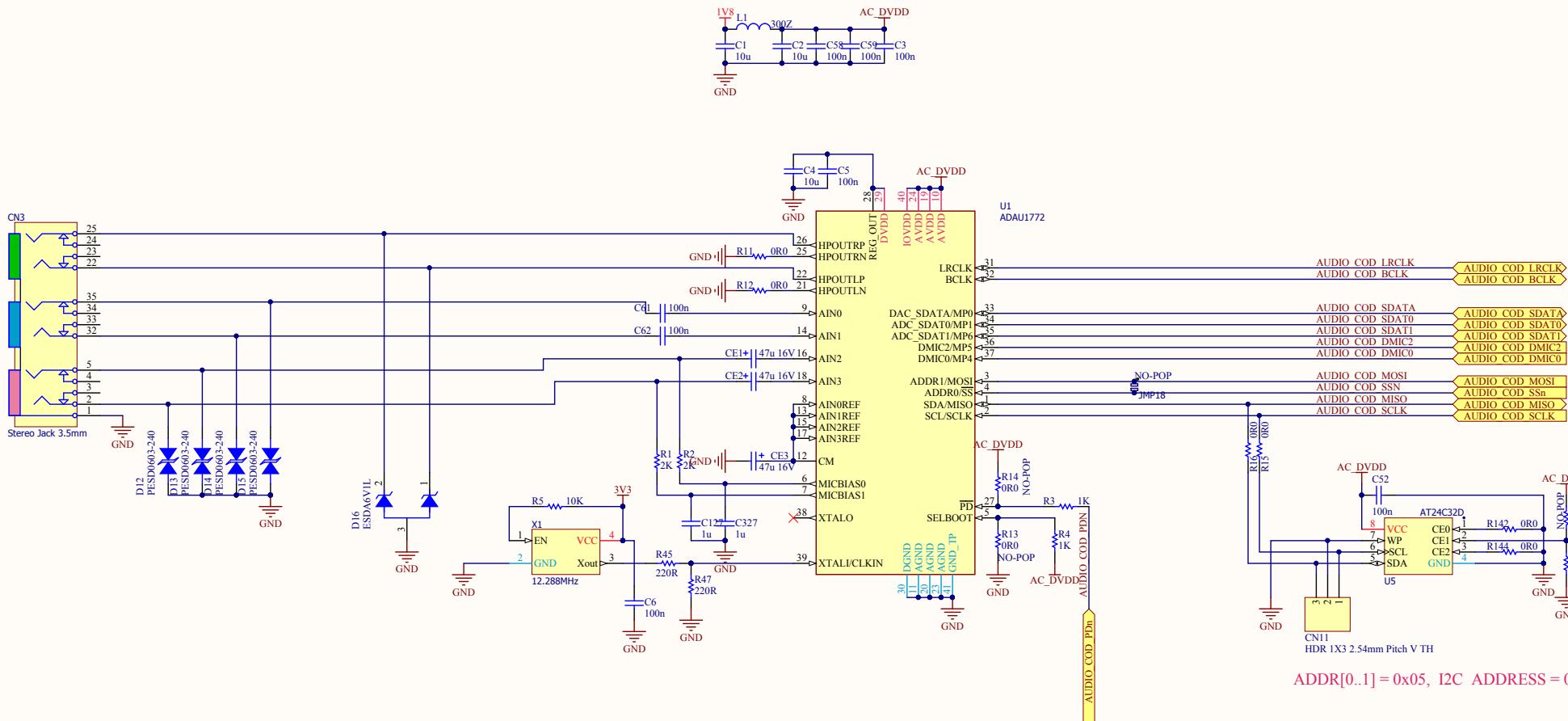
The ADV7125 should be located as close as possible to the output connectors

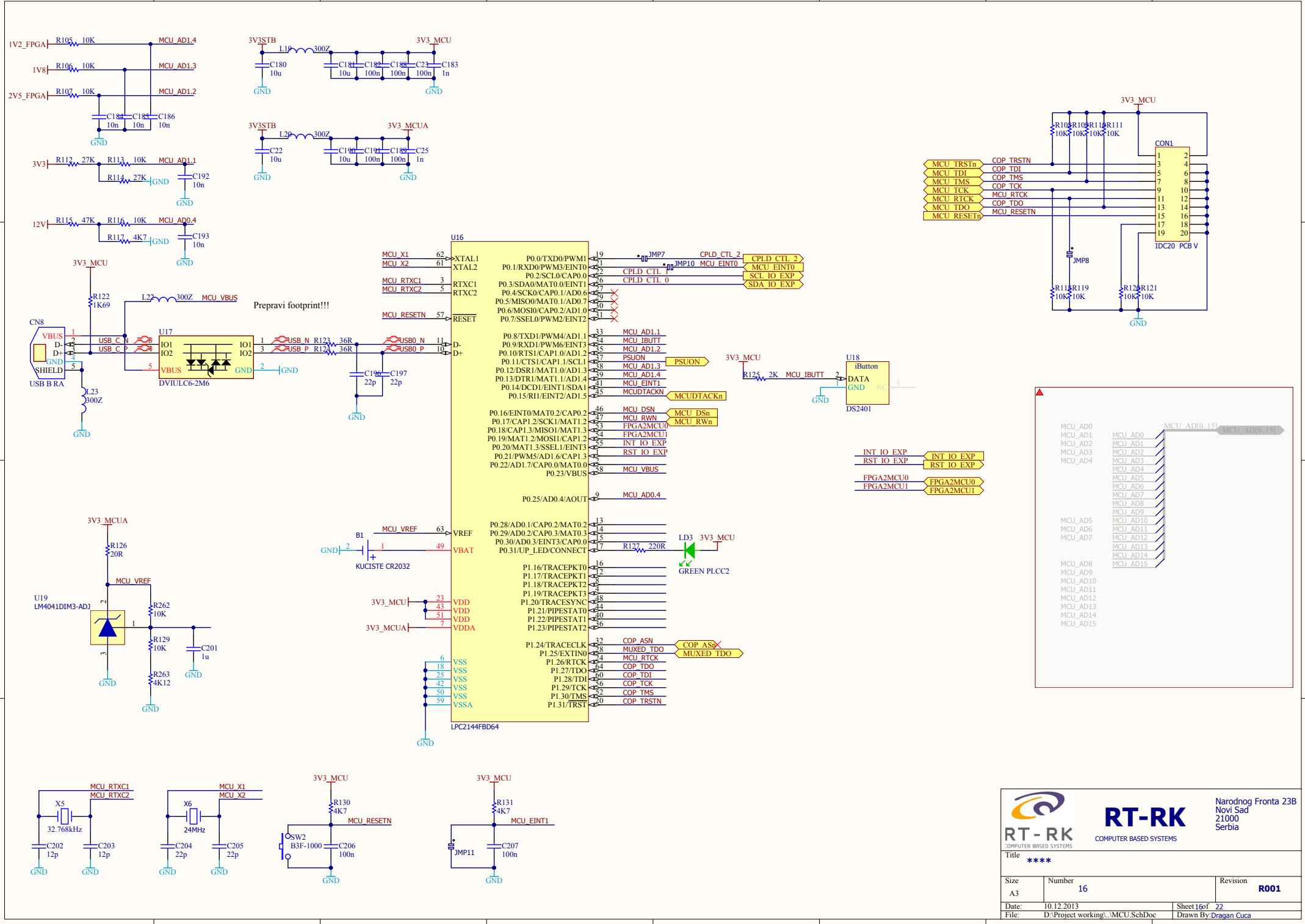




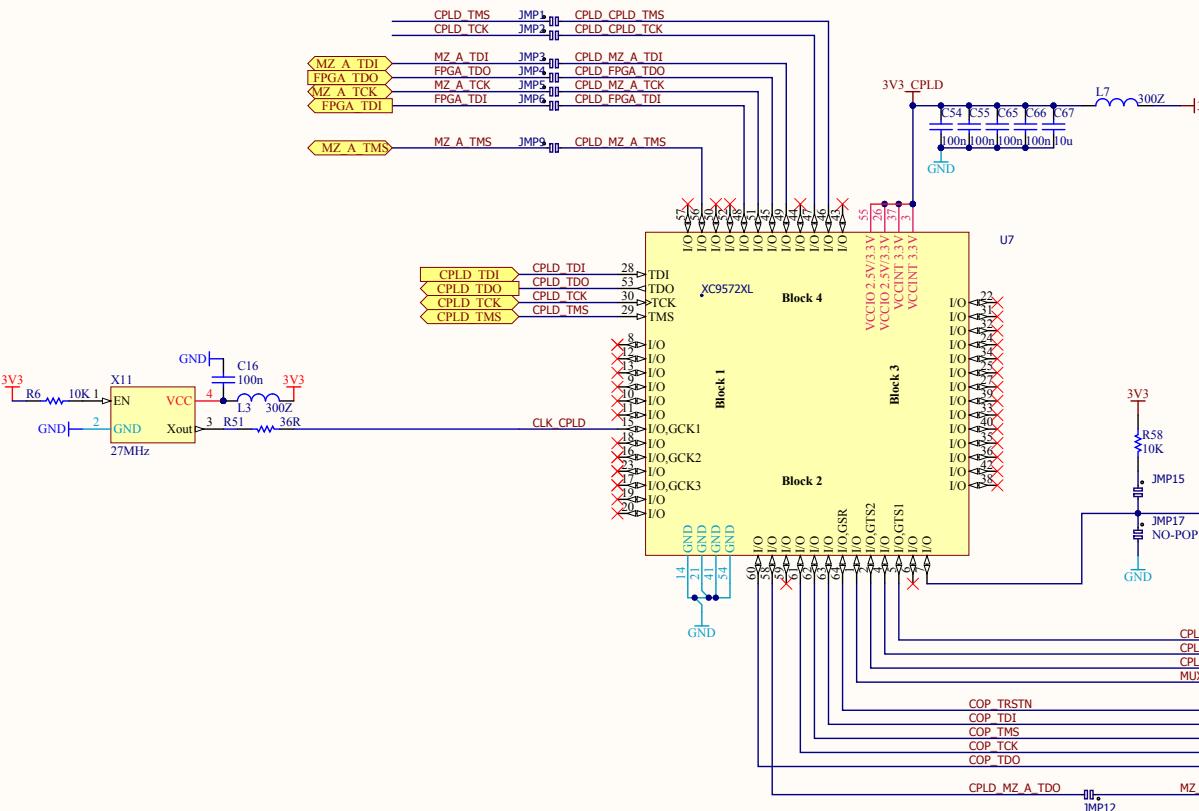


The values stored in the parameter RAM control individual signal processing blocks. The ADAU1772 also has a self-boot function that can be used to load the program and parameter RAM along with the register settings on power-up using an external EEPROM. The SigmaStudio software is used to program and control the core through the control port. Along with designing and tuning a signal flow, the tools can be used to configure all of the ADAU1772 registers.





A



A

B

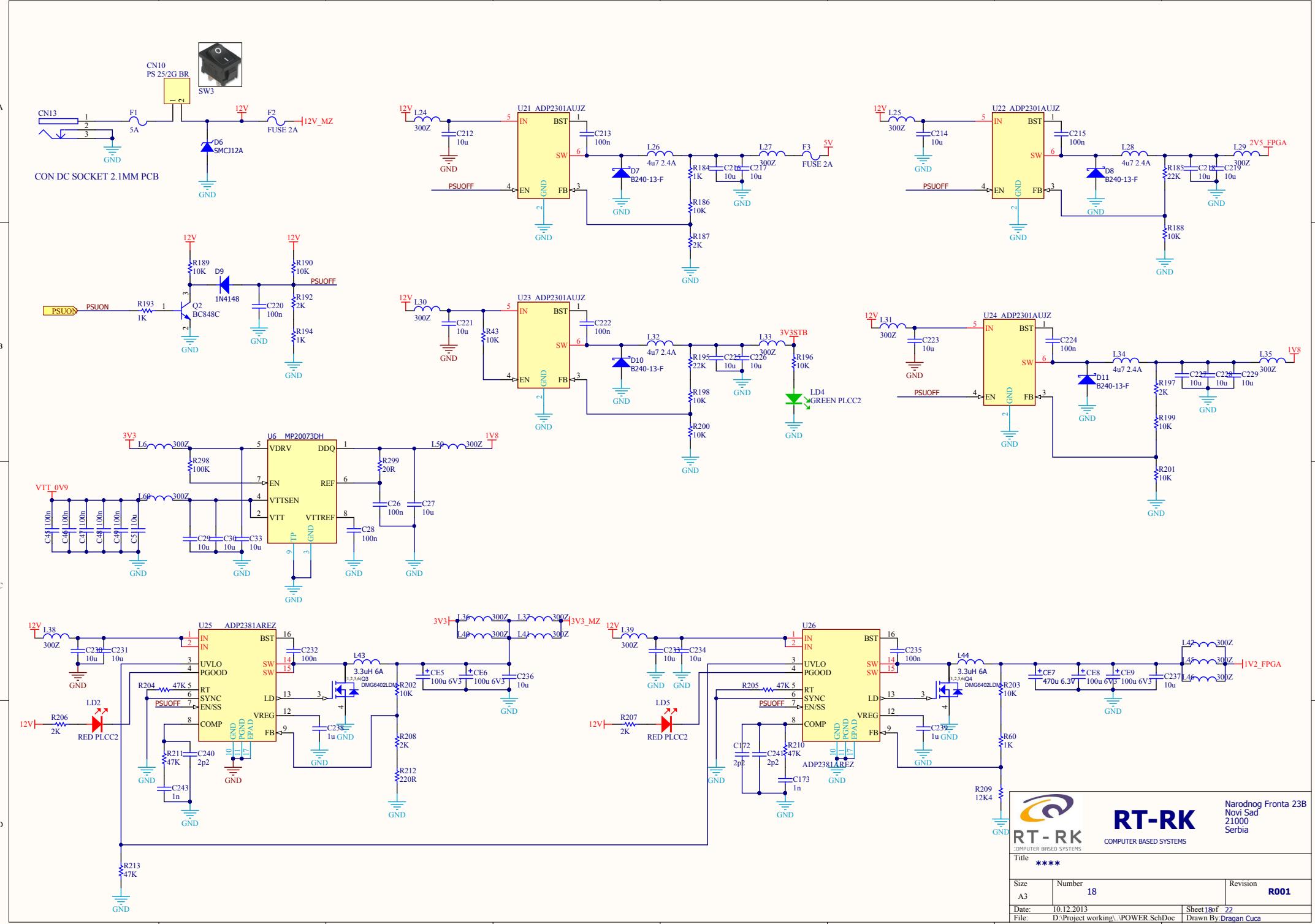
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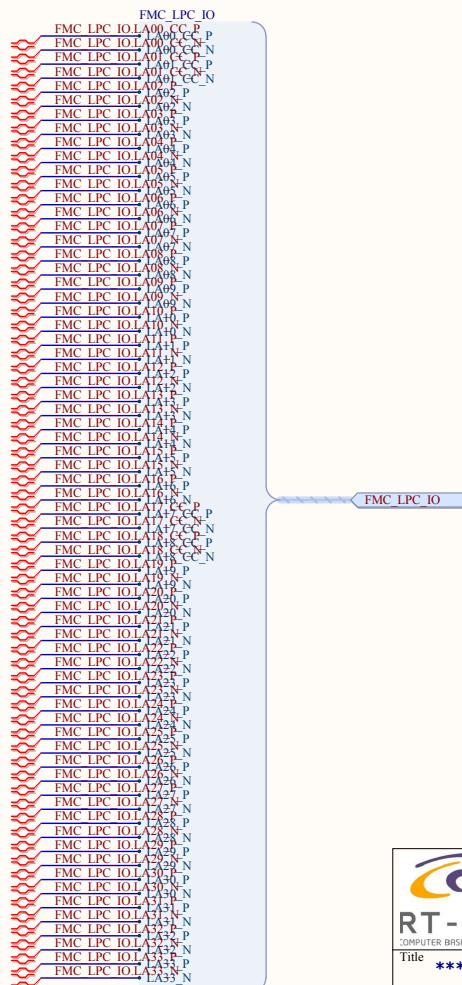
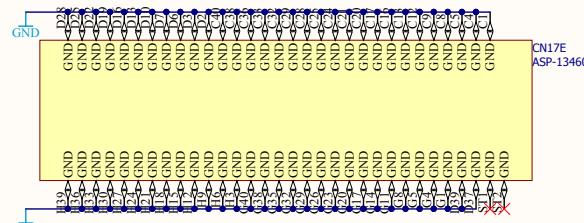
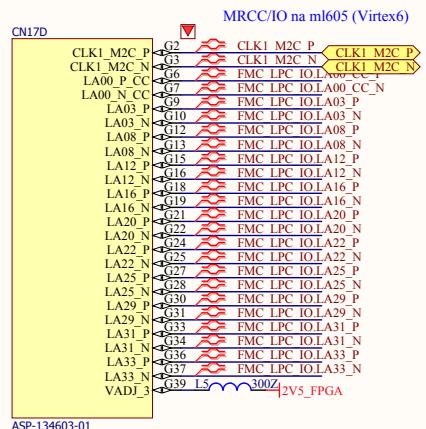
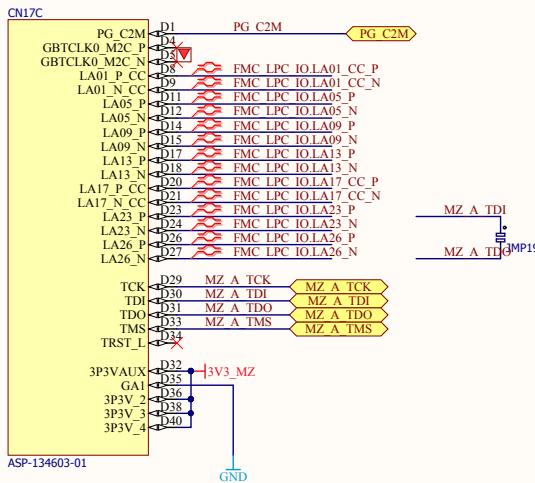
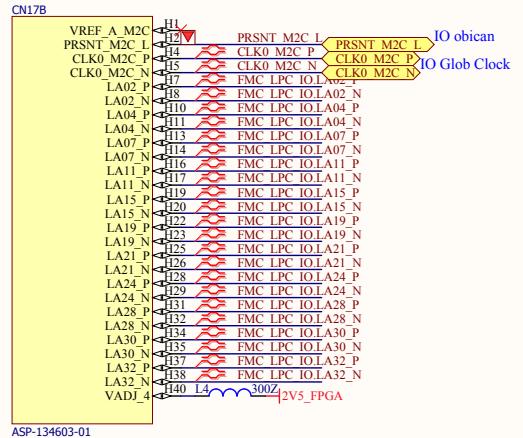
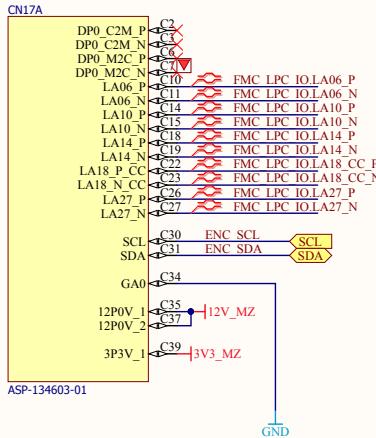
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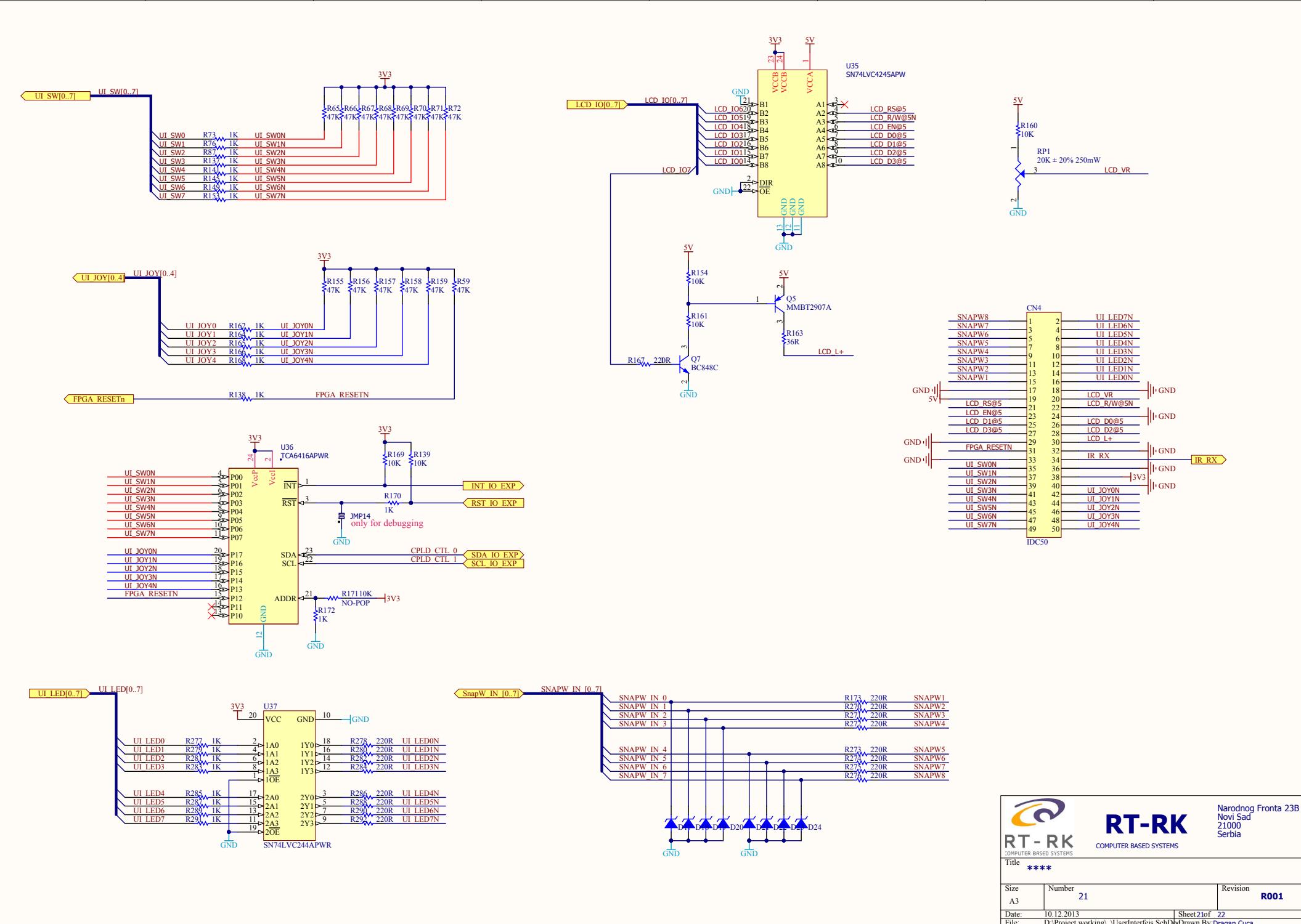
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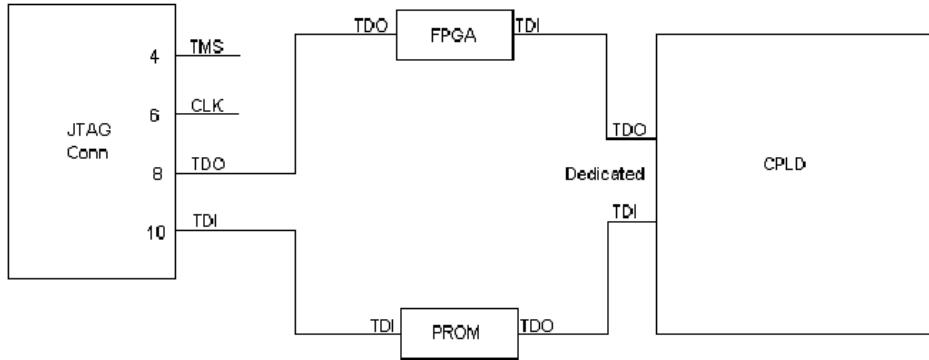
D

D

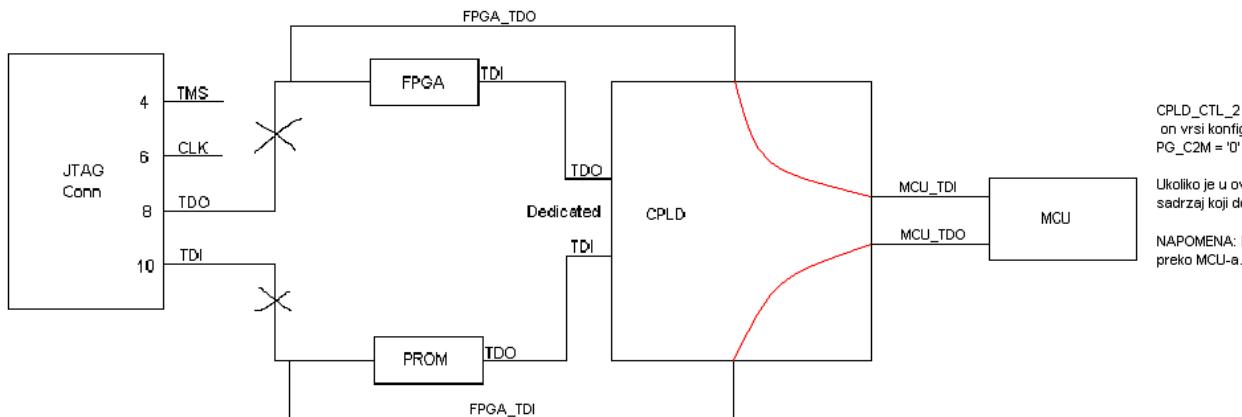








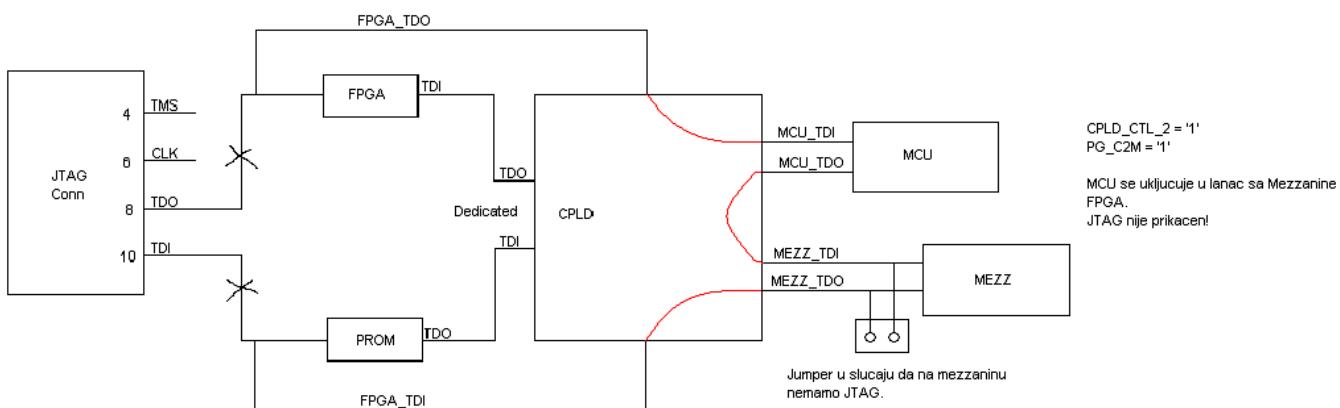
JTAG se koristi za konfiguriranje FPGA.
 $PG_C2M = '0'$
 $CPLD_CTL_2 = '0'$



$CPLD_CTL_2 = '1'$ --> MCU salje '1' CPLD-u kao zahtev da on vrši konfiguriranje.
 $PG_C2M = '0'$ --> Mezzanine nije prisutan.

Ukoliko je u ovoj konfiguraciji JTAG priključen prebriseće sadržaj koji dolazi od strane MCU.

NAPOMENA: Izvaditi JTAG ukoliko se zeli programiranje preko MCU-a.



$CPLD_CTL_2 = '1'$
 $PG_C2M = '1'$

MCU se ulijuje u lanac sa Mezzanine i FPGA.
JTAG nije prikacen!

Jumper u slučaju da na mezzaninu nemamo JTAG.

Title		
Size	Number	Revision
A3		
Date:	10.12.2013	Sheet of
File:	D:\Project working\JTAG Configuration Schematic	8