E2LP
embedded engineering learning platform

D3.2

PRODUCED AND ASSEMBLED E2LP BASE BOARD

CONTENTS

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Abstract: Deliverable "D3.2 - E2LP design specification" reports on results of work defined under the work package "WP3 – Learning Platform Design". The objective of D3.2 is to produce and assemble E2LP base board and perform basic bring-up testing.

The E2LP Consortium consists of:

FTN	Coordinating – Contractor WP1 and WP9 leader	Serbia
RBI	Contractor - WP5 leader	Croatia
IMTEK	Contractor	Germany
CEA	Contractor - WP2 leader	France
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CTIC	Contractor - WP4 leader	Spain
RT-RK	Contractor - WP3 leader	Serbia
FER	Contractor - WP8 leader	Croatia
BGU	Contractor - WP7 leader	Israel

Document Revision History

Date	Issue	Author/Editor/Contributor	Summary of main changes
August 08, 2013	a	Ivan Kastelan	First draft
August 22, 2013	b	Ivan Resetar	Schematics
August 27, 2013	c	Ivan Kastelan	Second draft
August 29, 2013	d	Ivan Kastelan	Final version

1. Introduction

As embedded systems are becoming more complex, the industry requires embedded system engineers to tackle increasingly complex problems and to be able not only to solve basic everyday issues in system design, but also to envision and suggest new solutions and systems in order to achieve a specific task. This increasing complexity in the industry requires a significant change in the education of future embedded system engineers. E2LP project aims to bring that change with its usability in the whole curriculum and with its elimination of the overhead in teaching.

This deliverable, being a part of the work package WP3 “Learning Platform Design” describes the implemented and assembled E2LP Base Board. The implementation was performed by closely following the specification defined in deliverable D3.1 “E2LP Platform Specification” [1] which responded to the students’ and teachers’ requirements summarized in deliverables D2.1 “Partners’ Skills and Current Practices” [2] and D2.2 “E2LP Requirement List" [3].

This document describes the electrical and mechanical design of E2LP Base Board. The document includes schematic files which present the components of the system. Configuration user guide is included at the end of the document. Besides the Base Board, the E2LP platform is composed of a number of Mezzanine extension boards and is intended to provide the unified platform for the complete embedded system engineering curriculum.

2. E2LP Base Board Overview

The E2LP Base Board performs the following functions:

- based on FPGA, provides the central point of the E2LP platform on which all other parts are connected;
- supplies power for the whole E2LP platform;
- controls programming the FPGA and CPUs on extension boards;
- provides a basic user interface;
- provides storage, multimedia and communication interfaces for the platform;
- provides the platform for digital system design;
- provides test points for debugging.

The block diagram (Fig. 1) gives a high level overview of the E2LP Base Board.

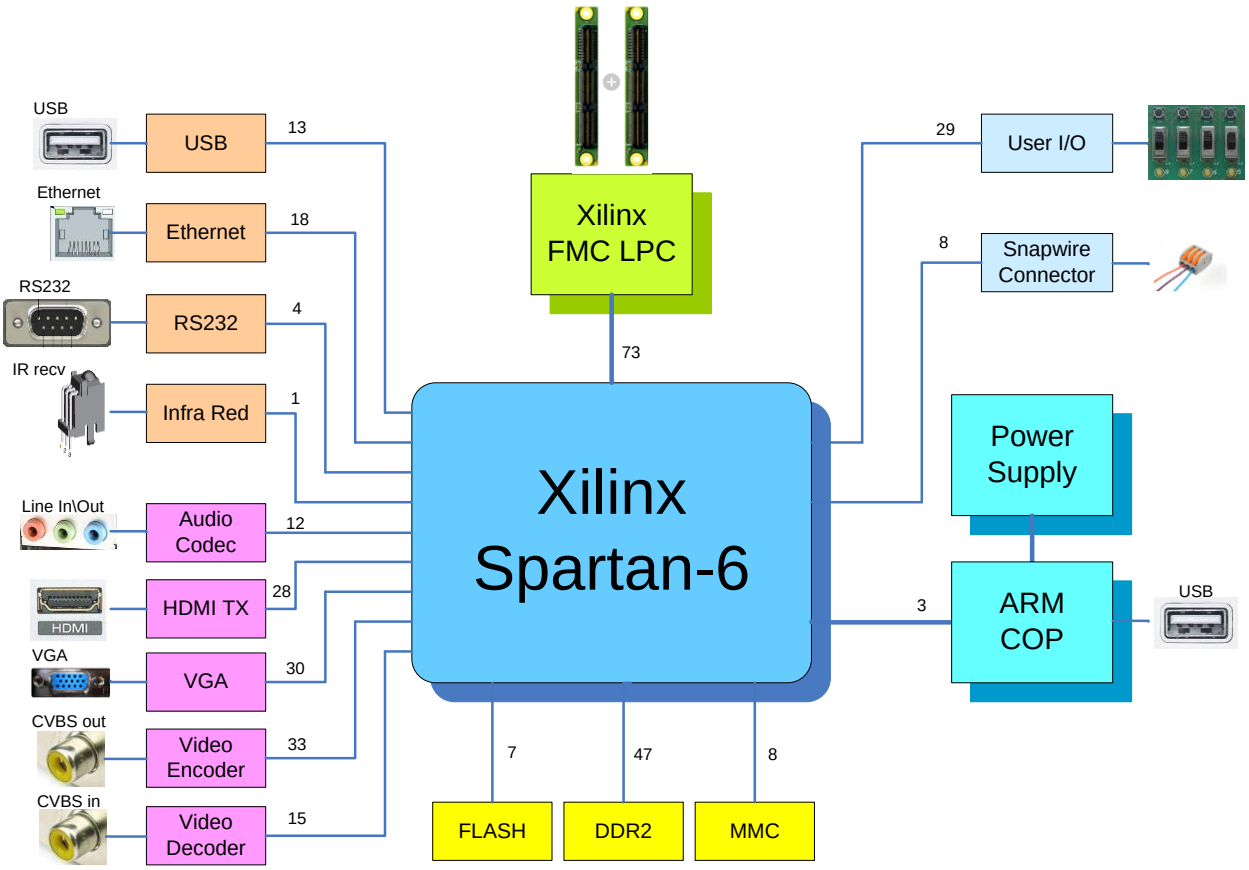


Figure 1. E2LP block diagram

The details of each component are given in [1].

3. Part and Pin-out Summary for FPGA on the E2LP Base Board

I/O Block	Part	Pin Count
Control processor	Philips LPC2144FBD64	3
Mezzanine connector	Xilinx FMC LPC	73
DDR2	Micron MT47H128M16HG-37E	47
FLASH	Macronix MX25L25635E	7
MMC	-	8
IO - LED	-	8
IO – Switches	-	8
IO – Buttons	-	5
LCD alphanumeric	Display Elektronik DEM16216SYH-LY	8
IO – Snapwire	-	8
Video Encoder	Analog Devices ADV7343BSTZ	33
Video Decoder	Analog Devices ADV7180BCPZ	15
Video DAC	Analog Devices ADV7125JST240	30
HDMI TX	Analog Devices ADV7511WBSWZ	28
Audio Codec	Analog Devices ADAU1772	12
RS232	Analog Devices ADM3232E	4
Infra-Red RX	Vishay Semiconductors TSOP34836RF1	1
USB	Microchip Techn. USB3300-EZK	13
Ethernet	Intel WJLXT972MLC.A4	18
FPGA configuration	-	13
Dedicated CLK/RST	-	4
Test points and misc.	-	12
TOTAL		**358**

The previous table summarizes the I/O pin-out from FPGA to the rest of the board. FPGA on the board is Xilinx Spartan-6 XC6SLX45 with FGG676 pin package and speed grade -2.

4. E2LP Base Board Components

This section gives more detail about the design of the components of the E2LP Base Board.

4.1. ARM Control Processor (COP)

The control processor (COP) is implemented using a Philips ARM based controller LPC2144FBD64. The features on the COP are summarized in D3.1 “E2LP Platform Specification” [1] and the control software running on it is described in D3.4 “E2LP Software Implementation” [4].

Schematic design of the control processor section of the E2LP platform is given in Appendix A.

COP is connected to FPGA with 2 general-purpose bits and 1 interrupt bit, table 1.

Table 1. USB connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
Y22	FPGA2MCU0	FPGA2MCU[0]
AA22	FPGA2MCU1	FPGA2MCU[1]
V19	MCU_EINT0	MCU_EINT

4.2. Power Supply

The schematic design of the power supply section is given in Appendix B.

The Box is using a single low voltage input with DC 12 V stabilized. The total input power consumption is approx. 60 W (5A). All internal low voltages are processed on board. The maximum individual consumed currents are: 1.2A on+5V; 6A on +3.3V and +3.3V_MEZ; 1.2A on +3.3Vstb; 1.2A on +2.5V; 1.2A on +1.8V; 6A on +1.2V; 2A on +VTT_0.9V.

Power supply topology is shown in Figure 2.

Each power supply voltage is accomplished from DC/DC step down converter directly from 12V.

Low current power supplies (1.2A) are made with ANALOG DEVICES ADP2301, and major supply for the FPGA and for the board IO stage is made with ANALOG DEVICES ADP2381 DC/DC converter.

The ADP2300/ADP2301 are compact, constant-frequency, current-mode, step-down dc-to-dc regulators with integrated power MOSFET. The ADP2300/ADP2301 devices run from input

voltages of 3.0 V to 20 V, making them suitable for a wide range of applications. A precise, low voltage internal reference makes these devices ideal for generating a regulated output voltage as low as 0.8 V, with ±2% accuracy, for up to 1.2 A load current. There are two frequency options: the ADP2300 runs at 700 kHz, and the ADP2301 runs at 1.4 MHz.

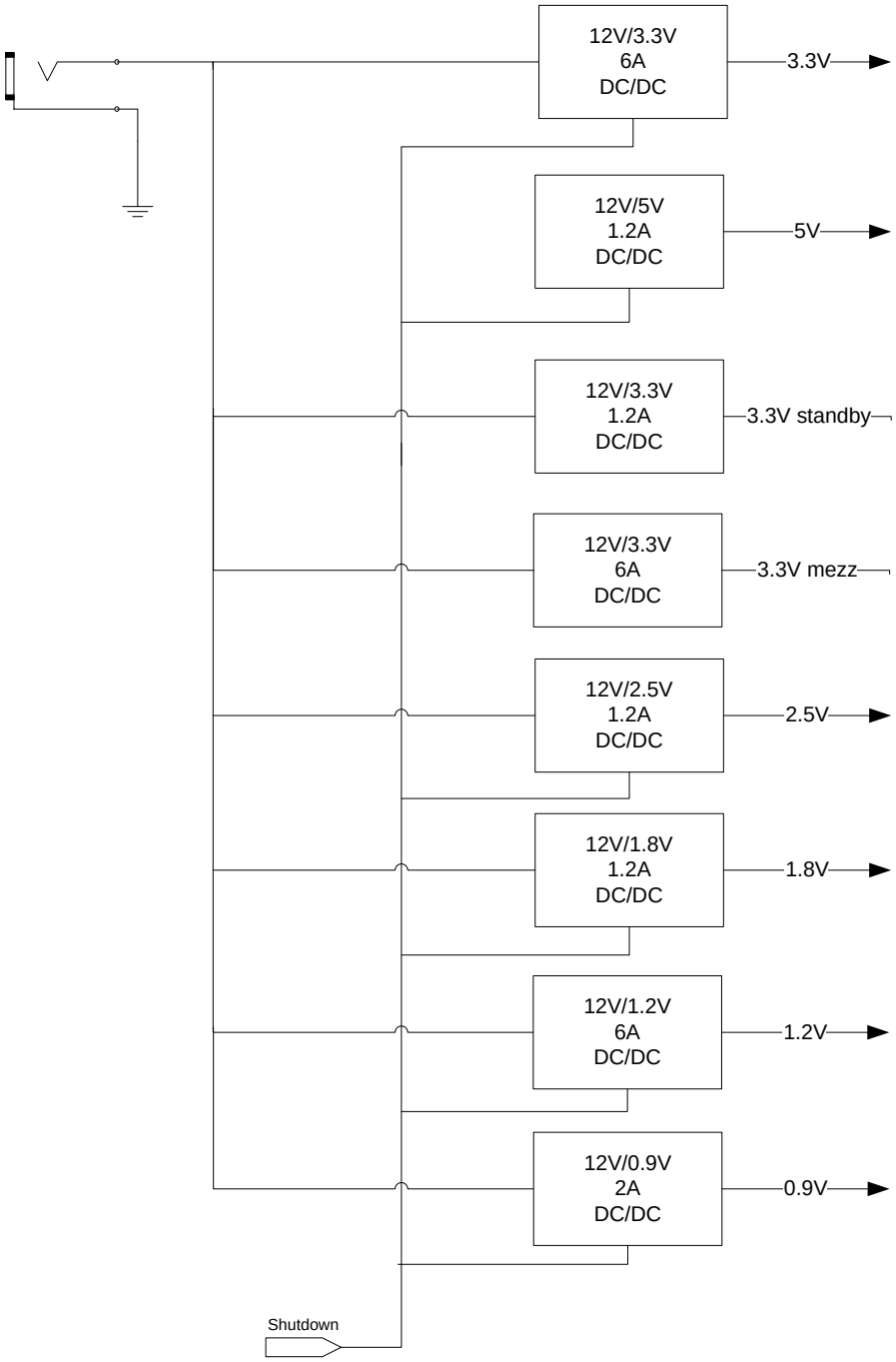


Figure 2. Power supply block diagram

The ADP2381 is a current mode control, synchronous, step-down, dc-to-dc regulator. It integrates a 44 mΩ power MOSFET and a low-side driver to provide a high efficiency solution. The ADP2381 runs from an input voltage of 4.5 V to 20 V and can deliver 6 A of output current. The output voltage can be adjusted to 0.6 V to 90% of the input voltage. The switching frequency of the ADP2381 can be programmed from 250 kHz to 1.4 MHz or fixed at 290 kHz or 550 kHz.

For more precise info on theory of operation and characteristics of used ANALOG DEVICES DC/DC converters please refer to the manufacturer resources (www.analog.com).

There is no specific voltage sequencing requirements (Xilinx DS099 Spartan-3 Complete data sheet, page 51). However, different turn-on sequences eventually required for mezzanine boards can be accomplished by hardware sequencing using passive RC circuits on shutdown input of each DC/DC converter (initially not assembled).

Voltages: +12V, +5V, +3.3V, +2.5V, +1.8V and +1.2V are monitored by control processor.

All DC/DC converters except +3.3V standby voltage can be switched off by ‘housekeeping’ ARM7 controller (shutdown signal, tied to controllers pin 37, P0.11/CTS1/CAP1.1/SCL1).

4.3. USB

The USB interface on the E2LP Base Board consists of a Microchip Technology’s USB3300-EZK integrated circuit which provides a bridge between an ULPI interface connected to FPGA and the 4-pin USB interface on the connector.

Schematic design of the USB section on the E2LP Base Board is given in Appendix C.

USB is connected to Bank 1 of the FPGA. Connection list is shown in Table 2.

Table 2. USB connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
V23	USB_CLOCKOUT	CLOCKOUT
K19	USB_DATA0	DATA[0]
AC25	USB_DATA1	DATA[1]
AC26	USB_DATA2	DATA[2]
AB26	USB_DATA3	DATA[3]
AA25	USB_DATA4	DATA[4]
AA26	USB_DATA5	DATA[5]
Y26	USB_DATA6	DATA[6]
W25	USB_DATA7	DATA[7]
V26	USB_DIR	DIR
U25	USB_NXT	NXT
U26	USB_RESET	RESET
W26	USB_STP	STP

4.4. Ethernet

The Intel® LXT972M Single-Port 10/100 Mbps PHY Transceiver is an IEEE compliant Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). Both full and half-duplex operation at 10 Mbps and 100 Mbps is supported. Operation mode can be set to auto-negotiation, parallel detection, or manual control. The device is powered from a single 3.3V power supply.

Ethernet represents a network of computers connected via twisted pair cable (previously it was a coaxial cable). Point-to-point links are connected together by hubs and/or switches in order to reduce installation costs, increase reliability, and enable point-to-point management and troubleshooting. Although the speed (data rate) of Ethernet changed significantly, from 10MBit/s up to 1GBit/s and more, which was also followed by changes in encoding schemes, the basic frame format remained the same. This makes it easy from the programmer's point of view to interconnect different variants of Ethernet.

100 BASE-TX is the predominant form of Fast Ethernet, providing 100 Mb/s Ethernet. When 100 BASE-TX Ethernet is used to build a LAN, the devices on the network (computers, printers, etc.) are typically connected to a hub or a switch, creating a star network. With all 100 BASE-TX Ethernet, the raw bits of a packet to be transmitted (a series of 0 and 1 bits) are typically

transferred 4 bits at a time clocked at 25 MHz to the Ethernet hardware. It is possible to transfer 4 bits at a time because 100 BASE-TX Ethernet uses 2 twisted pairs for data transfer.

MLT-3 (Multilevel Transmission Encoding – 3 levels) is a line code used by 100 BASE-TX Ethernet, together with 4B5B. A MLT-3 interface emits less electromagnetic interference and requires less bandwidth than most ordinary binary or ternary interfaces that operate at the same data rate, such as Manchester code or Alternate Mark Inversion. MLT-3 cycles through the voltage levels -1, 0, 1 and 0. It moves to the next state to transmit a 1 bit and stays in the same state to transmit a 0 bit (Figure 3).

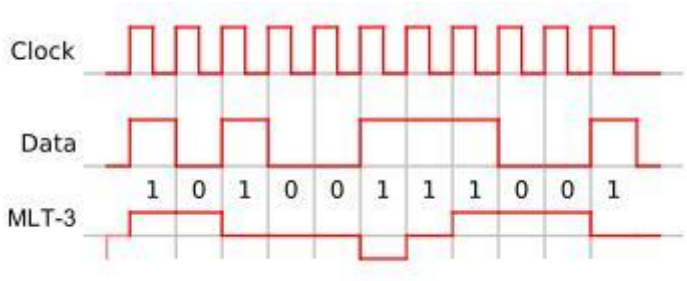


Figure 3. The principle of MLT-3 code

The schematic diagram is given in Appendix D.

Ethernet is connected to Bank 1 of the FPGA. Connection list is shown in Table 3.

Table 3. Ethernet connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
T23	ETH_COL	COL
U22	ETH_CRS	CRS
L19	ETH_MDC	MDC
L18	ETH_MDIO	MDIO
T20	ETH_RSTN	RSTn
C15	ETH_RX_CLK	RX_CLK
M19	ETH_RX_DV	RX_DV
N19	ETH_RX_ER	RX_ER
N22	ETH_RXD0	RXD[0]
N21	ETH_RXD1	RXD[1]
M23	ETH_RXD2	RXD[2]
N20	ETH_RXD3	RXD[3]
A15	ETH_TX_CLK	TX_CLK
P20	ETH_TX_EN	TX_EN
P21	ETH_TXD0	TXD[0]
P22	ETH_TXD1	TXD[1]
R20	ETH_TXD2	TXD[2]
T22	ETH_TXD3	TXD[3]

4.5. RS-232

The E2LP Base Board has a single RS-232 port. The RS-232 port is configured as a Data Communication Equipment with hardware handshake using a standard DB-9 serial connector. Considering +/-12V logic levels on RS232 connectors, ADM3232 high speed rs232/v.28 interface from Analog Devices is used for coupling.

A voltage level-shifter circuitry is needed to connect the FPGA to a PC using RS232. The selected IC is Analog Devices ADM3232. The surrounding capacitors are needed for voltage-pump inside ADM3232 and to filter the supply voltages. The circuit is connected for a hardware flow control possibility (RTS, CTS) if it is supported by the IP in the FPGA.

Schematic design of the RS-232 section of the E2LP Base Board is given in Appendix E.

RS-232 is connected to Bank 0 of the FPGA. Connection list is shown in Table 4.

Table 4. RS-232 connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
A19	UART_CTS	CTS
B20	UART_RTS	RTS
A21	UART_RX	RX
A20	UART_TX	TX

4.6. Infra-Red

The Infra-red receiver on the E2LP Base Board is a Vishay Semiconductors TSOP34836RF1.

Schematic design of the Infra-Red section on the E2LP Base Board is given in Appendix O together with the user interface.

Infra-Red is connected to Bank 0 of the FPGA. Connection list is shown in Table 5.

Table 5. Infra-red connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
AE23	IR_RX	RX

4.7. Audio Codec

The audio system on the E2LP Base Board consists of an Analog Devices ADAU1772. Audio block feeds codec chip with output serial data stream, frame synchronization and reset signal; receives from it bit clock and serial data stream.

Audio codec is connected to Bank 3 of the FPGA. Connection list is shown in Table 6.

Table 6. Audio codec connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
AB5	AUDIO_COD_BCLK	BCLK
W7	AUDIO_COD_DMIC0	DMIC0
Y5	AUDIO_COD_DMIC2	DMIC2
AB7	AUDIO_COD_LRCLK	LRCLK
W8	AUDIO_COD_MISO	MISO
AD5	AUDIO_COD_MOSI	MOSI
AF2	AUDIO_COD_PDN	PDN
U8	AUDIO_COD_SCLK	SCLK
AA5	AUDIO_COD_SDAT0	SDAT0
Y6	AUDIO_COD_SDAT1	SDAT1
AA7	AUDIO_COD_SDATA	SDATA
AC5	AUDIO_COD_SSN	SSN

Schematic diagram for the Audio codec is shown in Appendix G.

Audio codec is connected to triple stacked 3.5mm stereo connector with line-in, microphone in and line out signals.

4.8. HDMI Transmitter

The HDMI transmit interface on the E2LP Base Board consists of an Analog Devices ADV7511WBSWZ integrated circuit which provides a transmit function via HDMI interface.

Schematic design of the HDMI section on the E2LP Base Board is given in Appendix H.

HDMI is connected to Bank 1 of the FPGA. Connection list is shown in Table 7.

Table 7. HDMI connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
K26	HD_MAC_D0	DATA[0]
J26	HD_MAC_D1	DATA[1]
J25	HD_MAC_D2	DATA[2]
H26	HD_MAC_D3	DATA[3]
G26	HD_MAC_D4	DATA[4]
G25	HD_MAC_D5	DATA[5]
F26	HD_MAC_D6	DATA[6]
E26	HD_MAC_D7	DATA[7]
E25	HD_MAC_D8	DATA[8]
D26	HD_MAC_D9	DATA[9]
C26	HD_MAC_D10	DATA[10]
C25	HD_MAC_D11	DATA[11]
B26	HD_MAC_D12	DATA[12]
B25	HD_MAC_D13	DATA[13]
A25	HD_MAC_D14	DATA[14]
B24	HD_MAC_D15	DATA[15]
L25	HD_MAC_DE	DE
L26	HD_MAC_HSYNC	HSYNC
A14	HD_MAC_IDCK	IDCK
M26	HD_MAC_INT	INT
N25	HD_MAC_VSYNC	VSYNC
R25	I2S_CLK	SCLK
R26	I2S_DATA0	I2S0
P26	I2S_MCLK	MCLK
T26	I2S_WS	LRCLK
A23	TWI_CLK	SCL
B23	TWI_D	SDA
N26	SPDIF	SPDIF

4.9. VGA DAC

The VGA Digital-to-Analog converter (DAC) on the E2LP Base Board is Analog Devices ADV7125JST240. It provides VGA output.

Schematic design of the VGA DAC section on the E2LP Base Board is given in Appendix I.

VGA DAC is connected to Bank 0 of the FPGA. Connection list is shown in Table 8.

Table 8. VGA DAC connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
A18	VIDEO_DAC_B0	B[0]
B18	VIDEO_DAC_B1	B[1]
L17	VIDEO_DAC_B2	B[2]
M18	VIDEO_DAC_B3	B[3]
C18	VIDEO_DAC_B4	B[4]
K18	VIDEO_DAC_B5	B[5]
C19	VIDEO_DAC_B6	B[6]
C20	VIDEO_DAC_B7	B[7]
B16	VIDEO_DAC_BLANKN	BLANKn
C14	VIDEO_DAC_CLK	CLK
A9	VIDEO_DAC_G0	G[0]
A11	VIDEO_DAC_G1	G[1]
B12	VIDEO_DAC_G2	G[2]
A12	VIDEO_DAC_G3	G[3]
N17	VIDEO_DAC_G4	G[4]
A13	VIDEO_DAC_G5	G[5]
N18	VIDEO_DAC_G6	G[6]
A16	VIDEO_DAC_G7	G[7]
B22	VIDEO_DAC_HSYNC	HSYNC
A2	VIDEO_DAC_PSAVEN	PSAVEn
B4	VIDEO_DAC_R0	R[0]
A4	VIDEO_DAC_R1	R[1]
A5	VIDEO_DAC_R2	R[2]
B6	VIDEO_DAC_R3	R[3]
A6	VIDEO_DAC_R4	R[4]
A7	VIDEO_DAC_R5	R[5]
B8	VIDEO_DAC_R6	R[6]
A8	VIDEO_DAC_R7	R[7]
A17	VIDEO_DAC_SYNCN	SYNCn
A22	VIDEO_DAC_VSYNC	VSYNC

4.10. Video Encoder

The video encoder on the E2LP Base Board is Analog Devices ADV7343BSTZ. It accepts digital video (from FPGA) and provides analog CVBS video output.

Schematic design of the video encoder section on the E2LP Base Board is given in Appendix J.

Video encoder is connected to Banks 0, 1 and 3 of the FPGA. Connection list is shown in Table 9.

Table 9. Video encoder connection to FPGA

FPGA BALL	SCH Net Name	Interface Signal Name
B14	ENC_CLK	CLK
V17	ENC_SCL	SCL
U17	ENC_SDA	SDA
T6	VIDEO_ENC_D0	DATA[0]
T8	VIDEO_ENC_D1	DATA[1]
N1	VIDEO_ENC_D2	DATA[2]
N2	VIDEO_ENC_D3	DATA[3]
M1	VIDEO_ENC_D4	DATA[4]
L1	VIDEO_ENC_D5	DATA[5]
L2	VIDEO_ENC_D6	DATA[6]
K1	VIDEO_ENC_D7	DATA[7]
J1	VIDEO_ENC_D8	DATA[8]
J2	VIDEO_ENC_D9	DATA[9]
H1	VIDEO_ENC_D10	DATA[10]
E1	VIDEO_ENC_D11	DATA[11]
E2	VIDEO_ENC_D12	DATA[12]
D1	VIDEO_ENC_D13	DATA[13]
C1	VIDEO_ENC_D14	DATA[14]
C2	VIDEO_ENC_D15	DATA[15]
AB4	VIDEO_ENC_D16	DATA[16]
AA4	VIDEO_ENC_D17	DATA[17]
AA3	VIDEO_ENC_D18	DATA[18]
W5	VIDEO_ENC_D19	DATA[19]
V5	VIDEO_ENC_D20	DATA[20]
U5	VIDEO_ENC_D21	DATA[21]
U4	VIDEO_ENC_D22	DATA[22]
U3	VIDEO_ENC_D23	DATA[23]
F1	VIDEO_ENC_P_BLANK	P_BLANK
G1	VIDEO_ENC_P_HSYNC	P_HSYNC
G2	VIDEO_ENC_P_VSYNC	P_VSYNC
AC3	VIDEO_ENC_S_HSYNC	S_HSYNC
AC4	VIDEO_ENC_S_VSYNC	S_VSYNC
AD4	VIDEO_ENC_SFL	SFL

4.11. Video Decoder

The video decoder on the E2LP Base Board is Analog Devices ADV7180BCPZ. It accepts analog CVBS video input and provides digital output to FPGA.

Schematic design of the video decoder section on the E2LP Base Board is given in Appendix K.

Video decoder is connected to Banks 0 and 3 of the FPGA. Connection list is shown in Table 10.

Table 10. Video decoder connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
D14	DEC_CLK	CLK
E4	VIDEO_DEC_D0	DATA[0]
B2	VIDEO_DEC_D1	DATA[1]
D3	VIDEO_DEC_D2	DATA[2]
E3	VIDEO_DEC_D3	DATA[3]
F3	VIDEO_DEC_D4	DATA[4]
H3	VIDEO_DEC_D5	DATA[5]
U7	VIDEO_DEC_D6	DATA[6]
L7	VIDEO_DEC_D7	DATA[7]
K3	VIDEO_DEC_HSYNC	HSYNC
M4	VIDEO_DEC_IRQN	IRQn
C4	VIDEO_DEC_PWRDWNN	PWRDWNn
B1	VIDEO_DEC_RSTN	RSTn
L6	VIDEO_DEC_SFL	SFL
M3	VIDEO_DEC_VSYNC	VSYNC

4.12. Flash Memory

On board flash memory is Macronix MX25L25635E connected directly to Bank 1 of the FPGA.
Schematic design is given in Appendix L.
FPGA to flash connection list is shown in Table 11.

Table 11. Flash connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
AF25	FLASH_CLK	CLK
V22	FLASH_CSN	CSn
AE25	FLASH_DI	DI
AD26	FLASH_DO	DO
W22	FLASH_HOLDN	HOLDn
V20	FLASH_RSTN	RSTn
AE26	FLASH_WPN	WPn

4.13. DDR2

Double Data Rate Synchronous Dynamic Random Access Memory system on the E2LP Base Board consists of a Micron MT47H128M16HG-37E DDR2 integrated circuit.

Schematic design of the DDR2 section on the E2LP Base Board is given in Appendix M.

On board DDR2 is connected directly to Bank 3 of the FPGA. FPGA to DDR2 connection list is shown in the Table 12.

Table 12. DDR2 connection to FPGA

FPGA BALL	SCH Net Name	Interface Signal Name
N7	DDR2_A0	ADDR[0]
N6	DDR2_A1	ADDR[1]
R9	DDR2_A2	ADDR[2]
P7	DDR2_A3	ADDR[3]
N9	DDR2_A4	ADDR [4]
R2	DDR2_A5	ADDR [5]
R1	DDR2_A6	ADDR [6]
P10	DDR2_A7	ADDR [7]
N4	DDR2_A8	ADDR [8]
N3	DDR2_A9	ADDR [9]
M10	DDR2_A10	ADDR [10]
L3	DDR2_A11	ADDR [11]
M8	DDR2_A12	ADDR [12]
M6	DDR2_A13	ADDR [13]
P3	DDR2_BA0	BA[0]
P1	DDR2_BA1	BA[1]
N5	DDR2_BA2	BA[2]
P8	DDR2_CASN	CASn
R4	DDR2_CK_P	CK_P
R3	DDR2_CK_N	CK_N
M9	DDR2_CKE	CKE
L4	DDR2_CSN	CSn
Y3	DDR2_D0	DATA[0]
Y1	DDR2_D1	DATA[1]

FPGA BALL	SCH Net Name	Interface Signal Name
W2	DDR2_D2	DATA[2]
W1	DDR2_D3	DATA[3]
T3	DDR2_D4	DATA[4]
T1	DDR2_D5	DATA[5]
U2	DDR2_D6	DATA[6]
U1	DDR2_D7	DATA[7]
AA2	DDR2_D8	DATA[8]
AA1	DDR2_D9	DATA[9]
AE2	DDR2_D10	DATA[10]
AE1	DDR2_D11	DATA[11]
AD3	DDR2_D12	DATA[12]
AD1	DDR2_D13	DATA[13]
AB3	DDR2_D14	DATA[14]
AB1	DDR2_D15	DATA[15]
W3	DDR2_LDM	LDM
V3	DDR2_LDQS_P	LDQS_P
V1	DDR2_LDQS_N	LDQS_N
P6	DDR2_ODT	ODT
N8	DDR2_RASN	RASn
V4	DDR2_UDM	UDM
AC2	DDR2_UDQS_P	UDQS_P
AC1	DDR2_UDQS_N	UDQS_N
P5	DDR2_WEN	WEn

4.14. SD-Card

The E2LP Base Board has single SD Card slot directly connected to the FPGA. Electrical interface specification along with communication SPI (serial bus standard established by Motorola) access protocol for SD cards is accomplished with “SD Card Physical Layer System Specification, Version 1.01” defined by SD Card Association.

Schematic diagram for SD/MMC connector is shown in Appendix N.

FPGA to SD/MMC connection on Bank 1 is shown in Table 13.

Table 13. SD-card connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
AF9	MMC_CD	CD switch
R23	MMC_CLK	CLK
R24	MMC_CMD	CMD
T19	MMC_DATA0	DAT0
T24	MMC_DATA1	DAT1
P24	MMC_DATA2	DAT2
R19	MMC_DATA3	DAT3/CD
AF16	MMC_WP	WP

4.15. DIP Switches

The E2LP Base Board has 8 DIP switches defining 8-bit wide logical value. Position of each switch could be in one of two positions producing logical one or zero on corresponding input pin on the FPGA.

Slide switches are long life type (improved ruggedness) and placed in an array.

Schematic diagram for user interface is shown in Appendix O.

Table 14 shows FPGA to slide switch array connection list on Bank 0.

Table 14. DIP Switches connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
W19	UI_SW0	SW0
Y24	UI_SW1	SW1
K19	UI_SW2	SW2
V24	UI_SW3	SW3
U20	UI_SW4	SW4
U23	UI_SW5	SW5
U24	UI_SW6	SW6
U19	UI_SW7	SW7

4.16. Push Buttons

The E2LP Base Board has 5 general-purpose push buttons defining a 5-bit wide logical value. Each button could be pressed or not, producing logical one or zero on corresponding input pin on the FPGA. When pressed, the button produces the logical zero, i.e. it operates in the inverted logic.

User interface general-purpose push buttons are placed in a diamond shape pattern.

Schematic diagram for user interface is shown in Appendix O.

Table 15 shows FPGA to push buttons connection list on Bank 0.

Table 15. Push buttons connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
AC24	UI_JOY0	JOY0
AC23	UI_JOY1	JOY1
AB24	UI_JOY2	JOY2
AA24	UI_JOY3	JOY3
AA23	UI_JOY4	JOY4

4.17. LED

LED subsystem on the E2LP Base Board consists of a 220 Ohm resistor in series with each of diodes. Resistor purpose is to limit the current flow to about 6mA when diode is on.

LED interface is made from 8 SMD LEDs placed in array so can be used as bar graph.

Schematic diagram for user interface is shown in Appendix O.

Table 16 shows FPGA to LED bar graph connection list on Bank 0.

Table 16. LED connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
N24	UI_LED0	LED0
N23	UI_LED1	LED1
M24	UI_LED2	LED2
L24	UI_LED3	LED3
L23	UI_LED4	LED4
K24	UI_LED5	LED5
H24	UI_LED6	LED6
D24	UI_LED7	LED7

4.18. LCD 16x2 Character Display

LCD 16 X 2 character display on the E2LP Base Board consists of a 16 characters X 2 lines LCD Display.

The schematic diagram of the user interface is given in Appendix O.

All user interface signals are tied to two IDC 20 expansion connectors, which allows user interface to be accessible when the board is mounted into housing. E2LP uses Display electronic GmbH LCD module SYH 16216 SYH-LY in 4 bit mode.

Table 17 shows FPGA to LCD connection list on Bank 0.

Table 17. LCD connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
T18	LCD_IO0	DATA[3]
D18	LCD_IO1	DATA[2]
V18	LCD_IO2	DATA[1]
W18	LCD_IO3	DATA[0]
D21	LCD_IO4	EN
C21	LCD_IO5	R/W
F24	LCD_IO6	RS
AD24	LCD_IO7	L+

4.19. Snapwire connector

The E2LP Base Board has 8 snapwire connectors defining 8-bit wide logical value.

Schematic diagram for user interface is shown in Appendix O.

Table 18 shows FPGA to snapwire connector connection list on Bank 0.

Table 18. Snapwire connection to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
C5	SNAPW_IN0	SNAPW_IN[0]
C6	SNAPW_IN1	SNAPW_IN[1]
D6	SNAPW_IN2	SNAPW_IN[2]
C7	SNAPW_IN3	SNAPW_IN[3]
C9	SNAPW_IN4	SNAPW_IN[4]
C11	SNAPW_IN5	SNAPW_IN[5]
C13	SNAPW_IN6	SNAPW_IN[6]
C17	SNAPW_IN7	SNAPW_IN[7]

4.20. Mezzanine Boards Interface

This section specifies the detailed design issues relating to the E2LP Base Board mezzanine boards interface section. The part describes the connector specification, mechanical and electrical concept and the technical implementation for these. It should provide information for later HW/SW/FW development work.

The schematic diagrams are given in Appendix P.

The E2LP platform is composed of a Base Board and a number of Mezzanine boards and is intended to provide the prototyping capability for designing the hardware and the software of an embedded computing system. For that purpose one high speed connector (for mezzanine board) is implemented on the board. Interface consists of 80-bit bus connected straight to FPGA, IIC bus, two differential clocks from FPGA and dedicated JTAG lines.

12V and 3.3V power supplies are brought to connectors for powering up the mezzanine boards. 80-bit interface is routed as high speed 50ohm single ended lines or 100ohm differential pair lines, with equalized line length to achieve signal integrity for a wide range of possible mezzanine boards.

High speed connectors based on Xilinx FMC LPC standard are used for the mezzanine boards interconnecting. More information about extension boards implemented in the initial platform release is given in D3.3 “Produced and Assembled E2LP Extension Boards” [5].

FPGA to mezzanine connector connection list on Banks 1 and 2 of the FPGA is shown in Table 19.

Out of 80 bits on the FMC LPC bus, 68 are used as general-purpose inputs/outputs and are connected to FPGA. They can be used as 68 single-ended ports or 34 differential pairs. 4 pins are connected to the dedicated clock ports of the FPGA, meaning they can be used as 4 single-ended clocks or 2 differential pair clocks. One pin (PRSNT_M2C_L) is a dedicated reset signal for the extension board, but it can also be used as a general-purpose port.

The remaining 7 pins are used for I2C and JTAG chain, should the extension board have a JTAG-configurable component. These pins are not connected to FPGA and are not included in the Table 19.

Table 19. Mezzanine connection to FPGA

FPGA BALL	SCH Net Name	Interface Signal Name
AE5	LA00_CC_P	LA00_CC_P
AF5	LA00_CC_N	LA00_CC_N
U13	LA01_CC_P	LA01_CC_P
U12	LA01_CC_N	LA01_CC_N
AD6	LA02_P	LA02_P
AF6	LA02_N	LA02_N
V11	LA03_P	LA03_P
W11	LA03_N	LA03_N
AD8	LA04_P	LA04_P
AF8	LA04_N	LA04_N
Y10	LA05_P	LA05_P
AB10	LA05_N	LA05_N
AC9	LA06_P	LA06_P
AD9	LA06_N	LA06_N
AE11	LA07_P	LA07_P
AF11	LA07_N	LA07_N
AA11	LA08_P	LA08_P
AB11	LA08_N	LA08_N
AC11	LA09_P	LA09_P
AD11	LA09_N	LA09_N
AA12	LA10_P	LA10_P
AC12	LA10_N	LA10_N
AA13	LA11_P	LA11_P
AB13	LA11_N	LA11_N
AD12	LA12_P	LA12_P
AF12	LA12_N	LA12_N
V13	LA13_P	LA13_P
W14	LA13_N	LA13_N
V12	LA14_P	LA14_P
W12	LA14_N	LA14_N
U15	LA15_P	LA15_P
V14	LA15_N	LA15_N
Y14	LA16_P	LA16_P
AA14	LA16_N	LA16_N
AE13	CLK0_M2C_P	CLK0_M2C_P
AF13	CLK0_M2C_N	CLK0_M2C_N
AF4	PRSNT_M2C_L	PRSNT_M2C_L

FPGA BALL	SCH Net Name	Interface Signal Name
Y15	LA17_CC_P	LA17_CC_P
AA15	LA17_CC_N	LA17_CC_N
AE15	LA18_CC_P	LA18_CC_P
AF15	LA18_CC_N	LA18_CC_N
AC15	LA19_P	LA19_P
AD15	LA19_N	LA19_N
AB15	LA20_P	LA20_P
AC14	LA20_N	LA20_N
AC16	LA21_P	LA21_P
AD17	LA21_N	LA21_N
Y16	LA22_P	LA22_P
AA17	LA22_N	LA22_N
V15	LA23_P	LA23_P
W16	LA23_N	LA23_N
AD18	LA24_P	LA24_P
AF18	LA24_N	LA24_N
AA18	LA25_P	LA25_P
AB18	LA25_N	LA25_N
AB17	LA26_P	LA26_P
AC17	LA26_N	LA26_N
V16	LA27_P	LA27_P
W17	LA27_N	LA27_N
AC19	LA28_P	LA28_P
AD19	LA28_N	LA28_N
AE19	LA29_P	LA29_P
AF19	LA29_N	LA29_N
AE21	LA30_P	LA30_P
AF21	LA30_N	LA30_N
Y18	LA31_P	LA31_P
AA19	LA31_N	LA31_N
Y20	LA32_P	LA32_P
Y21	LA32_N	LA32_N
AC20	LA33_P	LA33_P
AD21	LA33_N	LA33_N
AC13	CLK1_M2C_P	CLK1_M2C_P
AD13	CLK1_M2C_N	CLK1_M2C_N

4.21. SSN

The E2LP Base Board has DS2401 (Property of Dallas Semiconductor) SSN chip defining unique 64-bit serial number for each board. Electrical interface specification along with communication access protocol for DS2401 is accomplished with One Wire interface specification which is also property of Dallas Semiconductor.

The SSN IC is connected to the COP. Resistor R820 is used to pull-up the SSN data line to 3.3V.

4.22. Dedicated clock and reset

The E2LP base board contains the 24 MHz oscillator which is connected directly to the FPGA and can be used as a general-purpose clock. Additionally, the board provides a 50 MHz oscillator, connected to FPGA as a differential signal, mainly to be used for DDR2 clocking, but it can also be used as a general-purpose clock.

One button is a dedicated reset button, although it can be used as a general-purpose input as well.

Table 20 summarizes these dedicated inputs to FPGA.

Table 20. Dedicated clock and reset inputs to FPGA

FPGA BALL	Schematic Net Name	Interface Signal Name
AD14	CLK_DDR2_P	CLK_DDR2_P
AF14	CLK_DDR2_N	CLK_DDR2_N
M21	FPGA_OSC	CLK
AE24	FPGA_RSTN	RSTn

5. Mechanical Design

The following figures present the 3D overview of the base board and some 2D views.

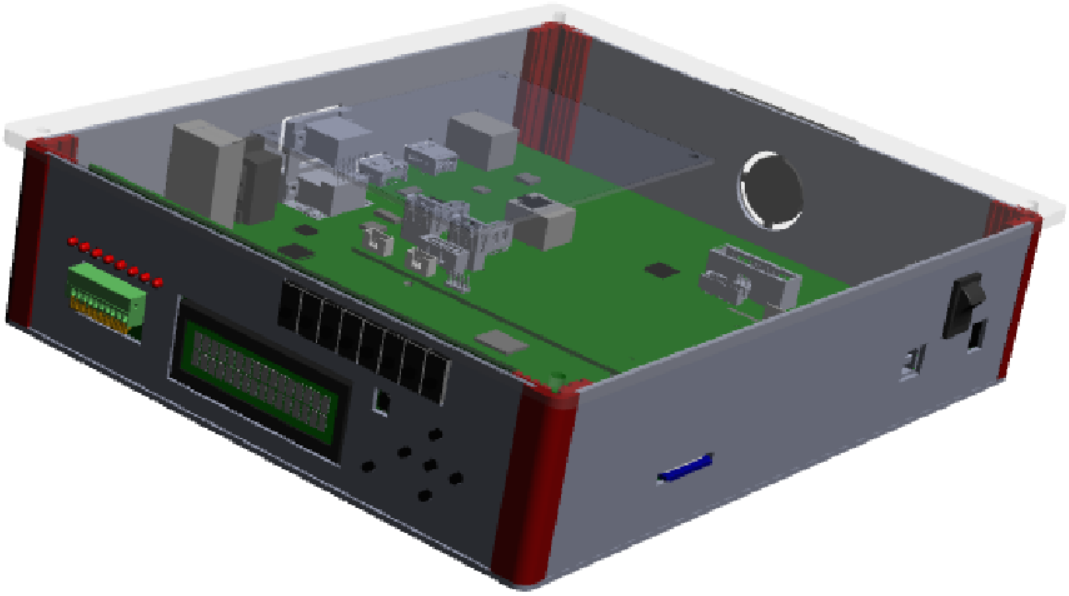


Figure 4. 3D view of the front of the board

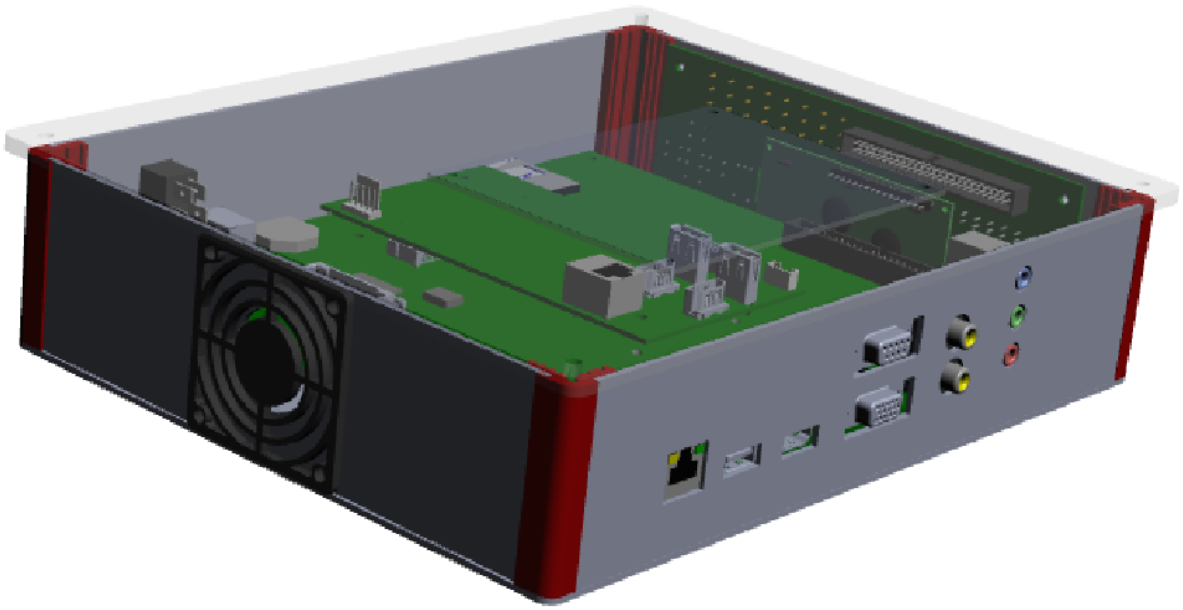


Figure 5. 3D view of the back of the base board

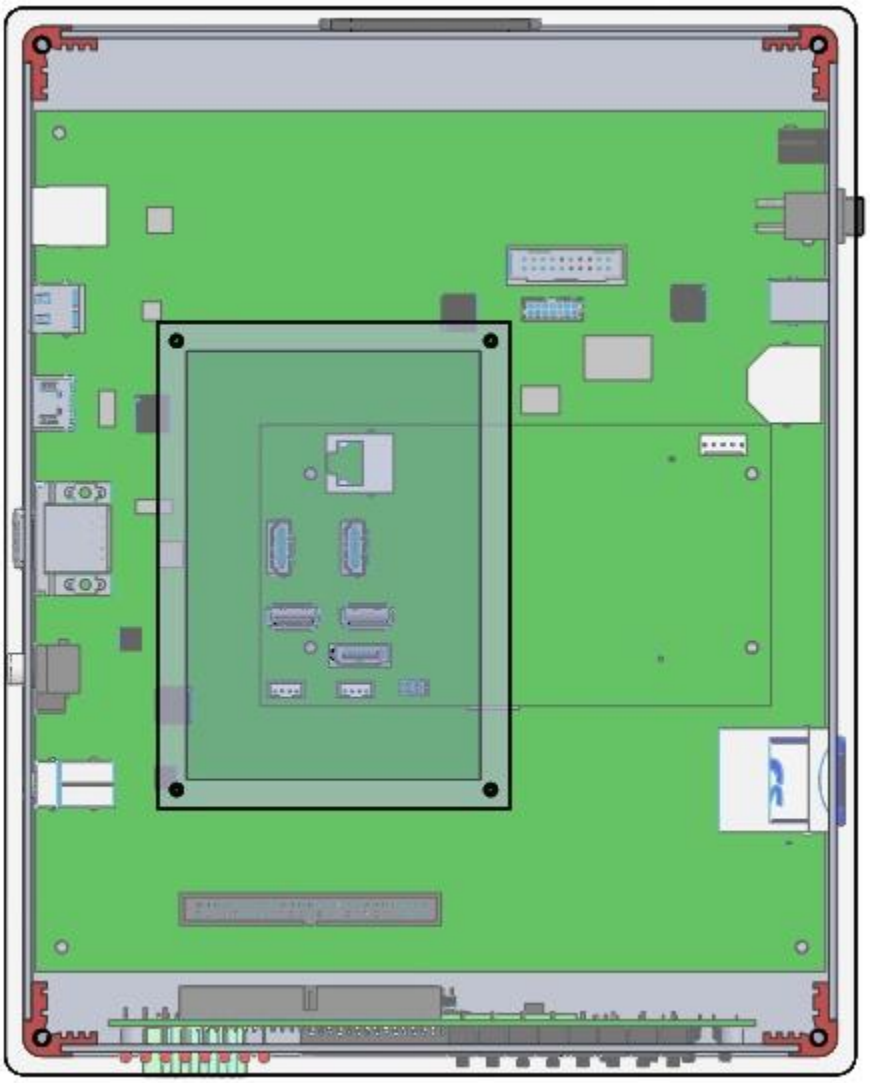


Figure 6. Upper view of the E2LP base board

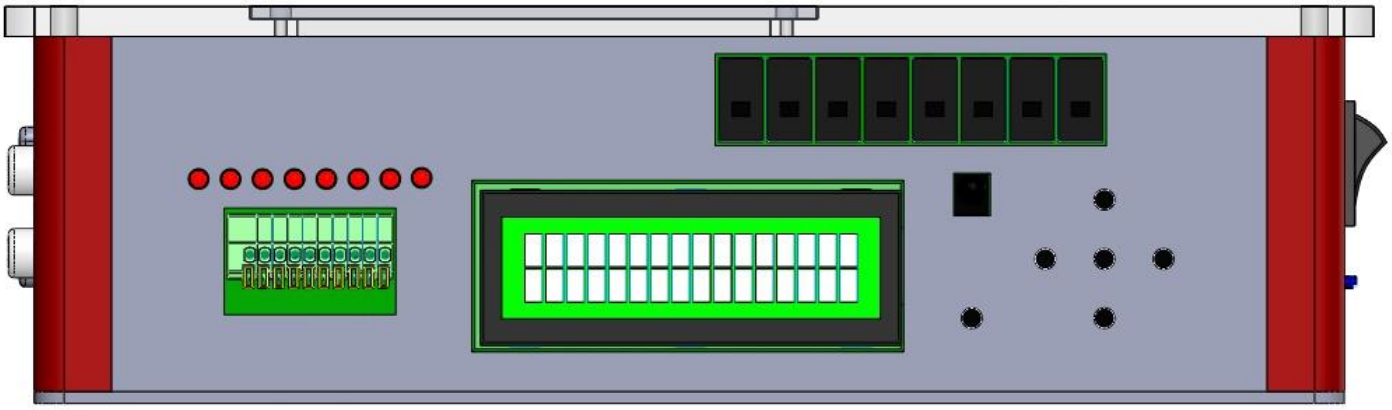


Figure 7. Front view of the E2LP base board

The board is enclosed in the box which has a transparent cover. The cover is removable and consists of two parts: a smaller and a larger cover. The following are the three use cases of the board, with respect to the state of the covers:

- both covers closed – suitable when the user wants to protect the board from external influences and still be able to see the contents on the board through a transparent cover; this case can be used with the Base Board only, or with the extension board which does not require cables,
- small cover open, large cover closed – suitable when the user wants to protect the board from external influences, but the extension board requires external connection with cables, which go through the open small cover,
- both covers open – suitable when the user wants to have physical access to all components of the board; this use case is the only one possible when the Augmented Reality interface wants to be used on the board.

6. Board Configuration

JTAG chain is used to configure FPGA, CPLD and Platform Flash on the E2LP base board.

CPLD is used as a central router of the JTAG chain on the board. The board supports three configuration cases:

- Platform Cable – Platform Flash – CPLD – FPGA

  In this configuration, the Xilinx Platform Cable is used to configure the three JTAG components on the board; this case is a required starting point for board configuration during the board bring-up, which configures the CPLD; this case can also be used whenever the configuration of Platform Flash and FPGA wants to be done using the Platform Cable.

- COP – Platform Flash – FPGA

  This configuration is triggered by the control processor on the board (COP). The COP sends the signal to the CPLD to re-route the JTAG chain such that the COP becomes the JTAG master. COP can then configure both Platform Flash and FPGA on the board. This is the suggested default configuration case since the E2LP software [4] can be used to configure the FPGA on the board.

- COP – Platform Flash – FPGA – Mezzanine

  This configuration is triggered by the Mezzanine board. When attached, the signal bit informs the CPLD to re-route JTAG chain such that the COP becomes the JTAG master and can configure Platform Flash, FPGA and Mezzanine extension board, if the JTAG-configurable component exists on the extension board. The extension board must physically close the JTAG chain even if there are no JTAG-configurable components, in order for the complete chain to be closed.

Figure 8 shows the diagrams of the three configuration cases.

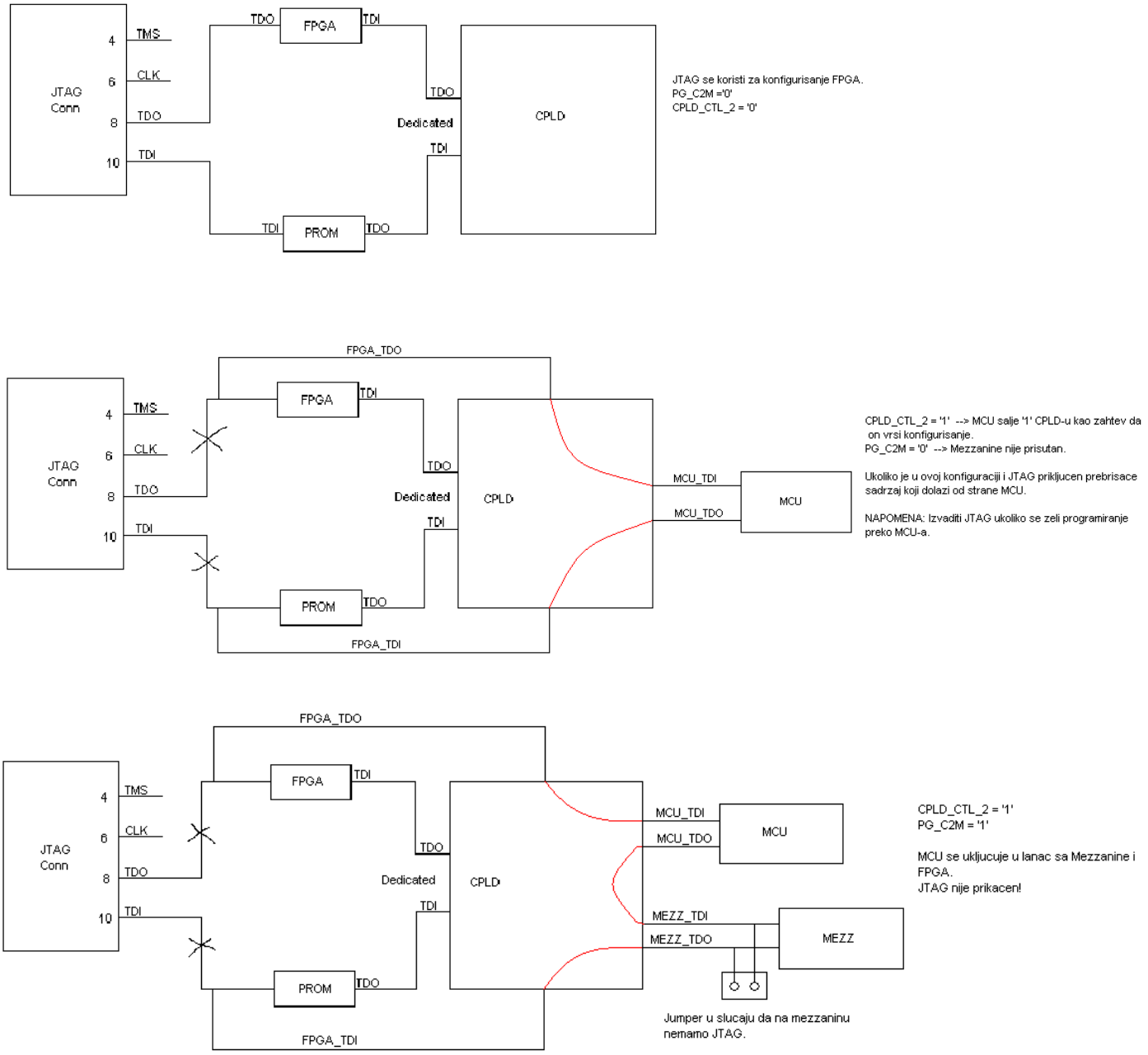


Figure 8. Three configuration cases – platform cable as master (upper), COP as master (middle) and COP as master with Mezzanine (lower)

7. Conclusions

This document presented the produced and assembled E2LP Base Board and specified requirements for the extension boards connecting to it.

The E2LP Base Board, as presented in this document, together with its extension boards, is working in fully satisfying the main requirement of the E2LP platform – to be used in the complete embedded engineering curriculum and significantly reduce the overhead in engineering education. Implementation of the extension boards whose mechanical requirements are specified in this document has been delivered in deliverable D3.3 [5].

References

[1] E2LP Consortium – Deliverable D3.1 “E2LP Design Specification”

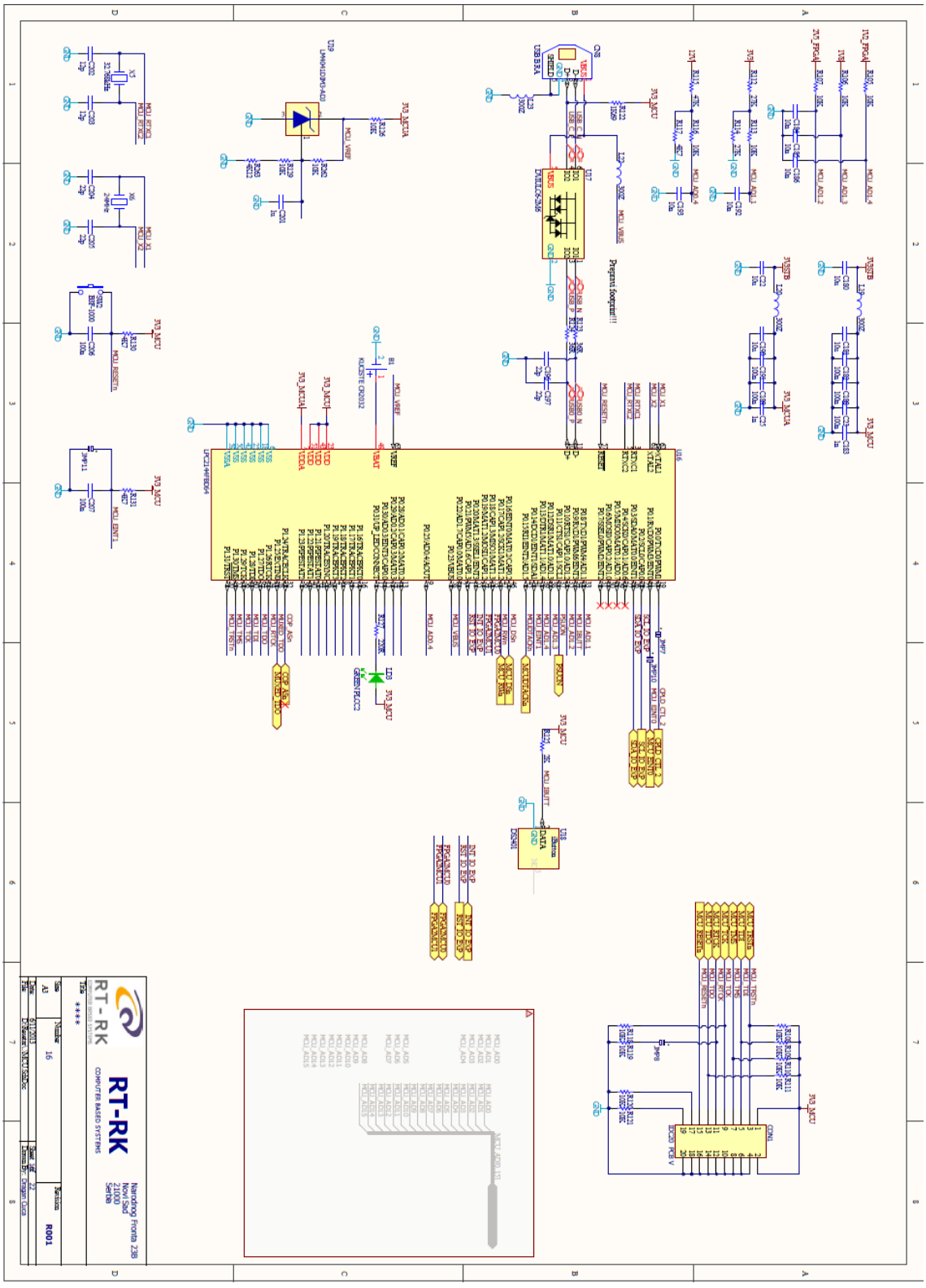
[2] E2LP Consortium – Deliverable D2.1 “Partners’ Skills and Current Practices”

[3] E2LP Consortium – Deliverable D2.2 “E2LP Requirement List”

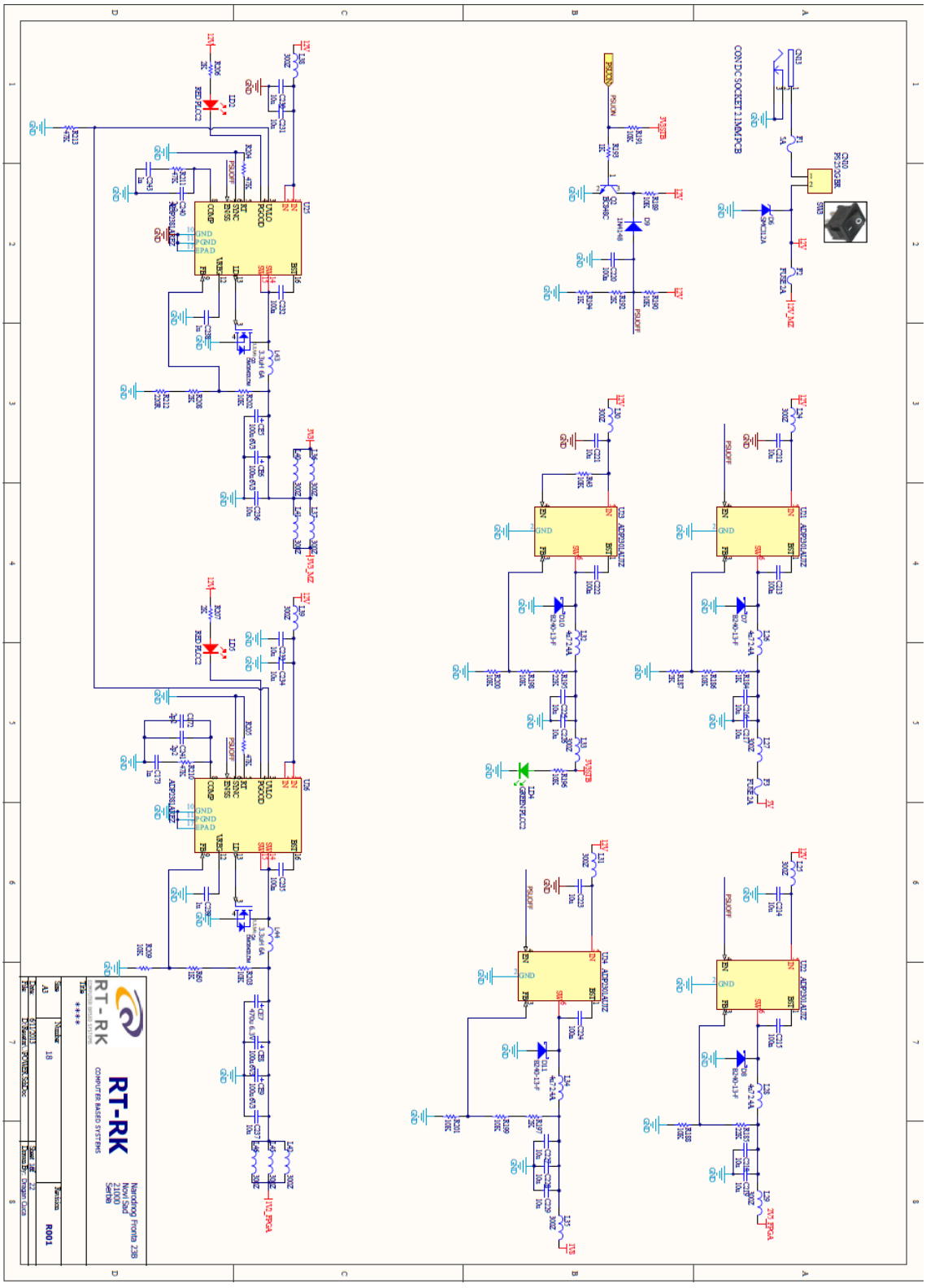
[4] E2LP Consortium – Deliverable D3.4 “E2LP Software Implementation”

[5] E2LP Consortium – Deliverable D3.3 “Produced and Assembled Extension Boards”

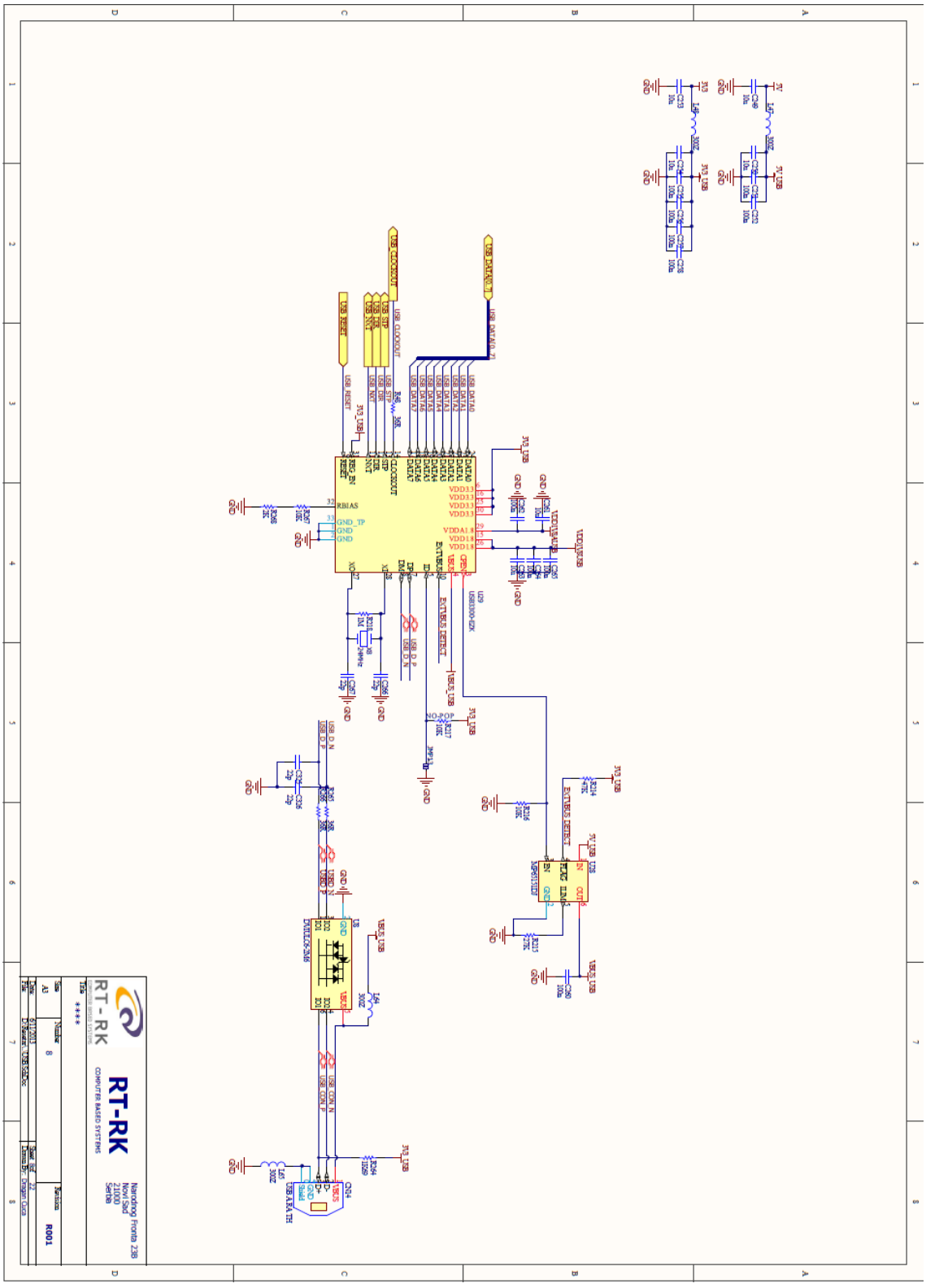
Appendix A – ARM COP



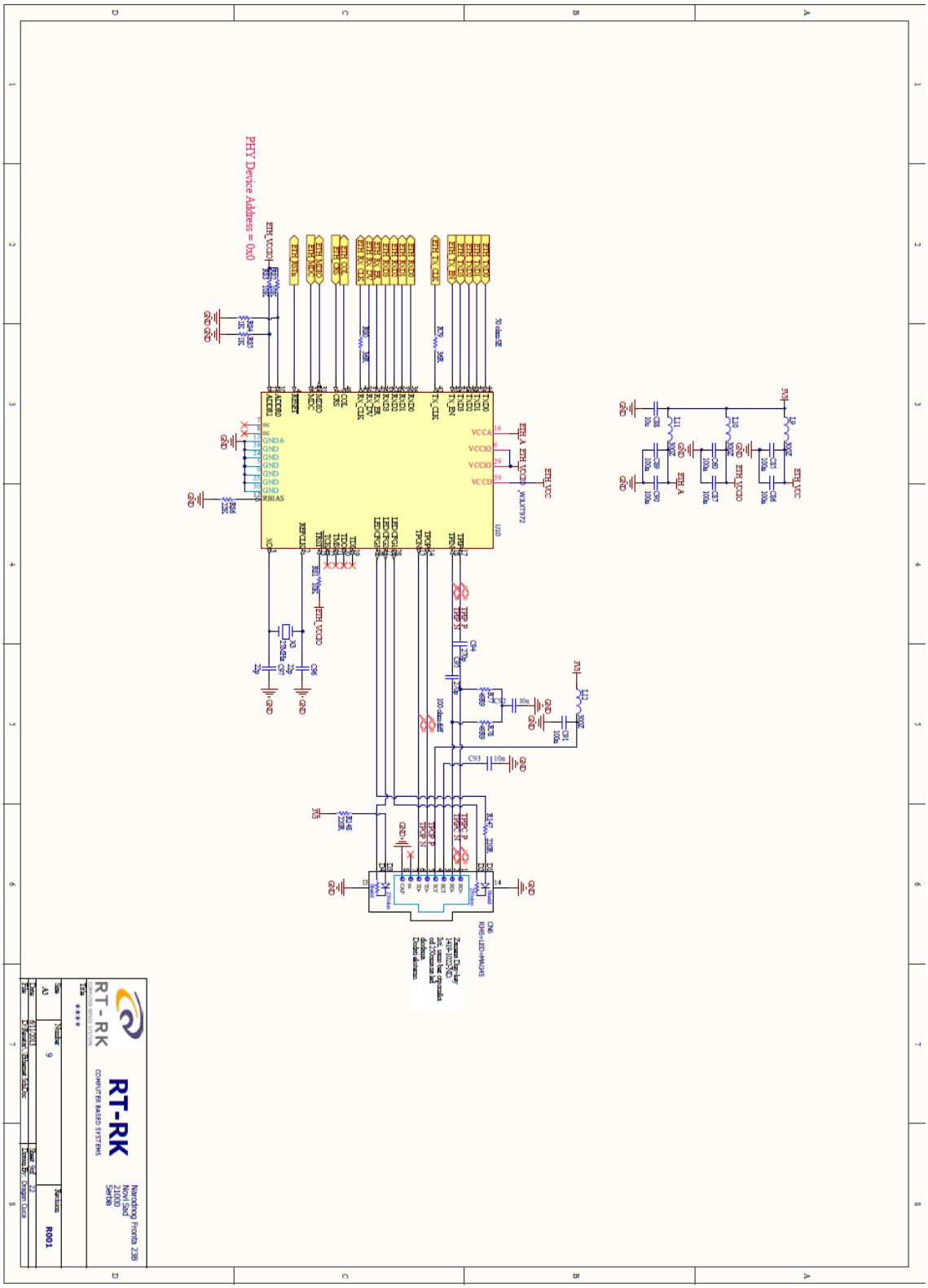
Appendix B – Power Supply



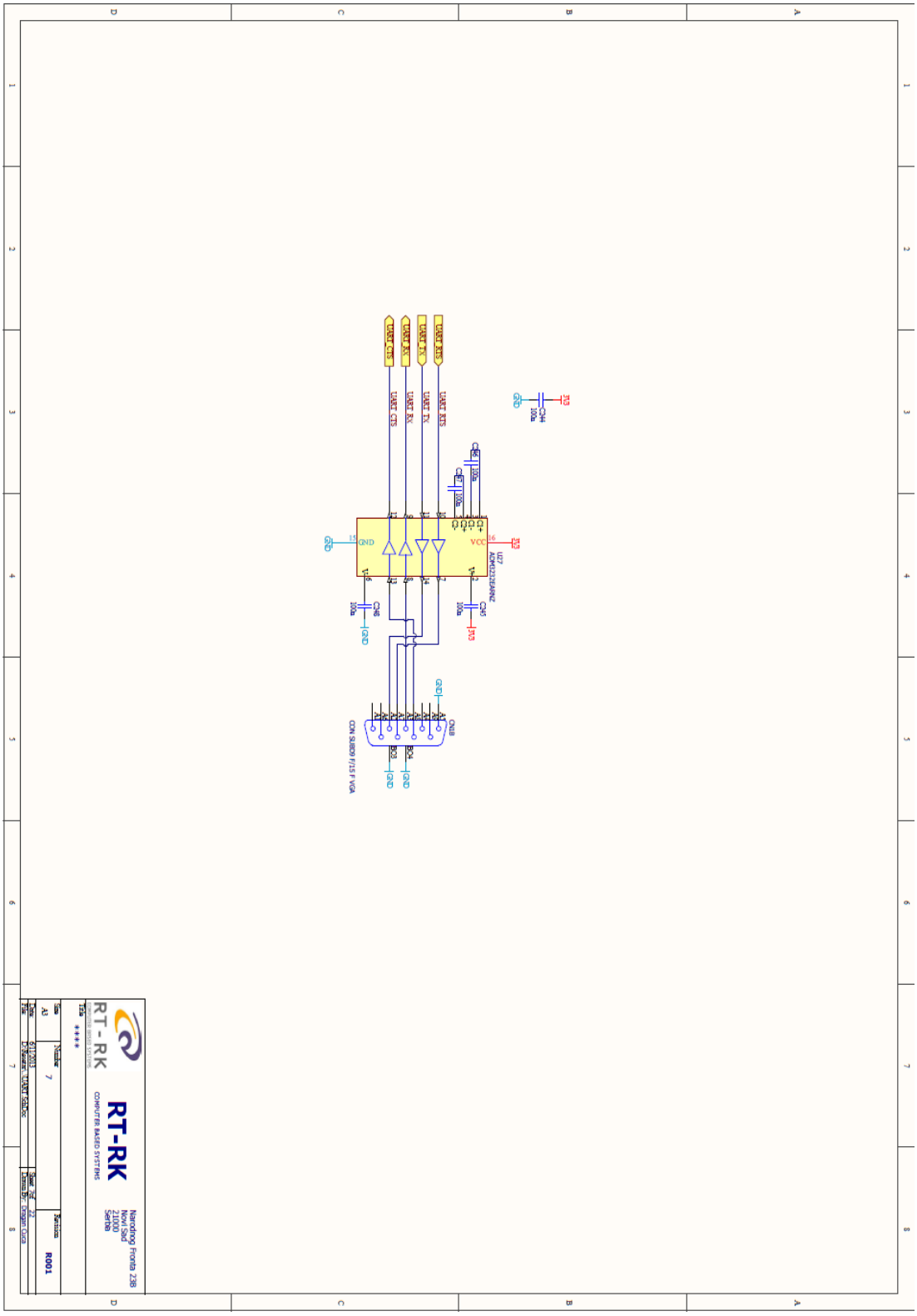
Appendix C – USB



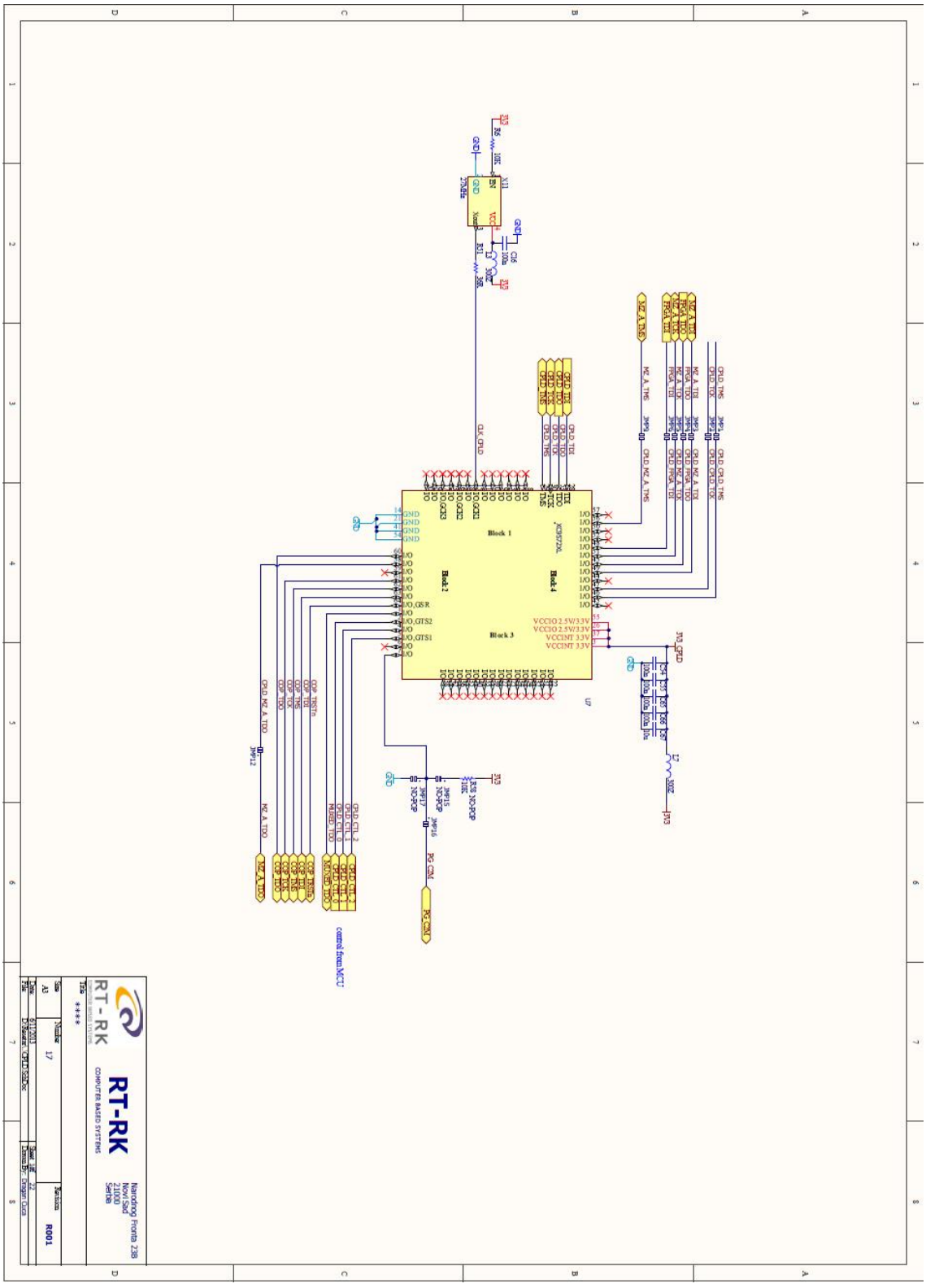
Appendix D – Ethernet



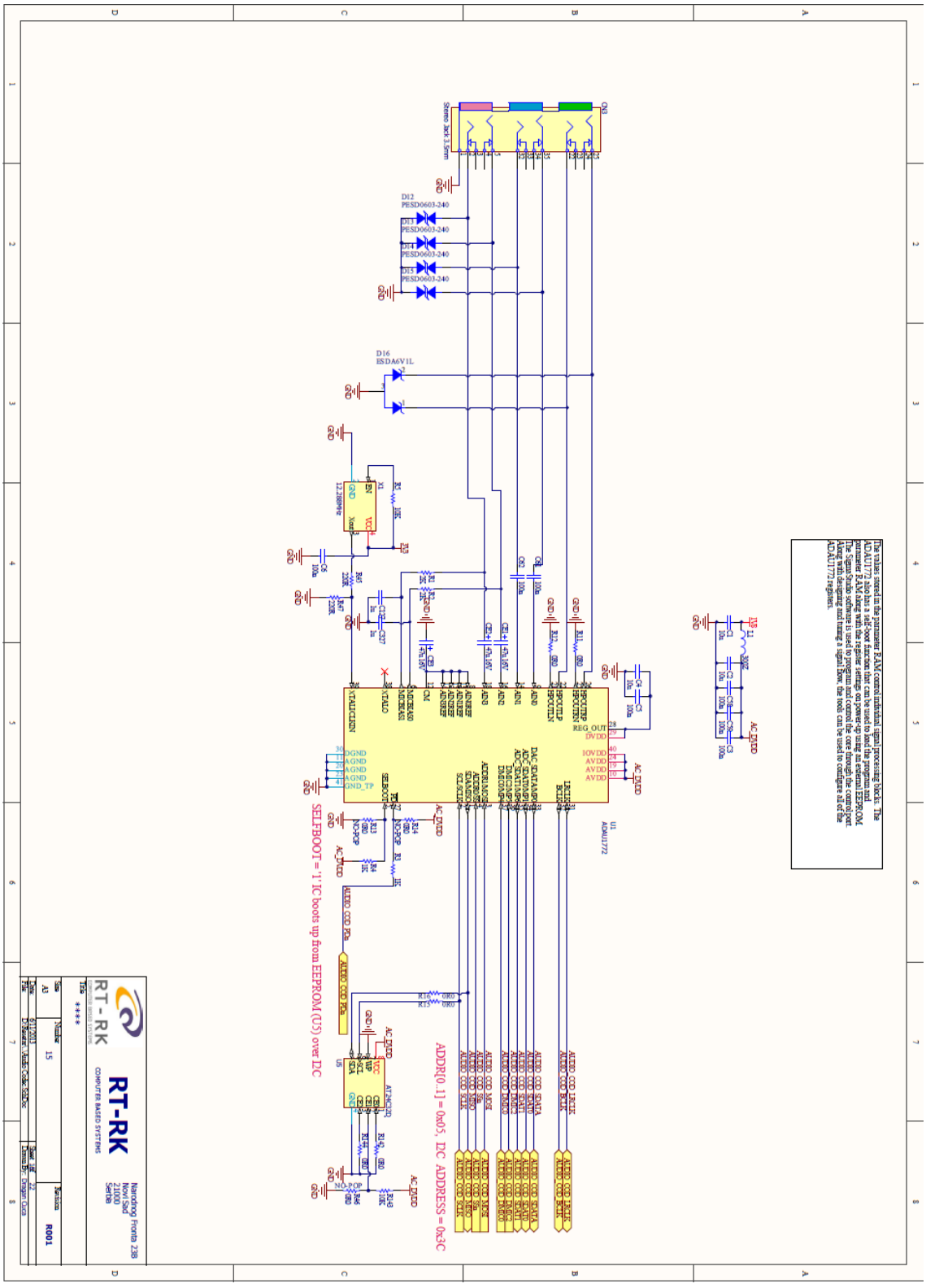
Appendix E – RS-232



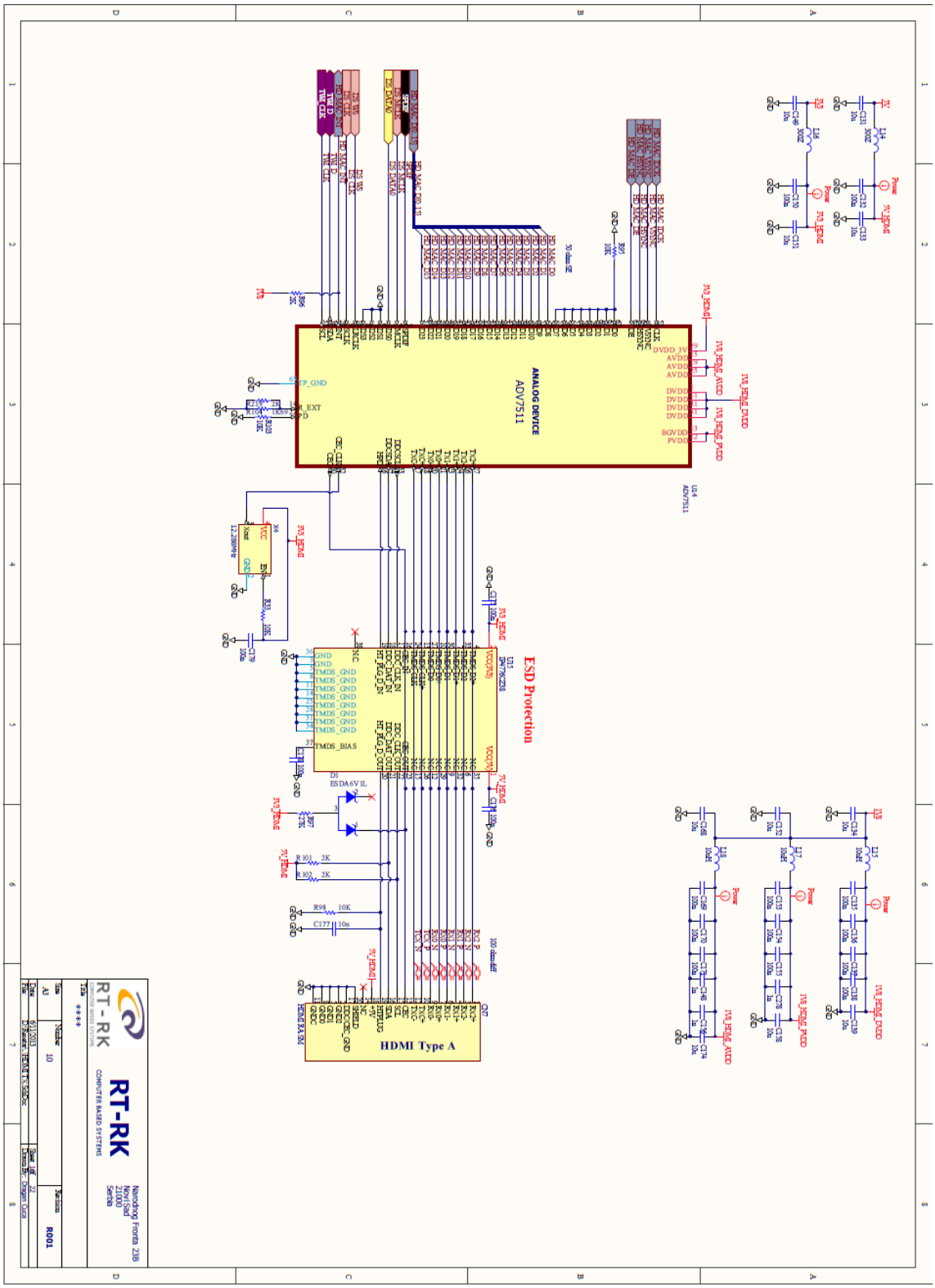
Appendix F – CPLD



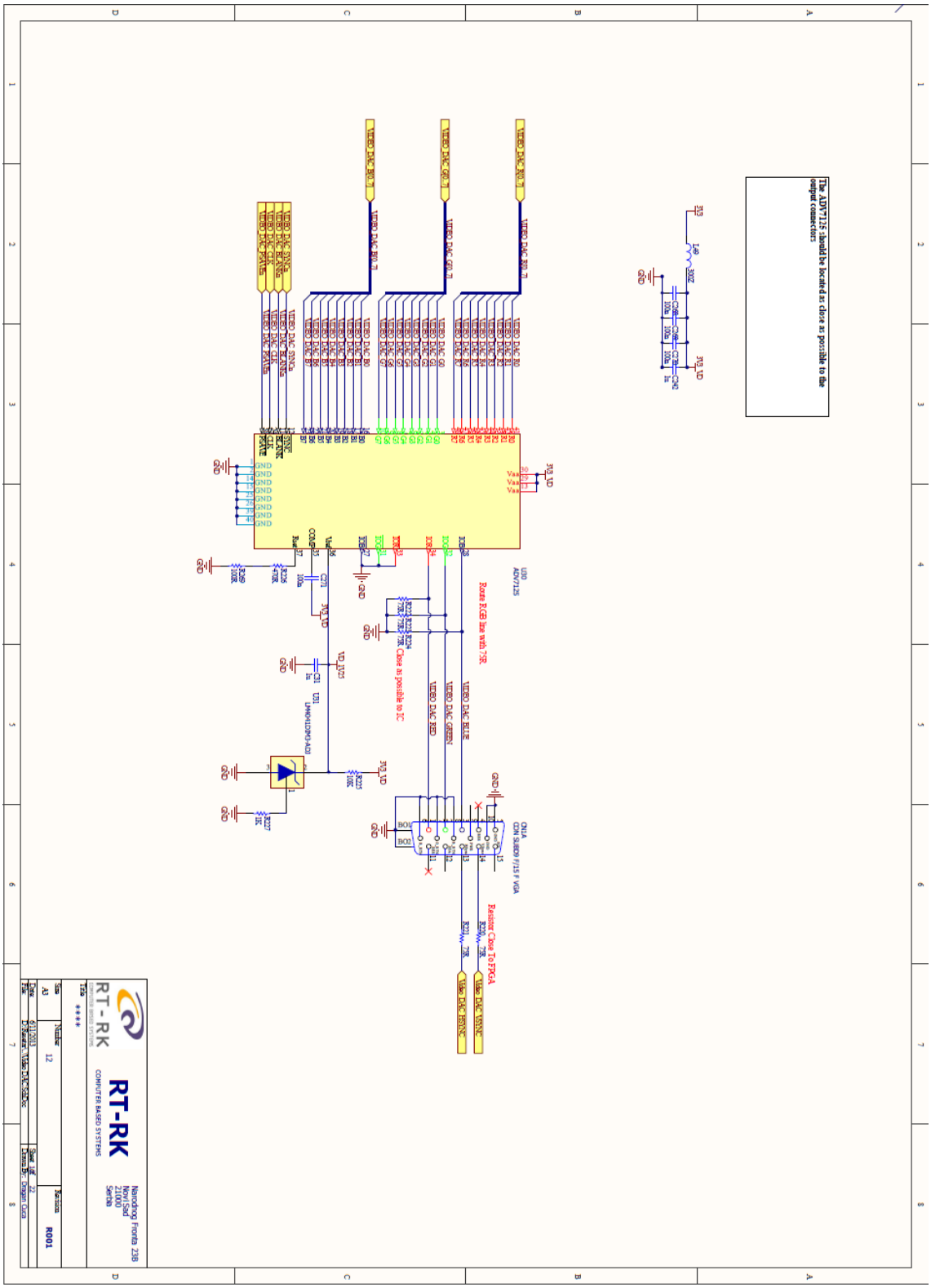
Appendix G – AC97 Audio Codec



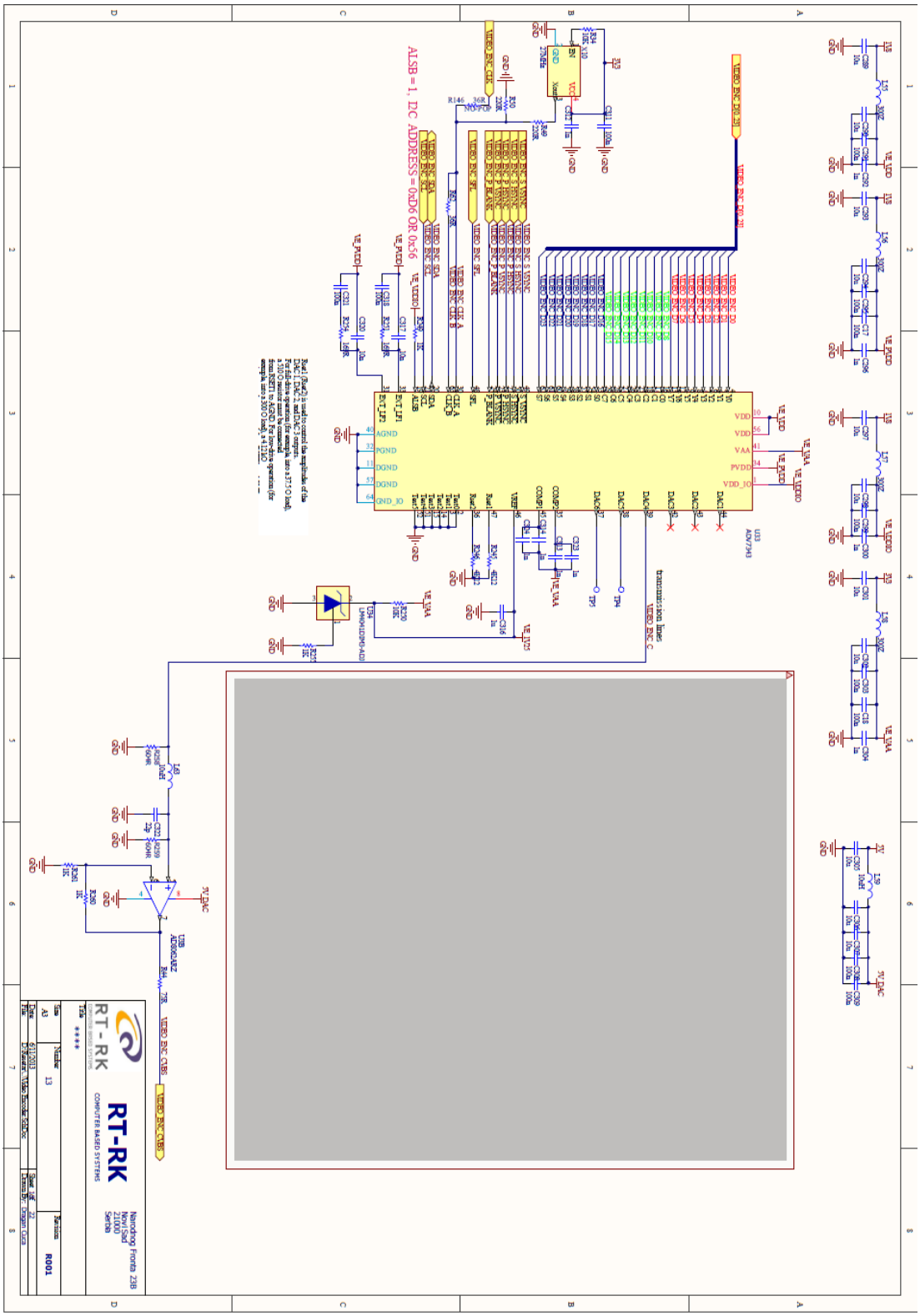
Appendix H – HDMI



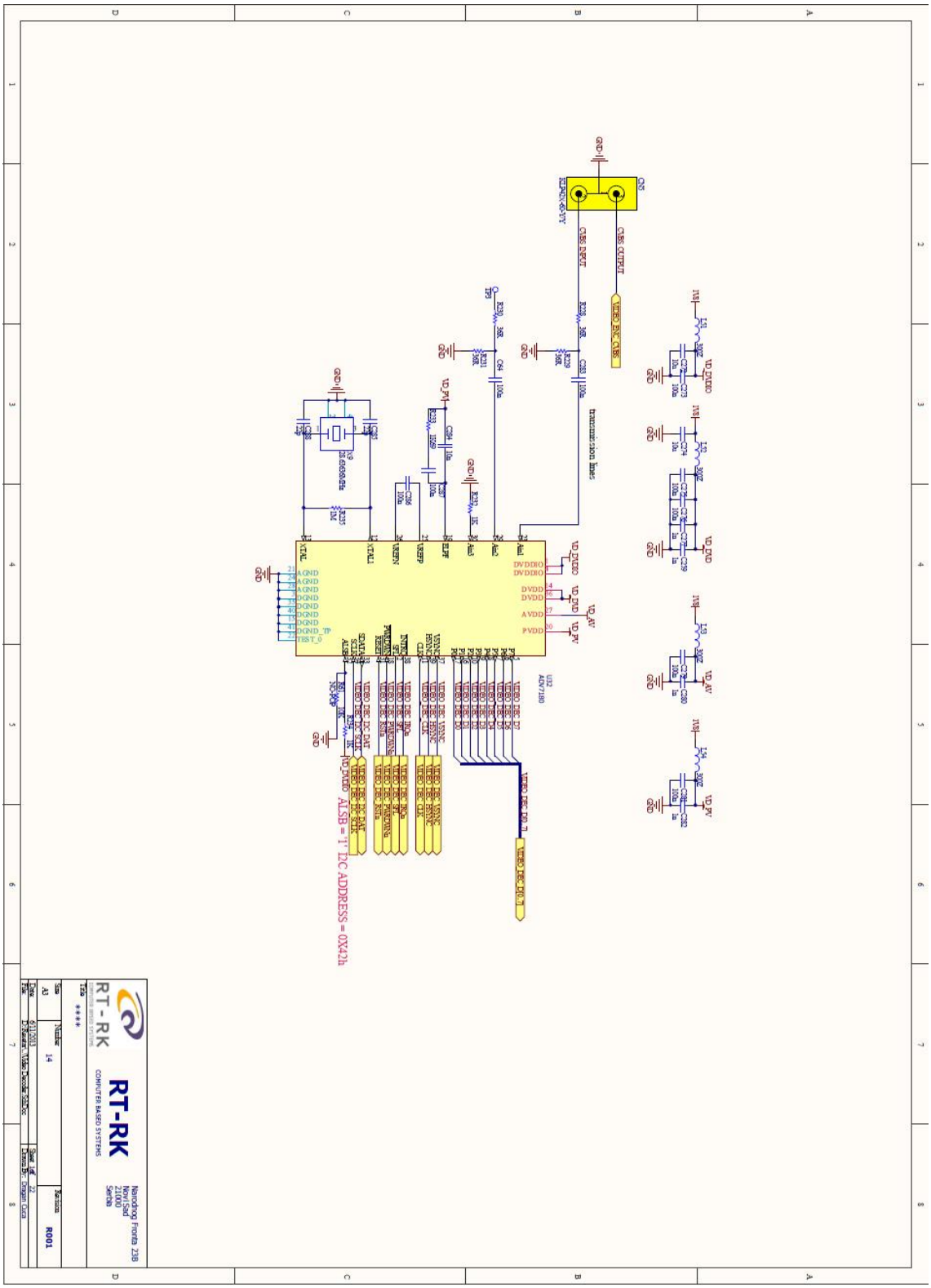
Appendix I – VGA DAC



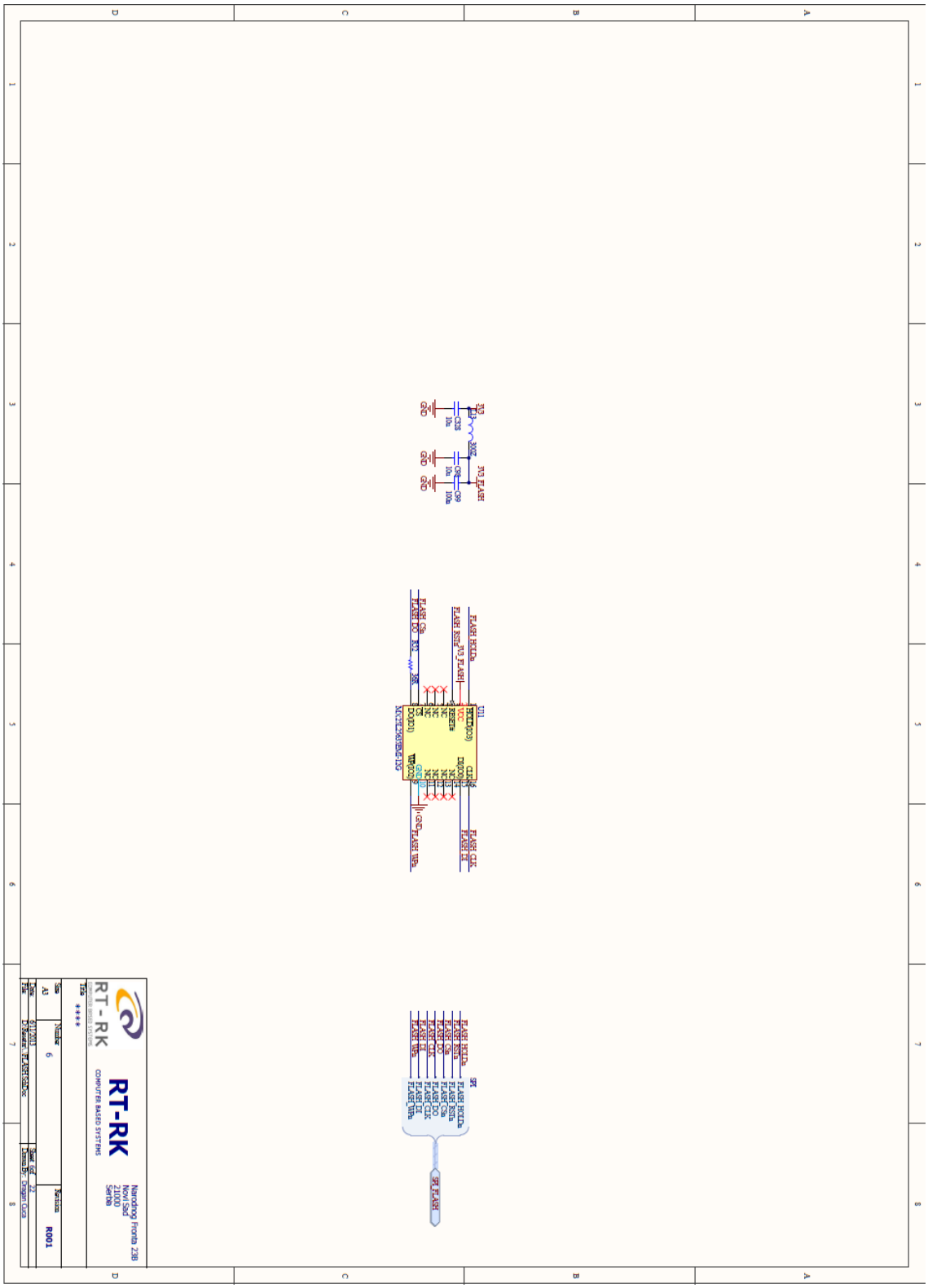
Appendix J – Video Encoder



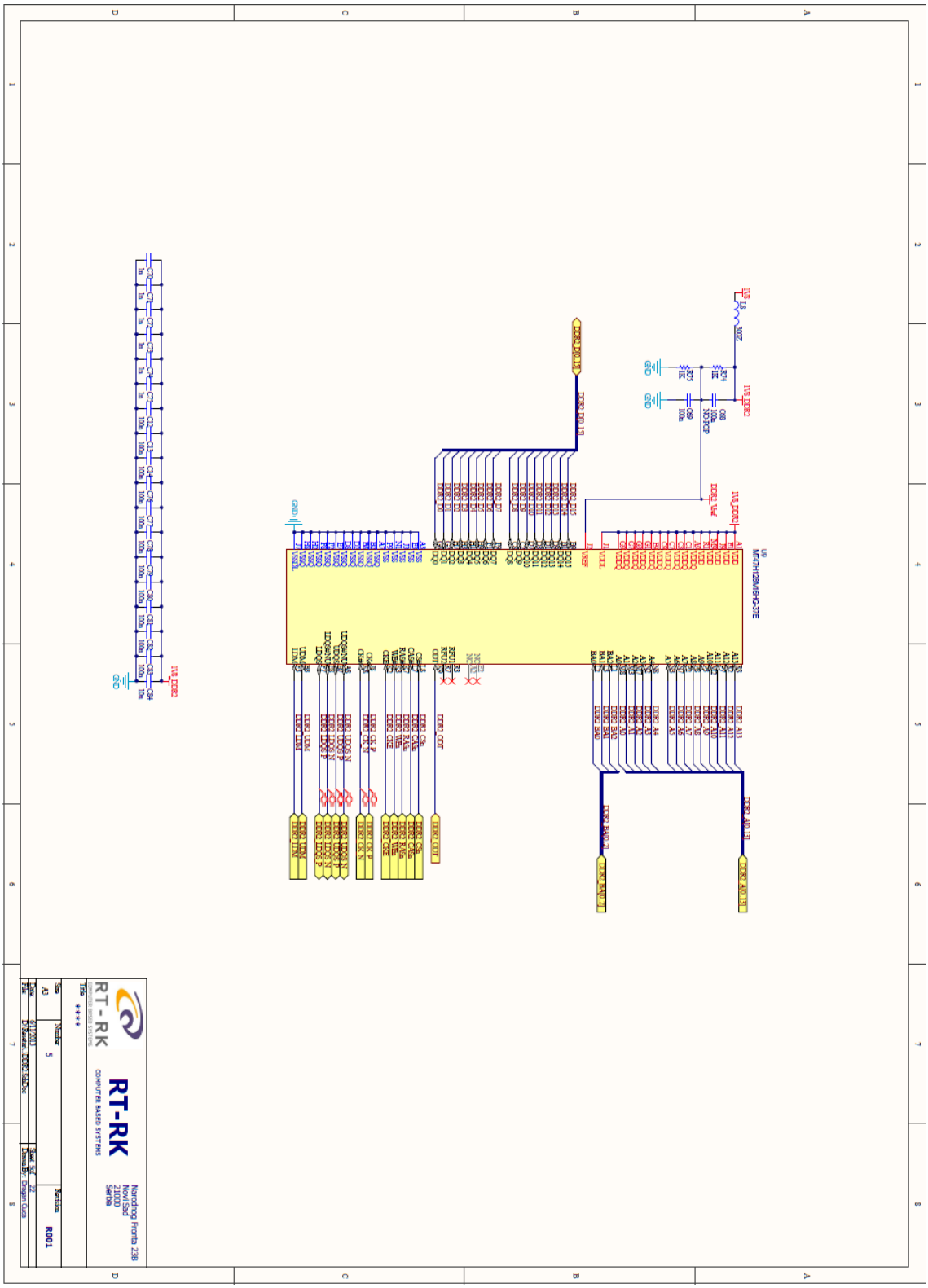
Appendix K – Video Decoder



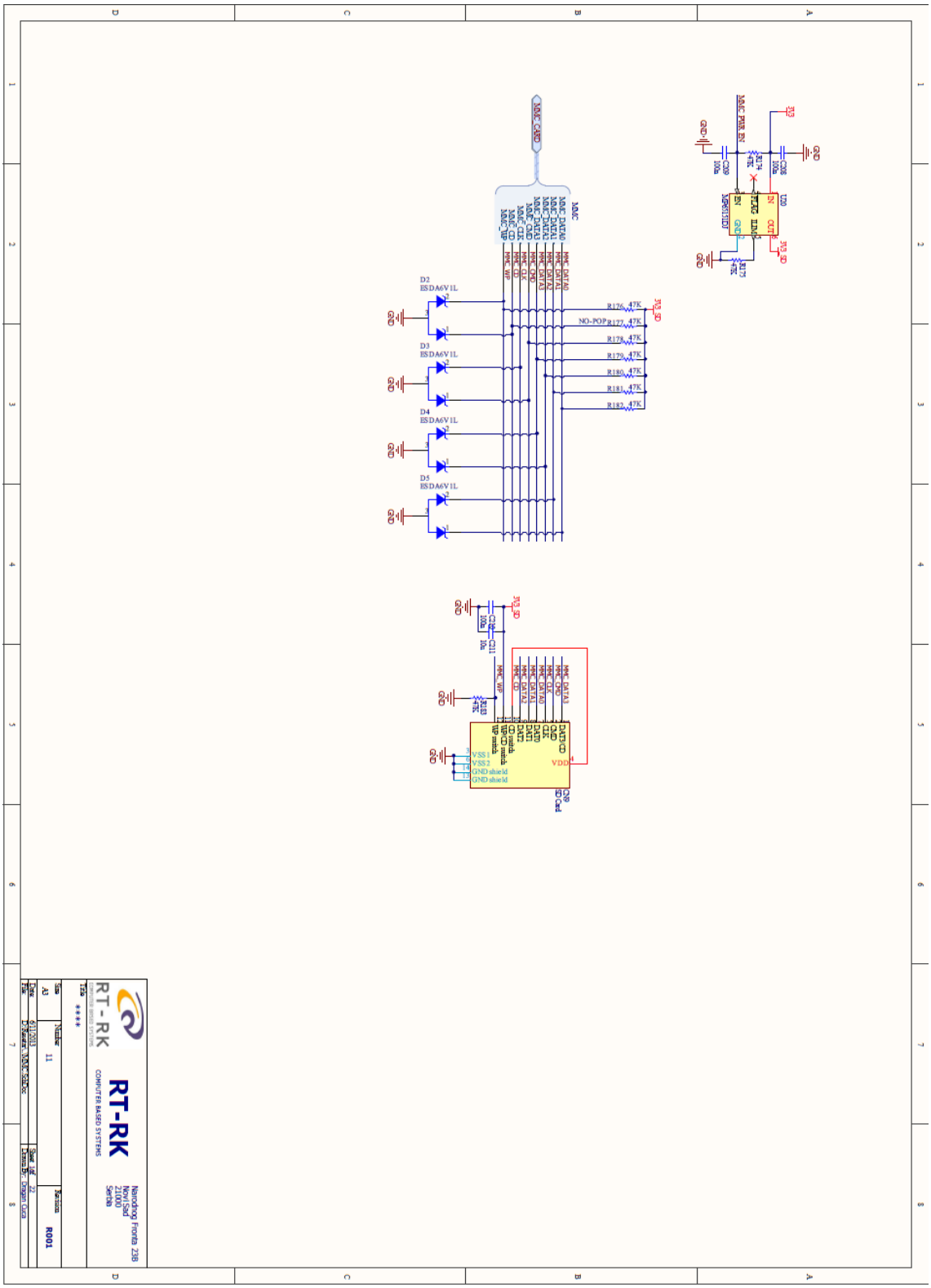
Appendix L – Flash



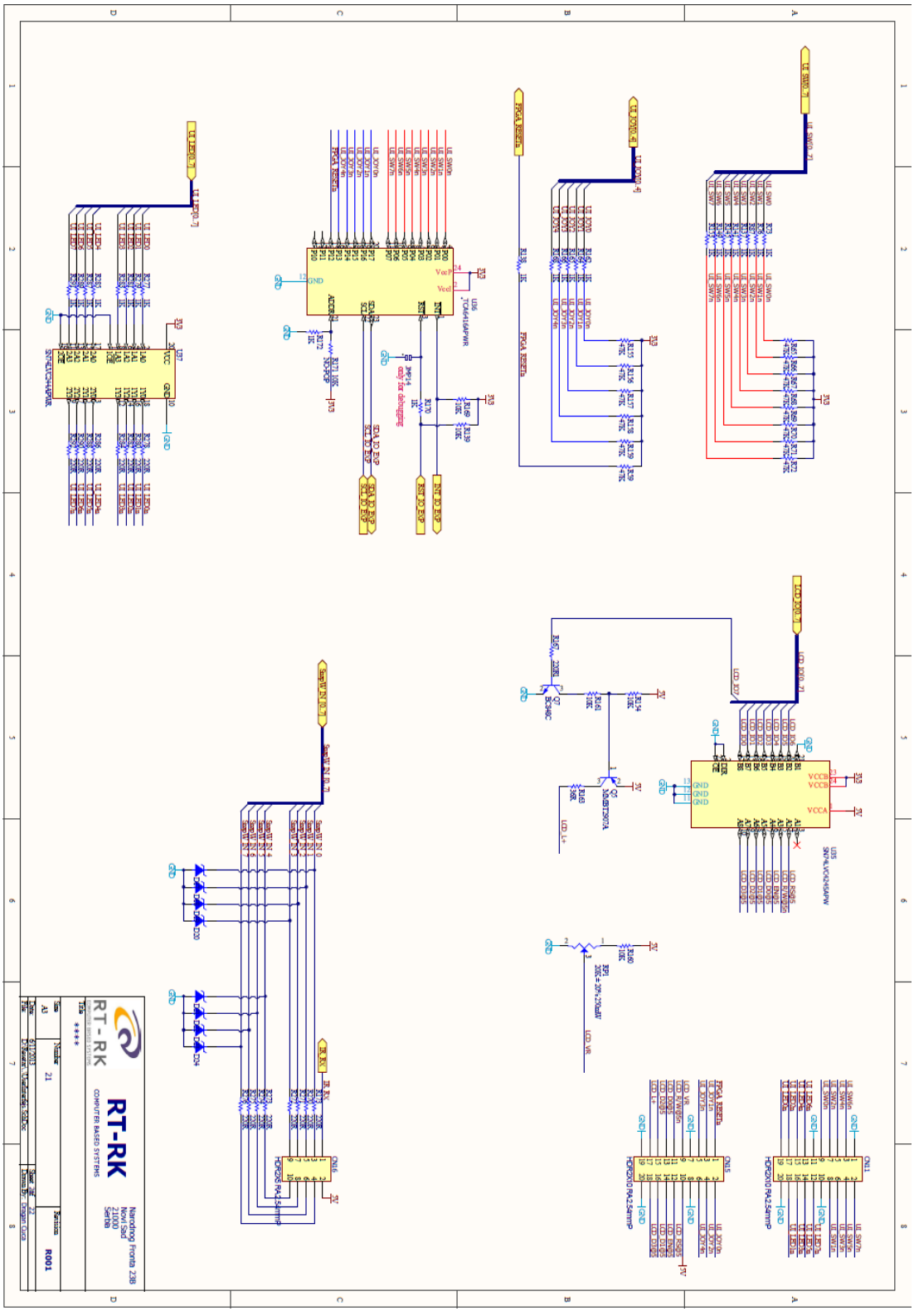
Appendix M – DDR2



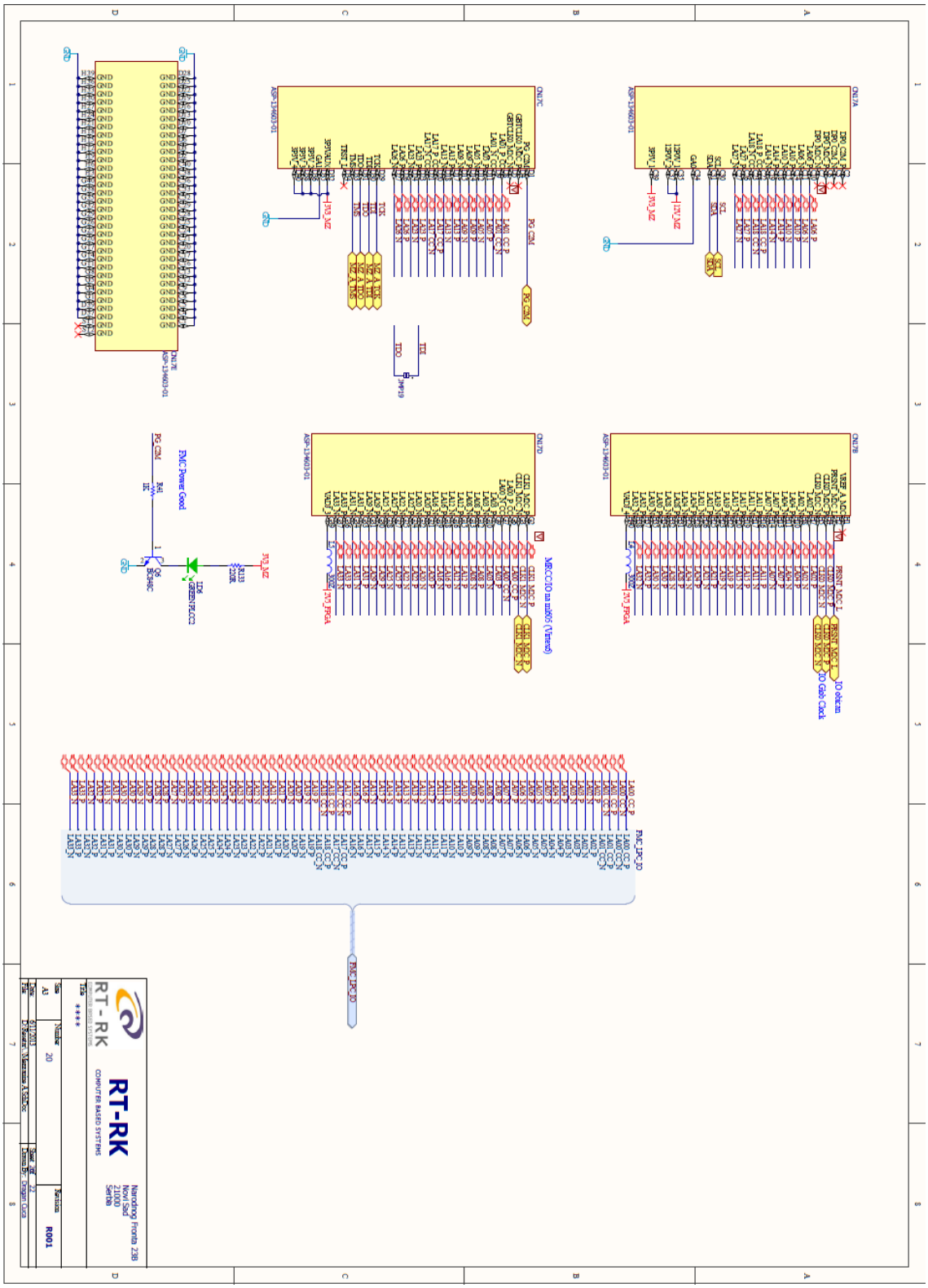
Appendix N – SD/MMC Card



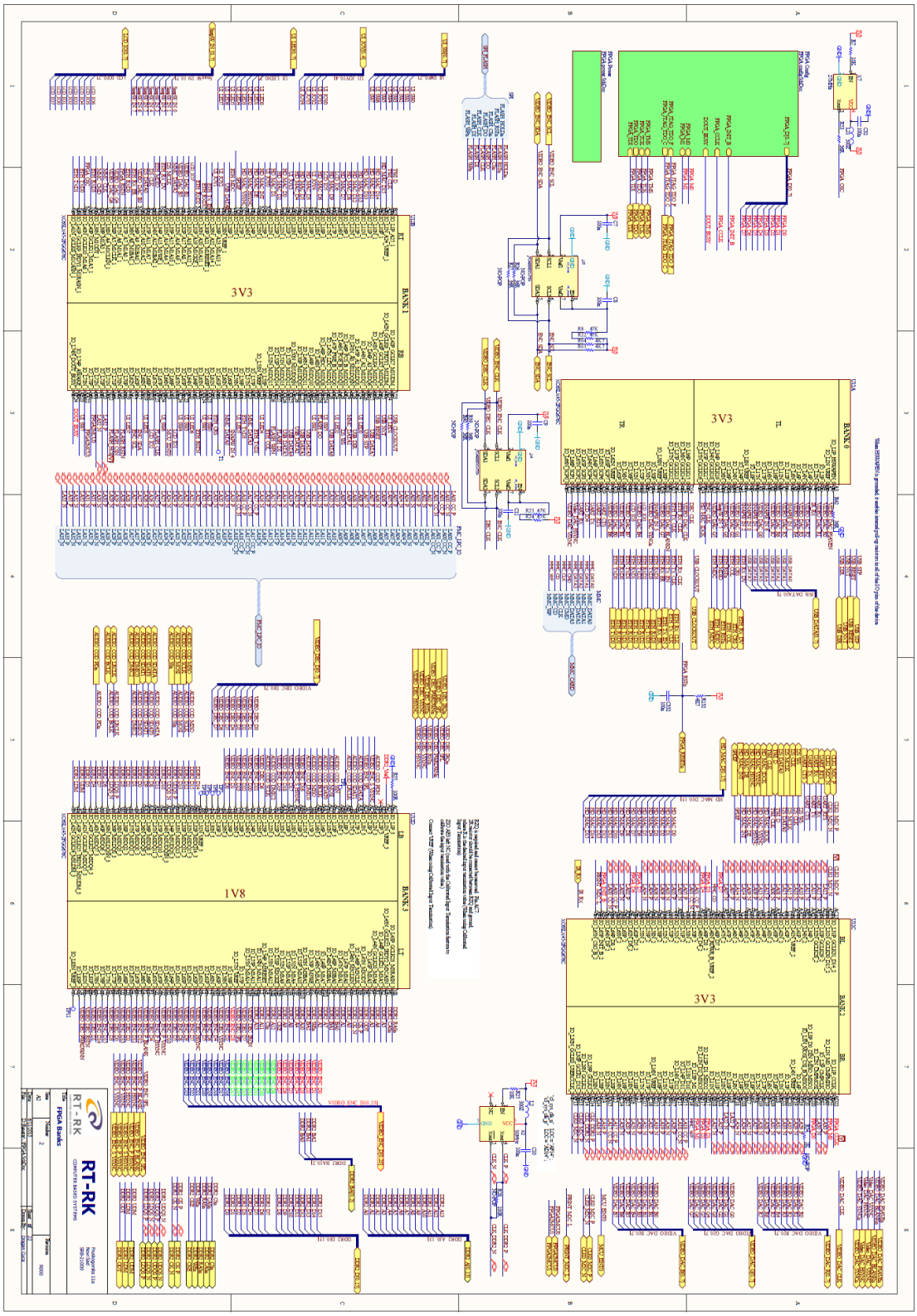
Appendix O – User Interface (Switches, Buttons, LED, LCD, Snapwire, IR)



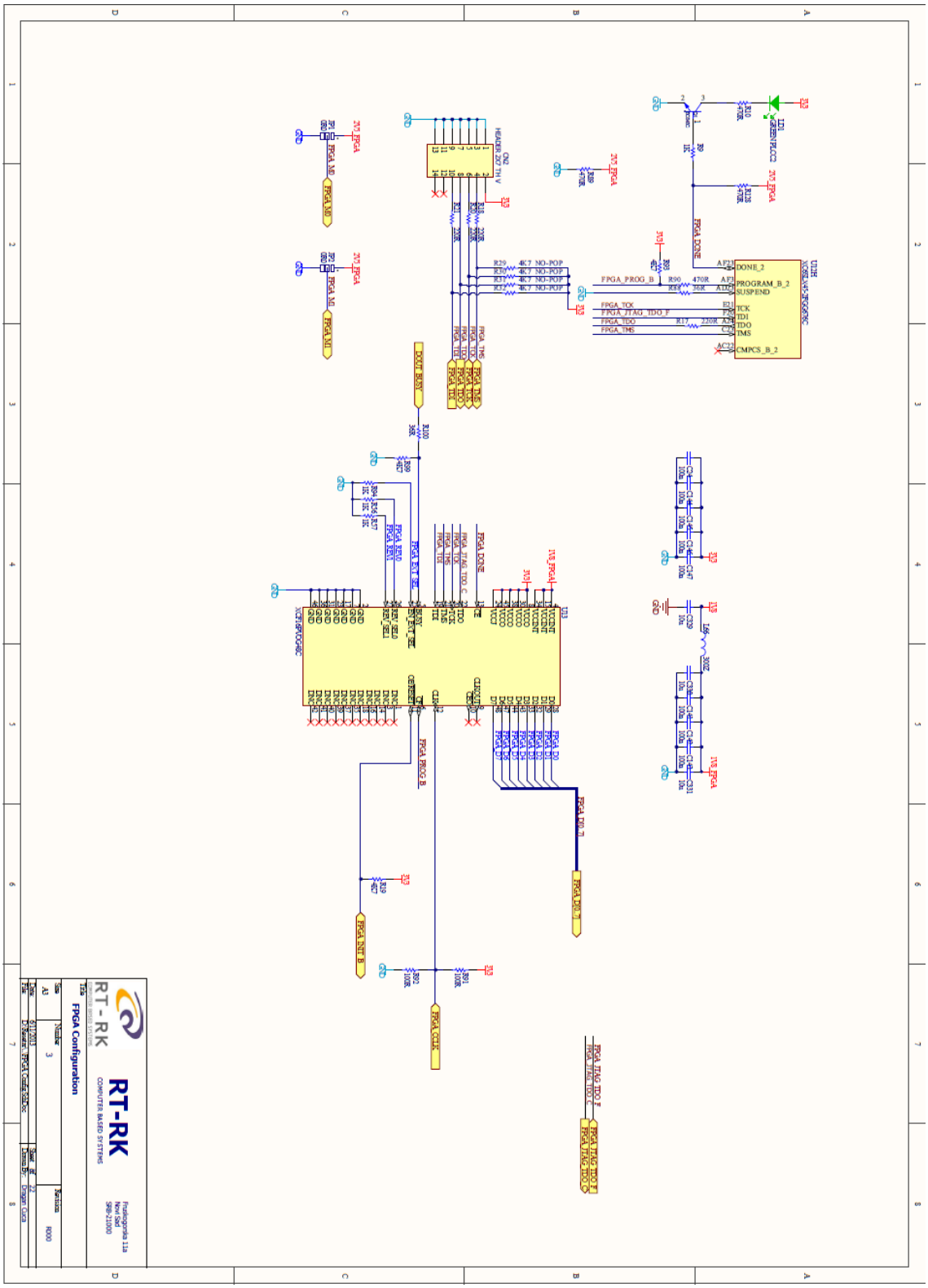
Appendix P – Xilinx FMC LPC Mezzanine Connection



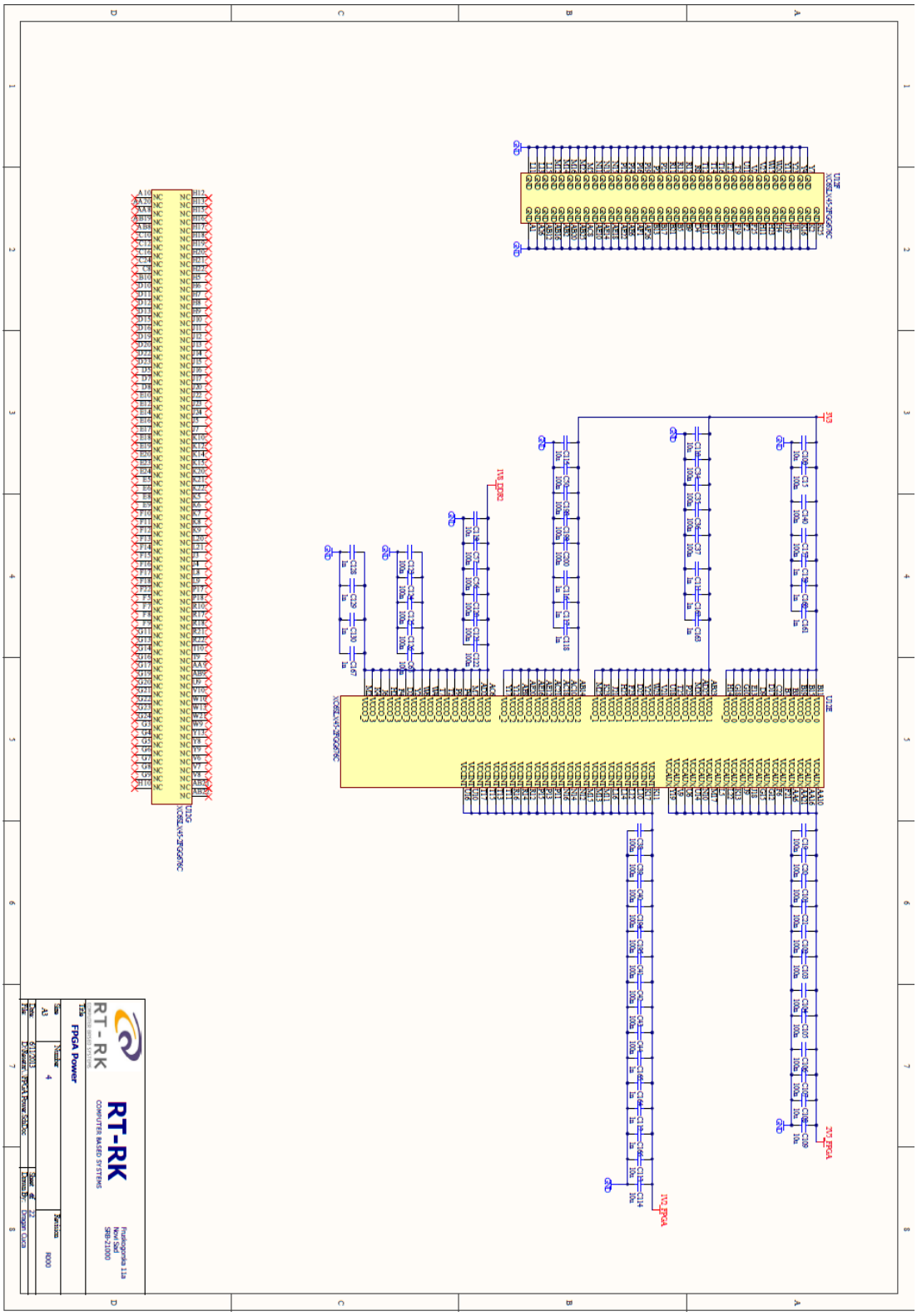
Appendix Q – FPGA Banks



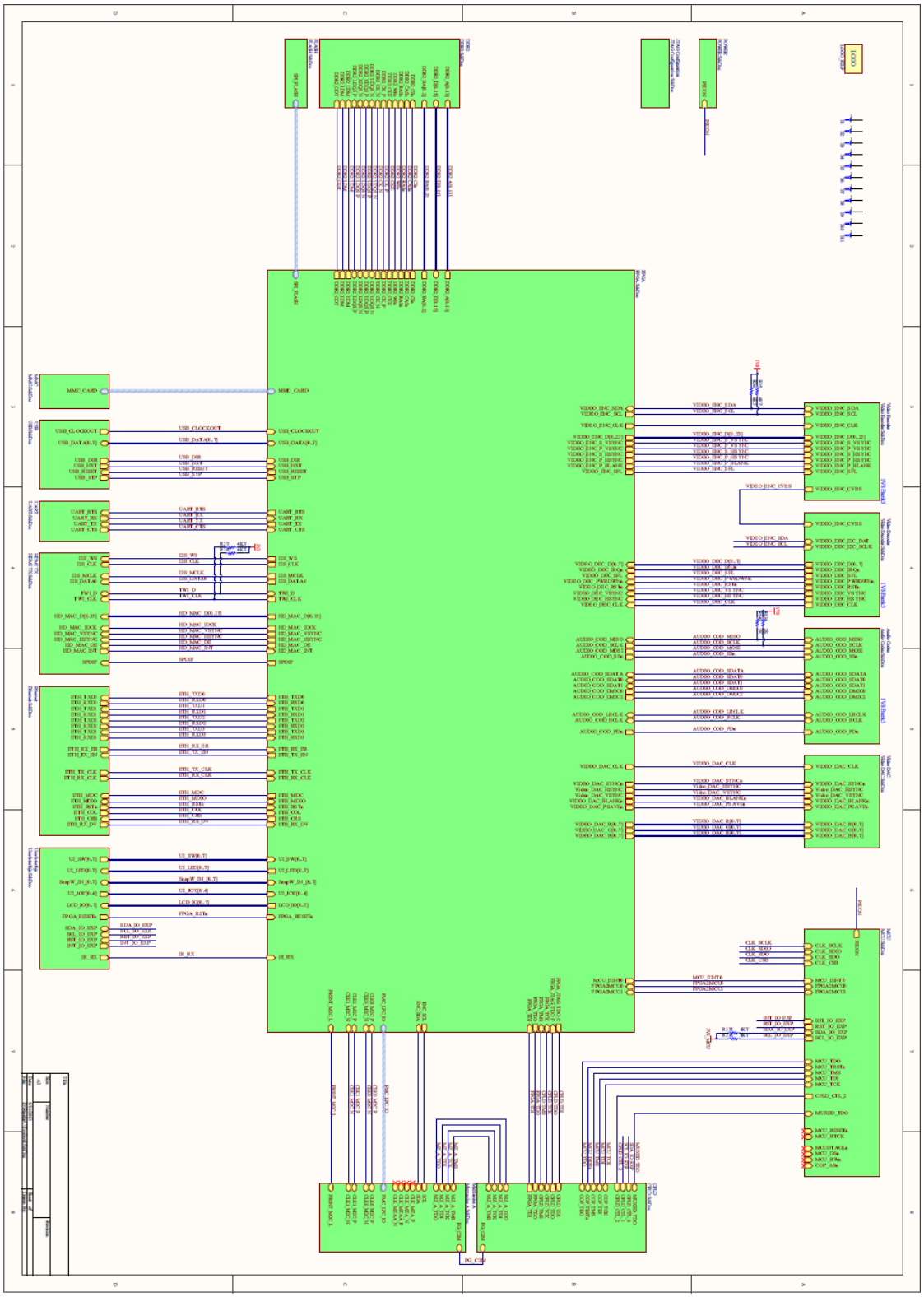
Appendix R – FPGA Platform Flash



Appendix S – FPGA Power



Appendix T – E2LP Base Board Top Level



Appendix U – Bill of Materials

Name	Description	Designator	Footprint	LibRef	Q.
KUCISTE CR2032	Batt Holder	B1	KEYSTON_2032	KUCISTE CR2032	1
10u	10u 6V3 X5R 0603	C1, C2, C4, C67, C84, C88, C98, C100, C108, C109, C110, C113, C114, C115, C119, C131, C133, C134, C139, C149, C151, C152, C158, C168, C174, C180, C181, C190, C211, C212, C214, C216, C217, C218, C219, C221, C223, C225, C226, C227, C228, C229, C230, C231, C233, C234, C236, C237, C249, C250, C253, C254, C261, C263, C272, C274, C289, C290, C293, C294, C297, C298, C301, C302, C305, C306, C307, C328, C329, C330, C331	CAPC1608X09N	10u	71
100n	100n 25V X5R CAPC1005X06	C3, C5, C6, C7, C8, C9, C10, C11, C15, C19, C20, C21, C32, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C50, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C68, C69, C76, C77, C78, C79, C80, C81, C82, C83, C85, C86, C87, C89, C90, C91, C99, C101, C102, C103, C104, C105, C106, C107, C120, C121, C122, C123, C124, C125, C126, C132, C135, C136, C137, C138, C140, C141, C142, C143, C144, C145, C146, C147, C150, C153, C154, C155, C157, C169, C170, C171, C175, C176, C178, C179, C182, C187, C188, C189, C191, C194, C195, C198, C199, C200, C206, C207, C208, C209, C210, C213, C215, C220, C222, C224, C232, C235, C244, C245, C246, C247, C248, C251, C252, C255, C256, C257, C258, C260, C262, C264, C265, C268, C269, C270, C271, C273, C275, C276, C279, C281, C283, C286, C287, C291, C295, C299, C303, C308, C309, C311, C318, C321, C332	CAPC1005X06N	100n	154
1u	1u 16V X5R 0603	C31, C127, C201, C238, C239, C242, C316, C327	CAPC1608X09N	1u	8
1n	1n 50V COG CAPC1005X06	C70, C71, C72, C73, C74, C75, C111, C112, C116, C117, C118, C128, C129, C130, C148, C156, C159, C160, C161, C162, C163, C164, C165, C166, C167, C173, C183, C243, C259, C277, C278, C280, C282, C292, C296, C300, C304, C312, C313, C314, C323, C324	CAPC1005X06N	1n	42
10n	10n 25V X7R 0402	C92, C93, C177, C184, C185, C186, C192, C193, C284, C317, C320	CAPC1005X06N	10n	11
270p	270p 50V X7R 0603	C94, C95	CAPC1608X09N	270p	2
22p	22p 50V NPO 0603	C96, C97, C196, C197, C204, C205, C266, C267, C285, C288, C322, C325, C326	CAPC1608X09N	22p	13
2p2	2p2 50V NP0 0402	C172, C240, C241	CAPC1005X06N	2p2	3
12p	12p 50V NP0 0402	C202, C203	CAPC1005X06N	12p	2
47u 16V	EL CAP 47uF 16V 6.6x5.5mm	CE1, CE2, CE3	CAPAE660X550N	47u 16V	3
100u 6V3	EL CAP 100uF 6.3V LESR 24mR 5.3x6.0mm	CE5, CE6, CE8, CE9	CAPAE530X600N	100u 6V3	4
470u 6.3V	EL CAP 470uF 6.3V 8.0x10.2mm	CE7	CAPAE800X1020N	470u 6.3V	1
CON SUBD9 F/15 F VGA	CON D-SUB Stacked R/A 2x15pos	CN1	Tyco_1734870-1	CON SUBD9 F/15 F VGA	1
HEADER 2X7 TH V	HEADER SHROUDED 2MM 2X7 TH V	CN2	MOLEX_87831142	HEADER 2X7 TH V	1
Stereo Jack 3.5mm	Stereo Jack 3.5mm Triple Stecked	CN3	Kycon_STX-4335-5BGP-S1	Stereo Jack 3.5mm	1

KLP42X-60-Y/Y	2 X RCA YELLOW/YELLOW Stacked P.J.	CN5	Kycon_KLP42X-60-Y/Y	KLP42X-60-Y/Y	1
RJ45+LED+MAG45	RJ45 JACK MAG45 LEDs	CN6	TYCO_5-6605758-1	RJ45+LED+MAG45	1
HDMI RA SM	Single HDMI CN RA SM	CN7	MOLEX_471511001	HDMI RA SM	1
USB B RA	USB B RA TH	CN8	MOLEX_670688001	USB B RA	1
SD Card	SD Card Socket	CN9	Molex_500998-0900	SD Card	1
PS 25/2G BR	HDR 1X2 2.54mm Vertical TH KK PS 25/2G BR	CN10	Reichelt_PS 25/2G BR	PS 25/2G BR	1
HDR2X10 RA 2.54mmP	HDR2X10 RA 2.54mmP	CN11, CN15	HDRRA_2X10	HDR2X10 RA 2.54mmP	2
CON DC SOCKET 2.1MM PCB	CN DC SOCKET 2.1MM RA TH	CN13	CLIFF_DC10A	CON DC SOCKET 2.1MM PCB	1
USB A RA TH	USB Type A RA TH	CN14	TYCO_292303-1	USB A RA TH	1
HDR2X5 RA 2.54mmP	HDR2X5 RA 2.54mmP	CN16	HDRRA_2X5	HDR2X5 RA 2.54mmP	1
ASP-134603-01	CON FMC LPC	CN17	ASP-134603-01	ASP-134603-01	1
IDC20 PCB V	IDC20 Header, 20-Pin, Dual row Straight 2.54mm	CON1	TYCO_2-1634688-0	IDC20 PCB V	1
ESDA6V1L	TVS Dual 6V1 300mW SOT-23	D1, D2, D3, D4, D5, D16	SOT95P245X150-3N	ESDA6V1L	6
SMCJ12A	TVS 12V 1500W Unidirectional SMC	D6	DIOM7959X27N SMC	SMCJ12A	1
B240-13-F	2A 40V Shottky SMB DO-214AA	D7, D8, D10, D11	DIOM4336X25N SMB DO-214AA	B240-13-F	4
1N4148	150mA 100V Small Signal DO-35	D9	DIOAD680W50L405D165A - DO-35	1N4148	1
PESD0603-240	TVS 45V 0603	D12, D13, D14, D15	INDC1608X10N	PESD0603-240	4
UCLAMP3301H	TVS 3V3 40W Unidirectional SOD532	D17, D18, D19, D20, D21, D22, D23, D24	SOD523	UCLAMP3301H	8
5A	5A 125Vac FAST OMNI BLOCK	F1	LITTELFUSE_154 xxx	5A	1
FUSE 2A	2A 125VAC FAST	F2, F3	LITTELFUSE_451/453 Series	FUSE 2A	2
HDR1X2	HDR 1x2 2.54mm Vertical TH	JMP1, JMP2, JMP3, JMP4, JMP5, JMP6, JMP7, JMP8, JMP9, JMP10, JMP11, JMP12, JMP13, JMP14, JMP15, JMP16, JMP17, JMP19	HDR1X2	HDR1X2	18
0R0	0R0 1% 0.063W RESC1608X06, Solder Jumper 3x0603	JP1, JP2, R11, R12, R13, R14, R15, R16, R142, R144	JMP_SOLDER_3, RESC1608X06N	0R0	10
300Z	FER 300Z 2A 0603	L1, L2, L3, L7, L8, L9, L10, L11, L12, L13, L14, L16, L19, L20, L21, L22, L23, L24, L25, L27, L29, L30, L31, L33, L35, L36, L37, L38, L39, L40, L41, L42, L45, L46, L47, L48, L49, L50, L51, L52, L53, L54, L55, L56, L57, L58, L64, L65, L66, L67, L68, L69, L70, L71	INDC1608X10N	300Z	55

10uH	IND 10uH 100mA 0805	L15, L17, L18, L59, L63	INDC2012X11N	10uH	5
4u7 2.4A	IND 4.7uH 2.4A 5.8x5.8mm	L26, L28, L32, L34	INDP5858X30N	4u7 2.4A	4
3.3uH 6A	IND 3.3uH 6A 7.3x6.6X3mm	L43, L44	INDP6868X30N	3.3uH 6A	2
GREEN PLCC2	GREEN 20mA 2V PLCC2	LD1, LD3, LD4, LD6	DIOM3528X21N GREEN	GREEN PLCC2	4
RED PLCC2	RED 20mA 2V PLCC2	LD2, LD5	DIOM3528X21N RED	RED PLCC2	2
BC848C	NPN 100mA 30V Hfe=110 SOT-23, TR BC848B SOT-23	Q1, Q2, Q6, Q7	SOT95P230X126-3N	BC848C	4
DMG6402LDM	N-Ch 5.3A 30V 27mR SOT-23-6	Q3, Q4	SOT95P280X145-6N	DMG6402LDM	2
MMBT2907A	PNP 800mA 60V Hfe=300 350mW SOT-23	Q5	SOT95P230X126-3N	MMBT2907A	1
2K	2K 1% 0.063W 0603	R1, R2, R96, R101, R102, R125, R134, R140, R187, R192, R197, R206, R207, R208, R219, R268	RESC1608X06N	2K	16
1K	1K 1% 0.063W 0603, 1K 1% 0.063W RESC1608X06	R3, R4, R9, R41, R54, R56, R57, R60, R73, R74, R75, R76, R84, R85, R87, R94, R137, R138, R141, R145, R149, R153, R162, R164, R165, R166, R168, R170, R172, R184, R193, R194, R227, R232, R234, R249, R255, R260, R261, R277, R279, R281, R283, R285, R287, R289, R291	RESC1608X06N	1K	47
10K	10K 1% 0.063W 0603	R5, R6, R7, R25, R33, R34, R58, R61, R81, R82, R83, R95, R98, R103, R105, R106, R107, R108, R109, R110, R111, R113, R116, R118, R119, R120, R121, R126, R129, R139, R143, R154, R160, R161, R169, R171, R186, R188, R189, R190, R191, R196, R198, R199, R200, R201, R202, R203, R209, R216, R217, R225, R250, R262, R267	RESC1608X06N	10K	55
47K	47K 1% 0.063W 0603	R8, R22, R23, R24, R59, R65, R66, R67, R68, R69, R70, R71, R72, R115, R155, R156, R157, R158, R159, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R204, R205, R210, R211, R213, R214	RESC1608X06N	47K	35
470R	470R 1% 0.063W 0603	R10, R89, R90, R128, R226	RESC1608X06N	470R	5
220R	220R 1% 0.0625W 50V 0402	R17, R18, R20, R21, R127, R133, R167, R173, R212, R270, R271, R272, R273, R274, R275, R276, R278, R280, R282, R284, R286, R288, R290, R292	RESC1005X04N	220R	24
4K7	4K7 1% 0.063W 0603, 4K7 1% 0.063W RESC1608X06	R19, R29, R30, R31, R32, R35, R36, R37, R38, R63, R64, R93, R99, R117, R130, R131, R132, R135, R136	RESC1608X06N	4K7	19
36R	36R 1% 0.063W 0603	R26, R27, R39, R40, R52, R53, R62, R79, R80, R88, R100, R123, R124, R146, R163, R228, R229, R230, R231, R265, R266	RESC1608X06N	36R	22
100R	100R 1% 0.0625W 50V 0402	R28, R55, R91, R92, R269	RESC1005X04N	100R	5
49R9	49R9 1% 0.063W 0603	R77, R78	RESC1608X06N	49R9	2
22K	22K 1% 0.063W 0603	R86, R185, R195	RESC1608X06N	22K	3
27K	27K 1% 0.1W 0603	R97, R112, R114, R215	RESC1608X06N	27K	4
1K69	1K69 1% 0.063W 0603	R104, R122, R233, R264	RESC1608X06N	1K69	4
1M	1M 1% 0.063W 0603	R218, R235	RESC1608X06N	1M	2
75R	75R 1% 0.063W 0603	R220, R221, R222, R223, R224	RESC1608X06N	75R	5

4K12	4K12 1% 0.063W 0603	R245, R246, R263	RESC1608X06N	4K12	3
169R	169R 1% 0.1W 0603	R251, R254	RESC1608X06N	169R	2
604R	604R 1% 0.1W 0603	R258, R259	RESC1608X06N	604R	2
20K ± 20% 250mW	20K ± 20% 250mW Turns=1 5x5x2.54mm SM	RP1	BI Technologies_23B	20K ± 20% 250mW	1
B3F-1000	6X6 V 4.5mm Omron	SW2	SW_OMRON B3F_1000	B3F-1000	1
SW	SW ROCKER SPST Panel Maunt 125Vac 16A	SW3		SW	1
TH 1.6mm	Round Hole 1mm, Pad 1.5mm	TP1, TP7, TP8, TP9, TP10, TP11	TP160	TH 1.6mm	6
SM 1.8mm	Round Pad 0.8mm	TP3, TP4, TP5	SM TP80	Visible	3
ADAU1772	Audio ADC/DAC 24-bit 40QFN	U1	QFN50P600X600X100-40M	ADAU1772	1
PCA9306DCUTE4	I2C BUS VOLTAGE-LEVEL TRANSLATOR, 1.2V-7V 8TSSOP	U2, U4	TSSOP50P310X90-8N	PCA9306DCUTE4	2
AD8062ARZ	300MHz Dual Rail-to-Rail OPAMP 8SOIC	U3	SOIC127P600X175-8N	AD8062ARZ	1
AT24C32D	EEPROM I2C 32Kbit 8SOIC	U5	SOIC127P600X175-8N	AT24C32D	1
XC9572XL	CPLD 1.6K 72MCELL 64-VQFP	U7	TSQFP50P1200X1200X120-64N	XC9572XL	1
DVIULC6-2M6	ESD protection 6V Breakdown 6SON	U8, U17	SON50P145X100X65-6N	DVIULC6-2M6	2
MT47H128M16HG-37E	2Gb 16 Meg x 16 x 8 banks DDR2 SDRAM	U9	BGA84C80P15X9_1400X1150X120	MT47H128M16HG-37E	1
WJLXT972	ETHERNET PHY 10/100 48QFN	U10	TSQFP50P900X900X160-48N	WJLXT972	1
MX25L25635EMI-12G	FLASH SPI 256MBIT 16SOIC	U11	SOIC127P1030X265-16N	MX25L25635EMI-12G	1
XC6SLX45-2FGG676C	Spartan-6 LX45 676-BGA 1mmP	U12	BGA676C100P26X26_2700X2700X260	XC6SLX45-2FGG676C	1
XCF16PVOG48C	FLASH 16Mbit 1.8V 48TSSOP	U13	TSSOP50P2000X120-48N	XCF16PVOG48C	1
ADV7511	HDMI 1.4 Transmitter 64LQFP	U14	TSQFP50P1200X1200X120-64N-EP	ADV7511	1
IP4776CZ38	HDMI ESD protection TSSOP38	U15	TSSOP50P640X110-38M	IP4776CZ38	1

LPC2144FBD64	ARM7 16/32-Bit Microcontroller, 512KB Flash, 32KB RAM (+8KB USB DMA shared), 2KB USB RAM, 64-Lead LQFP	U16	TSQFP50P1200X1200X120-64N	LPC2144FBD64	1
DS2401	Silicon Serial Number TO92	U18	TO92	DS2401	1
LM4041DIM3-ADJ	Precision Micropower Shunt Voltage Reference	U19, U31, U34	SOT95P237X112-3N	LM4041DIM3-ADJ	3
MP65151DJ	Current Limiter 1.5A 5V SOT23-6	U20, U28	SOT95P280X145-6N	MP65151DJ	2
ADP2301AUJZ	BUCK 1.2A, 20V, 1.4MHz 6TSOT	U21, U22, U23, U24	SOT95P280X145-6N	ADP2301AUJZ	4
ADP2381AREZ	BUCK 6A, 20V, up to 1.4MHz TSSOP16	U25, U26	TSOP65P640X120-16N_HS_ADP	ADP2381AREZ	2
ADM3232EARNZ	RS232 Driver-Receiver 3V-5.5V 16SOIC	U27	SOIC127P600X175-16N	ADM3232EARNZ	1
USB3300-EZK	USB Host High Speed , OTG PHY	U29	QFN50P500X500X100-32M	USB3300-EZK	1
ADV7125	Video DAC 8-bit 48QFP	U30	TSQFP50P900X900X160-48N	ADV7125	1
ADV7180	Video Decoder SDTV 40QFN	U32	QFN50P600X600X100-40M	ADV7180	1
ADV7343	Video Encoder 64QFP	U33	TSQFP50P1200X1200X120-64N	ADV7343	1
SN74LVC4245APW	Octal Bus Transceiver And Shifter (3-State)	U35	TSOP65P640X120-24N	SN74LVC4245APW	1
TCA6416APWR	I/O EXPANDER, I2C 16-bit	U36	TSOP65P640X120-24N	TCA6416APWR	1
SN74LVC244APWR	Octal Buffer and line Drivers	U37	TSOP65P640X120-20N	SN74LVC244APWR	1
12.288MHz	12.2880MHz 3V3 ±50ppm 7x5x1.3mm	X1, X4	CWX8x3 7.0x5.0x1.3	12.288MHz	2
50MHz	OSC 50 MHZ 3.3V LVDS	X2	Connor_5.13x7.62x2.54	50MHz	1
25MHz	25.000MHz 18pF ±20ppm 5x3.2x1.3mm	X3	ABM3 5X3.2X1.3	25MHz	1
32.768kHz	32.768KHz 12.5pF ±20ppm 3.2x1.5x0.9	X5	FC-135 3.2x1.5x0.9	32.768kHz	1
24MHz	24.000MHz 18pF ±50ppm 11.5x5x4.5mm	X6, X8	XTAL1150X490X450	24MHz	2
27MHz	27.000MHz 3V3 ±20 ppm 7x5x1.8mm	X7, X10	ABRACON_ASV 7.0x5.0x1.8	27MHz	3

28.63636MHz	28.63636MHz 10pF ±10ppm 5x3.2x1.1mm	X9	ABM3B 5X3.2X1.1	28.63636MHz	1