Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

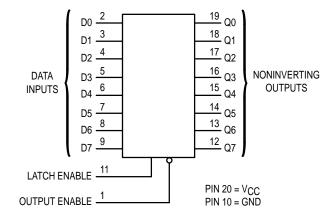
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HCT373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC573A is the noninverting version of the HC563A.

- · Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	54.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	рЈ

^{*} Equivalent to a two-input NAND gate.

MC54/74HC573A



J SUFFIX

CERAMIC PACKAGE CASE 732-03



N SUFFIX

PLASTIC PACKAGE CASE 738-03



DW SUFFIX

SOIC PACKAGE CASE 751D-04



DT SUFFIX

TSSOP PACKAGE CASE 948E-02

ORDERING INFORMATION

MC54HCXXXAJ Ceramic MC74HCXXXAN Plastic MC74HCXXXADW SOIC MC74HCXXXADT TSSOP

PIN ASSIGNMENT

			1
OUTPUT C	1 ●	20	□ vcc
D0 [2	19	D Q0
D1 [3	18	Q1
D2 [4	17	Q2
D3 [5	16	Q 3
D4 [6	15	Q4
D5 [7	14] Q5
D6 [8	13	D Q6
D7 [9	12] Q7
GND [10	11	LATCH ENABLE

FUNCTION TABLE

	Inputs		
Output Enable	Latch Enable	D	Ø
L	Н	Н	Н
L	Н	L	L
L	L	Х	No Change
Н	Χ	Х	Z

X = Don't Care Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
l _{in}	DC Input Current, per Pin	± 20	mA
l _{out}	DC Output Current, per Pin	± 35	mA
ICC	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq VCC. Unused inputs must always be tied to an appropriate logic voltage

level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

TSSOP Package: -6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
VCC	DC Supply Voltage (Referenced to GND)			6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)			Vcc	V
T _A	Operating Temperature, All Package Type	s	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter	Test Conditions	v _{CC}	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ l_{out} \le 20 \mu\text{A}$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
VIL	Maximum Low–Level Input Voltage	$V_{out} = 0.1 \text{ V or V}_{CC} - 0.1 \text{ V}$ $ l_{out} \le 20 \mu\text{A}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1 8	0.5 0.9 1.35 1.8	٧
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	٧
		$V_{in} = V_{IH} \text{ or } V_{IL} \qquad I_{out} \le 2.4 \text{mA} \ I_{out} \le 6.0 \text{ mA} \ I_{out} \le 7.8 \text{ mA}$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

^{*} Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

[†]Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter	Test Conditions	V _{CC}	– 55 to 25°C	≤ 85 °C	≤ 125°C	Unit
VOL	Maximum Low–Level Output Voltage	$V_{Out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{Out} \le 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$\begin{aligned} V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} & & I_{\text{Out}} \leq 2.4 \text{mA} \\ & I_{\text{Out}} \leq 6.0 \text{ mA} \\ & I_{\text{Out}} \leq 7.8 \text{ mA} \end{aligned}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
l _{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
loz	Maximum Three–State Leakage Current	Output in High-Impedance State Vin = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	- 0.5	- 5.0	- 10	μА
lcc	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND II _{out} I = 0 μA	6.0	4.0	40	160	μА

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

			Guaranteed Limit			
Symbol	Parameter	V _{CC}	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
tPLH, ^t PHL	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 3.0 4.5 6.0	150 100 30 26	190 140 38 33	225 180 45 38	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 3.0 4.5 6.0	160 105 32 27	200 145 40 34	240 190 48 41	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
^t PZL [,] ^t PZH	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t _{TLH} , tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 3.0 4.5 6.0	60 27 12 10	75 32 15 13	90 36 18 15	ns
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedan	ce State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V _{CC} = 5.0 V	
C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	23	pF

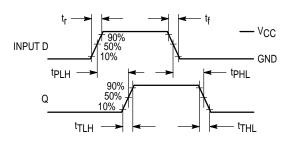
^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

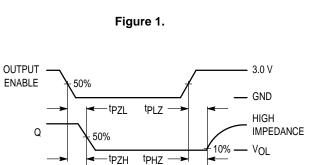
MC54/74HC573A

TIMING REQUIREMENTS ($C_L = 50 \text{ pF}$, Input $t_f = t_f = 6.0 \text{ ns}$)

				Guaranteed Limit						
			VCC	– 55 to	25°C	≤ 8	5°C	≤ 12	25°C	
Symbol	Parameter	Fig.	Volts	Min	Max	Min	Max	Min	Max	Unit
t _{su}	Minimum Setup Time, Input D to Latch Enable	4	2.0 3.0 4.5 6.0	50 40 10 9.0		65 50 13 11		75 60 15 13		ns
^t h	Minimum Hold Time, Latch Enable to Input D	4	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t _W	Minimum Pulse Width, Latch Enable	2	2.0 3.0 4.5 6.0	75 60 15 13		95 80 19 16		110 90 22 19		ns
t _r , t _f	Maximum Input Rise and Fall Times	1	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS





– Vон

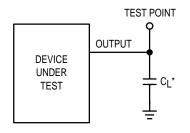
HIGH IMPEDANCE

90%-

Figure 3.

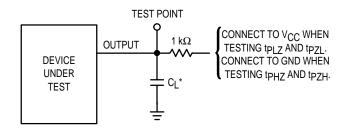
1.3 V

Q



* Includes all probe and jig capacitance

Figure 5. Test Circuit



* Includes all probe and jig capacitance

Figure 6. Test Circuit

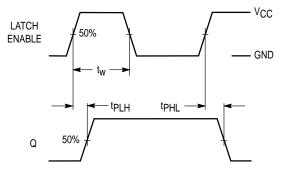


Figure 2.

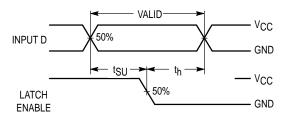
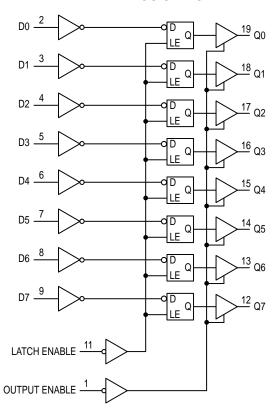
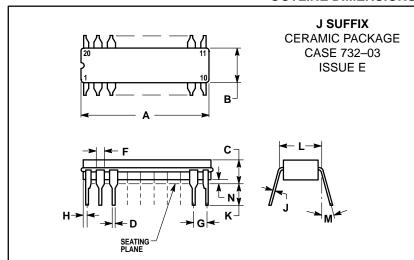


Figure 4.

EXPANDED LOGIC DIAGRAM

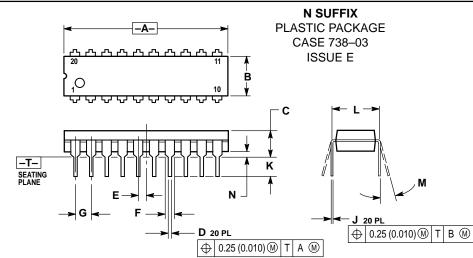


OUTLINE DIMENSIONS



- LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE
 POSITION AT SEATING PLANE, AT MAXIMUM
 MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSIONS A AND B INCLUDE MENISCUS.

	MILLIN	METERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	23.88	25.15	0.940	0.990	
В	6.60	7.49	0.260	0.295	
O	3.81	5.08	0.150	0.200	
D	0.38	0.56	0.015	0.022	
F	1.40	1.65	0.055	0.065	
G	2.54	BSC	0.100	BSC	
Η	0.51	1.27	0.020	0.050	
L	0.20	0.30	0.008	0.012	
K	3.18	4.06	0.125	0.160	
Г	7.62	BSC	0.300	BSC	
М	0 °	15°	0°	15°	
N	0.25	1.02	0.010	0.040	



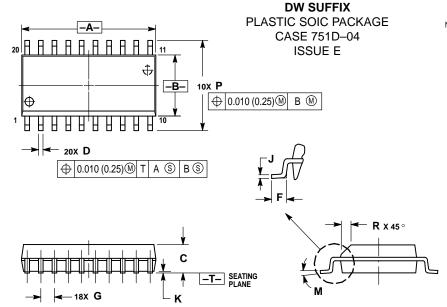
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION L TO CENTER OF LEAD WHEN

- FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD

	INC	HES	MILLIMETER			
DIM	MIN	MAX	MIN	MAX		
Α	1.010	1.070	25.66	27.17		
В	0.240	0.260	6.10	6.60		
C	0.150	0.180	3.81	4.57		
D	0.015	0.022	0.39	0.55		
Е	0.050	BSC	1.27	BSC		
F	0.050	0.070	1.27	1.77		
G	0.100	BSC	2.54	BSC		
J	0.008	0.015	0.21	0.38		
K	0.110	0.140	2.80	3.55		
L	0.300	BSC	7.62	BSC		
M	0°	15°	0°	15°		
И	0.020	0.040	0.51	1.01		



- OTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

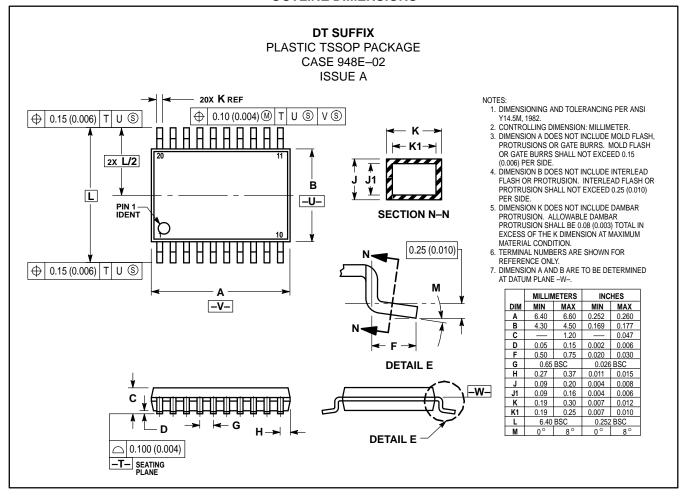
 4. MAXIMUM MOLD PROTRUSION 0.150

- (0.006) PER SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	12.65	12.95	0.499	0.510
В	7.40	7.60	0.292	0.299
С	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
М	0 °	7 °	0 °	7°
Р	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS



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