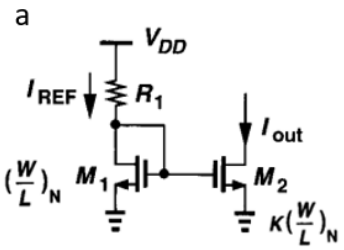
Tutorial 9 solutions
EE204: Analog Circuits

Dept of Electrical Engineering, IITB
Autumn Semester 2023

Q1.

A Derive expressions for **Iout** in the following 3 cases

a



Since VGS of M1 is equal to M2, Iout=K*Iref

$$V_{D1} = V_{G1} = Vdd - I_{ref}R_1 = \sqrt{\frac{2I_{ref}}{\frac{\mu_n C_{ox} W}{L}}} + V_{th}$$

Above equation gives a quadratic equation in Iref, solving for Iref gives

$$I_{ref} = \frac{Vdd - V_{th}}{R_1} + \frac{1}{\frac{\mu_n C_{ox} W}{L} R_1^2}\left(1 \pm \sqrt{1 + 2(Vdd - V_{th})R_1 \frac{\mu_n C_{ox} W}{L}}\right)$$

The Iref with Positive sqrt term is discarded as the Drop across Mosfet falls below Vth

So

$$I_{ref} = \frac{Vdd - V_{th}}{R_1} + \frac{1}{\frac{\mu_n C_{ox} W}{L} R_1^2}\left(1 - \sqrt{1 + 2(Vdd - V_{th})R_1 \frac{\mu_n C_{ox} W}{L}}\right)$$

$$I_{out} = K * I_{ref} = \frac{K(Vdd - V_{th})}{R_1} + \frac{K}{\frac{\mu_n C_{ox} W}{L} R_1^2}\left(1 - \sqrt{1 + 2(Vdd - V_{th})R_1 \frac{\mu_n C_{ox} W}{L}}\right)$$

B Derive expressions for **Iout**

From PMOS current mirror , VGS4=VGS3 so Iref=Iout

Let Iref=Iout=I

VG1=VG2

$$\sqrt{\frac{2I}{K_n}} + Vth1 + Vs1 = \sqrt{\frac{2I}{K*K_n}} + Vth2 + Vs2$$

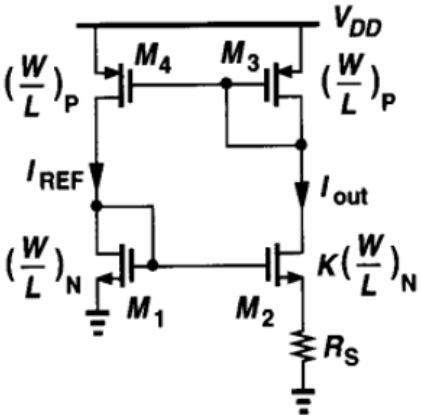
Vth1=Vth2, Vs1=0, Vs2=IRs

$$\sqrt{\frac{2I}{K_n}} = \sqrt{\frac{2I}{K*K_n}} + IR_s$$

$$\sqrt{\frac{2}{K_n}}\left(1 - \frac{1}{\sqrt{K}}\right) = \sqrt{I}\,R_s$$

$$I = \frac{2}{K_n R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

b



C Derive expressions for **Iout**

From PMOS current mirror , VGS4=VGS3 so Iref=Iout

Let Iref=Iout=I

VG1=VG2+IRs

$$\sqrt{\frac{2I}{K_n}} + Vth1 + Vs1 = \sqrt{\frac{2I}{K*K_n}} + Vth2 + Vs2 + IR_s$$

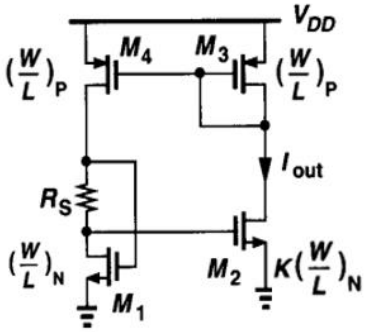
Vth1=Vth2, Vs1=Vs2=0

$$\sqrt{\frac{2I}{K_n}} = \sqrt{\frac{2I}{K*K_n}} + IR_s$$

$$\sqrt{\frac{2}{K_n}}\left(1 - \frac{1}{\sqrt{K}}\right) = \sqrt{I}\,R_s$$

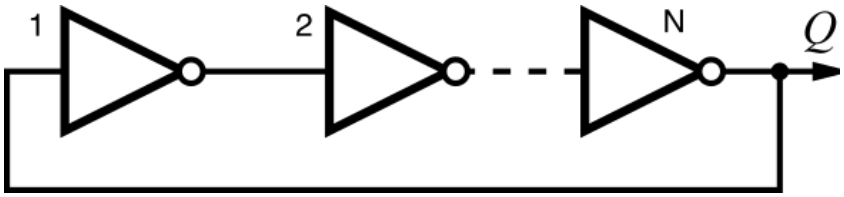
$$I = \frac{2}{K_n R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

C



Q2.

Calculate the number of Inverters in the ring oscillator to achieve the frequency of 0.8 GHz, given the T_{dHL}=20pS, T_{dLH} =30pS. Also, can 1GHz be generated with given delay times?



Timeperiod T = N(T_{dHL+} T_{dLH})= N*50pS

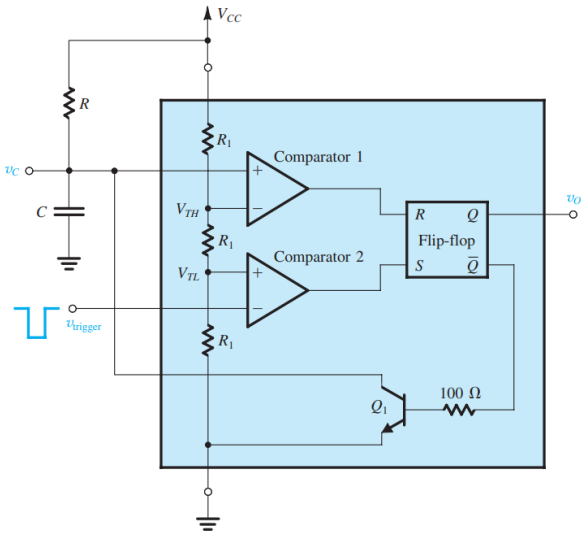
$\Longrightarrow$ 0.8GHz = 1/T =1/(N*50pS)

$\Longrightarrow$ N=25

For a frequency of 1GHz, N turns out to be 20. For N= even , the setup acts as a memory instead of oscillator , so cant generate 1GHz

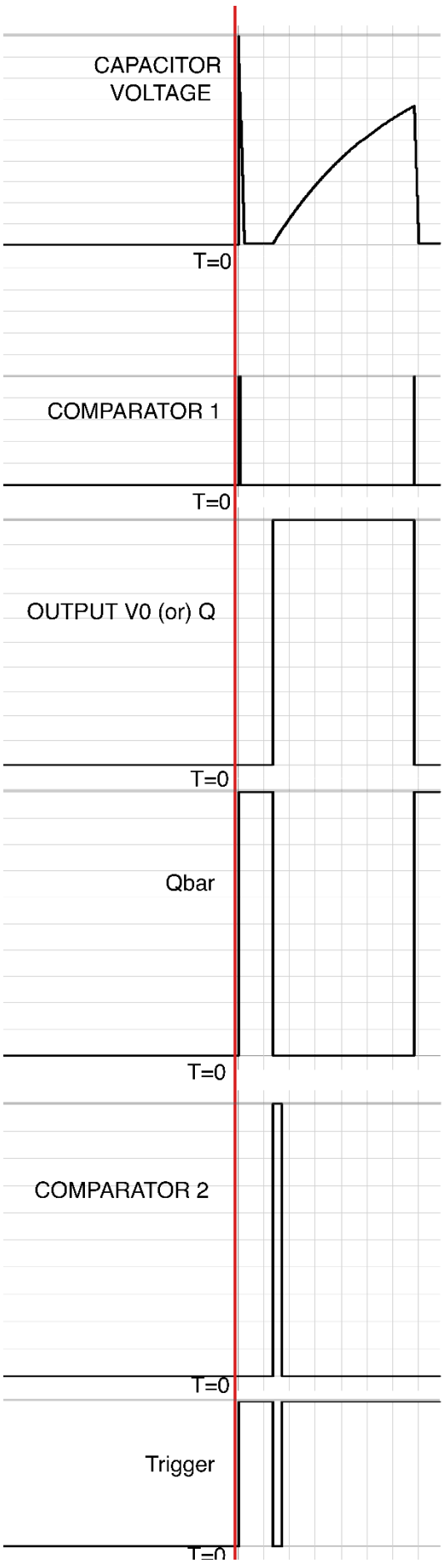
Q3.

Using a 10-nF capacitor C, find the value of R that yields an output pulse of 100 µs in the monostable circuit. Sketch the waveforms of Vc, Vo, Vtrigger, the output of comparators, and RS flipflop, assuming that capacitance is initially charged to Vcc.



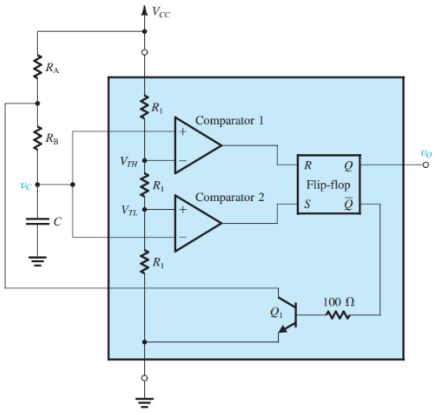
Pulse duration = Capacitance charging time from 0 v to 2/3 VCC = RCln(3)

$\Longrightarrow$R=100u/(10n*ln3)=10*1000/ln(3)=9.1Kohm


CAPACITOR
VOLTAGE
T=0
COMPARATOR 1
T=0
OUTPUT V0 (or) Q
T=0
Qbar
T=0
COMPARATOR 2
T=0
Trigger
T=0

Q4.

For the given circuit, find the values of RA and RB that result in an oscillation frequency of 100 kHz and a duty cycle of 75%, given C= 1-nF. Also, Sketch the waveforms of Vc, Vo



TH = capacitance charging time from 1/3 vcc to 2/3 vcc through RA and RB =C(RA+RB)*ln2

TL = capacitance charging time from 2/3 vcc to 1/3 vcc through RB =C*RB*ln(2)

Dutycycle = TH/(TH+TL)=[RA+RB]/[RA+2RB] = 3/4 (75%)

⟹RA=2RB

For 75% dutycycle of 100Khz wave the TL = ¼*10 uS

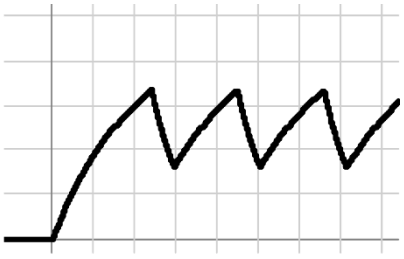
⟹ C*RB*ln(2)=10/4 u

⟹ 1n*RB*ln(2)=10/4 u

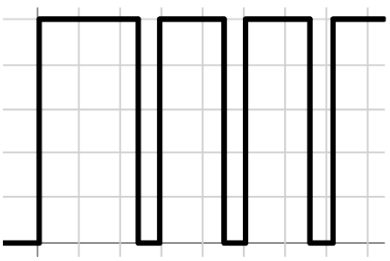
⟹RB=10 *1000 /(4*ln2)= 3606.73= 3.6 kohm

RA=2*RB=7.2 kohm

Max=2VDD/3 V
Min=VDD/3 V
capacitor, 1 nF

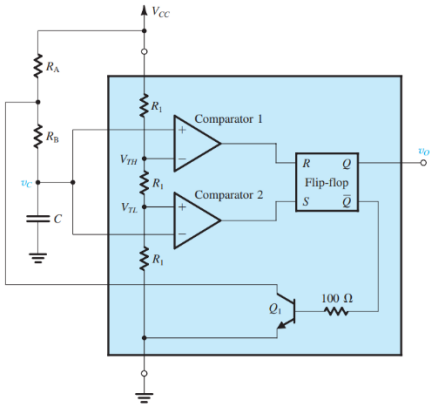


Max=VDD
Duty cycle 75%
output



Q5

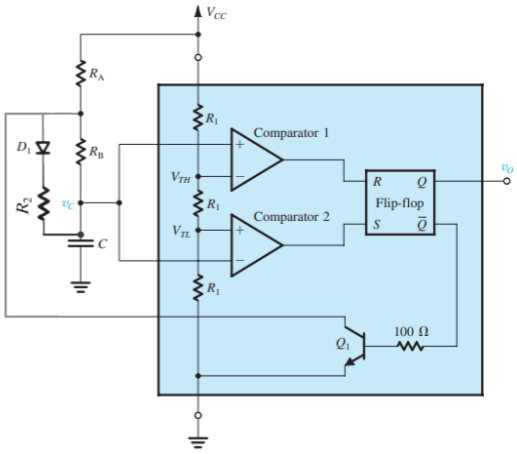
What is the minimum possible duty cycle with this configuration?



Dutycycle = TH/(TH+TL)=[RA+RB]/[RA+2RB]

Minimum possible duty cycle is 50% (when RA is much smaller than RB)

The following modification is made to the above circuit, Assume a diode is ideal, now derive the expression for the duty-cycle in terms of resistances Ra, Rb,R2.



During the charging process, the diode acts as short and Rb is parallel to R2

Hence the charging process happens through RA + (RB||R2)

Discharge through RB , diode blocks current through R2

So Dutycycle $= \frac{\text{TH}}{\text{TH+TL}} = \frac{\text{RA+RB||R2}}{\text{RA+RB+RB||R2}}$

Note that this duty cycle has no min limit as before (by chosing large enough Rb and small R2 one can less than 50% dutycycle)