EE204 : Analog Circuits
Dept of Electrical Engineering
IIT Bombay
Autumn Semester 2023

Assignment 2
Total Marks: 10
Submission Deadline: 11:59 p.m., 26-08-2023
Mode of Submission: Scan your assignment and upload on Moodle as a single pdf file.

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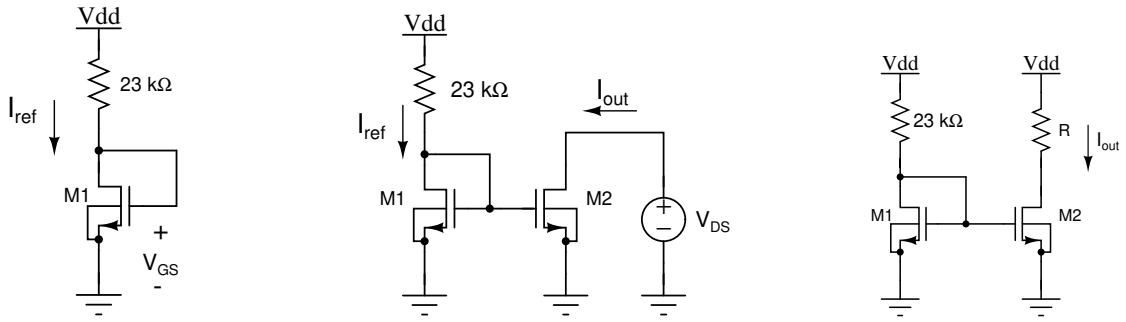
1. For the circuit shown in Figure 1, $V_{dd} = 1.8\,V$, $\mu_n C_{ox} = 260\mu A/V^2$, $V_t = 0.4\,V$, $\frac{3\mu m}{0.5\mu m} < \left(\frac{W}{L}\right)_1 < \frac{5\mu m}{0.5\mu m}$ (Choose any aspect ratio in this range).

   (a) Find V_{GS} of transistor M1 for the Figure 1(a). (1.5 Marks)

   (b) The circuit in Figure 1(b) is 1:1 current mirror, Plot I_{out} v/s V_{DS} for two lengths of M2, $(L_2)_1 = 0.5\,\mu m$ and $(L_2)_2 = 1\,\mu m$ (keeping aspect ratio same as Q1(a)) and write the approximate value of slope in saturation and ohmic region, given that $\lambda = 0.025\,V^{-1}$ for $L_2 = 1\,\mu m$ and $\frac{d\lambda}{dL} = -0.05\,V^{-1}/\mu m$ for $L \leq 1\mu m$. (1.5 Marks)

   (c) The circuit in Figure 1(c) is 1:1 current mirror, Find the region of operation of M2 and I_{out} for $R = 20\,k\Omega$ and $R = 40\,k\Omega$. (2 Marks)



(a) (b) (c)

Figure 1: Circuits for Q1

2. Refer to Figure 2 and answer the following questions:

   (a) What should be the value of R2 such that I_{load} is independent of R_1. Given that $R_1 = 1\,k\Omega$, $R_3 = 1\,k\Omega$, $R_4 = 9\,k\Omega$, $A = 100$? (1.5 Marks)

   (b) Derive the expression for the I_{load}, if R_3 reduces by $a\%\,(0 < a \leq 5)$ and R_2 increases by $b\%\,(0 < a \leq 4)$. Then specify the condition for worst-case error in the load current.(2.5 Marks)

   (c) Use the worst-case values you obtained in Q2(b) and calculate the numerical value of the error in the worst-case condition (Choose a reasonable value of V_{ctrl}).(1 Mark)

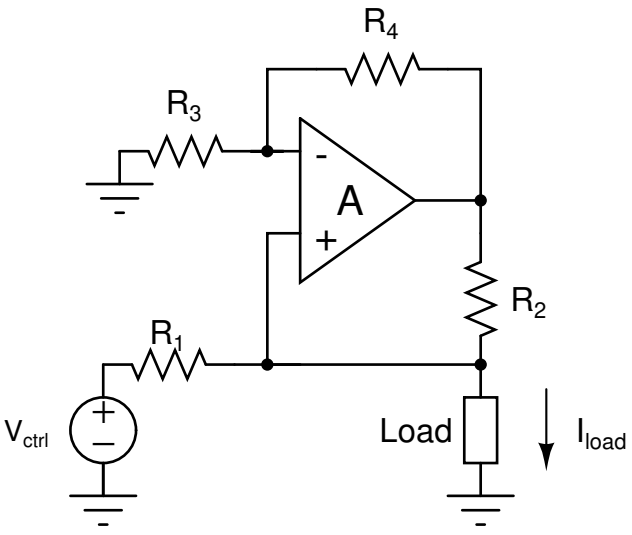


Figure 2: Circuit for Q2