

EE204: Analog Circuits

Tutorial 5

Dept. of Electrical Engineering, IIT Bombay

Autumn Semester 2023

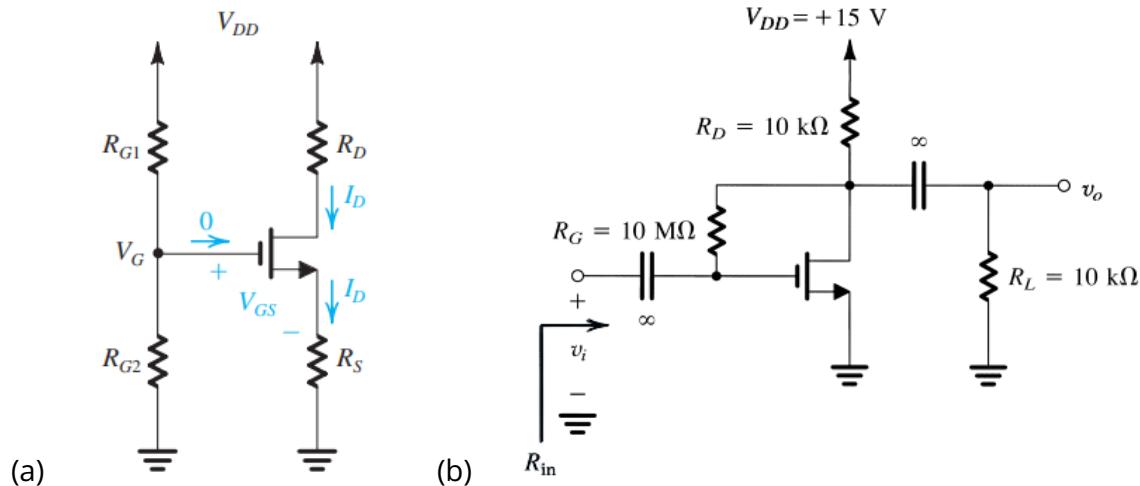
13-09-2023

Q1.

In Figure a, The MOSFET is specified to have $V_t = 1$ V and $k_nW/L = 1$ mA/V². Assume $\lambda = 0$, $V_{DD} = 15$ V, $R_s = R_d = 10$ kΩ.

(a) Bias the circuit so that the DC drain current is $I_D = 0.5$ mA.

(b) Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having $V_t = 1.5$ V for the same bias conditions.



Q2.

For the circuit shown in Figure b, Determine the following

- Drain current,
- small-signal voltage gain
- input resistance,
- largest allowable input signal

Given , $V_{DD} = 15$ V, $R_D = 10$ kΩ, $k_n = 0.25$ mA/V² , and $V_t = 1.5$ V, $g_0=21.2\mu\text{S}$.

Q3.

The NMOS transistor-based amplifier, shown in the figure below, Given $V_t = 0.7$ V.

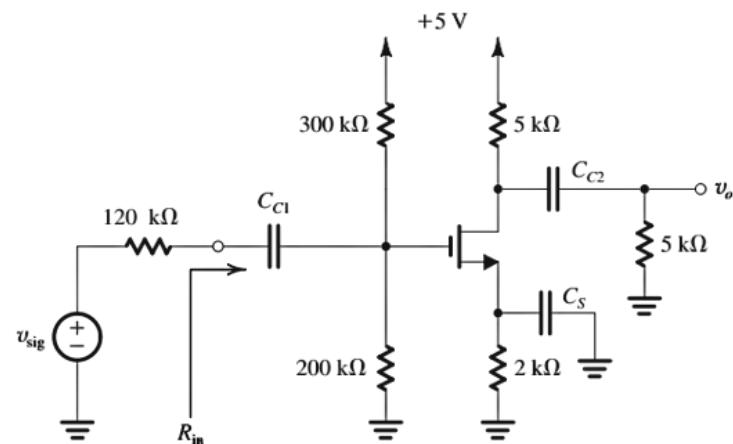
- (a) Neglecting the Early effect, verify that the MOSFET is operating in saturation with $ID = 0.5$ mA and $V_{OV} = 0.3$ V.

What must the MOSFET's k_n be? What is the DC voltage at the drain?

- (b) Find R_{in} , g_m and V_o/V_{sig} (assume $g_0=10\mu S$)

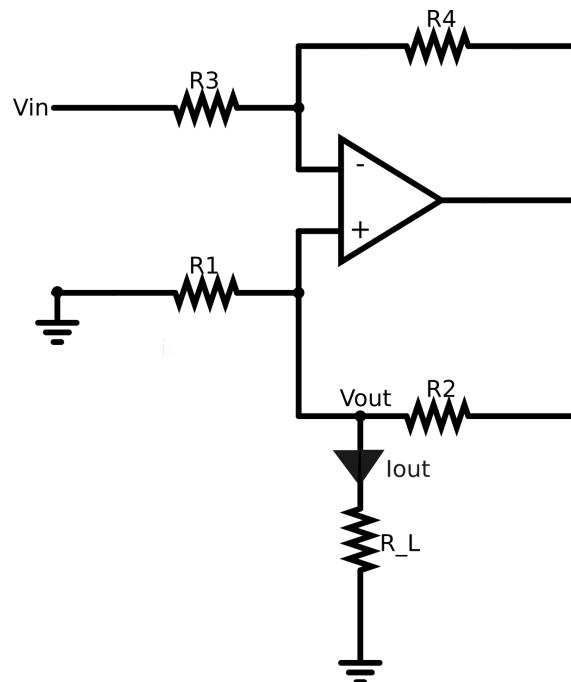
(c) If v_{sig} is a sinusoid with a peak amplitude 'x', find the maximum allowable value of 'x' for which the transistor remains in saturation. What is the corresponding amplitude of the output voltage?

(d) What is the value of resistance R_s that needs to be inserted in series with capacitor C_S in order to allow us to double the input signal 'x'? What output voltage now results?

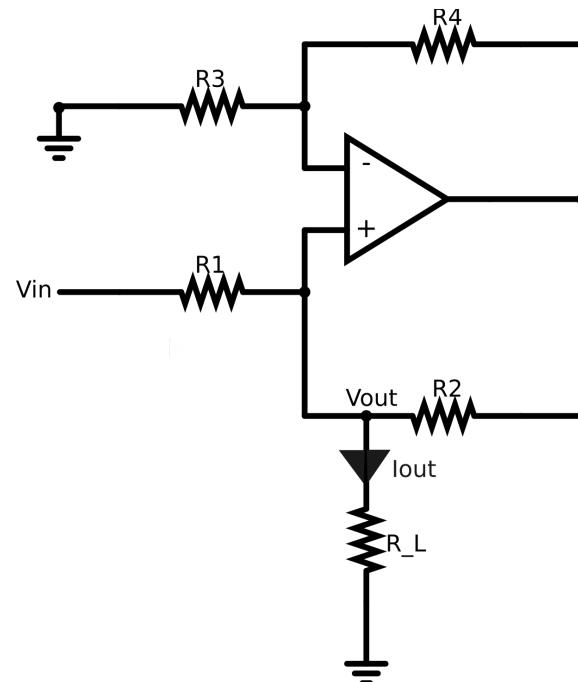


Q4.

- i. Consider the circuits given below with ideal opamps to evaluate the expression of I_{out} in terms of V_{in} and V_o (and resistances).



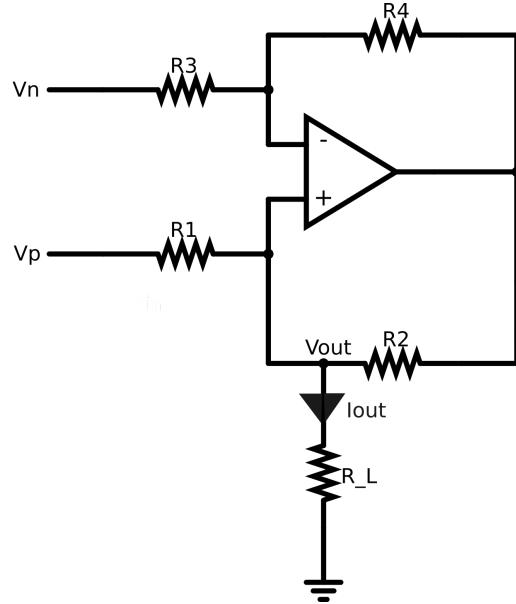
(a)



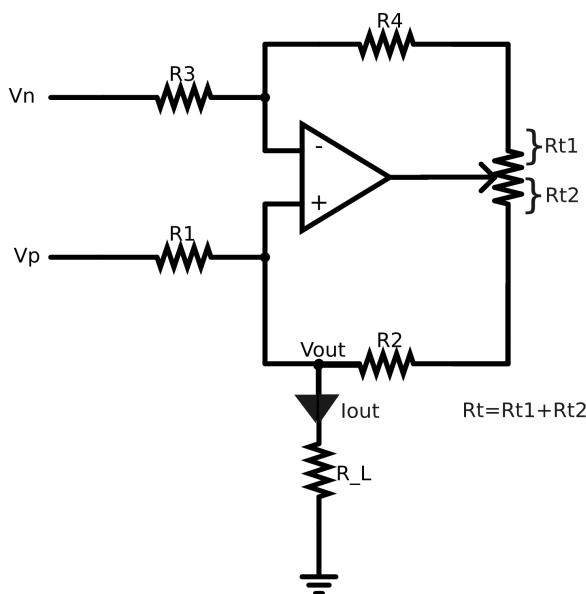
(b)

ii. For the above circuits to be current sources Driving **Iout** into Load(R_L) from Node **Vout**, Derive the constraints on the resistances and also evaluate **Iout** values with these constraints.

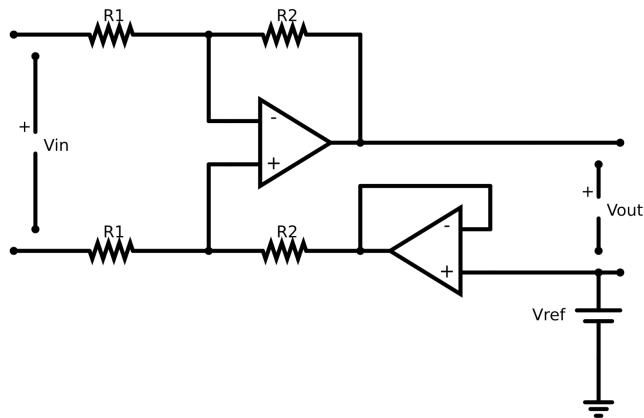
iii. Using the principle of superposition, find the **Iout** of the following circuit using the results from part ii.



iv. In the figure below, If $R_1 = 9.8K$, $R_2 = 9.9K$, $R_3 = 10.3K$, $R_4 = 10.1K$, what should be the trimming resistors setting (R_{t1} , R_{t2}) to obtain maximum output resistance for this Howland Current Source. Given $R_t = 5K$ Ohm



V. Consider a diff amp with the following modifications



Find an expression for V_{out} . Comment on how it changes with V_{ref} .

A resistance R is now connected between output terminals; comment on the current through This resistance R and V_{ref} when V_{in} is kept constant, and V_{ref} is varied.

Solutions

Q1 a

Biassing is used to set the quiescent point to fix the drain current of the transistor in this single-transistor amplifier circuits.

Since ID required is 0.5mA , we can find VD and VS from the RD and RS Ir drops.

$$V_{DD} = R_D I_D + V_D \quad , \quad V_S = I_D R_S$$

$$\Rightarrow V_D = 10V \text{ and } V_S = 5V$$

We need to find the VG Such that ID = 0.5MA

$$I_D = \frac{1}{2} \times 1 \times V_{GST}^2 \text{ mA}$$

$$0.5 = \frac{1}{2} \times 1 \times V_{GST}^2$$

$$V_{GST} = 1V$$

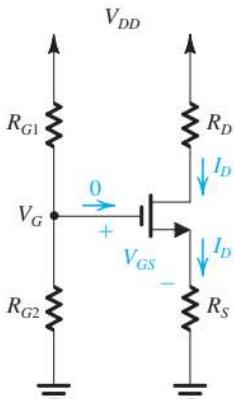
$$V_{GS} - V_t = 1V$$

$$V_{GS} = 1 + 1 = 2V$$

$$V_{GS} = 2V$$

$$V_G - V_S = 2V$$

$$V_G = 2 + 5 = 7V$$



To obtain this voltage at the Gate

R_{G1} and R_{G2} should be in the ratio 8:7

Q1 b

If the V_t of NMOS is changed to 1.5V

$$\text{then } I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad \textcircled{2}$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10I_D \quad \textcircled{3}$$

from a,b

$$V_{GS} =$$

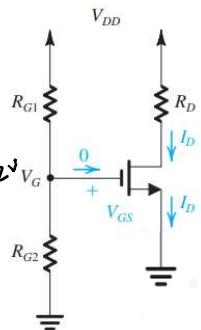
$$I_D = 0.455 \text{ mA}$$

$$\text{Change in } I_D \quad \Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

$$\% \text{ change} = \frac{\Delta I_D}{I_D} \times 100 = \frac{-0.045}{0.5} \times 100 \\ = -9\%$$

Key Observation

If the transistor is biased without R_s as shown in the figure, then for the same starting ID of 0.5mA, VG should be 2V

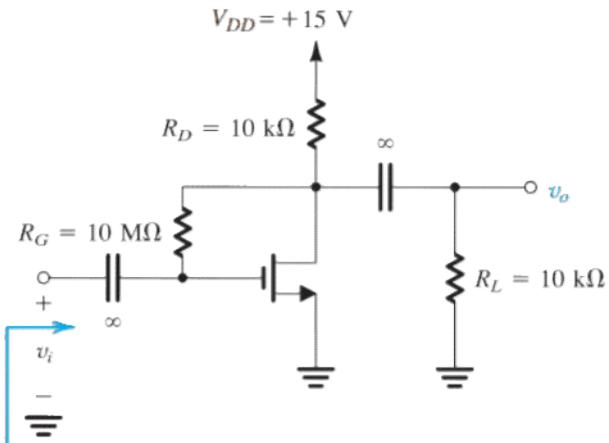


For the same VG, if the V_t of NMOS changes to 1.5V then ID changes to 0.125mA

*for a fixed V_{GS} of 2V in absence of R_s resistor
the impact of mismatch will produce a change
from 0.5mA to 0.125mA a 75% change*

Hence R_s tries to minimize the impact of transistor mismatches on bias point

Q2



a

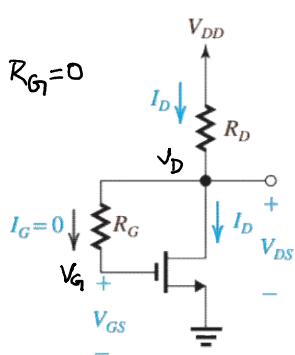
Quiescent Point calculation

For this purpose, the input signal is eliminated, and the two capacitors are open-circuit since they block dc currents.

Since $I_G = 0$, drop across $R_G = 0$

$$\text{So } V_D = V_G$$

$\Rightarrow V_{DS} = V_{GS} \Rightarrow \text{Saturation}$



also

$$V_{DS} = V_{GS} = V_{DD} - R_D I_D$$

$$V_{DS} = V_{GS} = 15 - 10 I_D \quad \textcircled{a}$$

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad \textcircled{b}$$

from a and b

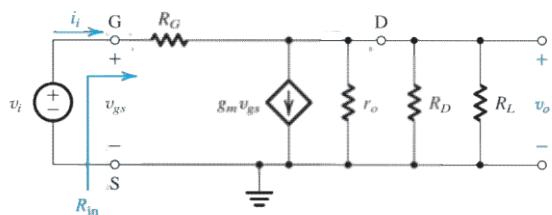
$$V_{GS} = 15 - 10 \times \frac{1}{8} \times (V_{GS} - 1.5)^2$$

$$\Rightarrow V_{GS} = 4.41 \text{ V}$$

b $I_D = 1.06 \text{ mA}$

Small Signal Analysis

(b)

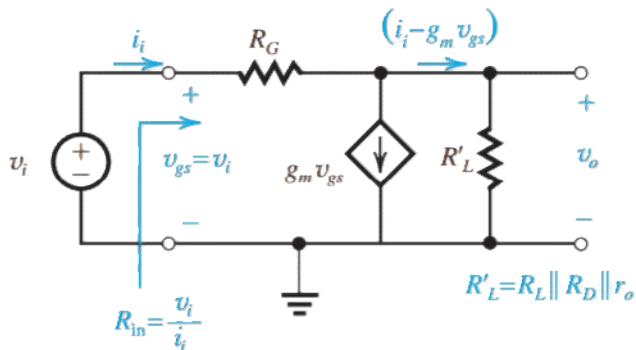


$$\begin{aligned} g_m &= \frac{2 I_{Dq}}{V_{GSQ} - V_t} = \frac{2 \times 1.06}{4.41 - 1.5} \text{ mA/V} \\ &= \frac{2 \times 1.06}{2.91} \\ &= 0.728 \text{ mA/V} \end{aligned}$$

$$\gamma_0 = \frac{1}{g_m} = \frac{1}{2 \times 0.728} = 47.2 \text{ k}\Omega$$

lets Simplify the circuit by combining \$r_o\$, \$R_D\$ and \$R_L\$

$$\text{let } R'_L = R_L || R_D || \gamma_0 = 10 || 10 || 47 = 4.5 \text{ k}\Omega$$



Small Signal Voltage Gain

$$A_V = \frac{\gamma_0}{g_m}$$

Voltage drop across R_G

$$R_G \times i_i = V_{GS} - V_o \quad \text{--- (2)}$$

Voltage drop across R_L'

$$V_o = (i_i - g_m V_{GS}) R_L' \quad \text{--- (3)}$$

from c, d

$$\frac{V_o}{V_{GS}} = -g_m R_L' \left(\frac{R_G - \frac{1}{g_m}}{R_G + R_L'} \right)$$

one should note that $\frac{1}{g_m} = 1.3\text{k}$, $R_L' = 4.5\text{k}$
both are much less than R_G

$$\text{also } V_{in} = V_{GS}$$

$$\therefore \frac{V_o}{V_{in}} = \frac{V_o}{V_{GS}} \approx -g_m R_L'$$

$$A_V = -g_m R_L'$$

$$= -0.725 \times 4.52 \\ A_V = -3.3 \text{ V/V}$$

c Input Resistance.

$$R_{in} = \frac{V_i}{i_i} = \frac{V_i}{\left(\frac{V_{GS} - V_o}{R_G} \right)} = \frac{V_i}{\frac{V_i - A_V V_o}{R_G}} = \frac{R_G}{1 - A_V}$$

$$R_{in} = \frac{R_G}{1 - A_V} = \frac{10M}{1 + 3.3} = 2.33M\Omega$$

d

Largest allowable Input Signal

Here one should analyse the large signal behaviour.

DC circuit + Small signal circuit

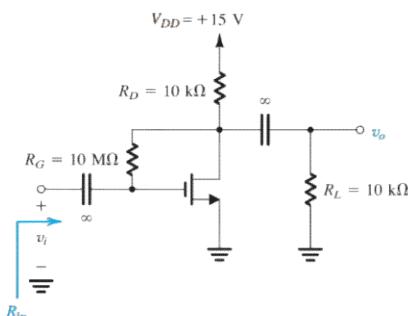
$$V_G = V_{GQ} + V_i$$

$$V_D = V_{DQ} + A_V \times V_i$$

for the transistor to stay in saturation

$$V_{DS} \geq V_{GS} - V_t$$

$$V_D \geq V_G - V_t$$



$$V_{DQ} + A_V V_{GS} \geq V_{GQ} + V_{GS} - V_t$$

$$V_{DQ} - V_{GQ} + V_t \geq V_{GS} (1 - A_V)$$

$$\frac{V_{DQ} - V_{GQ} + V_t}{1 - A_V} \geq V_{GS}$$

$$\Rightarrow \text{max value for } V_{GS} = \frac{V_{DQ} - V_{GQ} + V_t}{1 - A_V}$$

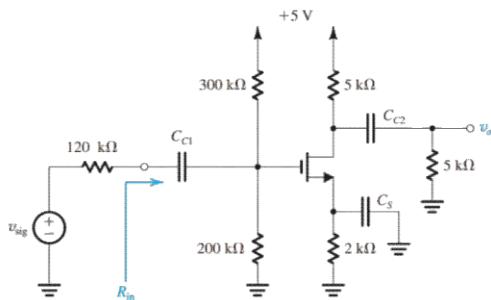
$$V_{GS_{\max}} = \frac{V_{DQ} - V_{GQ} + V_t}{1 - A_V} - \textcircled{2}$$

from our Quiescent point calculation
we have $V_{DQ} = V_{GQ}$

$$V_{GS_{\max}} = V_{i_{\max}} = \frac{V_t}{1 - A_V}$$

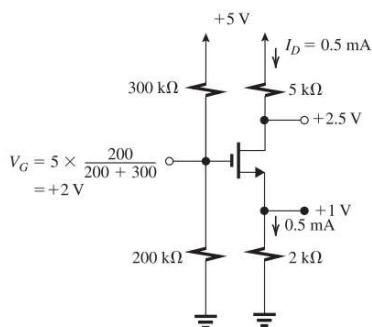
$$= \frac{1.5}{1 + 3.3} = 0.35V$$

Q3



a Quiescent Point calculation

For this purpose, the input signal is eliminated, and the two capacitors are open-circuit since they block dc currents.



$$V_G = 2V, V_D = 2.5V, I_D = 0.5mA$$

$$V_{DS} = 1.5V, V_{GS} = 1V, V_t = 0.7V$$

$V_{DS} \geq V_{GS} - V_t$ so transistor is in Saturation region

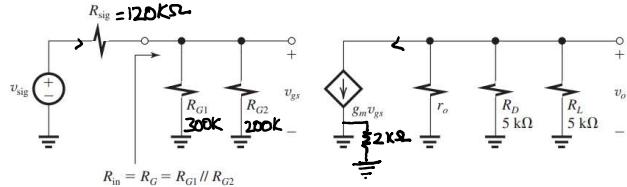
$$I_D = \frac{1}{2} K_n \times (V_{GS} - V_t)^2$$

$$\begin{aligned} K_n &= 2I / (V_{GS} - V_t)^2 \\ &= 1 / (1 - 0.7)^2 \end{aligned}$$

$$K_n = 1/(0.3)^2 = 11.1 \text{ mA/V}^2$$

b

Small Signal Analysis



$$g_m = \frac{2I_{DQ}}{V_{GSQ} - V_t} = \frac{2 \times 0.5}{0.3} = 3.33 \text{ mA/V}$$

$$g_m = 3.33 \text{ mA/V}$$

$$\gamma_0 = \frac{1}{g_m} = \frac{1}{3.33} \times 10^6 = 100 \text{ k}\Omega$$

$$\begin{aligned} R_{in} &= 300 \text{ k}\Omega \parallel 200 \text{ k}\Omega \\ &= 120 \text{ k}\Omega \end{aligned}$$

$$v_{gs} = \frac{R_{in}}{R_{sig} + R_{in}} v_{sig}$$

$$v_o = -g_m v_{gs} (\gamma_0 \parallel R_D \parallel R_L)$$

$$v_o = -g_m \frac{R_{in}}{R_{sig} + R_{in}} \cdot (\gamma_0 \parallel R_D \parallel R_L) v_{sig}$$

$$\frac{v_o}{v_{sig}} = -g_m \times \frac{R_{in}}{R_{sig} + R_{in}} \times R'_L \quad \text{where } R'_L = \gamma_0 \parallel R_D \parallel R_L$$

by substituting values from our circuit

$$g_m = 3.33 \text{ mA/V}, R_{in} = R_{sig} = 120 \text{ k}\Omega, R'_L = 2.4 \text{ k}\Omega$$

$$\text{Gain} = \frac{v_o}{v_{sig}} = -4.1 \text{ V/V}$$

c

Largest allowable Input Signal

Here one should analyse the large signal behaviour.

DC circuit + Small signal circuit

$$V_{G1} = V_{GQ} + V_t$$

$$V_D = V_{DQ} + A_{v \times} V_i$$

for the transistor to stay in saturation

$$V_{DS} \geq V_{GS} - V_t$$

$$V_D \geq V_{GS} - V_t$$

$$V_{DQ} + A_v \cdot V_{GS} \geq V_{GQ} + V_{GS} - V_t$$

$$V_{DQ} - V_{GQ} + V_t \geq V_{GS} (1 - A_v)$$

$$\frac{V_{DQ} - V_{GQ} + V_t}{1 - A_v} \geq V_{GS}$$

$$\Rightarrow \text{max value for } V_{GS} = \frac{V_{DQ} - V_{GQ} + V_t}{1 - A_v}$$

$$V_{GS\max} = \frac{V_{DQ} - V_{GQ} + V_t}{1 - A_v} - \textcircled{2}$$

one should observe that $V_{GS\max}$ is fixed for a Quiescent point

$$V_{GQ} = 2V, V_{DQ} = 2.5V, V_t = 0.7V$$

$$A_v = -g_m R_L^1 = -8.1V/V$$

$$\therefore V_{GS\max} = \frac{2.5 - 2 + 0.7}{1 + 8.1} = 0.132V$$

$$x = V_{sig\max} = \frac{R_{sig} + R_{in}}{R_{in}} \times V_{GS\max} - \textcircled{3}$$

$$= \frac{120 + 120}{120} \times 0.132V$$

$$x = V_{sig\max} = 0.264V$$

$$\text{its corresponding output } V_o = \frac{V_o}{V_{sig}} \times x$$

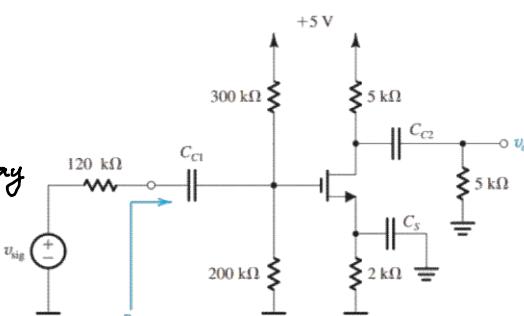
$$= -4.1 \times 0.264$$

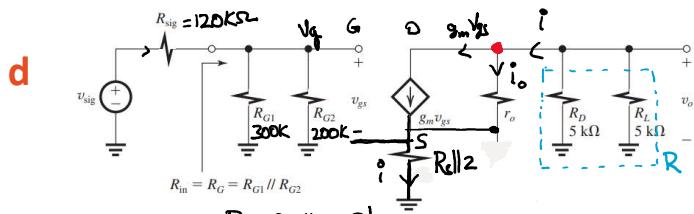
$$= -1.08V$$

for a Sine wave at input with peak amplitude 0.264V

the V_o will be a Sine with amplitude of 1.08V

In Other Words Maximum allowed output signal amplitude is 1.08V





$$\text{Let } R_L \parallel R_D = R, \quad R_S \parallel 2 = R'_S$$

$$i = g_m v_{ds} + i_0, \quad i = -\frac{v_o}{R}$$

$$v_s = R_s^{-1} \times i = -\frac{R_s}{R} v_o$$

applying KCL at highlighted node,

$$-\frac{V_o}{R} = \frac{V_0 - (-\frac{V_0 R_s}{R})}{\frac{R_o}{R}} + g_m V_{GS} \Rightarrow -\frac{V_o}{R_o} = \frac{V_0 (1 + \frac{R_s}{R}) + g_m (V_g - (-\frac{V_0 R_s}{R}))}{\frac{R_o}{R}}$$

$$-\frac{V_0}{R} \left(\frac{1}{R} + \frac{1}{\frac{V_0}{R}} + \frac{R_L'}{R_{L0}} + \frac{g_m R_L'}{R} \right) = g_m V_g \Rightarrow \frac{V_0}{V_g} = -\frac{\frac{1}{R} + \frac{1}{\frac{V_0}{R}} + \frac{R_L'}{R_{L0}} + \frac{g_m R_L'}{R}}{-\frac{g_m}{R}}$$

$$\frac{V_o}{V_{in}} = \frac{-g_m}{\frac{1}{R_s} + \frac{1}{R_D} + \frac{R_L}{R_{in}} + \frac{g_m R_L}{R}} \times \frac{R_{in}}{R_s g_m + R_{in}}$$

by a similar analysis from Part C

$$V_{DQ} + V_0 \geq V_{GQ} + V_g - V_t, \text{ let's call } \frac{V_0}{V_g} = y$$

$$V_{DG} + V_f - Y \geq V_{GA} + Vg - V_t$$

$$V_g(1-y) \leq V_{Dg} - V_{Gg} + k$$

$$V_g \leq \frac{V_{DQ} - V_{GQ} + V_L}{1-y}$$

$$V_{in\ max} = 2 \cdot Z = \frac{R_{sig} + R_{in}}{R_{in}} \cdot \frac{V_{DQ} - V_{GQ} + V_U}{1 - \gamma}$$

$$2 \times \chi = 2 \times \frac{1.2}{1 - \frac{-g_m}{\frac{\frac{1}{R} + \frac{1}{R_0}}{\frac{R_0}{R}} + \frac{R_0^2}{R}}} = \frac{2.4}{1 - \frac{-g_m}{\frac{R_0 + R}{R} + \frac{R_0^2}{R}}}$$

$$x = 0.264V, g_m = 3.33 \text{ mA/V}, R = 2.5 \text{ k}\Omega, V_o = 100 \text{ k}\Omega$$

$$2 \cdot 0 \cdot 264 = \frac{2 \cdot 4}{1 + \frac{3 \cdot 33}{\frac{1}{2 \cdot 5} + \frac{1}{100} + \frac{R_S'}{2 \cdot 50} + \frac{3 \cdot 33 \cdot R_S'}{2 \cdot 5}}}$$

$$R_S^1 = 0.606 \text{ k}\Omega \Rightarrow 2 \parallel R_S = 0.6 \text{ k}\Omega \Rightarrow R_S = 0.869 \text{ k}\Omega$$

so this configuration achieves same output swing as before but allows double the input signal
this is achieved by compromising on the gain

$$\text{Previous gain} = -g_m \times \frac{R_{in}}{R_{out} + R_{in}} \times \frac{1}{\frac{1}{R} + \frac{1}{T_0}}$$

$$\text{Present gain} = -g_{mR} \frac{R_m}{R_{in} + R_m} \times \frac{1}{\frac{1}{R} + \frac{1}{T_0} + \frac{R_s^2}{R_{in}} + \frac{R_m R_s^2}{R}}$$

Q4 i

for circuit 'a'

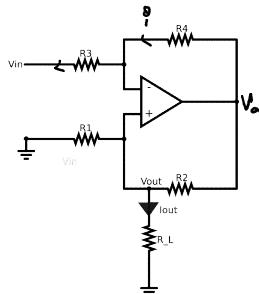
$$\frac{V_{out} - V_{in}}{R_2} = \frac{V_a - V_{out}}{R_4} = i$$

$$\frac{V_a - V_{out}}{R_2} = I_{out} + \frac{V_{out}}{R_1}$$

from above two equations

$$\frac{R_4}{R_2} \times \frac{1}{R_3} \times (V_{out} - V_{in}) - \frac{V_{out}}{R_1} = I_{out}$$

$$V_{out} \times \left(\frac{R_4}{R_2 R_3} - \frac{1}{R_1} \right) - V_{in} \times \frac{R_4}{R_2 R_3} = I_{out} \quad \textcircled{1}$$

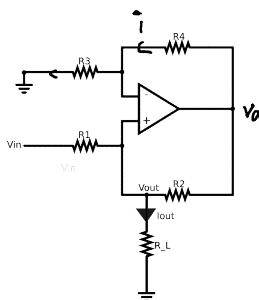


for Circuit 'b'

$$\frac{V_a - V_{out}}{R_2} = I_{out} + \frac{V_{out} - V_{in}}{R_1}$$

$$\frac{V_a - V_{out}}{R_4} = \frac{V_{out}}{R_3} = i$$

from above two equations



$$\frac{R_4}{R_2} \times \frac{V_{out}}{R_3} + \frac{V_{in} - V_{out}}{R_1} = I_{out}$$

$$V_{out} \left(\frac{R_4}{R_2 R_3} - \frac{1}{R_1} \right) + \frac{V_{in}}{R_1} = I_{out}$$

ii

for the above circuits to act as current sources

the I_{out} should be independent of V_{out}

$$\Rightarrow \text{for both Circuit 'a' and 'b', } \frac{R_4}{R_2 R_3} = \frac{1}{R_1}$$

$$\text{then for circuit 'a', } I_{out} = -\frac{V_{in}}{R_1}$$

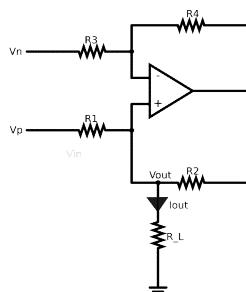
$$\text{for circuit 'b', } I_{out} = \frac{V_{in}}{R_1}$$

iii

$$I_{out} \text{ due to } V_n = -\frac{V_n}{R_1}$$

$$I_{out} \text{ due to } V_p = \frac{V_p}{R_1}$$

$$I_{out} = \frac{V_p - V_n}{R_1}$$

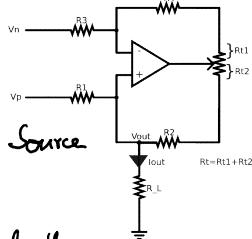


iv

Ideally when the condition

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

is satisfied
the output Resistance of the current Source
will become infinite



A trimmer Resistance is used to satisfy the
Resistance condition.

$$\frac{R_4 + R_{t1}}{R_3} = \frac{R_2 + R_{t2}}{R_1}, \quad R_{t1} + R_{t2} = R_t$$

$$\frac{R_4 + R_{t1}}{R_3} = \frac{R_2 + R_t - R_{t2}}{R_1}$$

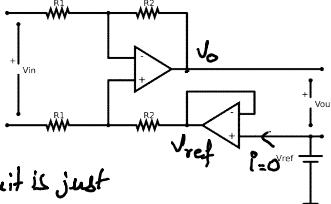
$$R_{t1} \left(\frac{1}{R_3} + \frac{1}{R_1} \right) = \left(\frac{R_2 + R_t}{R_1} - \frac{R_4}{R_3} \right)$$

$$R_{t1} = 2.711 \text{ k}\Omega$$

$$R_{t2} = 2.289 \text{ k}\Omega$$

v

One should observe that
 V_{ref} has no impact on
 V_{out} .

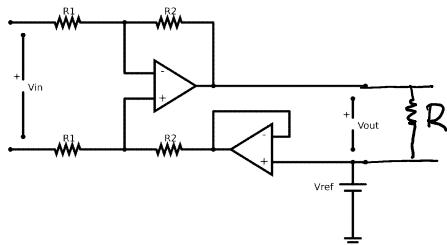


Consider $V_{ref} = 0$, the circuit is just
a difference amplifier

$$V_0 = \frac{R_2}{R_1} \cdot V_{in}$$

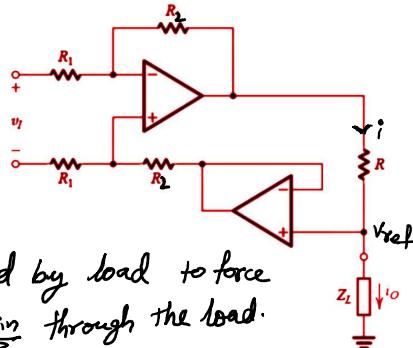
$$\text{when } V_{ref} \neq 0, \quad V_0 = \frac{R_2}{R_1} \cdot V_{in} + V_{ref}$$

$$V_{out} = V_0 - V_{ref} = \frac{R_2}{R_1} \cdot V_{in}$$



Now when the Resistor is added, the current through
Resistance $R = \frac{R_2}{R_1} \cdot \frac{V_{in}}{R}$

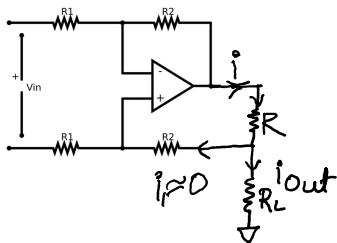
this current doesn't depend on V_{ref}
 and this current is forced to flow through
 the battery V_{ref} irrespective of the value of V_{ref}



This V_{ref} can be Replaced by load to force
 the current $\frac{R_2}{R_1} \cdot \frac{V_{in}}{R}$ through the load.

Going further, the 2nd opamp

can be removed if R_2
 is much larger than
 R and R_L to maintain the
 $i = i_{out}$, i should be negligible



$$\text{then still } i_{out} = \frac{R_2}{R_1} \times \frac{V_{in}}{R}$$