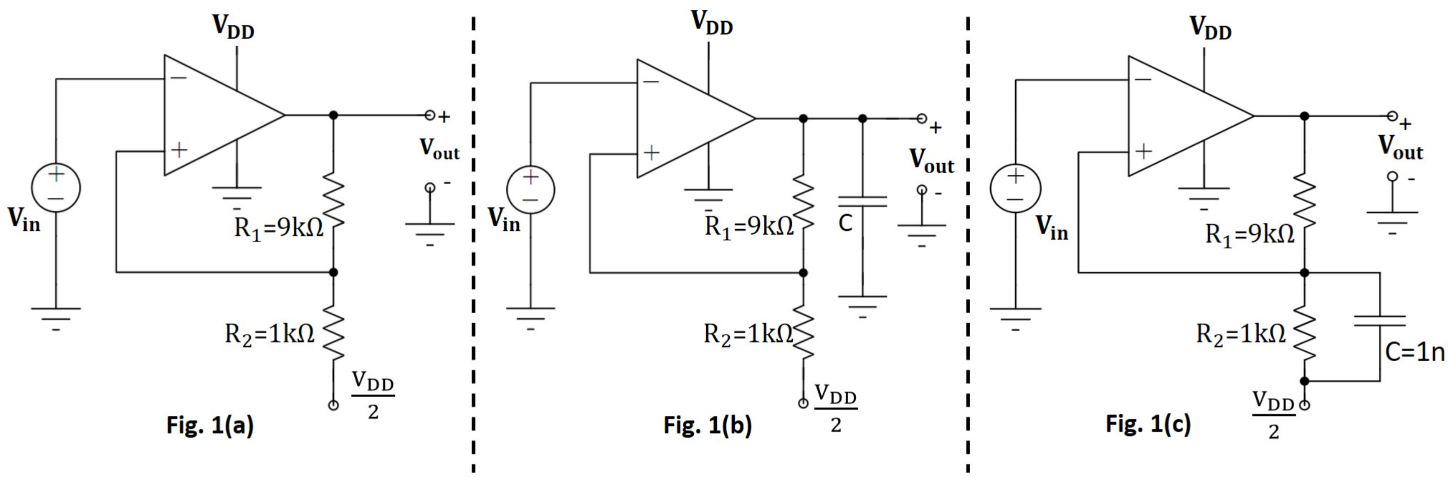
EE204 - Analog Circuits
Electrical Engineering Department
IIT-Bombay
Autumn 2023

Mid-semester Examination

Total Marks : 20

Date: 23^{rd} **September 2023**, **Time: 1.30 pm to 3.30 pm**.

Q1)



(a) Fig. 1(a) shows schematic of a single-supply non-inverting amplifier (Op-Amp is ideal).
$V_{in}(t) = V_m sin(\omega_0 t) + V_{DD}/2$
where, $V_m = 0.04V_{DD}$. Derive the expression for $V_{out}(t)$ {1 *mark*}

(b) All conditions remain same as the conditions in Q1(a) except adding a parasitic capacitor at the output as shown in Fig. 1(b). Will there be any change in V_{out} as compared to Fig. 1(a)? If answer is yes, derive the new expression of $V_{out}(t)$ with C as a parameter. If answer is no, explain the reason. {1 *mark*}

(c) All conditions remain same as the conditions in Q1(a) except adding a capacitor of 1nF parallel to R_2 as shown in Fig. 1(c). Consider only sinusoidal components of V_{in} and V_{out} (i.e. small signal voltages). Determine how voltage gain of the circuit will vary with frequency. Plot 20log(magnitude of voltage gain) as a function of log(ω). $\{1 + 1 + 1$ *marks*$\}$

Q2)

Consider fully differential instrumentation amplifier shown in Fig. 2. Op-Amps are ideal but with limited swing, i.e.
$V_{1_{max}} = V_{2_{max}} = 4V$; $V_{1_{min}} = V_{2_{min}} = 1V$.
$V_{o1_{max}} = V_{o2_{max}} = 4.5V$; $V_{o1_{min}} = V_{o2_{min}} = 0.5V$.

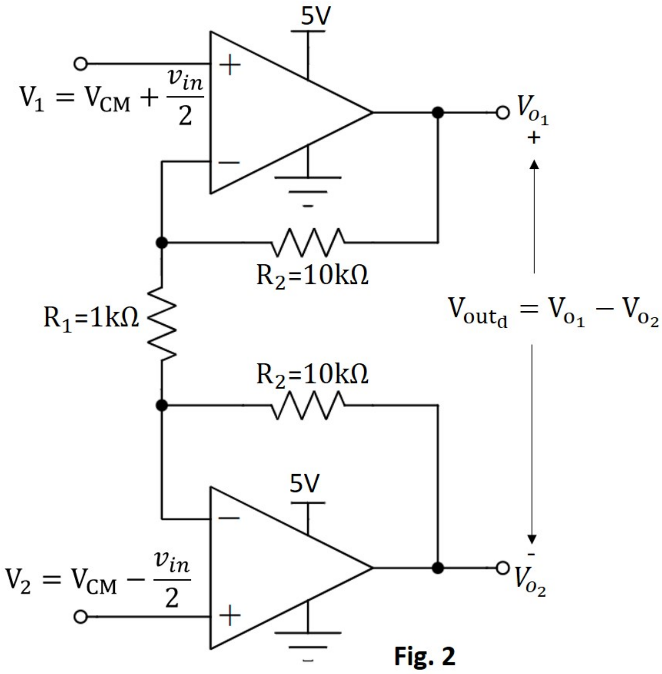


Fig. 2

(a) For $v_{in_{max}}$=50mV, determine $V_{CM_{max}}$ and $V_{CM_{min}}$. {1 *mark*}

(b) If $V_{CM} = 2$V, determine $v_{in_{max}}$. {1 *mark*}

(c) Determine amount of current sourced to/or sunk from output of each Op-Amp for Q2(a) and Q2(b) each. {1 + 1 *marks*}

(d) If a resistor R $= 40k\Omega$ is connected between V_{o1} and V_{o2}, how will $A_{vd} = V_{out_d}/v_{in}$ change? {1 *mark*}

Information related to questions 3 and 4:

For NMOS transistors: $\mu_n C_{ox} = 400\mu A/V^2$, $\lambda \approx 0$(negligible), $V_{tn} = 0.4V$.

$I_D \approx \frac{\mu_n C_{ox}}{2}(\frac{W}{L})(V_{GS} - V_{tn})^2$; $V_{GST} = V_{GS} - V_{tn}$, (Saturation or pinch-off region)

$I_D \approx \mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{tn})V_{DS}$ (Ohmic or linear region).

Q3)

Consider the circuit schematic of common source amplifier followed by a source follower stage as shown in Fig. 3.

- C_1 and C_2 will be almost like a short circuit at the frequency of small signal v_{in}.
- DC information: $V_{GST_1} = V_{GST_2} = 0.2V$, $I_{D_{M_1}} = 0.2mA$

(a) If small signal voltage gain $\frac{v_{out_1}}{v_{in}} = -20$, determine $(\frac{W}{L})_{M_1}$, V_B and R_2. Show transistor M_1 is biased in the saturation region. {0.5 + 0.5 + 0.5 + 1 *marks*}

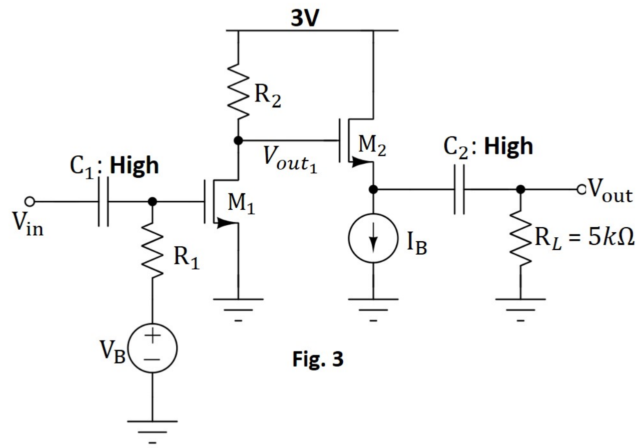


Fig. 3

(b) If small signal transfer function $\frac{v_{out}}{v_{out_1}}$=0.9, determine bias current I_B. For this purpose, first derive the small signal $\frac{v_{out}}{v_{out_1}}$ as a function of g_{m_2} and R_L by drawing the small signal circuit of M_2 and then calculate I_B. $\{1 + 1\ marks\}$

(c) Determine small signal gain $\frac{v_{out}}{v_{in}}$, DC value of V_{out} and DC voltage across current source I_B. $\{0.5 + 0.5 + 0.5\ marks\}$

(d) What would be the problem if the source follower stage is removed and capacitor C_2 & resistor R_L are directly connected to the drain of M_1 in Fig. 3. $\{1\ mark\}$

Q4)

An ideal current source I_B was used in Fig. 3 to bias transistor M_2. In this question you will design an actual circuit for generating I_B, shown in Fig. 4.

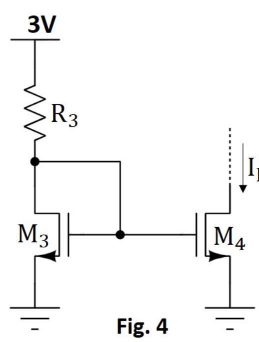


Fig. 4

Requirements:

- Transistors M_3 and M_4 must be biased in saturation (pinch-off) region.
- I_B = The value you calculated in Q3(b), $I_{D_{M3}} < 100\mu A$, $V_{DS_{4_{min}}} = 150mV$.

Determine value of R_3, $(\frac{W}{L})_{M3}$ and $(\frac{W}{L})_{M4}$. $\{1{+}1{+}1\ marks\}$

Notice: This question is a design problem and there are many solutions.

All the Best!

Q1) a)

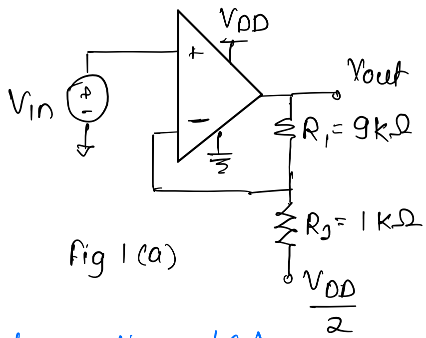


fig 1 (a)

We have from figure 1 (a)

$V_{cm} = \frac{V_{DD}}{2}$

$V_{in} = V_m \cdot \sin(\omega_0 t) + V_{cm}$ where $V_m = 0.04\, V_{DD}$

Thus $V_{out} = \left(1 + \frac{R_2}{R_1}\right)(V_{in} - V_{cm}) + V_{cm}$ — <0.5 mark>

$= \left(1 + \frac{9}{1}\right)(V_m \cdot \sin(\omega_0 t) + V_{cm})$

$\therefore V_{out} = 10 \times 0.04\, V_{DD} \cdot \sin(\omega_0 t) + \frac{V_{DD}}{2}$

$\therefore V_{out} = 0.4\, V_{DD} \cdot \sin(\omega_0 t) + \frac{V_{DD}}{2}$ — <0.5 mark>

(b)

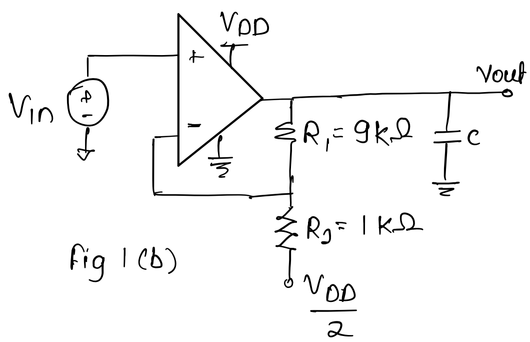


fig 1 (b)

The opamp is ideal.
Hence it can provide current to charge & discharge of capacitor C of any value at freqn of ω_0. <0.5 mark>
Hence presence of parasitic capacitor C will not change the o/p of the opamp. <0.5 mark>

(c)

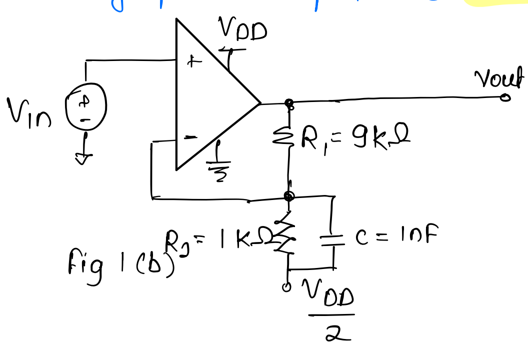


fig 1 (b)

The Transfer function

$$V_{in}(s) = \frac{\frac{R_2}{R_2 C s + 1}}{R_1 + \frac{R_2}{R_2 C s + 1}} \cdot V_{out}(s)$$ — <0.5 mark>

Hence $V_{in}(s) = \dfrac{R_2}{R_2 + R_1(R_2Cs+1)} \cdot V_{out}(s)$

$\therefore \dfrac{V_{out}(s)}{V_{in}(s)} = 1 + \dfrac{R_1}{R_2}(R_2Cs+1)$ — <0.5 mark>

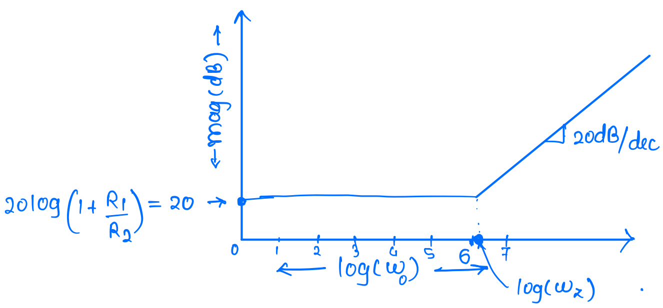
Thus $\dfrac{V_{out}(j\omega)}{V_{in}(j\omega)} = 1 + \dfrac{R_1}{R_2}(1 + jR_2C\omega)$ — ① — <0.5 mark>

We have $R_1 = 9K\Omega$, $R_2 = 1K\Omega$ & $C = 1nF$

$\therefore \dfrac{V_{out}(s)}{V_{in}(s)} = 1 + 9(10^{-6}s+1) = 10 + 9(10^{-6}s) = \dfrac{10^7 + 9s}{10^6}$ $\quad \omega_z = \dfrac{10^7}{9} = 1.1 \times 10^6 \text{ rad/s}$ — <0.5 mark>

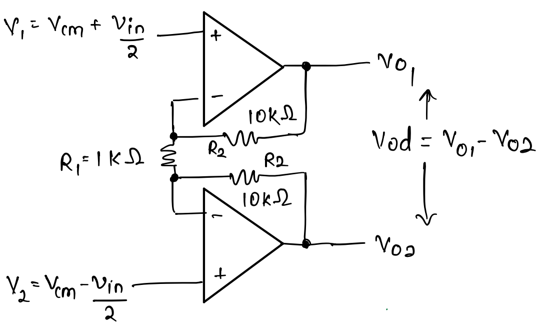
From eqⁿ ①, the voltage gain of the circuit will increase with ω. i.e High Pass filter behavior is obtained.

The frequency plot will be as follows



0.5 marks for graph
0.25 mark for X axis annotations
0.25 mark for Y axis annotations

Q2)



$V_{1max} = V_{2max} = 4V$

$V_{1min} = V_{2min} = 1V$

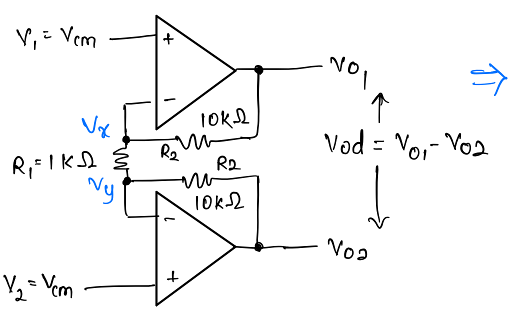
$V_{o1max} = V_{o2max} = 4.5V$

$V_{o1min} = V_{o2min} = 0.5V$

(a) $V_{in\,max} = 50mV$

$V_1 = V_{ic} + V_{id}$ & $V_2 = V_{ic} - V_{id}$ where $V_{ic} = \dfrac{V_1+V_2}{2} = V_{cm}$ & $V_{id} = \dfrac{V_1 - V_2}{2} = \dfrac{V_{in}}{2}$

Considering only common mode signal



⇒

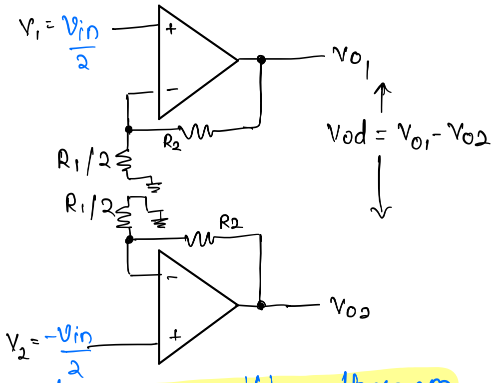
$V_x = V_y = V_{cm}$

$I_{R_1} = 0$ & Hence $I_{R_2} = 0$ $\therefore$

$V_{o1} = V_{cm}$ & $V_{o2} = V_{cm}$

$V_{od} = 0$ — ①

Considering only differential mode signal



$$V_{o1} = \left(1 + \frac{R_2}{R_1/2}\right) V_1$$

$$= \left(1 + \frac{2R_2}{R_1}\right) \cdot \frac{V_{in}}{2}$$

$$\& \; V_{o2} = \left(1 + \frac{2R_2}{R_1}\right) \cdot \left(\frac{-V_{in}}{2}\right) \quad \text{— (11)}$$

$$V_{od} = \left(1 + \frac{2R_2}{R_1}\right)(V_{in})$$

Thus by superposition theorem,

$$V_{o1} = V_{cm} + \left(1 + \frac{2R_2}{R_1}\right)(V_{in}/2)$$

$$V_{o2} = V_{cm} + \left(1 + \frac{2R_2}{R_1}\right)\left(-\frac{V_{in}}{2}\right)$$

0.5 mark

$V_1 = V_{cm} + \frac{V_{in\,max}}{2} = V_{cm} + 25mV.$

$\& \; V_2 = V_{cm} - 25mV. \qquad \& \quad V_{o1} = V_{cm} + \left(1 + \frac{2R_2}{R_1}\right)(V_{in}/2)$

$\therefore V_{o1} = (21)(25mV) + V_{cm} = 0.525\,V + V_{cm}.$

$V_{o1\,max} = 4.5V$ thus

$V_{cm\,max} = V_{o1\,max} - 0.525V = 3.975\,V.$ — <0.25 mark>

$V_2 = V_{cm} - \frac{V_{in\,max}}{2} = V_{cm} - 25mV \qquad \& \quad V_{o2} = V_{cm} + \left(1 + \frac{2R_2}{R_1}\right)(-V_{in}/2)$

$\therefore V_{o2} = (21)(-25mV) + V_{cm} = -0.525\,V + V_{cm}$

$V_{o2\,min} = 0.5V$

$\therefore V_{cm\,min} = V_{o2\,min} + 0.525\,V = 1.025\,V$ — <0.25 mark>

<b> $V_{cm} = 2V$

$V_{o1}/V_{o2} = V_{cm} + \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{\pm V_{in}}{2}\right)$ - 0.5 marks

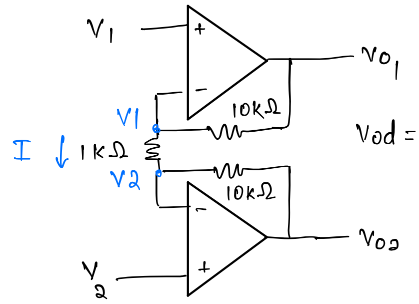
$$0.5 < V_{cm} + \left(1 + \frac{2R_2}{R_1}\right)\left(\pm\frac{V_{in}}{2}\right) < 4.5$$

$$-0.142 < \pm V_{in} < 0.238$$

$\boxed{-0.142 < V_{in} < 0.238}$ and $\boxed{0.142 > V_{in} > -0.238}$

$V_{in}|_{max} = 0.142$ (0.5 marks)

<c> current sourced/sinked by op-amp



$V_{od} = V_{o_1} - V_{o_2}$

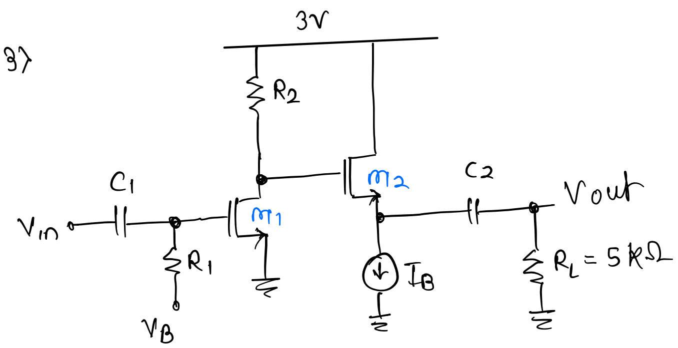
$\therefore I = \dfrac{V1 - V2}{1K\Omega}$ — <0.5 mark> & $|I_{sourced}| = |I_{sinked}|$ — <0.5 mark>

for 2<a> $I_{sourced} = \dfrac{50mV}{1K\Omega} = 50\,\mu A$ — <0.5 mark>

for 2<b> $I_{sourced} = \dfrac{238.1\,mV}{1K\Omega} = 238.1\,\mu A$ — <0.5 marks>

<d> The OPAMP used in Q2 are ideal except for min/max range of input & o/p, the <0.5mark> Hence OPAMP can source/sink any current, thus adding a 40kΩ resistance betn V_{o_1} & V_{o_2} will not have any impact on o/p ← <0.5 mark>

<Q3>



<a> $\dfrac{v_{out1}}{v_{in}} = -20 = -gm_1 \cdot R_2$ — <0.5 mark>

$gm_1 = \dfrac{2 I_{D1}}{V_{GST_1}} = \dfrac{2 \times 0.2mA}{0.2} = 2mA/V$ — <0.25mark>

$\therefore -2mA/V \times R_2 = -20$

$\therefore R_2 = 10k\Omega$ — <0.25mark>

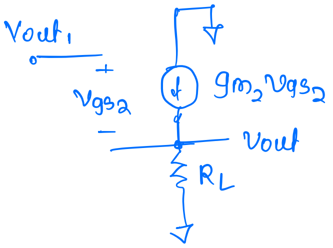
$I_{D_1} = \dfrac{\mu n C_{ox}}{2} \left(\dfrac{W}{L}\right)_1 (V_{GST_1})^2 = \dfrac{400\mu}{2} \left(\dfrac{W}{L}\right)_1 (0.2)^2 = 0.2mA$

$\therefore \left(\dfrac{W}{L}\right)_1 = 25$ — <0.5 mark>

$V_{GS_1} = V_B = V_{GST} + V_{T_n}$

$\therefore V_B = 0.2V + 0.4V = 0.6V$ — <0.5 mark>

<b> The small signal equivalent circuit of only M_2 & R_L is as follows



$\Rightarrow$ $g_{m_2} v_{gs_2} = g_{m_2}(V_{out_1} - V_{out})$

$\therefore \dfrac{V_{out}}{R_L} = g_{m_2}(V_{out_1} - V_{out})$

$\therefore \dfrac{V_{out}}{V_{out_1}} = \dfrac{g_{m_2} \cdot R_L}{1 + g_{m_2} R_L}$ — <0.5 mark>

$\therefore \dfrac{g_{m_2} \cdot 5K}{1 + g_{m_2} 5K} = 0.9$

$\therefore g_{m_2} = 1.8\,mA/V$ — <0.5 mark>

$g_{m_2} = \dfrac{2 \times I_B}{V_{oST_2}} = \dfrac{2 \times I_B}{0.2} = 1.8 \times 10^{-3}$ — <0.5 mark>

$\therefore I_B = 180\,\mu A = 0.18\,mA$ — <0.5 mark>

<c> $\dfrac{V_{out}}{V_{in}} = \dfrac{V_{out}}{V_{out_1}} \times \dfrac{V_{out_1}}{V_{in}} = 0.9 \times -20 = -18\ V/V$ — <0.5 mark>

The capacitor C_2 will block DC voltage hence no DC current will flow through R_L

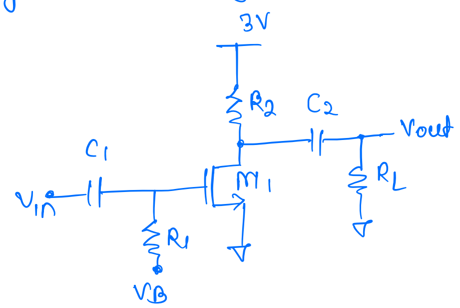
$\therefore V_{out_{DC}} = 0V$ — <0.5 mark>

DC voltage across I_B $= V_{DD} - I_{D_1} R - V_{GS_2} = V_{DD} - I_{D_1} R - (V_{oST} + V_{Tn})$ — <0.25 mark>

$= 3 - 0.2m \times 10k - (0.2 + 0.4)$

$= 0.4\,V$ — <0.25 mark>

<d> if the source follower stage is removed i.e



$\Rightarrow$ Load resistance will become $R_L \| R_2$ instead of R_2 with source follower stage

Hence gain of this stage will drop by a factor of $\dfrac{R_2 \| R_L}{R_2} = \dfrac{5k \| 10k}{10k} = \dfrac{1}{3}$ — <0.5m>

Thus $A_{v_1} = -20 \times \dfrac{1}{3} = -6.67\ V/V$ — <0.5 mark>

<Q4>

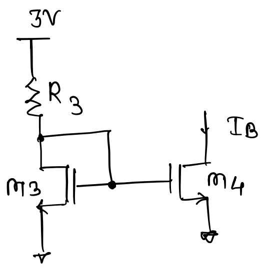


Fig 4

∴ We have $V_{GS_3} = V_{GS_4}$

Hence $\dfrac{I_{D3}}{I_{D4}} = \dfrac{(W/L)_3}{(W/L)_4}$ — <0.5 mark>

From Q3 b>, $I_{D_4} = I_B = 180\,\mu A$

Requirement 1 :- $V_{DS_{4min}} = 0.15V$

Step 1> students can choose any V_{GST_4} value less than or equal to $V_{DS_4 min}$

$V_{GST_4} \leq V_{DS_4 min}$ i.e $V_{GST_4} \leq 0.15$

For example $V_{GST_4} = 0.15V$

$\therefore V_{GS_4} = V_{GST_4} + V_{Tn} = 0.15 + 0.4 = 0.55V$ — <0.5 mark>

Requirement 2 :- $I_{D3} < 100\,\mu A$

Step 2> students can choose any value less than $100\,\mu A$

For example consider $I_{D_3} = 90\,\mu A$

We have from fig 4 & Step I, $V_{GS_3} = V_{GS_4} = 0.55V$

$$\therefore R_3 = \frac{3V - V_{GS3}}{I_{D3}} = \frac{3 - 0.55}{90\mu} = 27.22\,k\Omega$$ — < 1 mark >

$$I_{D_3} = \frac{\mu n \cdot C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GST_3})^2$$

$$\therefore 90\mu = \frac{400\mu}{2}\left(\frac{W}{L}\right)_3 (0.15)^2$$

$$\therefore \left(\frac{W}{L}\right)_3 = 20$$ — <0.5 mark>

$$\therefore \left(\frac{W}{L}\right)_4 = \frac{I_B}{I_{D3}} \times (W/L)_3 = \frac{180\mu}{90\mu} \times 20 = 40$$

$$\therefore \left(\frac{W}{L}\right)_4 = 40$$ — <0.5 mark>