Q1) We have $R = 100k\Omega$, $C = 1nF$

Initial condition $Q = 0$; $\bar{Q} = V_{DD} \Rightarrow V_c = 0$

a) When $V_{Trigger}$ goes low, comparator 2 o/p goes high, $Q = V_{DD}$; $\bar{Q} = 0$

Transistor Q is OFF & hence capacitor C starts charging

$$V_c(t) = V_{DD}\left(1 - e^{-t/RC}\right)$$ — <1 mark>

When $V_c(t)$ reaches $\frac{2}{3}V_{DD}$, o/p of comparator 1 goes high

Hence $Q = 0$ & $\bar{Q} = V_{DD} \Rightarrow V_c = 0$

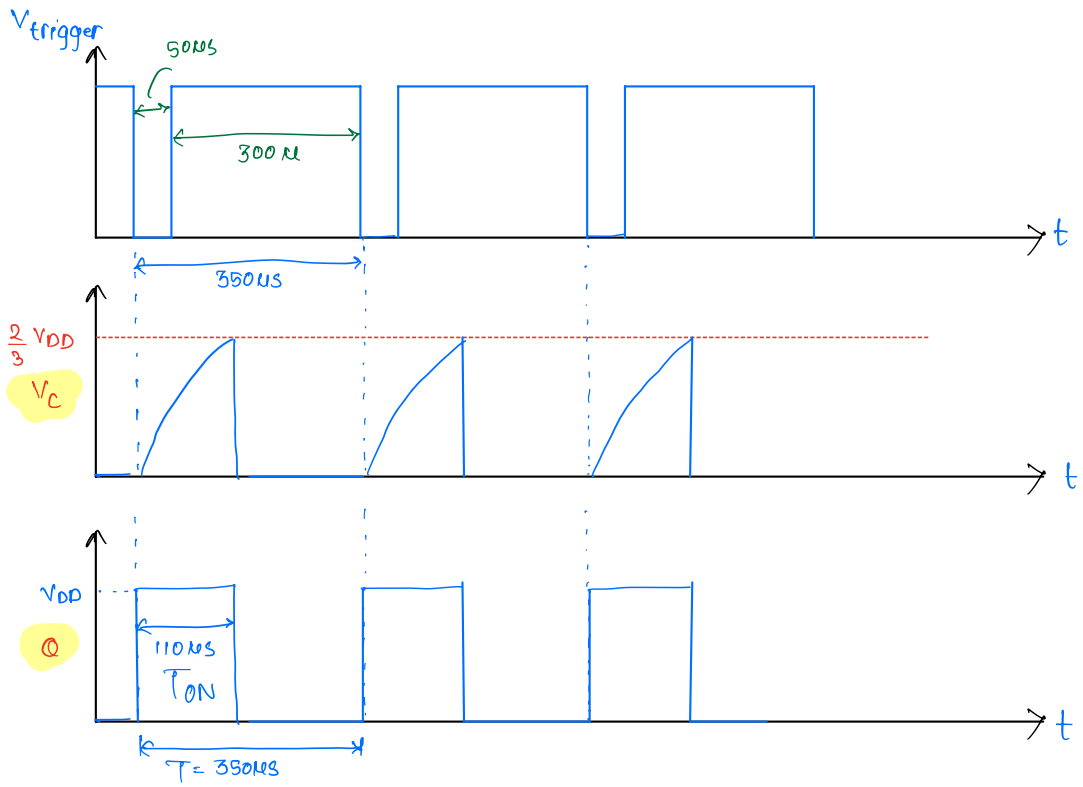
$V_c(t=0) = 0$ $\quad V_c(t=T) = \frac{2}{3}V_{DD}$

$$\therefore \frac{2}{3}V_{DD} = V_{DD}\left(1 - e^{-T/RC}\right)$$

$$T = R \cdot C \cdot \ln(3)$$ — <1 mark>

When $R = 100k\Omega$ & $C = 1nF$

$$T_{ON} = 100k \times 1n \times \ln(3) = 109.9\,\mu s \approx 110\,\mu s$$ — <1 mark>

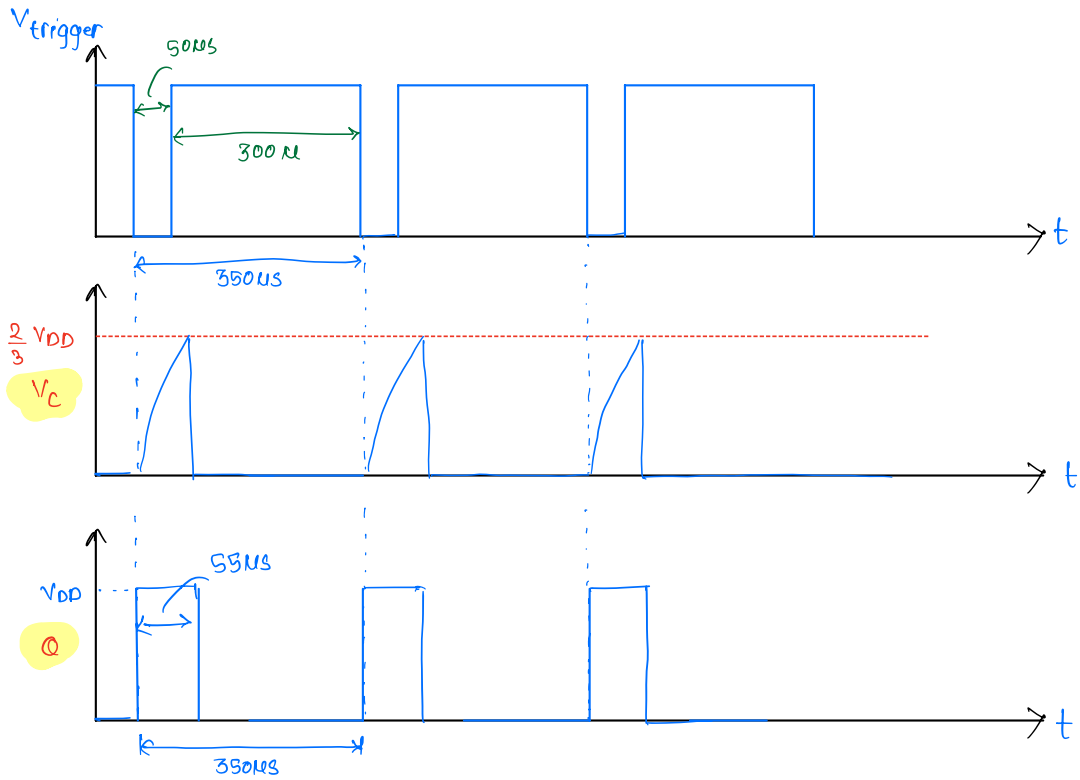


<graph = 1 mark
Annotation 0-5 mark>

<graph = 1 mark
Annotation 0-5 mark>

b) when C = 1nF & R = 50kΩ

then T = ln(3) × R × C = 54.9 µs ≈ 55 µs ⟨0.5 mark⟩

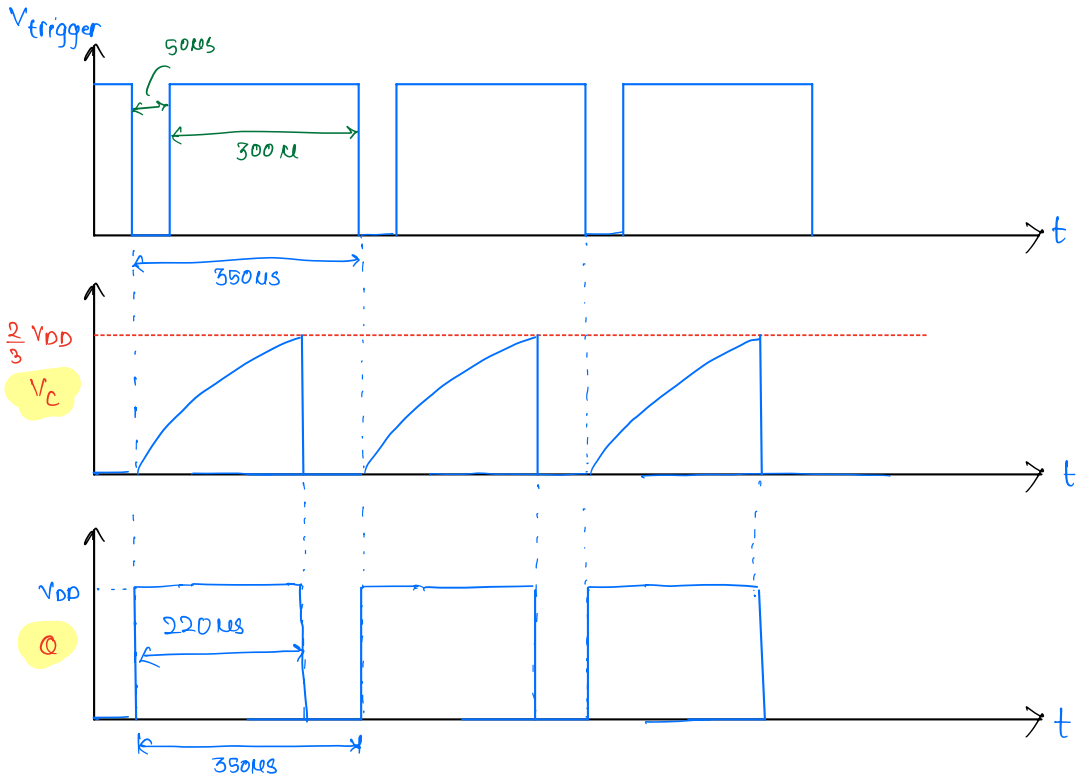


⟨1 mark⟩

⟨0.5 mark⟩

when C = 1nF & R = 200kΩ

then T = ln(3) × R × C = 219.7 µs ≈ 220 µs ⟨0.5 mark⟩



⟨1 mark⟩

⟨0.5 mark⟩

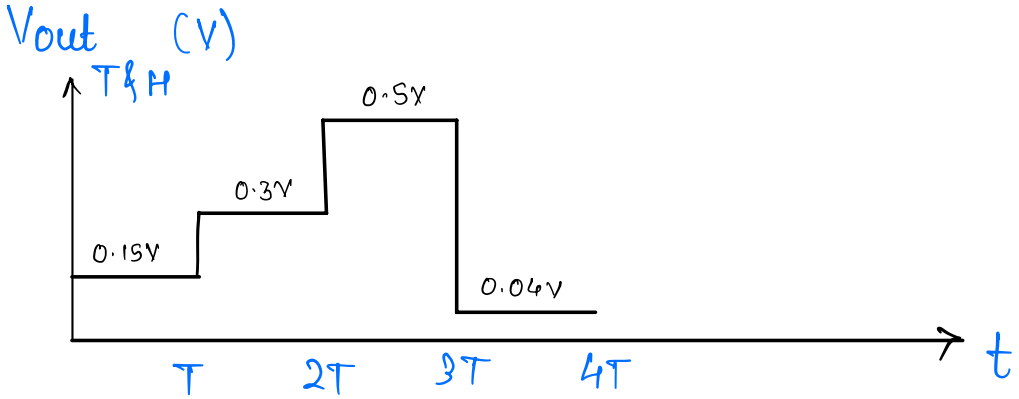
Q2) we have $V_{Full\ scale} = 1.6V$

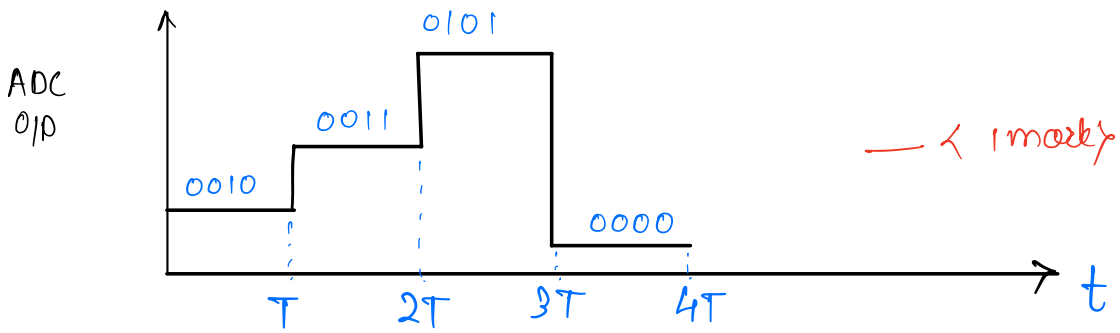
$n = 4$ bits

a) $\Delta = V_{LSB} = \frac{1.6}{2^4} = \frac{1.6}{16} = 0.1V$ <2 mark>

b) ADC o/p switches at 50mV, (i.e $\frac{LSB}{2}$).

i/p V	o/p of ADC	
0.15V	0010	— <0.5 mark>
0.3V	0011	— <0.5 mark>
0.5V	0101	— <0.5 mark>
0.04	0000	— <0.5 mark>



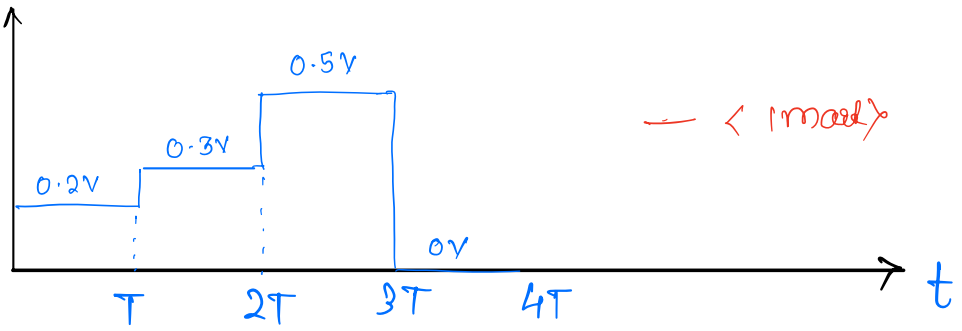


— <1 mark>

<C> $LSB_{DAC} = LSB_{ADC}$

DAC i/p	DAC o/p	
0010	0.2 V	— <0.5 mark>
0011	0.3 V	— <0.5 mark>
0101	0.5 V	— <0.5 mark>
0000	0 V	— <0.5 mark>

DAC O/P



— < 1 mark >

(d) $V_{out_{comp}}(t) = V_{out_{(0)}} e^{t/\tau}$; $\tau = 0.4\,\mu s$ $V_{out_{(0)}} = 10\,mV$

for comparator to switch, $V_{out_{comp}}(t)$ should cross 1 V

$\therefore$

$\therefore$ $1\,V = 10\,m\, e^{T/0.4\mu}$ — < 1 mark >

$\therefore$ $T = 1.84\,\mu sec$

Thus maximum delay of comparator is 1.84 μs — < 1 mark >