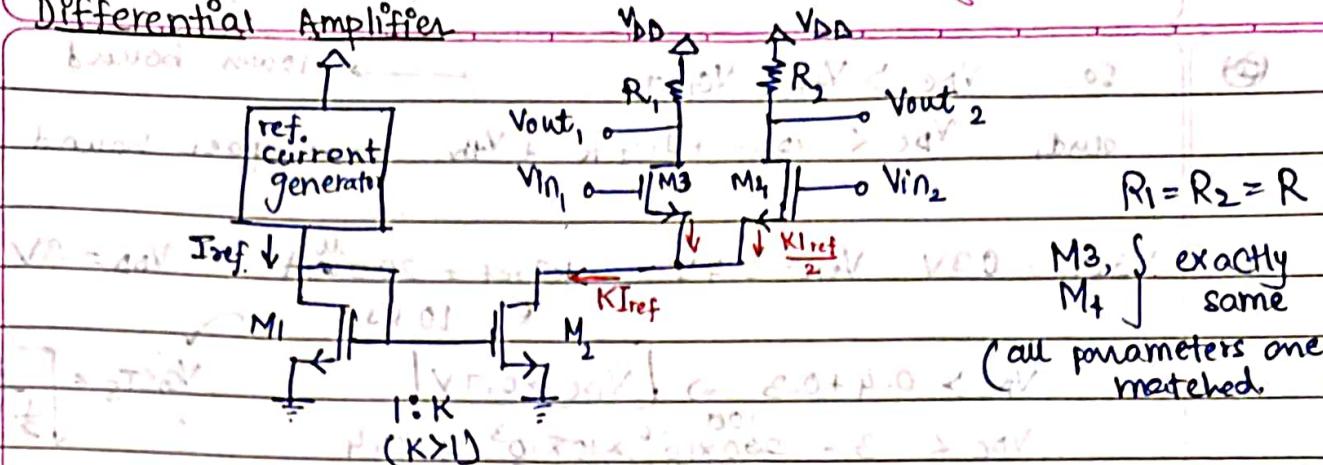


Differential Amplifier

1:K current mirror

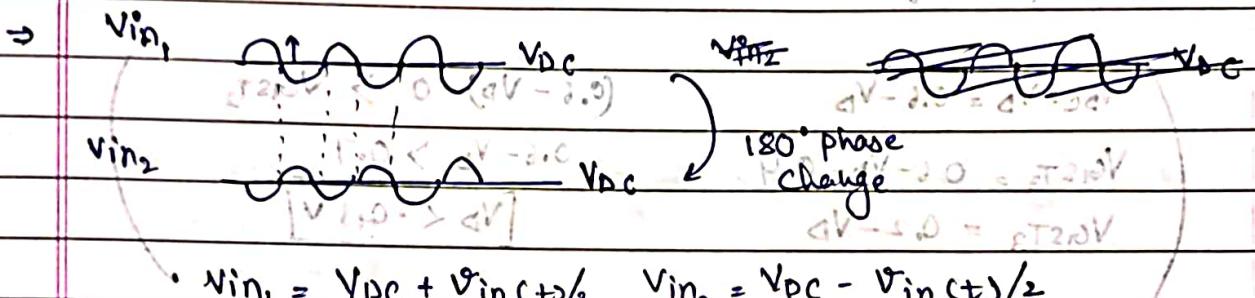
 K_{Iref} → used to bias the circuits

Two modes of operation

↳ Differential Mode
↳ Common-Mode

(added) only for linear analysis.

$V_{D.C.} = 5V$ \Rightarrow unipolar mode



$V_{in_1} = V_{DC} + \frac{V_{in}(t)}{2}$ $V_{in_2} = V_{DC} - \frac{V_{in}(t)}{2}$

$V_{CM} = V_{DC}$ $V_{id} = \frac{V_{in}(t)}{2}$ Assumption: $\left| \frac{V_{in}(t)}{2} \right| \ll V_{DC}$

→ BIAS point of the transistor → determined by K_{Iref} only.↳ V_{DC} : needs to satisfy some conditions just to keep the transistor in the triode mode of operation.amplifies $V_{in}(t)$
circuit rejects (attenuates) V_{DC} ① M_3, M_4 are always in SATURATION REGIONsaturation: $V_{DS} > V_{GS} - V_t$ or $V_D > V_g - V_{tn}$ and $V_{GS} > V_{tn}$ $V_{GS} > V_{tn}$ using KVL, $V_{DC} - V_{tn} < V_{DD} - \frac{K_{Iref} \cdot R}{2}$ ① $\Rightarrow V_{DC} = V_{GS_3} + V_{DS_2} \rightarrow$ (KVL) [saturation of M_2 , turn-on of M_3] $V_{DC} > V_{tn} + V_{GST_2}$ $V_{GS_3} > V_{tn}$ and $V_{DS_2} > V_{GST_2}$ $V_{DC} > V_{GST_2}$ (threshold condition)② $\Rightarrow M_3$ in saturation $\Rightarrow V_{DC} - V_{tn} < V_{DD} - \frac{K_{Iref} \cdot R}{2}$

$V_{GST_3} / V_{GST_4} < V_{DS_3} / V_{DS_4}$

$$V_{DS2} > V_{GS2} - V_{th}$$

$$V_{DS2} = V_{G1_3} - V_{GS_3} - V_{SS} > V_{GS_2} - V_{th}$$

$$V_{cm} > V_{th} + V_{SS}$$

$$V_{cm} > (V_{ov})_3 + V_{GS_2} + V_{SS}$$

(2)

$$\text{So, } V_{DC} > V_{th} + V_{GST_2} \rightarrow \text{lower bound}$$

$$\text{and, } V_{DC} < V_{DD} - K_I \text{ref} R + V_{th} \rightarrow \text{upper bound}$$

$$\text{eg.-1 } V_{GST_2} = 0.3V \quad V_{th} = 0.4V \quad K_I \text{ref} = 200 \mu A \quad V_{DD} = 3V \\ R = 10 k\Omega$$

$$V_{DC} > 0.4 + 0.3 \Rightarrow V_{DC} > 0.7V$$

$$V_{DC} < 3 - \frac{100}{200 \times 10^{-6}} \times 10 \times 10^3 / 4 + 0.4$$

$$V_{GST_3} = \sqrt{\frac{I}{2k'(\omega)}}$$

$$V_{DC} < 3 - 1 + 0.4 \Rightarrow V_{DC} < 2.4V$$

$$V_{cm} > 0.3 + 0 + V_{GST_3} \quad (\text{stricter bound})$$

Q2) what happens if $V_{DC} = 0.6V$

$$V_{DC} - V_D = 0.6 - V_D$$

$$(0.6 - V_D) - 0 > V_{GST_2}$$

$$V_{GST_3} = 0.6 - V_D - 0.4$$

$$0.6 - V_D > 0.7$$

$$V_{GST_3} = 0.2 - V_D$$

$$V_D < -0.1V$$

Suppose : M_3 remains in saturation and M_2 : ohmic

V_{GST_3} current

is not $K_I \text{ref}$ for from $2A12$

if V_{GST_3} is not $K_I \text{ref}$ then I_{D2} is not $K_I \text{ref}$

$$\Rightarrow \text{if } V_{DC} < 0.6V \text{ then } I_{D2} \text{ is not } K_I \text{ref}$$

c1) M_3 : saturⁿ, M_2 : ohmic \rightarrow NOT Possible

$$I \downarrow \rightarrow V_{GS} \downarrow \text{current} \rightarrow \text{threshold}$$

c2) M_3 : moderate/weak inversion, M_2 : saturⁿ \rightarrow XX

$$\text{not possible } V_{GST_3} \downarrow \text{and } V_{GST_2} \downarrow \text{and } \Delta V_{GST_3} + \Delta V_{GST_2} = -100mV \quad (0.7 \rightarrow 0.6)$$

$$\text{eg. } V_{GST_3} = 0.1 \quad V_{DS_2} = 0.16 \text{ when } V_{DC} = 0.7V$$

if output impedance of transistor is high
both don't change as V_{GST_3} is already very low.
(boundary cond^t)

\rightarrow GOOD Current Source

V_{GST_3} NOT at boundary

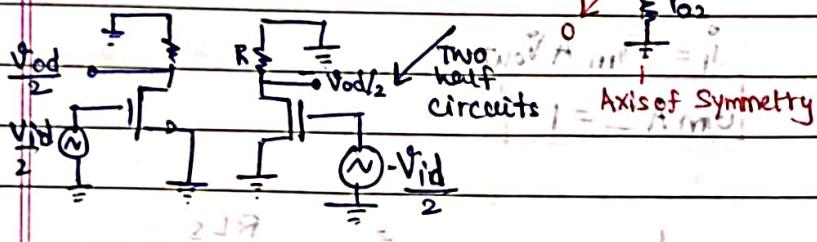
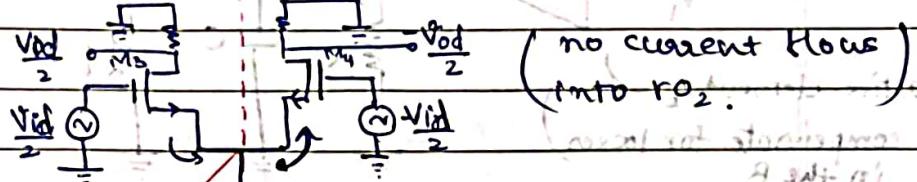
$$\rightarrow V_{R1} = V_{R2} = 1V \quad V_{O3} = V_{O4} = 2V \quad V_{DC} < 2.4V$$

2.4 $\rightarrow V_{CM(0)}$

0.7

acceptable region

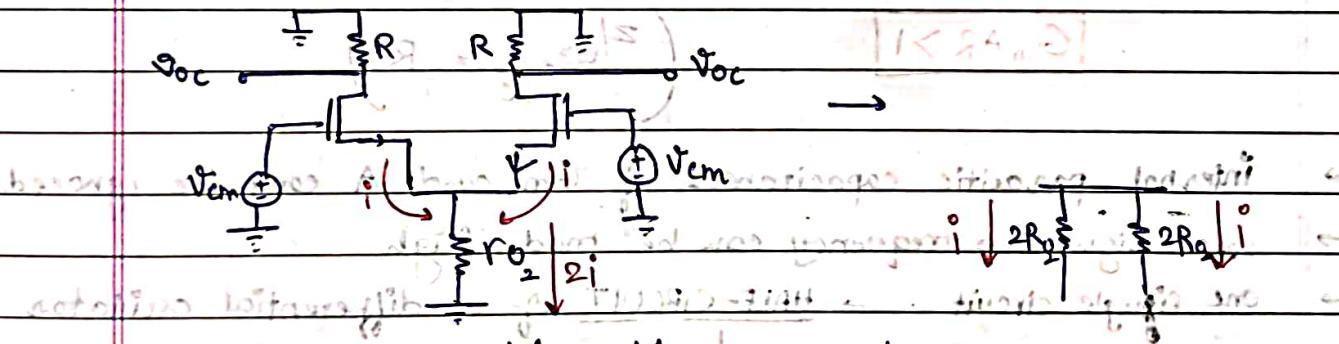
large-signal noise

Small-signal
Models

Two half circuits, with a differential mode gain as,

$$AV_d = \frac{V_{od}/2}{V_{id}} = -\frac{g_m R_o}{2} \quad \text{or,}$$

$$AV_d = \frac{V_{od}}{V_{id}} = -g_m (R_o || R_o) \quad R_o = R_o3 = R_o4 = R_o$$



now, source of M3 & M4, will not be grounded

$$AV_{CM} = \frac{V_{OC}}{V_{IC}} = \frac{g_m R}{1 + g_m \cdot (2R_o)}$$

$$AV_d = -\frac{g_m R_o}{2}$$

$$AV_{CM} \approx \frac{g_m R}{g_m \cdot 2R_o} = \frac{R}{2R_o}$$

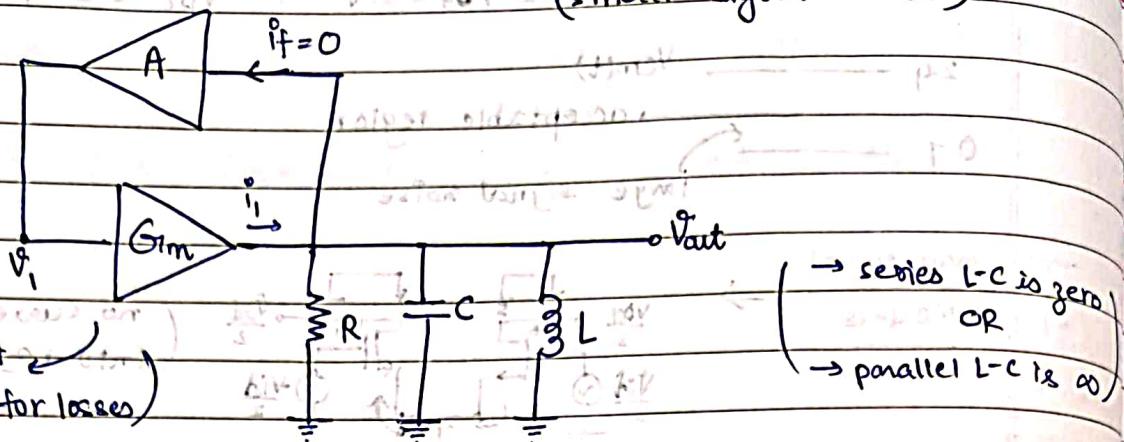
$$CMRR = \frac{g_m R / 2}{R / 2R_o} = \frac{g_m \cdot R_o}{R_o} = CMRR$$

$R_o \uparrow \text{ (high)}$

Will the following circuit oscillate?

Date _____
Page _____

$V_{1+2} > 20V$ $V_{2+3} = 10V$ (small signal circuit)



$$i_1 Z = V_{\text{out}}$$

$$i_1 = G_m A V_{\text{out}}$$

$$G_m A Z = 1$$

$$|Z| = \frac{1}{\frac{1}{R} + \frac{1}{Ls} + \frac{1}{Cs}} = \frac{1}{RLs} \quad \text{no loss}$$

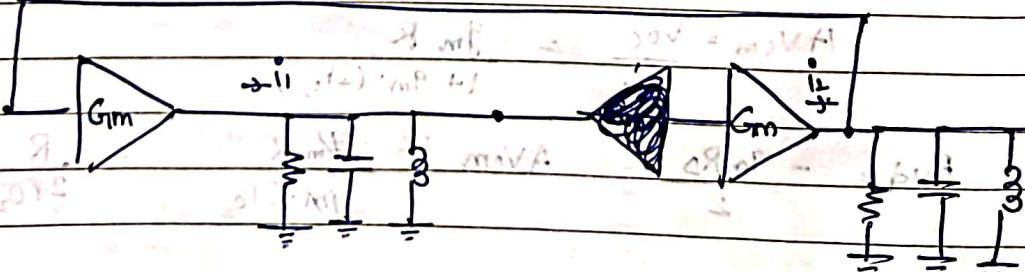
$$\text{so, } Z = \frac{s/C}{s^2 + s/RC + 1/LC}$$

$$\cancel{\omega_0^2 = \frac{1}{LC}} \rightarrow \omega_0^2 = \frac{1}{LC}, \text{ then } Z = R \text{ and } \phi = 0$$

$$G_m A R > 1 \quad \left(Z = \frac{1}{\omega_0^2 = \frac{1}{LC}} = R \right)$$

- internal parasitic capacitances of G_m and A can't be ignored.
- small-signal \rightarrow frequency can be made high.
- one single circuit \rightarrow HALF-CIRCUIT of a differential oscillator

No need of A as we already have one extra G_m



$$Z = \frac{1}{s^2 + s/RC + 1/LC}$$

ref.
current
generator
using
mixer

For min V_{BSAT}

$$V_{DD} - I_D R_D \geq 0.72 - 0.4$$

$$1.8 - (6.494 \times 10^{-3}) R_D \geq 0.39$$

$$R_D \leq 2.854 \text{ k}\Omega$$

\therefore If $R_D \leq 2.56 \text{ k}\Omega$, all conditions satisfied.

$$G_m^2 Z^2 = 1$$

$$\Rightarrow -\frac{G_m^2 \omega^2 C^2}{= 1}$$

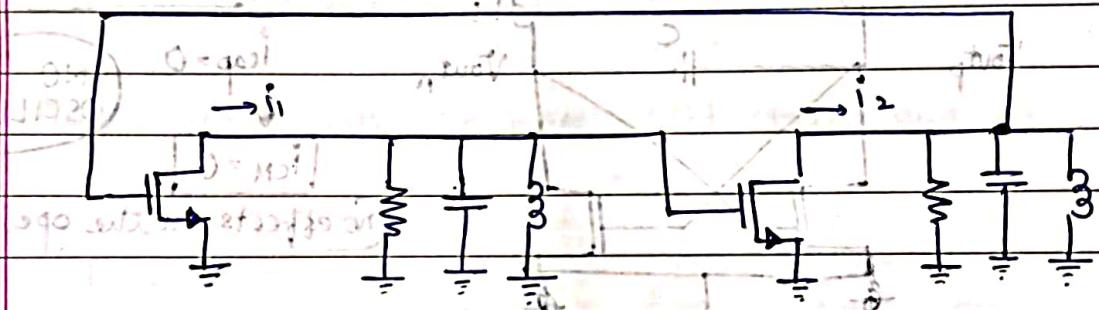
$$\left(\frac{(-\omega^2 + j)}{LC} + \frac{j\omega}{RC} \right)^2$$

$$\text{at } \omega_0^2 = \frac{1}{LC}$$

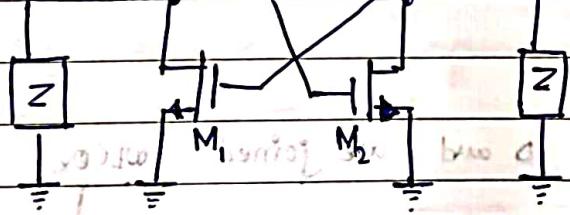
$$\rightarrow T(j\omega) = G_m^2 R^2, G_m R > 1 \text{ (for oscil^n to start)}$$

Transistor-Oscillator Circuit

340M-140MM103

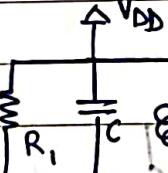


$+V_{out1}$ $-V_{out2}$



(SMALL SIGNALS)

LC TANK CIRCUIT



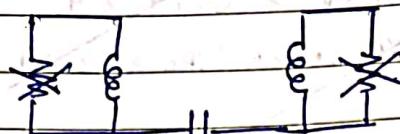
Known as LC circuit tank

$$g_m(R_{\parallel} r_o) > 1$$

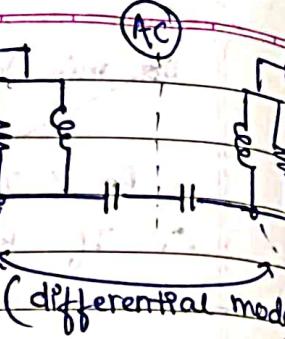
- parasitic capacitance of transistors

• ohmic component of L

ref. current generator



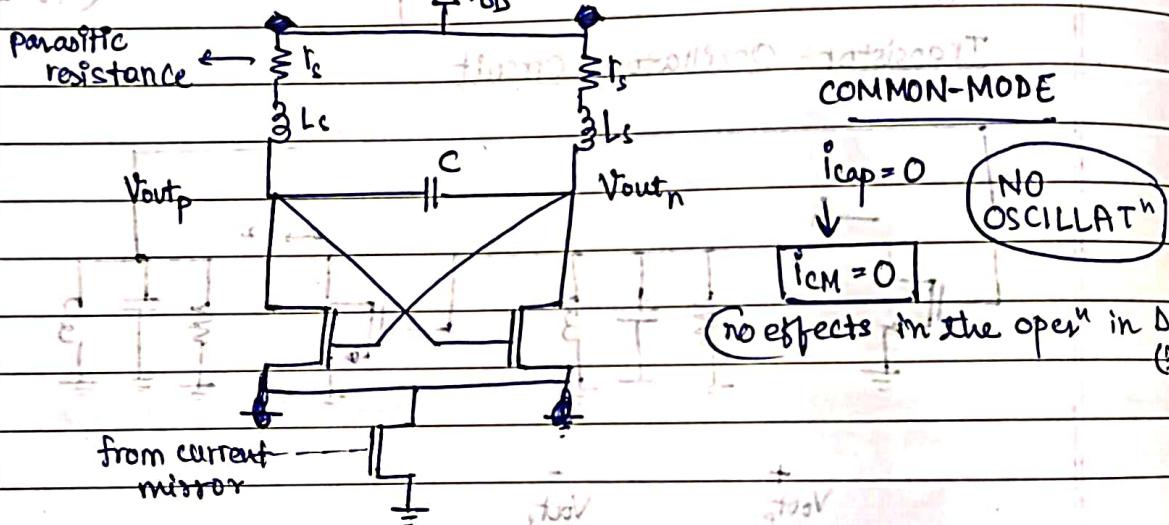
at DC $\rightarrow L \rightarrow$ shorted $\rightarrow R$ of no use



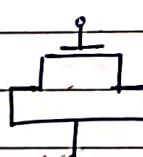
(R is not needed)
(Ls/Sc)

(Inductor has a
series resistance)

(L will always
have some
R with
it
(it
transistors))



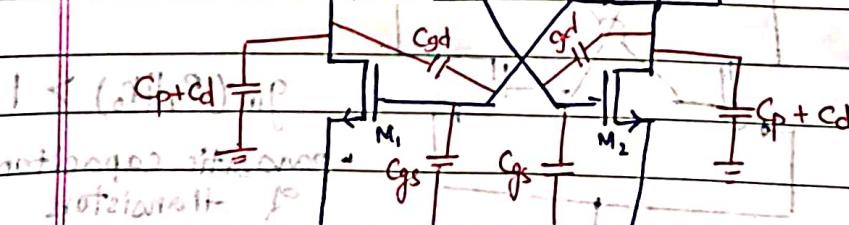
from current
mirror



D and S are joined
WLCox. | WLCox.



(LC TANK
circuit)



(M₁ & M₂)
CROSS-COUPLED TRANSISTOR

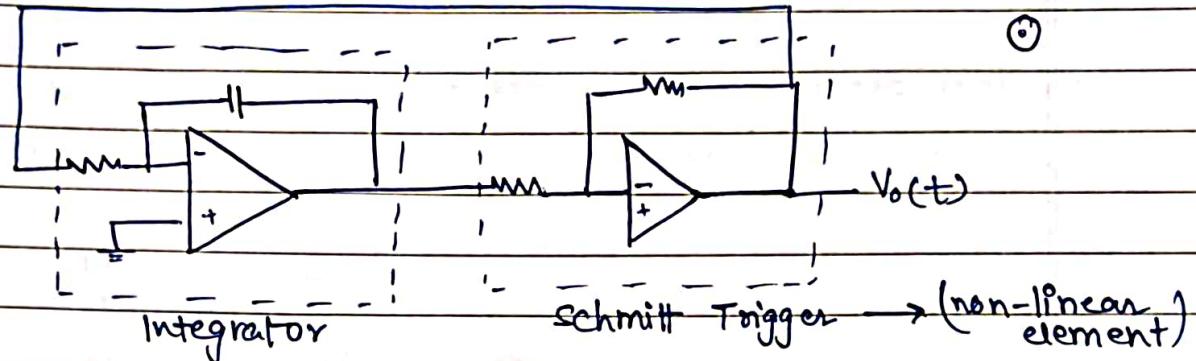
(created an eventual
+ve feedback law with
min.)

Relaxation Oscillator

Schmitt Trigger or any switching circuit with hysteresis

- Astable Multivibrator

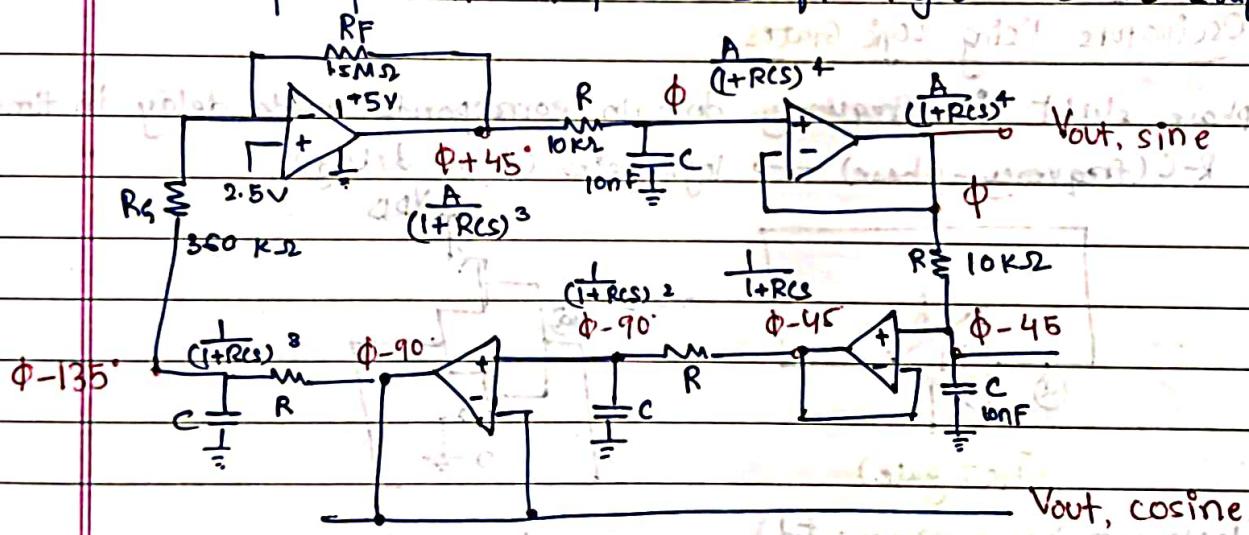
eg.-



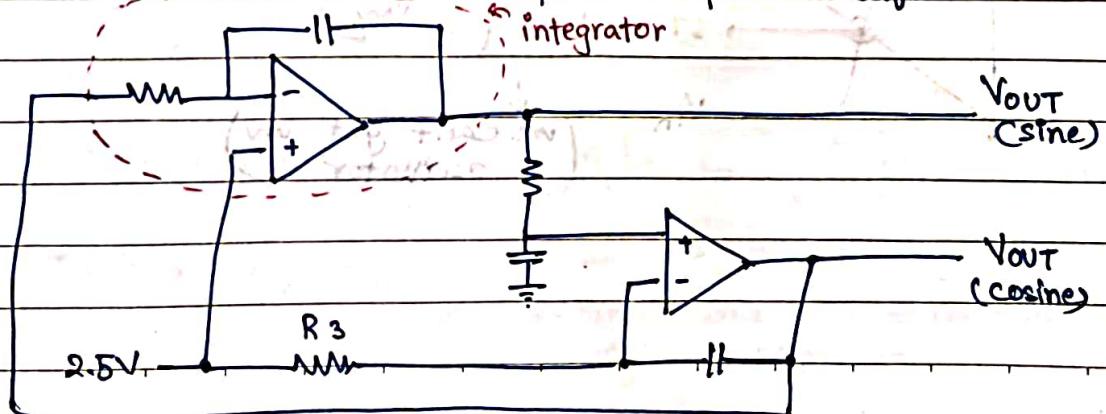
Oscillators with Multiple Stages for Phase-Shift Control

$$\text{Loop gain} \Rightarrow T(s) = \frac{A}{(1+RCS)^4}; A < 0 \text{ here}$$

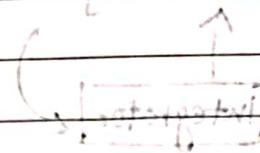
- Quad OpAmp with 4-phase shift stages and 45° shift per phase



- Quadrature Oscillator Example: 90° phase shift

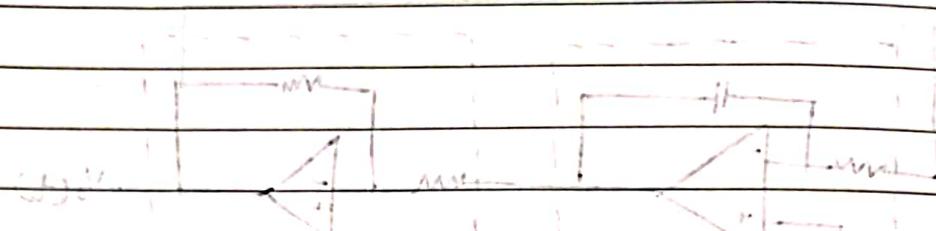


classroom notes taken during class on 12/08/2017 Page No. 2



negative feedback idea

①



frequency response of the circuit

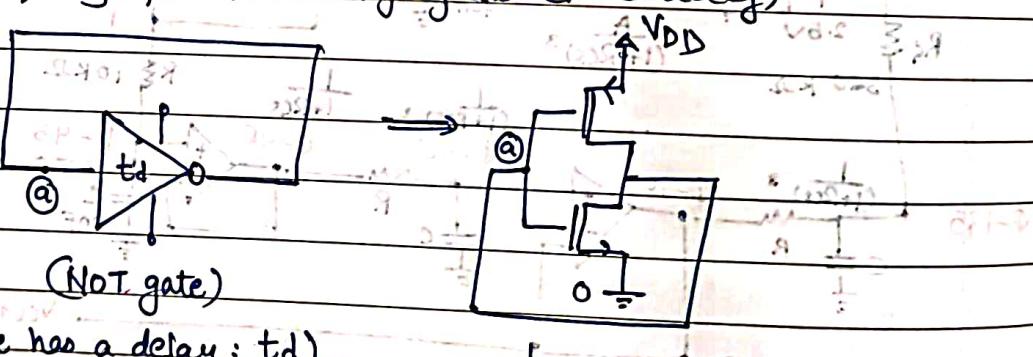
negative

frequency response of the circuit

A NOT & also dual
(odd + 1)

Oscillators Using Logic Gates

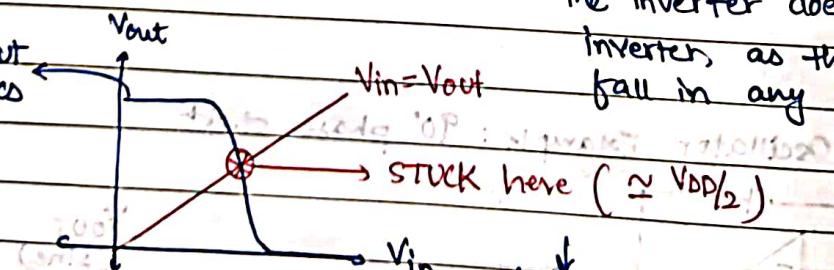
→ phase shift in frequency domain corresponds with delay in time domain
R-C (frequency - phase) → logic gates (time delay)



(Not gate)

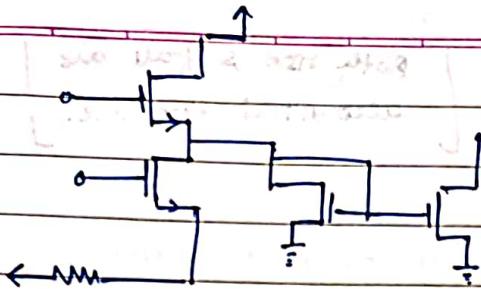
Logic gate has a delay : t_d

input-output characteristics

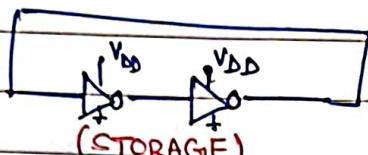


The inverter doesn't operate as an inverter, as the voltage doesn't fall in any logical 0 or 1.

(we can't get an oscillator)



(differential amplifier) + (current mirror)



→ static random-access memory
(STORAGE element)

uses only 2 inverters.

H L H L

$V_{DD}/2$ $V_{DD}/2$ $V_{DD}/2$

$\frac{V_{DD} + V_x}{2}$ $\frac{V_{DD} - V_x}{2}$

$\frac{V_{DD} + V_x}{2}$

+ve

FDBK

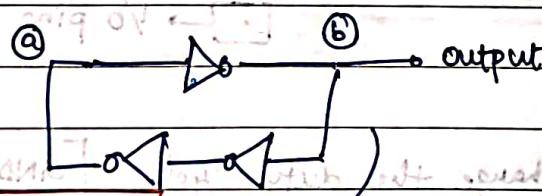
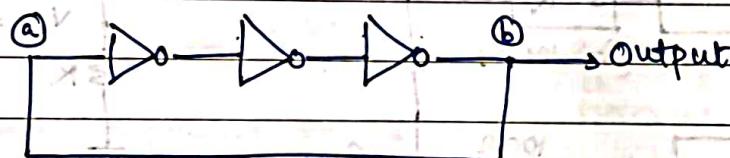
UNSTABLE! inverter gain is very high at $V_{DD}/2$

a very little noise

gain drops, FDBK stops \Rightarrow (can go in any dir^w) from here.

→ 3 inverters

we need a minimum of 3 inverters



RING OSCILLATOR This signal comes after some delay.

all the nodes are identical and have the same type of waveform.

as delays are in picoseconds, $f \rightarrow \infty$:

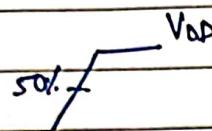
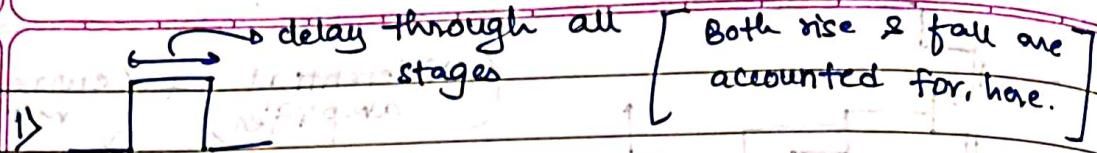
e.g. 91-stage ring-oscillator Higher no. of stages \Rightarrow Better sq. wave

$$T = N \times (t_{dH} + t_{dL})$$

→ NMOS & PMOS ($w-s/s-w/s-s/w-w$)

propagation delays for transition to logic H and logic L, respectively.

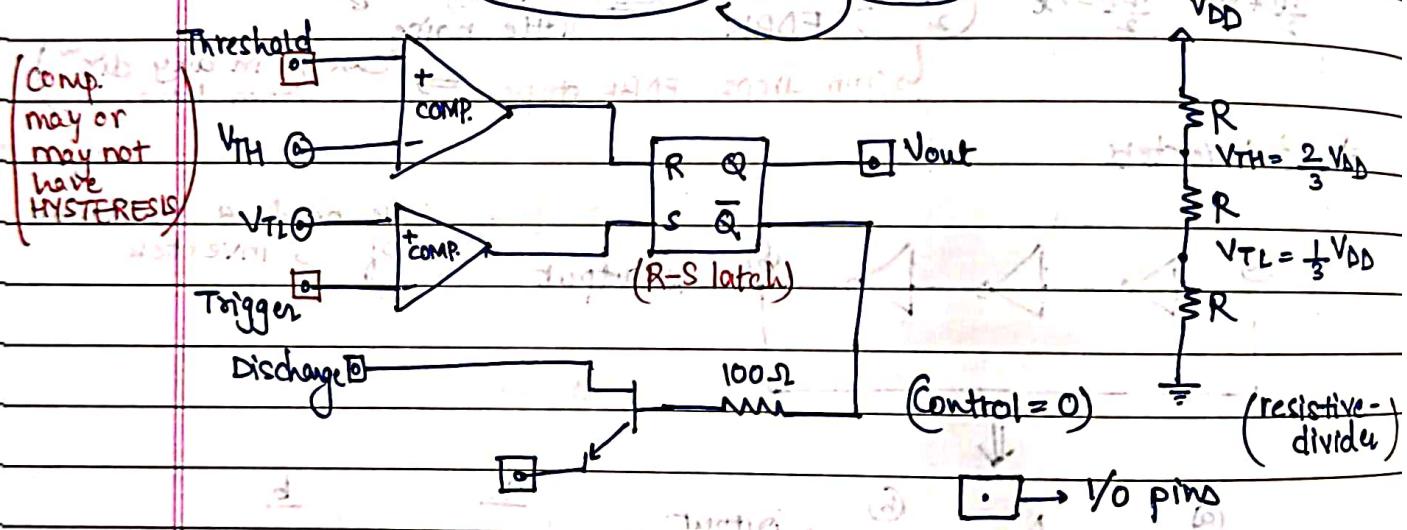
→ used on CMOS chips \rightarrow testing the process corner etc



555 TIMER I.C.

→ Can be programmed to operate as a relaxation oscillator (astable multivibrator) or as a monostable circuit (single-pulse generator).

switching circuit with hysteresis → integrator



→ 2 comparators → hysteresis

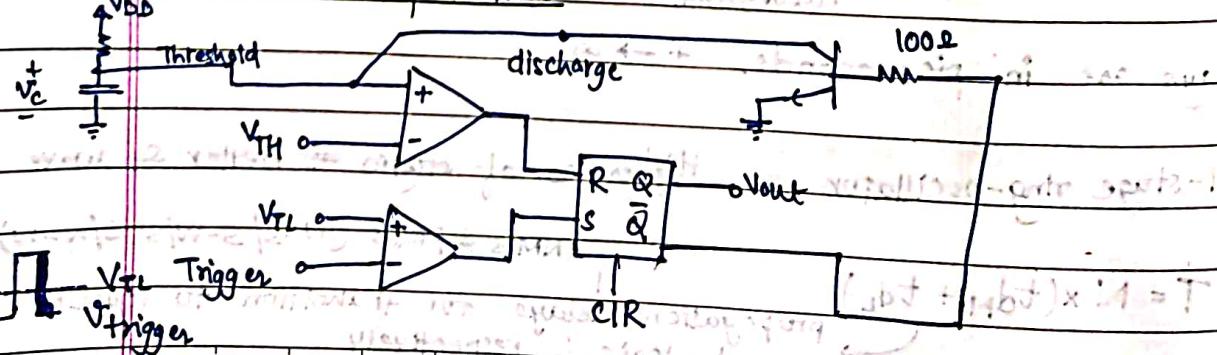
→ V_{TH} can be changed → change the duty cycle. [GND the 2nd resistor]

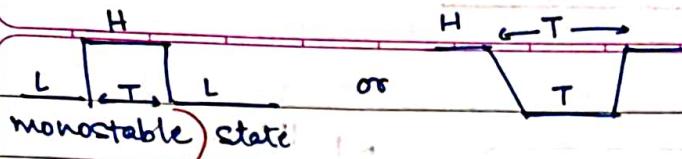
→ when $\bar{Q}=1 \rightarrow Q=0$ → we want I_B to be low (P-N diode)

(B/E is P-N)

→ 100 Ω resistor

Monostable Operation





Trigger specifies when we want to generate the pulse.

↳ start operⁿ of the circuit.

→ charge upto some level (R-C circuit) → voltage reaches V_{TH}
 comparator toggles.

$$\Rightarrow V_{trigger} > V_{TL} \rightarrow S=0$$

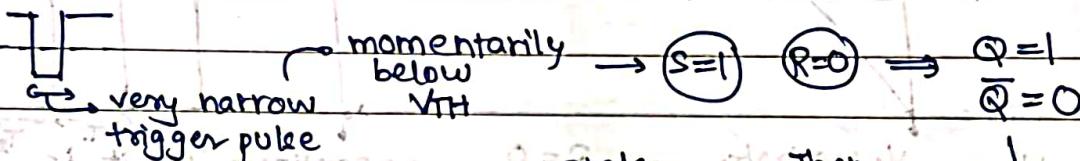
$$\Rightarrow \text{capacitor connected externally / } V_{DD} \text{ is not connected or is at } 0 \rightarrow R=0$$

(TURN IT ON, BUT KEEP)

Initial condition: $R=S=0$

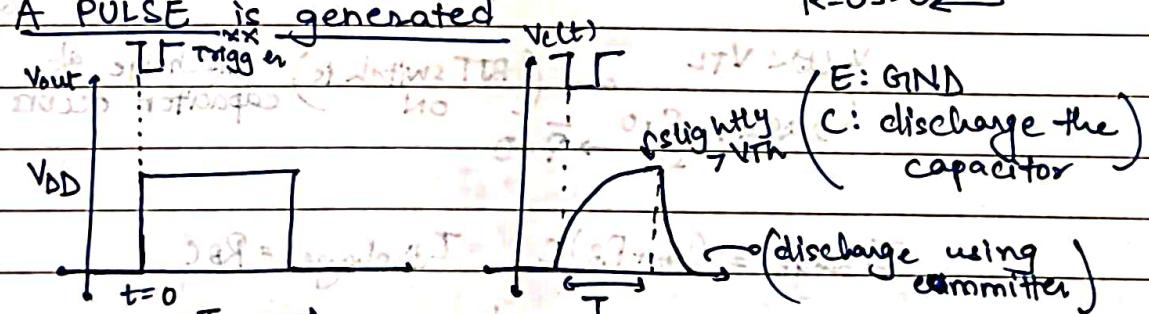
→ preserve the state (NO CHANGE)

FF will be initially reset $\Rightarrow Q$ remains at 0
 \bar{Q} remains at V_{DD} [INITIAL]



other comparator controls when Q goes back to 0 $\rightarrow V_{cap} > V_{TH} \rightarrow R=1 \ S=0 \rightarrow Q=0 \ \bar{Q}=1$

⊕ A PULSE is generated $R=0 \ S=0 \leftarrow$



$$T = RC \quad V_C(t) = 1 - e^{-\frac{t}{RC}} = V_{TH}$$

$$e^{-\frac{t}{RC}} = 1 - \frac{V_{TH}}{V_C}$$

$$t = -RC \ln \left(1 - \frac{V_{TH}}{V_C} \right)$$

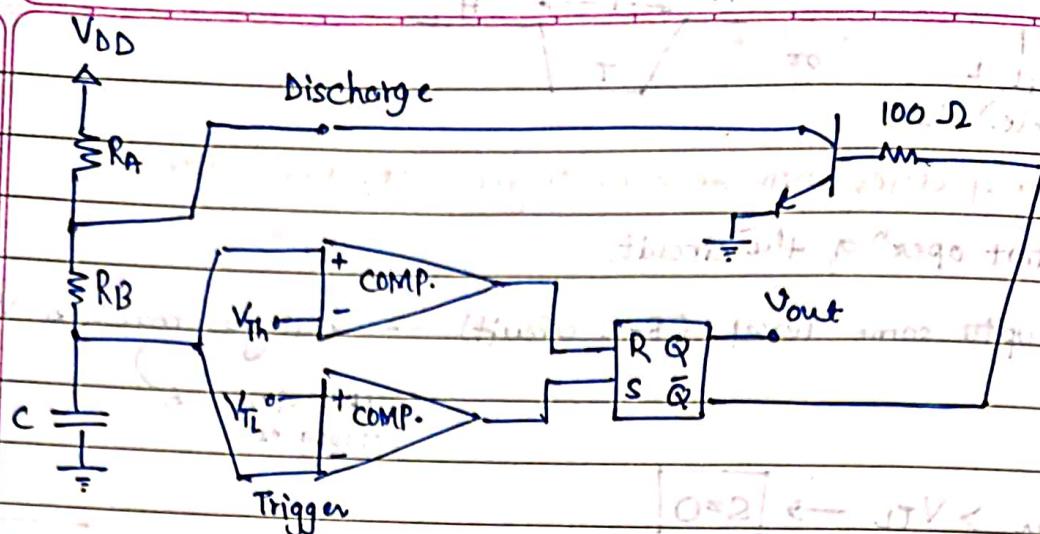
$$t = -RC \ln \left(1 - \frac{V_{TH}}{V_{DD}} \right)$$

$$V_C^\infty = V_{DD}$$

$$T = RC \quad t = -RC \ln \left(1 - \frac{V_{TH}}{V_{DD}} \right)$$

555-Timer : Oscillator Operation

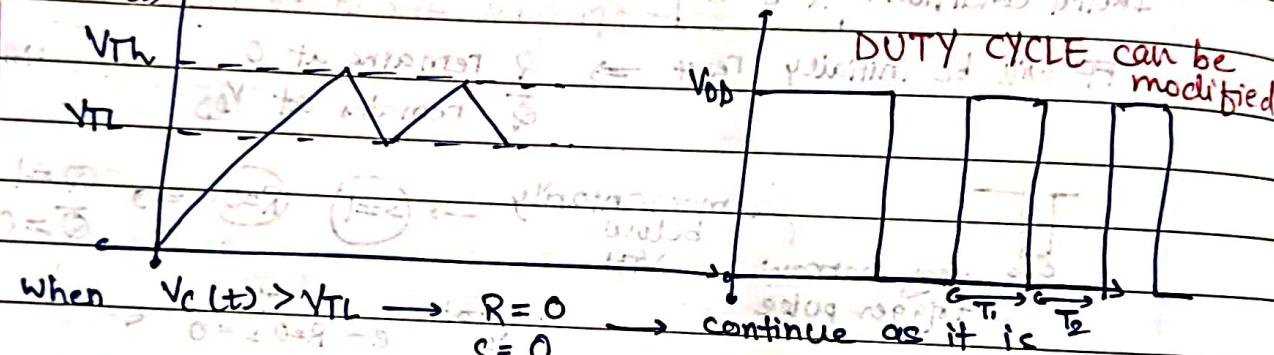
Date _____
Page _____



only difference \Rightarrow we have ② resistors

\rightarrow initially $\rightarrow S=1, R=0 \Rightarrow Q=1, \bar{Q}=0$

$V_c(t)$ V_{TH} V_{TL} V_{DD} $V_{out}(t)$ $Q=Q(t)$ or $V_{out}(t)$



When $V_c(t) > V_{TH} \rightarrow R=0, S=0$

continue as it is
 $as soon as V_c(t) = V_{TH} (\text{slightly above}) \rightarrow R=1, S=0 \Rightarrow \text{Toggle}, Q=0, \bar{Q}=1$

$V_c(t) < V_{TL}$ \leftarrow (BJT switch is ON) \rightarrow discharge of capacitor occurs
again $R=0, S=1 \rightarrow \bar{Q}=0$

$$T_{charge} = (R_A + R_B)C \quad T_{discharge} = R_B C$$

$$V_c(t) = A_1 + A_2 e^{-\frac{t}{T_{charge}}}$$

$$(A_1 = V_{DD}, A_2 = V_{TL} - V_{DD})$$

$$and \quad V_c(t) = B_2 e^{-\frac{t}{T_{discharge}}} \quad (B_2 = V_{TH})$$

$$T_1 = T_{charge} \ln \left(\frac{V_{DD} - V_{TH}}{V_{DD} - V_{TL}} \right)$$

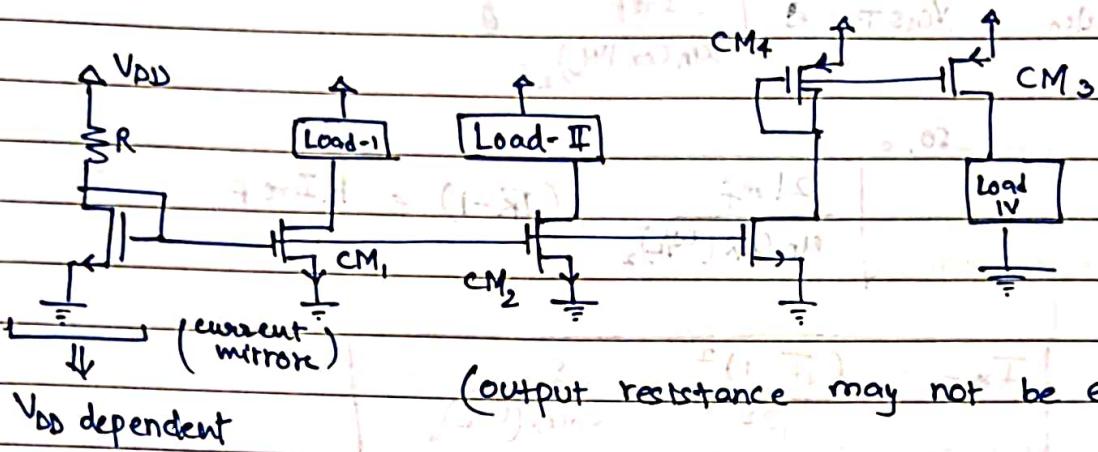
$$T_2 = T_{discharge} \ln \left(\frac{V_{TH}}{V_{TL}} \right)$$

Transistor Level Reference Current Generator

→ NO NEED TO MAKE HOWLAND CURRENT SOURCE !!

→ This is the simplest transistor level current source.

(C.M.:
current
mirror)

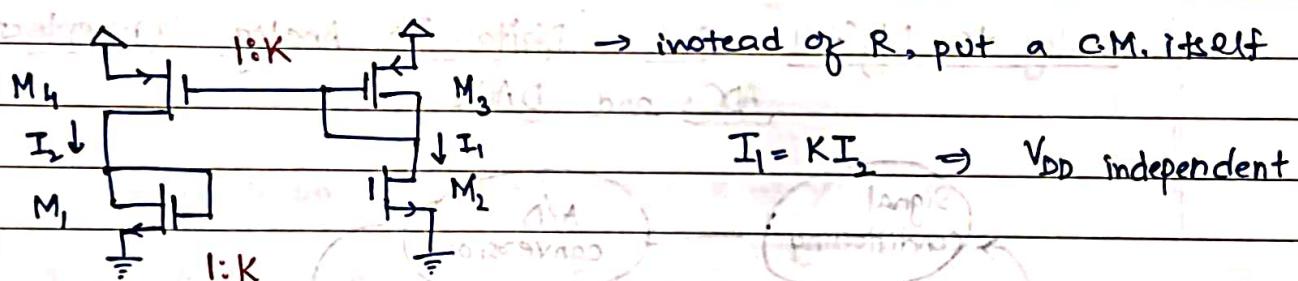


(output resistance may not be enough)

→ Long-length of channel in transistor ~~resistor~~ ($r_o \downarrow$)

→ A differential amplifier of p-MOS transistors has C.S. across source.

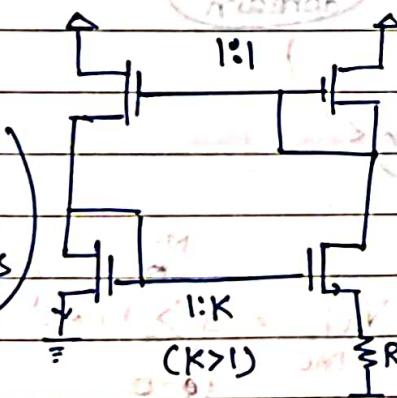
→ Adding one eqⁿ to avoid dependency on V_{DD} .



(Two stacked current mirrors)

CONSTANT g_m CURRENT SOURCE

(Long
channel
length
transistors)



$$I_1 = I_2 = I_{ref}$$

$$V_{GSI_1} = V_{GSI_2} + V_{ref}$$

$$V_{GSI_1} = V_{GSI_2} + I_{ref} \cdot R$$

$(V_{GSI_2} < V_{GSI_1}$,
aspect ratio $K > 1$)

$$\frac{Un Cox}{2} \left(\frac{W}{L} \right)_1, V_{GST_1} = \frac{Un Cox}{2} \left(\frac{W}{L} \right)_1 \cdot K \left(V_{GST_2} \right)^2$$

$$\Rightarrow \left[\frac{W}{L} \right]_2 = K \cdot \left[\frac{W}{L} \right]_1$$

$$V_{GST_1} = K \cdot V_{GST_2}$$

$$V_{GST_1} = \sqrt{K} \cdot V_{GST_2} \quad \text{--- (1)}$$

$$V_{GST_1} = V_{GST_2} + R I_{ref} \quad \text{--- (2)}$$

$$V_{GST_2} (\sqrt{K} - 1) = I_{ref} \cdot R$$

(Known)

Here, $V_{DD} = |V_{DS_3}| + V_{GS_1}$, and $|V_{DS_3}| > V_{min}$.

also, $V_{GST_2} \Rightarrow$

$$\frac{2I_{ref}}{e_{nCox}(w_L)_2}$$

so,

$$\frac{2I_{ref}}{e_{nCox}(w_L)_2} (JK-1) = RI_{ref}$$

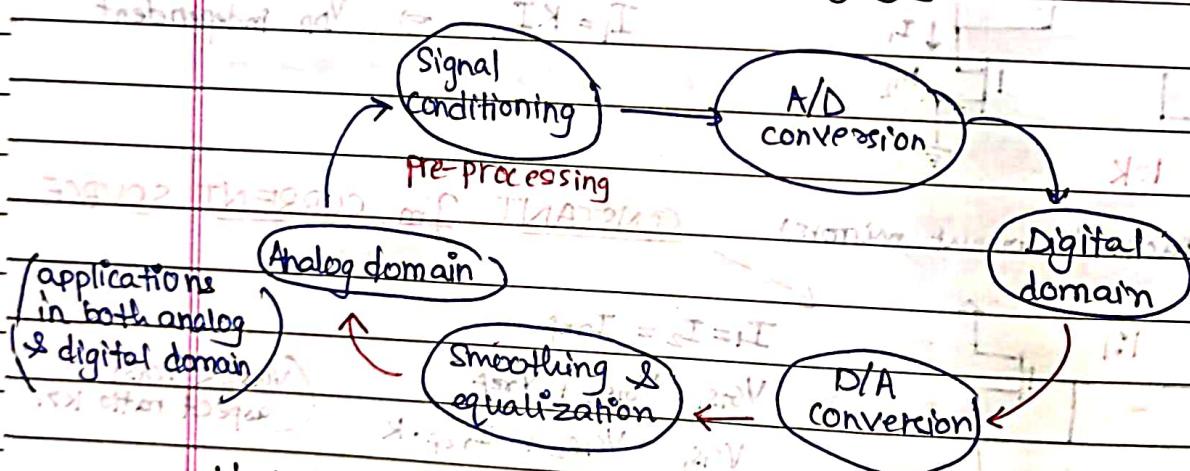
$$I_{ref} = \frac{(\sqrt{K}-1)^2}{R^2} \times \frac{2}{e_{nCox}(w_L)_2}$$

$$g_m = \frac{2I_{ref}}{V_{GST_2}} = \frac{2I_{ref}}{RI_{ref}} (\sqrt{K}-1) \Rightarrow g_m = \frac{2(\sqrt{K}-1)}{R}$$

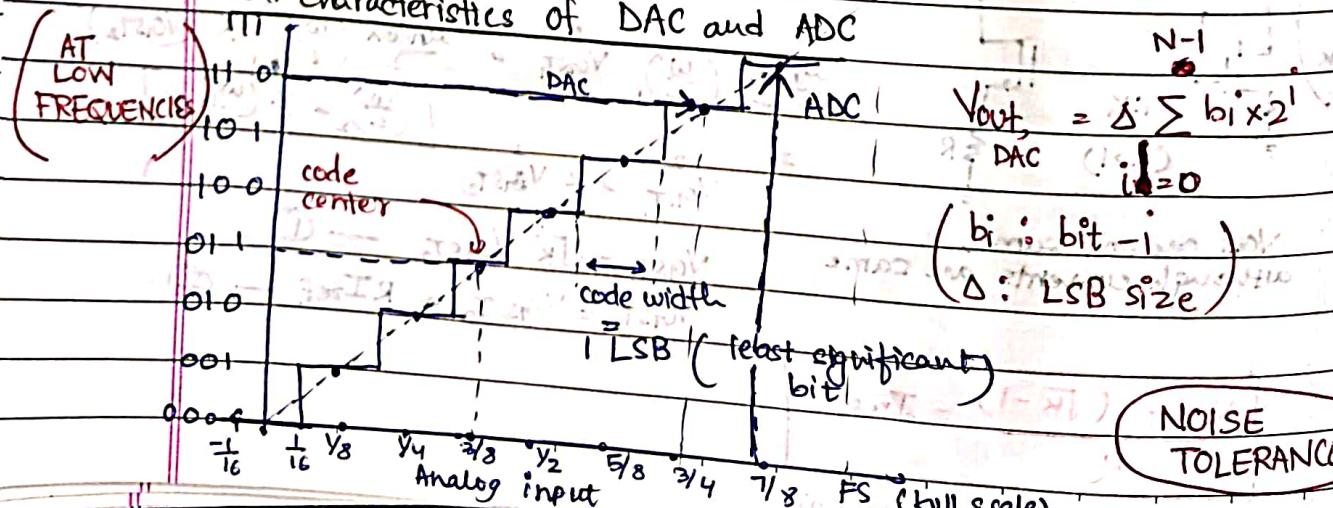
Many applications
constant g_m
if R is constant.

Analog to Digital and Digital To Analog Converters

ADC's and DAC's



Ideal characteristics of DAC and ADC



→ You loose info. : $(A \rightarrow D)$ $b_2 b_1 b_0 \rightarrow$ 3 digit code; $b_i = 1/0$

→ codes are monotonic →

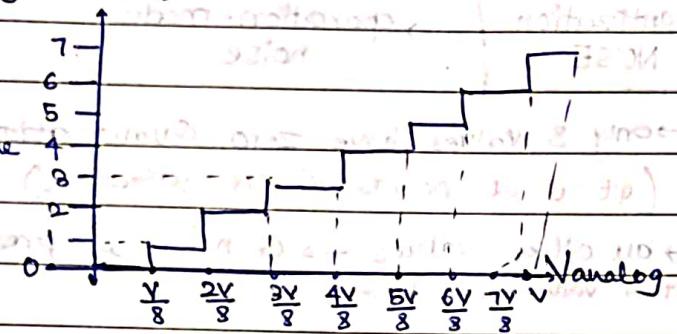
$$[0 \text{ } V_{FS}/8] \rightarrow 000$$

$$[V_{FS}/8 \text{ } V_{FS}/4] \rightarrow 001$$

one method

mapping ∞ values to one single code & losing info
Digital code

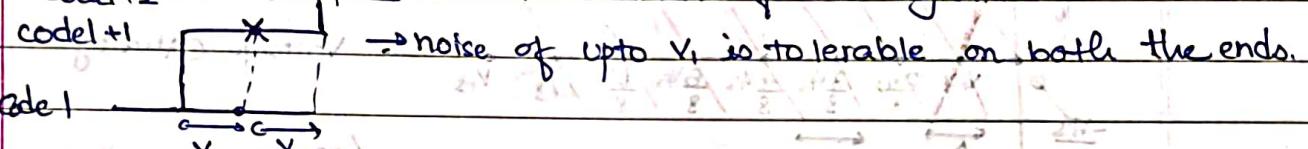
Mapping to the boundary & not the centre of the interval.



Transition at the end point of the intervals

a little noise will cause decision to go wrong.

→ More transition points to the middle of the region.



→ Interval I : $[\frac{1}{16}, \frac{3}{16}] \rightarrow [\frac{3}{16}, \frac{5}{16}], [\frac{5}{16}, \frac{7}{16}], \dots$

$$\text{also, } [-V_{FS}/16, V_{FS}/16] \rightarrow 000$$

⇒ DAC: maps Y on X ; ADC: maps X on Y.

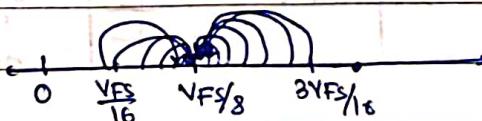
⇒ $V_{DD} = 1.8V$ → range is $0.15 \text{ to } 1.65V$ [analogous to common-mode]
 $V_{FS} = 1.5V$

$$\rightarrow \text{range is } \left[-\frac{V_{FS}}{2}, \frac{V_{FS}}{2} \right]$$

[" "]
diff.-mode

⇒ LSB ⇒ size of interval → $\frac{V_{FS}}{8}$ for 3-bit DAC

⇒ The 8 values are quantized → Quantization



$$\left[\frac{V_{FS}}{16}, \frac{3V_{FS}}{16} \right] \rightarrow \left\{ \frac{V_{FS}}{8} \right\}$$

(Quantized levels)

all of them are showing one single value

→ linearity → we don't want distortions

↳ as close to ideal as possible.

QUANTIZATION

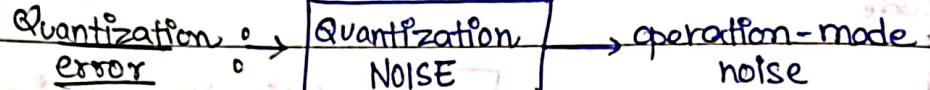
> Analog signals are time-varying \rightarrow by the time we sample the signal might change

$$\text{as } N \uparrow \Rightarrow \Delta = \frac{V_{FS}}{2^N}$$

$$900 \rightarrow (V_{FS}/2)$$

$$\text{resol}^n: \Delta = \frac{V_{FS}}{2^N}$$

Δ : resolution \rightarrow more finer



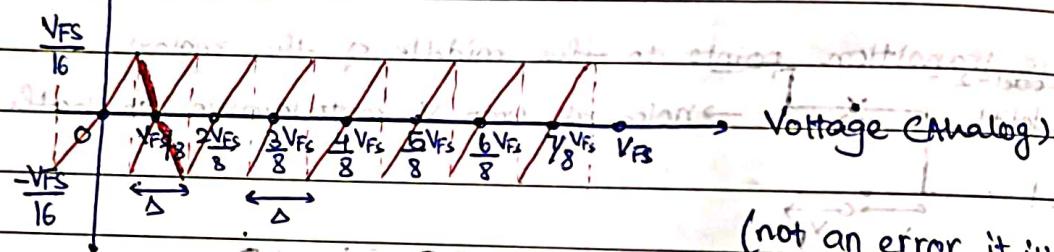
Quantization noise

noise

→ only 8 values have zero Quantization noise/error
($Q.E=0$ at points of Quantization)

→ all other values \rightarrow Q. noise is present

$$\text{Quantization Noise} = (\text{Actual Value}) - (\text{Code Value})$$



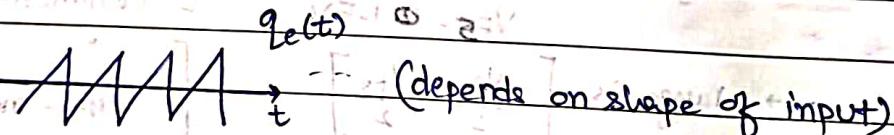
(not an error, it just happens)

Why not $N=20$ and $N=8$ for audio?

Quantization noise is there \rightarrow push it to higher frequencies ($T \uparrow \rightarrow$ lesser $f \downarrow$) \Rightarrow Effective no. of bits

Quantization Error in IDEAL ADC

Signal to Quantization Noise Ratio (SQNR)



$$q_e(t) \rightarrow \text{avg. power of noise } (e) \Rightarrow \int_{-\infty}^{+\infty} e^2 \cdot p(e, t) \, dt$$

$P = 1/\Delta$ \leftarrow uniform RV \leftarrow probability of e

$$\text{so, } P_{\text{Q.Noise}} = \int_{-\Delta/2}^{\Delta/2} e^2 \cdot \frac{1}{\Delta} \cdot de \Rightarrow \langle P_{\text{Q.noise}} \rangle = \frac{\Delta^2}{12} \quad \text{if equally uniformly distributed}$$

(ideal instrument)

$$\frac{\Delta^2}{12} = \frac{V_{FS}^2}{(2^N)^2 \times 12}$$

For a sine wave with amplitude ~~A~~ A ,

$$\langle P \rangle = A^2$$

$$\text{so, } P_{\text{rms}} = \frac{A^2}{2\sqrt{2}}$$

max. amplitude sine-wave with amplitude V_{FS}

$$\Rightarrow P_{RMS} = \frac{V_{FS}^2}{2\sqrt{2}}$$

$$x_{RMS} = \frac{V_{FS}}{\sqrt{2}}$$

best possible sine wave has this as RMS amplitude/ $\sqrt{2}$

For a sinusoidal signal $x(t)$ & approx. uniform distrib' of q_e .

Best $SQNR = 10 \log \left(\frac{x_{RMS}}{q_e} \right) \Rightarrow SQNR = 6.02N + 1.76 \text{ dB}$

$$N=6 \rightarrow SQNR = 37.9 \text{ dB}$$

$$N=10 \rightarrow SQNR = 62.0 \text{ dB}$$

NYQUIST RATE ADC's

(Converting A to D when time comes into the picture)

→ How fast can we do the conversion?

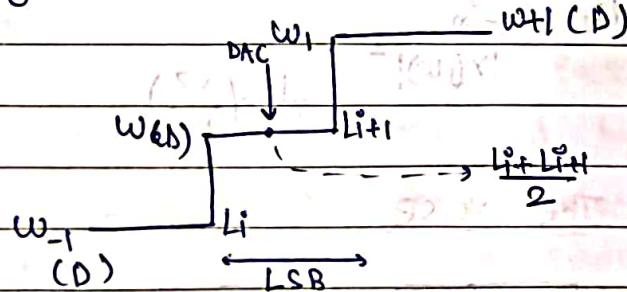
$$f_s > 2f_m \rightarrow \text{aliasing}$$

→ If we increase the sampling frequency \rightarrow gap b/w samples (aliased)

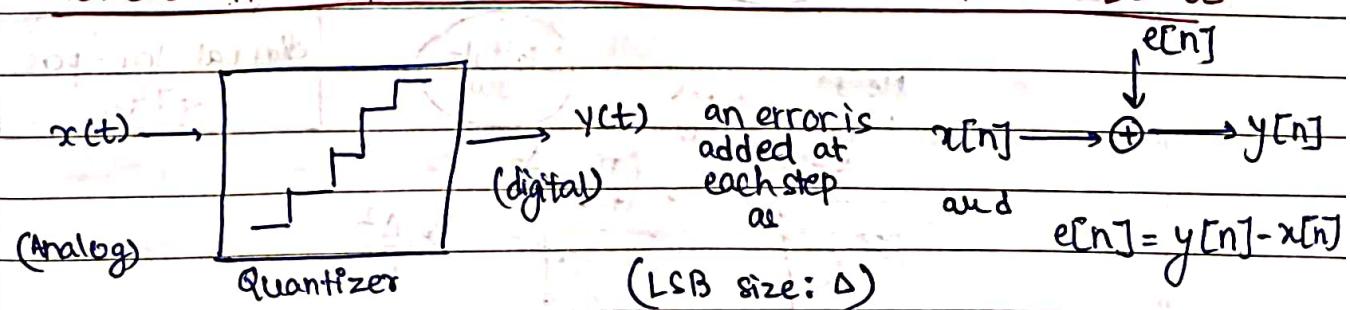
↳ very high frequency \rightarrow switching noise

⇒ w.r.t. sampling $\begin{cases} \text{Nyquist-Rate ADC's/DAC's } (f_s \text{ close but more than } 2f_{max}) \\ \text{Over-sampling data conversion } (\text{much higher above } 2f_{max}) \end{cases}$

Digital Code (word) $\rightarrow w$



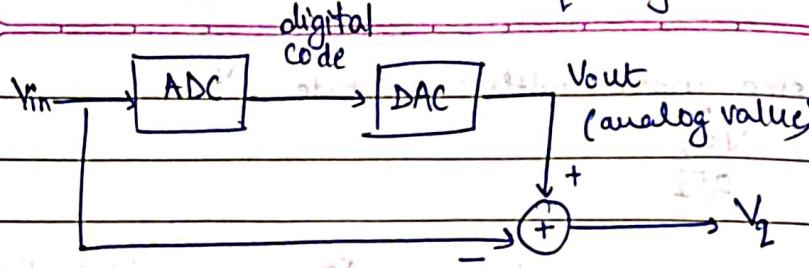
MODELLING OF QUANTIZATION NOISE AT SYSTEM LEVEL



Q. noise depends on the STEP SIZE only

it doesn't depend on the sampling frequency.

Sampling at higher frequencies reduces the noise over signal band.



The input may have a single frequency → Q.E. has rapid changes and so has a lot of different frequency components.

Power Spectral Density: How the power of a signal / time series is distributed over frequency.

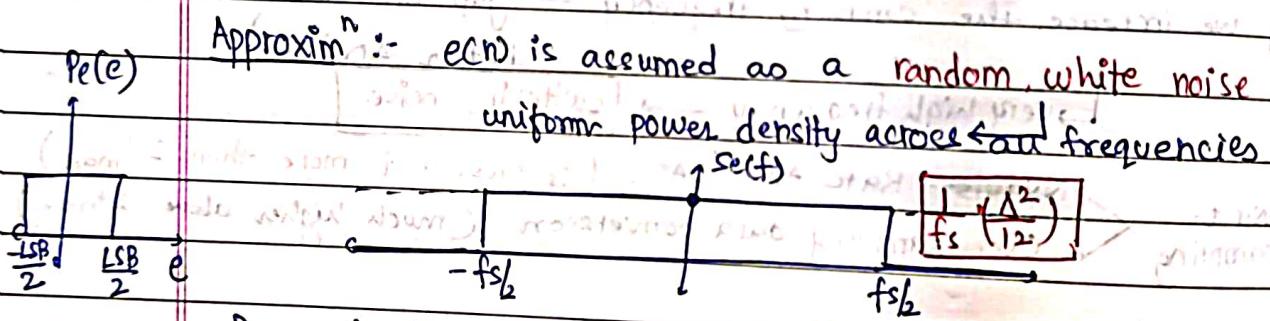
$$P_{\text{avg}} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\infty}^{+\infty} |x_T(t)|^2 dt$$

Parseval's theorem $\Rightarrow P = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\infty}^{+\infty} |\hat{x}_T(f)|^2 df$

avg. power of noise in diff. frequency bands

$$S_{xx}(f) = \lim_{T \rightarrow \infty} \frac{1}{T} |\hat{x}_T(f)|^2$$

power spectral density $F(\bar{x}(-t) * x(t))$



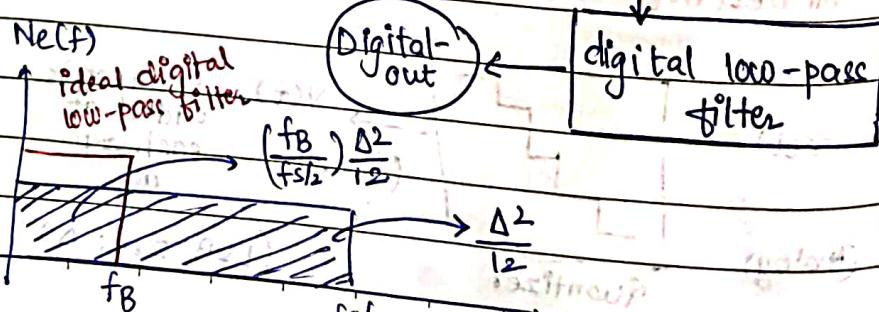
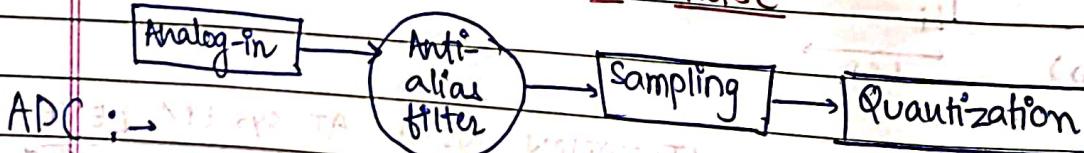
Parseval's theorem:-

$$\frac{\Delta^2}{12} = \int_{-\infty}^{+\infty} |X(j\omega)|^2 d\omega = |X(j\omega)|^2 \cdot \frac{1}{2\pi}$$

$$\text{Height, } K_x = \frac{\Delta}{\sqrt{2}} \cdot \frac{1}{\sqrt{fs}}$$

$$|X(j\omega)|^2 = \frac{1}{fs} \cdot \left(\frac{\Delta^2}{12} \right)$$

DIGITAL FILTERING OF THE NOISE



$$\frac{P_{noise}}{OSR} = P_{noise} (\text{new resol'n})$$

$$\frac{1}{2^{2n} OSR} = \frac{1}{2^{2n}}$$

$$OSR = 2^K$$

$$n' = n + K/2$$

increased resolution $\frac{1}{2} \log_{10}(OSR)$

- We filter out the noise beyond the signal frequency band.
- Here, we reduce the in-band Q. noise to achieve higher resol'n.
- Total Q. noise power is reduced by the factor

$$\left(\frac{f_s/2}{f_B}\right) \rightarrow \text{oversampling ratio}$$



$$\frac{f_s}{2 \cdot f_B}$$

2x BW of input signal

ratio of the sampling frequency to the Nyquist frequency of the input signal

~~the ratio~~

→ resolution of oversampled converter \propto OSR

→ BW of input signal $\propto \frac{1}{OSR}$

To increase resolution → give up f_B and make $f_B < (f_s/2)$.
give up B.W. for precision.



SQNR improvement By Oversampling

→ The total Q. power (noise) is reduced by oversampling, let the oversampling ratio be OSR:

→ Then, $SQNR = 10 \log_{10} \left(\frac{P_{sig} \times OSR}{P_{noise}} \right)$

\Rightarrow factor by which Q.noise is reduced

$$SQNR = 6.02N + 1.76 + 10 \log_{10}(OSR)$$

e.g. $OSR = 2$

→ SQNR increased by a factor 2 in linear scale (3dB in dB scale)
→ Resolution is increased by 0.5 bits

similar to
averaging

$OSR = 4 \rightarrow 1\text{-bit extra resolution (6 dB)}$

~~n/2~~: $OSR = 2$ bits

$OSR = 16 \rightarrow 2\text{-bit extra resolution (12 dB)}$

$OSR = 64 \rightarrow 3\text{-bit extra resolution (18 dB)}$

not an ideal LPF

e.g. assume $f_B = 500 \text{ kHz}$ and (ADC) resolution = 8 bits

if target resolution = 14 bits, ~~6dB~~ $\rightarrow OSR = 4$

~~6 bits~~: $OSR = 2^{6/0.5} = 4096$

$$\frac{f_B}{fs/2} = \frac{1}{4096} \Rightarrow fs = 4096 \times 2 \times 0.5 \text{ MHz}$$

$$fs = 4096 \text{ MHz}$$

(OVERSAMPLING IS NOT ENOUGH)

NYQUIST - RATE ADC's

- Nyquist-rate → Word-at-a-time

FLASH ADC's

instantaneous comparison with 2^B-1 reference levels.

WORD-AT-A-TIME

→ One comparator-per-transition point

→ Transition points:

$$\left(\frac{1}{2}\text{ LSB}\right) \text{ to } \left(2^N - 1 - \frac{1}{2}\right) \text{ LSB}$$

$$(2 - \frac{1}{2}) \text{ LSB}$$

$$(1 - \frac{1}{2}) \text{ LSB}$$

$$(\frac{3}{2} \text{ LSB})$$

for $N=3$, upto

$$(7 - \frac{1}{2}) \text{ LSB}$$

→ Each comparator identifies

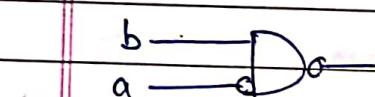
start of a segment, not middle

→ All comparators operate simultaneously.

FLASH-ADC

$$I = \frac{V_{ref}}{8R} \cdot \frac{R}{2}$$

May be set to V_{DD} if over range not needed.



a b c

$0 \quad 0 \quad 0 \quad 1$

$0 \quad 1 \quad 0$

$1 \quad 0 \quad 1$

$1 \quad 1 \quad 1$

it gives 0 at point

where lower comparator

is 1 and upper comparator

is 0 i.e.

say COMP 5V4 COMP6 X

voltage lies b/w 5 & 6

Thermometer code

→ Very fast → can be just 1 conversion per 2 clock phases

analog input voltage

PC sampled & held

sampling

decision

comparators

perform their operation

- A sample and hold circuit is used \rightarrow ADC holds that input voltage at a const. level throughout duration of sampling phase (T&H stage (Track-and-hold)) \rightarrow may/may-not be used
- Size :- $(2^N - 1)$ comparators + 2^N resistors of equal R values if a resistive ladder is used
 \downarrow
 (capacitive ladder ?)
- Loading at the input = $Z_{in\ (comp.)} \times (2^N - 1)$
- Condition :- $|V_{in, os\ (comp.)}| < (LSB/2)$
 \downarrow
 Non-linearities arise due to input-dependent $V_{in, os}$.
- Kickback noise of the comparator to be taken care.

