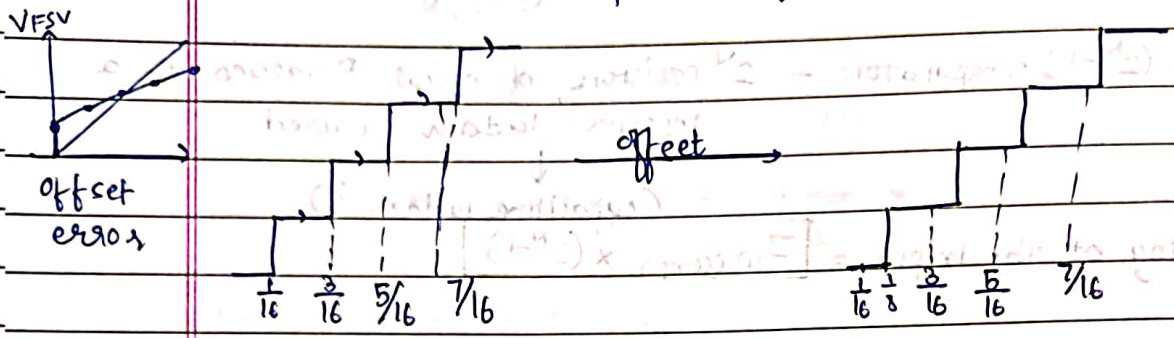
$V_{\text{Full scale value}} = (1 - 2^{-N}) V_{FSR}$ ($V_{FSV} = V_{FSR} - 1LSB$) $\left(\frac{V_{FSR}}{2^N}\right)$

Date
Page

OFFSET ERROR
(Zero scale error)

→ it is the shift of the first transition point and subsequently all other transition points shift.



→ All the comparators in the ADC are matched, but all have an offs

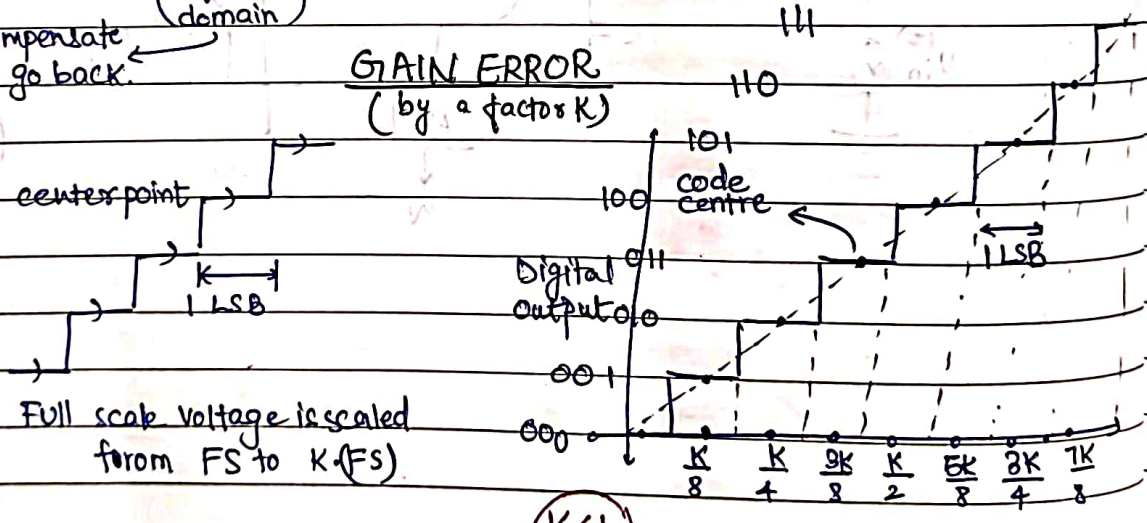
→ Doesn't change any characteristics of the ADC.
↳ (+ve) or (-ve) offsets.

⇒ If the shift is by (Y8) → the last code (111) is missing code

⇒ Detect the shift ⇒ (Soft-DAC) (software domain) becomes 110 ← we dont know what happens after Full-scale.

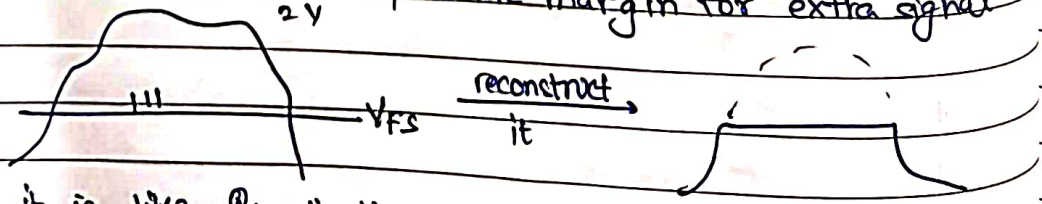
compensate & go back.

GAIN ERROR
(by a factor K)



eg.-

$V_{FS} \longrightarrow V_{P_K P_K}$ → Keep some margin for extra signal



it is like Quantization error, but Q.E. could have been minimized, here it is high.

No. of missing codes = 0

E.N.O.B. ⟶ effective no. of bits (if there are missing codes)

INTRODUCTION TO INL and DNL

Integrated Non-Linearity ↳ Differential Non-Linearity

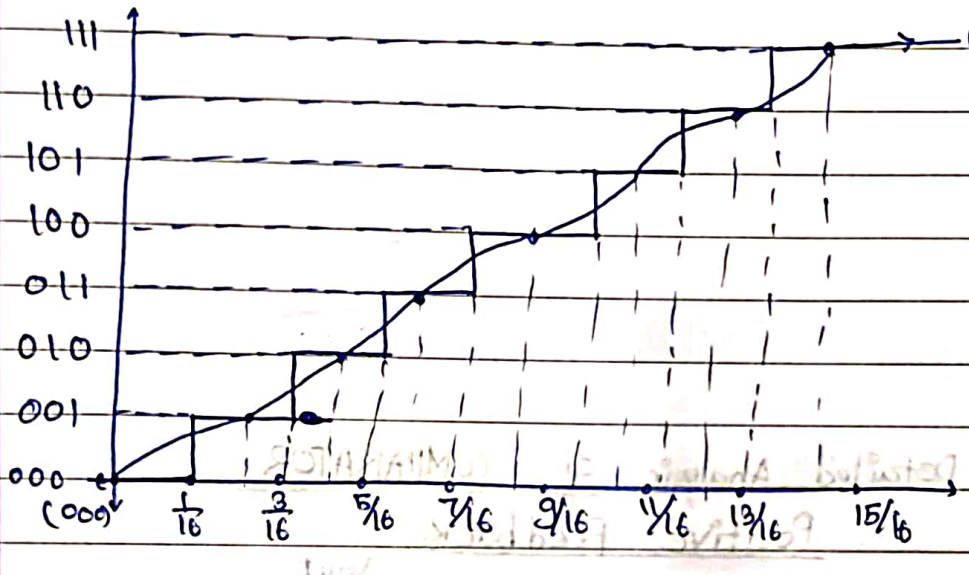
1) Monotonic
2) No missing code

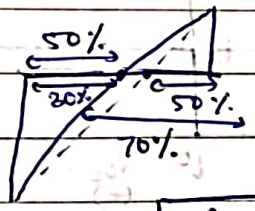
reduce errors → control matching of resistors
↳ comparators offset $\ll$ LSB/2

⇒ LSB size changes with code ⟶ Non linearity

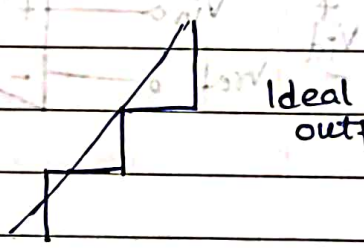
DNL and INL are extracted after offset correction

(distortion is allowed as long as it is acceptable)



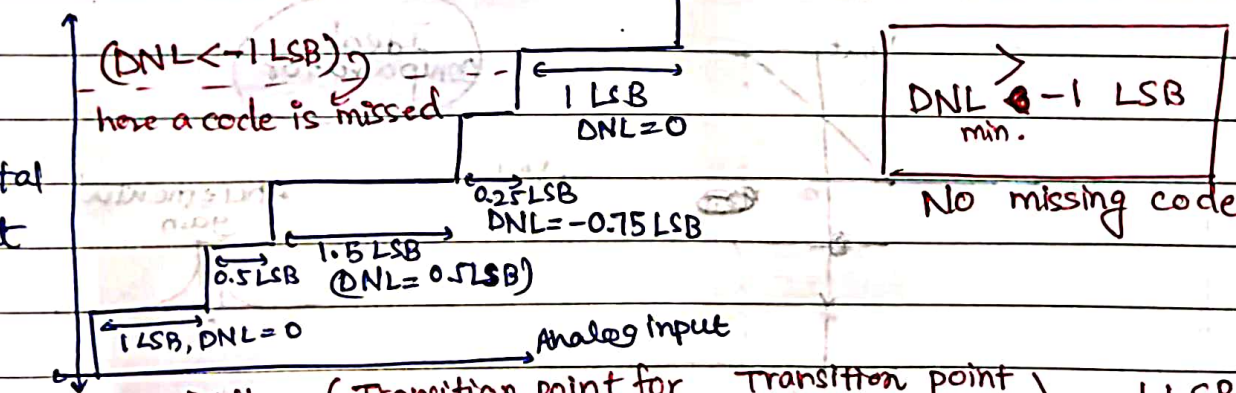


so, it is a non-linearity



both are no longer equal.

eg.-



DNL $\geq$ -1 LSB
min.

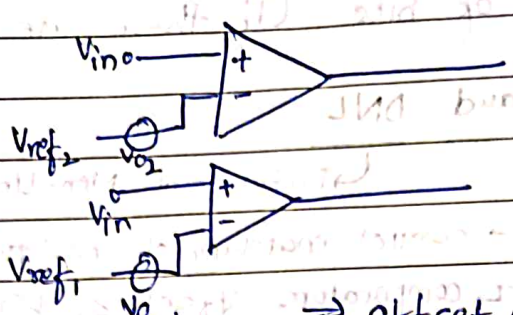
No missing code

DNL, $DNL = (\text{Transition point for code } i - \text{Transition point for code } i-1) - 1\,LSB$

$$INL = (\text{Transition point for code } i) - \frac{(2i-1) \times FS}{2^{N+1}}$$

$1 \leq i \leq 2^N - 1$

Thresholds change here :→



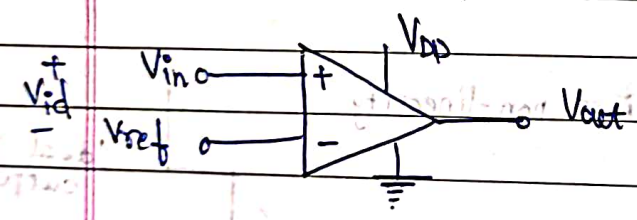
$V_{ref_2} \rightarrow V_{ref_2} + V_{O_2}$

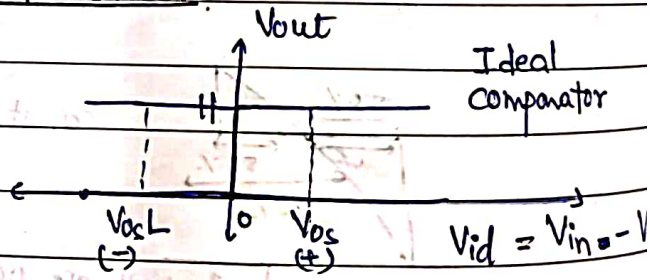
$V_{ref_1} \rightarrow V_{ref_1} + V_{O_1}$

⇒ offset errors in comparators change the threshold values.

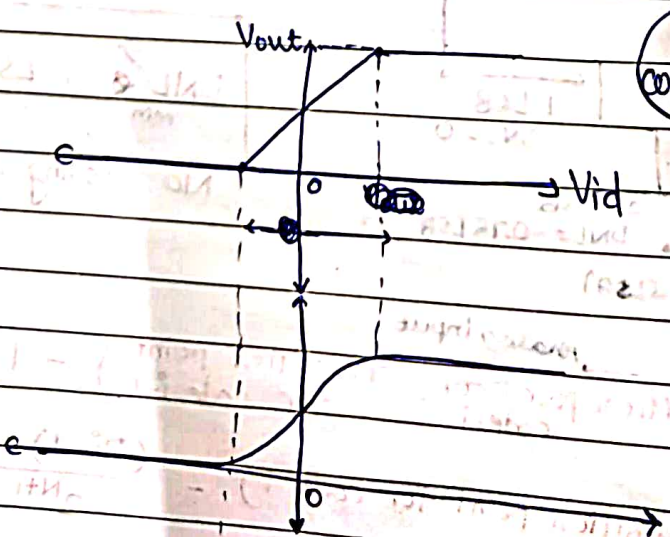
Detailed Analysis of COMPARATOR

Positive Feedback

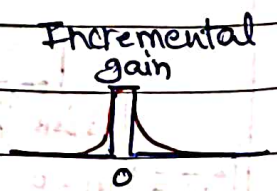




Non linear elements



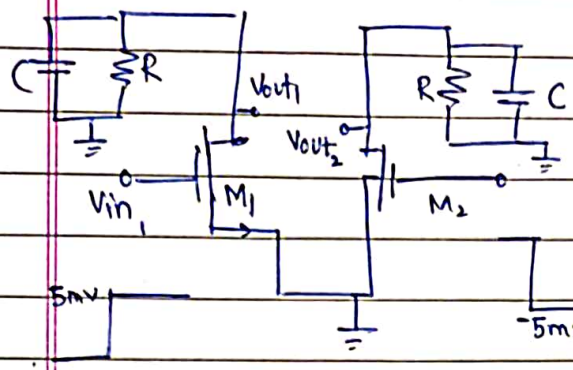
Ideal comparator



$$\frac{dV_{out}}{dV_{id}} = \frac{\Delta V_{out}}{\Delta V_{id}}$$

→ gain can't be ∞

FULLY-DIFFERENTIAL COMPARATOR

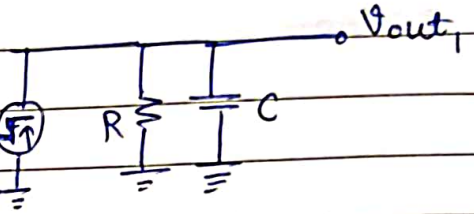


$V_{in_1}(t) = V_{CM} + V_{id}/2\,(t)$

$V_{in_2}(t) = V_{CM} - V_{id}/2\,(t)$

$V_{id}(t) = \boxed{10mV\ u(t)}$ (Here)

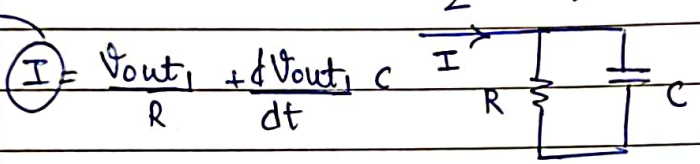
Differential-mode analysis :



$V_{gs_1} = V_1 (u(t))$

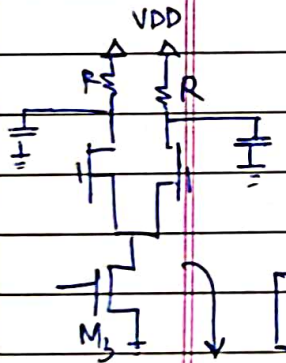
So, $V_{out_1} = -g_m \frac{V_{id}}{2} R \left[e^{-t/\tau} - 1\right] u(t)$

constant w.r.t. Vout



$I = \frac{V_{out_1}}{R} + \frac{d V_{out_1}}{dt} C$

$\frac{I - V}{R} = C\frac{dV}{dt} \Rightarrow \frac{IR - V}{RC} = \frac{dV}{dt}$



$\int_0^t \frac{-1}{RC} dt = \int \frac{dV}{V - IR} \Rightarrow \ln\left(\left|\frac{V - IR}{(V - IR)_0}\right|\right) = \frac{-t}{RC}$

$-V + IR = +IR\, e^{-t/\tau}$

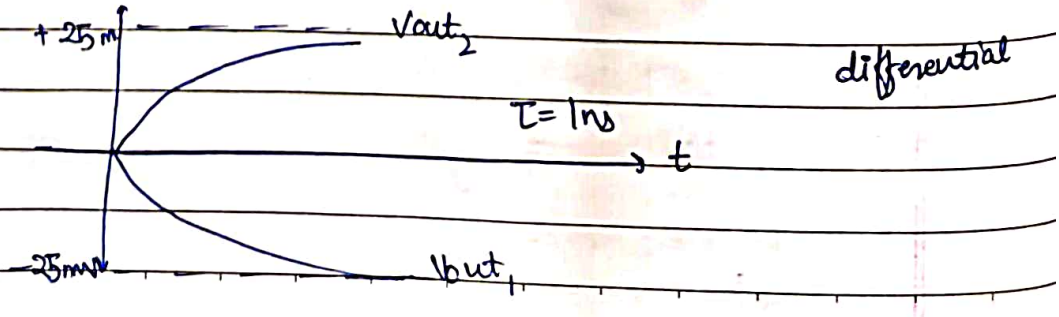
$-V = IR\,(-1 + e^{-t/\tau})$, so, $\boxed{V_{out}(t) = +g_m \frac{V_{id}}{2} R\,(e^{-t/\tau} - 1)\,u(t)}$

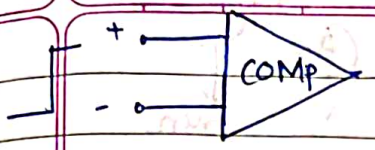
$\boxed{V_{out}(t) = g_m R\, V_{id}/2\,(1 - e^{-t/\tau})\,u(t)}$

→ Large signals : $V_{out_1} \Rightarrow V_{out_1} = V_{DD} - R \cdot \frac{I_{D3}}{2}$

So, net $\boxed{V_{out_1} = V_{DD} - R\frac{I_{D3}}{2} + g_m \frac{V_{id}}{2} R\,(e^{-t/\tau} - 1)\,u(t)}$

$g_m = 0.5\ mA/V^2$, $R = 10K\Omega$, $V_{id} = 10mV$, using $C = 0.1pF$, $RC = 1ns$, $V_{out} = V_{DD} - R I_{D3}/2 + 25mV\,(e^{-t/\tau} - t)$

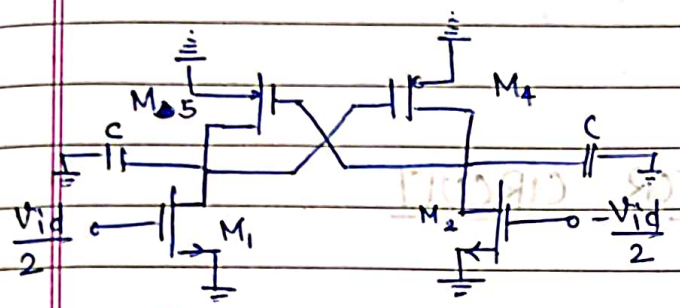




Higher is the magnitude of step ⟹ Faster output

→ To get a faster response → higher magnitude of step i.e. lower resolution.

→ High resolution ⇒ Low magnitude of step ⇒ slower output ∴ → resolution v/s output delay



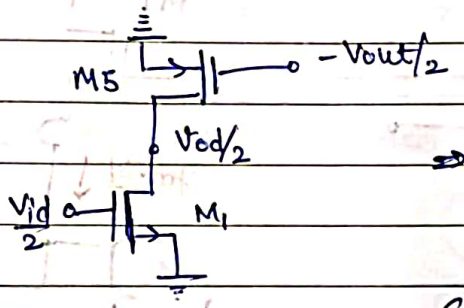
C: source of delay, can't get rid of

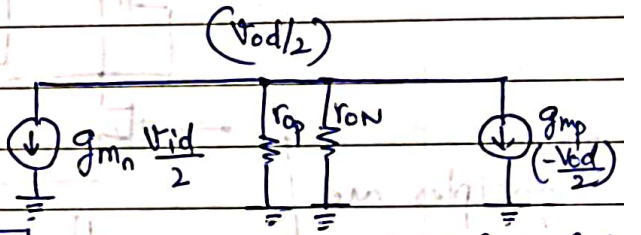
Matched MOSFET's

$M_1 \equiv M_2$; $M_4 \equiv M_5$

resistance : r_{op}, r_{ON}

SS doesn't depend on type of MOSFET





C=0 (assume)

$= (-g_{mp}) \frac{V_{od}}{2}$

(-ve resistor) (cross-coupled resistor)

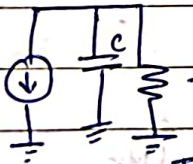
if $g_{mp} > g_{op} + g_{ON}$ → (oscillator)

↳ current source and a -ve resistor

↳ energy grows : regenerative circuit

regenerative +ve feedback loop

↳ push out of active region → STOP ⇒ almost approaching a logic device

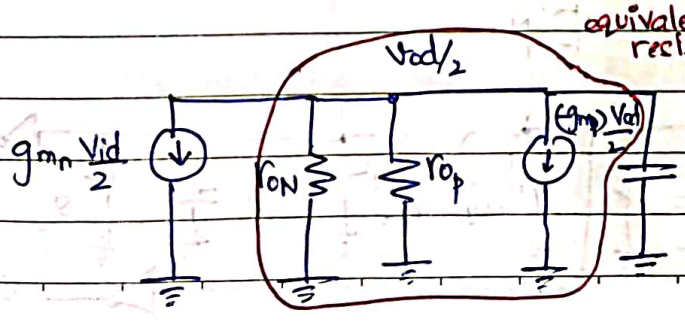


energy is generated : $g_{mp} > g_{ON} + g_{op}$

Positively grown exp^n ($\tau < 0$)

$\tau < 0$

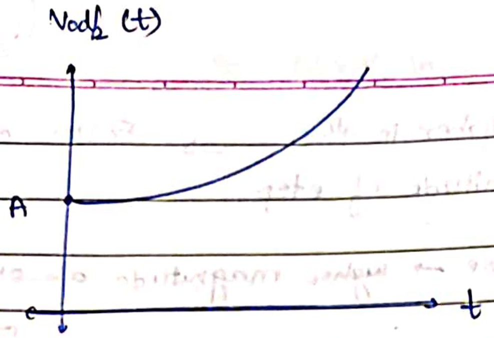
$e^{-t/\tau} \Rightarrow (e^{+x})$: increases with time → growing exponential



$$\frac{V_{od}(t)}{2} = A e^{t/\tau}$$

$$\tau = \frac{C}{g_{mp} - g_{ON} - g_{op}}$$

(growing exponential)



$A e^{t/\tau}$

A → max. (FAST)

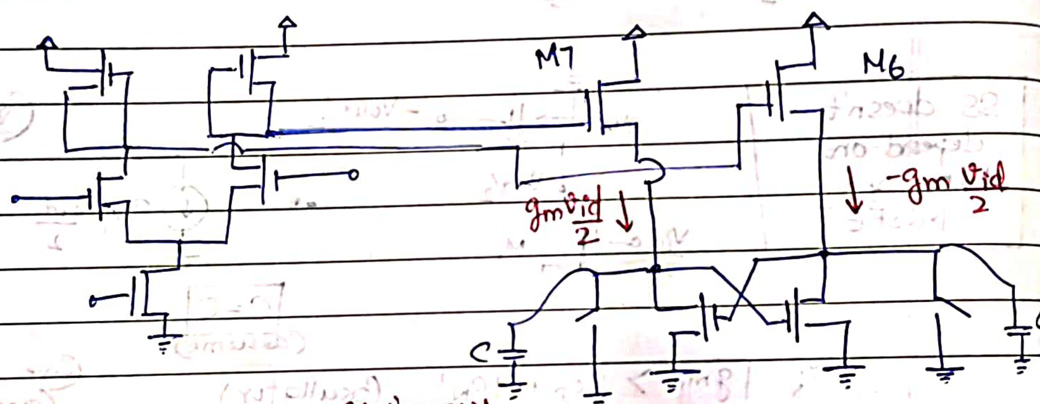
τ → min.

reduce τ and increase A

speed v/s resolution trade-off

FINAL COMPARATOR CIRCUIT

Principles are the same



CAN'T SAY speed → ∞ (C: limit)

output → imbalance, L.S.

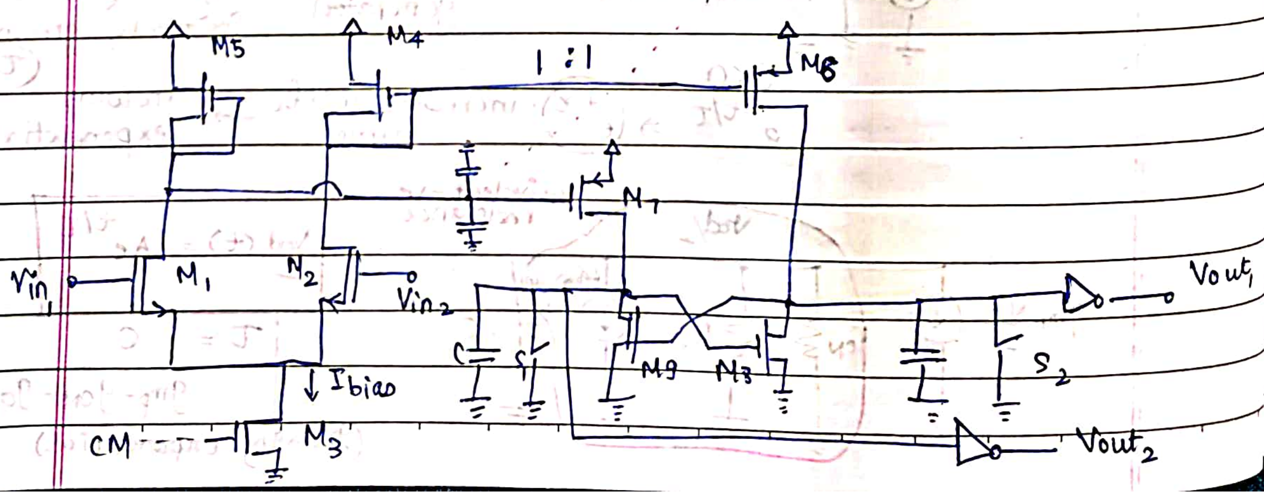
+ve feedback → switches are closed

regenerative circuit : open switches

└→ depending on signs of current

M7, M6 is simply a current mirror

→ analog memory / parasitic capacitances

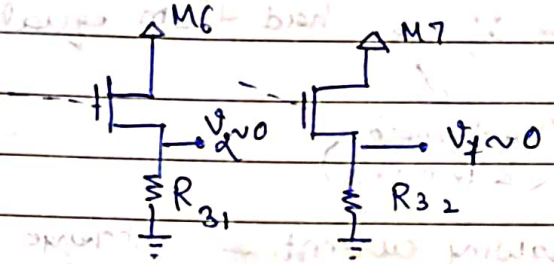


S_1	S_2	
closed	closed	⟶ reset and pre-amp
open	open	⟶ decision making

S_1, S_2 : closed : $I_{M6} = I_{M5} = \underbrace{\frac{I_{bias}}{2}}_{DC} + \frac{\Delta I}{2}$ ⟶ small signal (diff. in inputs)

$$I_{M7} = I_{M8} = \frac{I_{bias}}{2} - \frac{\Delta I}{2}$$

reset & pre-amp

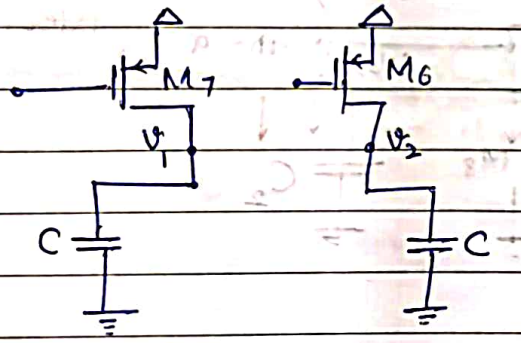


decision-making :-

$t = t_0$ ⟶ S_1 & S_2 are opened ⟶ C won't change instantly

Transistors are OFF ⟵ (can be removed from the circuit)

regenerative circuit



capacitors are charged mainly by $\frac{I_{bias}}{2}$

C: determine V_{gs} of transistors

V_{gs} changes

both are effectively charged by $I_{bias}/2$, but one has $\frac{I_{bias}}{2} + \Delta I$ and other is $\frac{I_{bias}}{2} - \Delta I$

$$C\frac{dV}{dt} \approx \frac{I_{bias}}{2} \Rightarrow C\left(\frac{\Delta V}{\Delta T}\right) \simeq \frac{I_{bias}}{2}$$

M_8 and M_9 has $V_{gs} = V_{cap}$ ⟶ They will turn on when $V_{cap} = V_t$

V_{tn} ⟵ when switches were opened

$\Delta V_C = V_{tn} - V(t_0)$

so, $C\left(\frac{V_{tn} - V(t_0)}{\Delta t}\right) = \frac{I_{bias}}{2}$

So, $\Delta t = \frac{C \Delta V_c}{I_{Bias}} \times 2$ → APPROX.

Delay of turning transistors of reg. circuit ON.

M_6 → less current
M_7 → more current
C charges faster.

→ M_8: leading
M_9: lagging

(left C charges faster) → (right transistor faster) helps the regenerative circuit take the right decision.

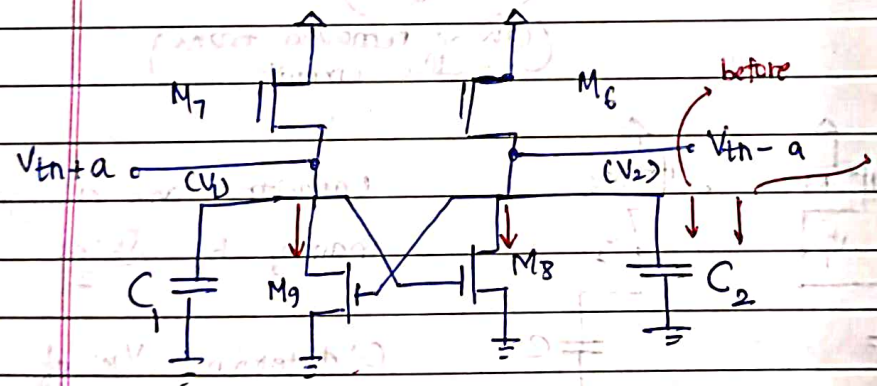
→ Random decision if we had them equal, noise would then decide.

randomness is removed

M_8: starts drawing current → discharge C_{right}

↓

M_9 again turns off ← C_{left} charges upto Vdd ← V_2 was



if a is small (50mV) → both M_8 and M_9 are in moderate region

↓

M_8 will draw more current ← C_2 won't be charged as earlier, trying to be discharged

(drawn) $I_{M_8} > I_{M_9}$

C_2 will receive less current, ← C_1 also will, but charging rate of C_2 will reduce more

→ C_2 current becomes opposite in dir^n when $I_{M_8} > I_{Bias}$, M_9 always lags

∴ M_8 becomes stronger by +ve FDBK.

Date
Page

M_4 turns off or M_1 reaches ohmic region
↓
as V crosses threshold of NOT gate

→ C_1 & C_2 observe red^n in charging current → C_2 gets discharged more or less charged → V_2 will reduce faster

V_1 reaches V_{DD}. ← give it enough time ← V_1 increases ← M_4 draws even less current ← goes below

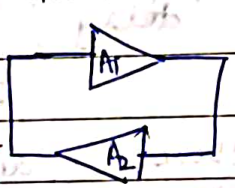
→ Time constant = f(gm) → changing with time.

$V_{in_1} > V_{in_2}$ → ΔI is +ve ⟹ $V_{out_1} \Rightarrow H$, $V_{out_2} \Rightarrow L$
(COMPARATOR)

∞-time : C_1 charges completely, C_2 discharges completely

cross coupled transistors → +ve FDBK

CS amplifier → inverting amplifier



Loop gain, $A_1A_2 > 0$

$A_1, A_2 < 0$

propogation delay of NOT gate

Total delay = D_1 + D_2 + D_3 → circuit itself

$D_2 < D_1$

depends on τ → determined by C

c↓ : D_1↓ → D_2 also ↓

$V_{out_1}(t) = Ae^{t/\tau} = V_{1(t)} - V_{2(t)}$ (discharging)

$\Delta V_{1(t)} = B_1(e^{t/\tau} - 1)$ $\quad$ $\Delta V_{2(t)} = B_2(e^{t/\tau} - 1)$ (clear)

M_8 & M_4 are ON → $\Delta V_1(t) = Be^{t/\tau}$ $\quad$ $\Delta V_2(t) = B_2 e^{t/\tau}$

$\Delta V_1(0^+) = a$ $\quad$ $\Delta V_2(0^+) = -a$

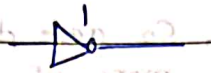
$(a > 0)$

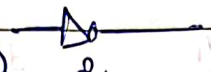
$\Delta V_1(t) = ae^{t/\tau}$	$\Delta V_2(t) = -ae^{t/\tau}$

T: calculated at a particular V_{gs}

initial time: V_{tn} across M_8 & M_9

CMOS inverter → threshold = $\frac{V_{DD}}{2}$.





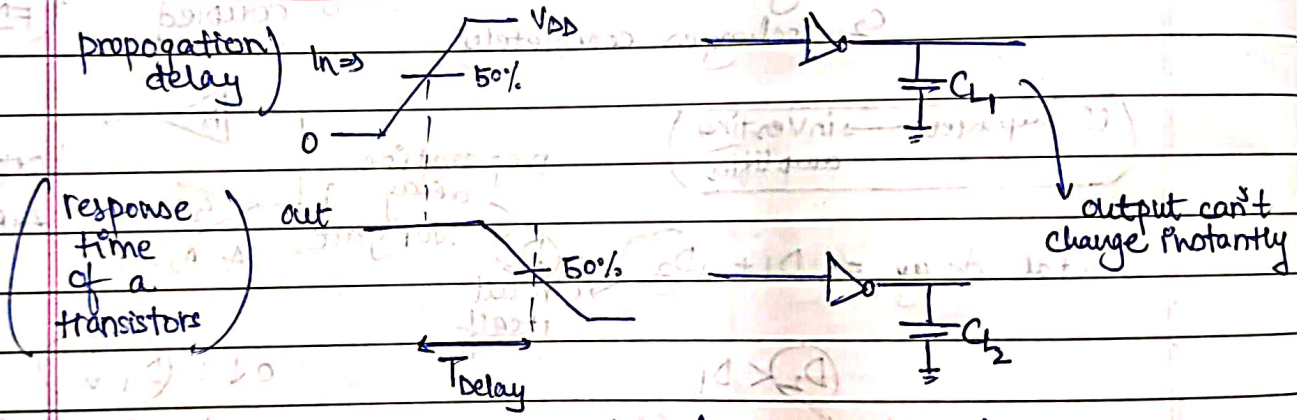
ΔInv_1 = V_{tn} (OR $\frac{V_{dd}}{2} - V_{tn}$) when $\Delta Input \geq V_{tn}$ if $V_{tn} < \frac{V_{dd}}{2}$

Inv_2 = V_{tn} (OR $\frac{V_{dd}}{2} - V_{tn}$) ; $V_{tn} < \frac{V_{dd}}{2}$

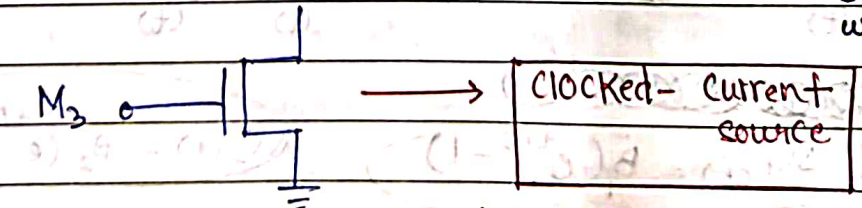
Inp. = V_{tn}

Input of inverter doesn't behave the same for both → (one of them gives faster)

dynamic regenerative circuit



Delays → (Turn the circuit ON) + (delay of the regen. circuit)



can be made OFF when we want to; saves power

(FLASH ADC → Imp.)
↳ otherwise very high current needed.

(Turn off the earlier stage during decision making)