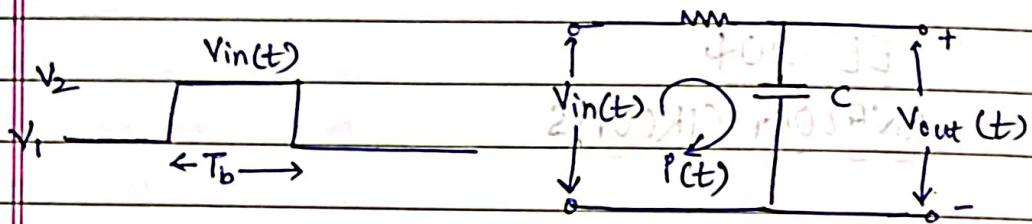


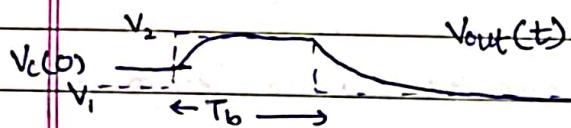
- Active elements:- enhance the power or energy level of a system.
 ↳ spend power from somewhere else, and enhance power somewhere else by consuming energy elsewhere.
 (e.g.-transistors)

RC-CIRCUITS

- Pulse response and frequency response - 1st order Low pass RC Filter



c1) $RC \ll T_b$



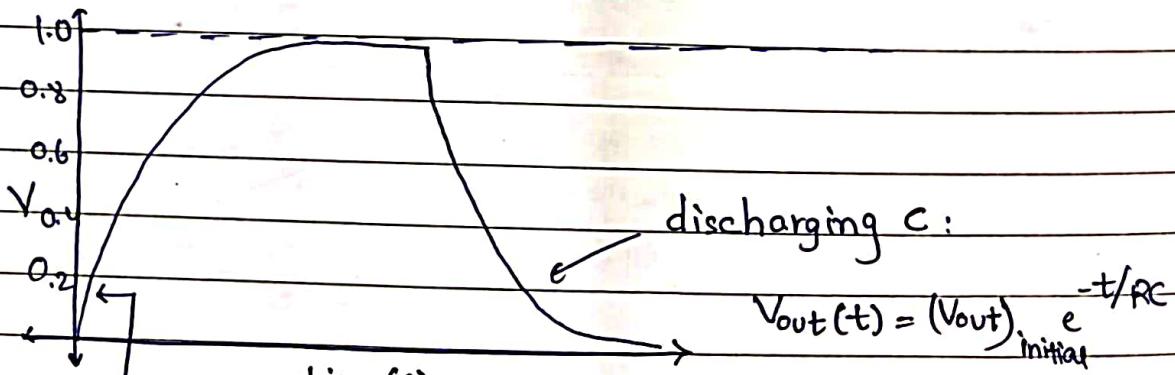
Time Domain :- $RC \frac{dV_{out}(t)}{dt} + V_{out}(t) = V_{in}(t)$

with any initial condition of $V_{out}(t)$

Frequency Domain :- $H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + RCs}$

1st order Linear
Time Invariant System

with initial condition $V_{out}(0) = 0$

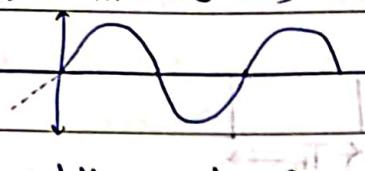


charging C :
 $V_{out}(t) = (V_{out})_{\text{final}} (1 - e^{-t/RC})$

t	V_{out} (V)	$(V_{out} = 0, V_2 = 1)$ $T = 100 \text{ ms}$
100ms	0.63	
200ms (2T)	0.86	
500ms (5T)	0.99	

Fourier series

$$x(t) = \hat{x}_m \sin(\omega_0 t)$$



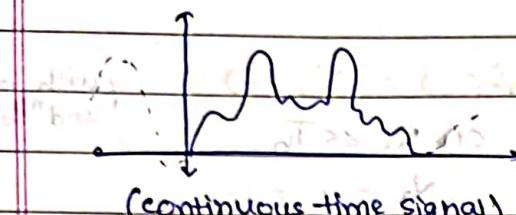
$$|X(j\omega)|$$

x_m

ω_0

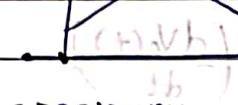
all other frequencies have NO energy component.

some arbitrary signal



→ it has ALL FREQUENCIES, but the level of energies will change.

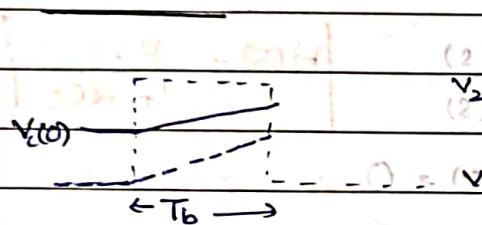
(continuous-time signal)



(continuous frequency spectrum)

C. Frequency spectrum
C. Time \leftrightarrow discrete F. spectrum

case-2) $RC \gg T_b$



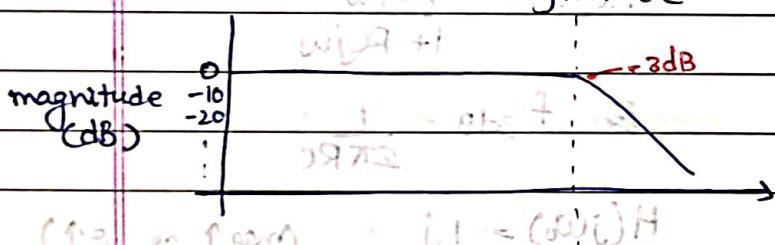
t	Vout(v)
60 ns	0.095
120 ns	0.18
300 ns	0.39
600 ns	0.63

Frequency domain

$$s = j\omega \quad H(j\omega) = \frac{1}{1 + R(j\omega)}$$

BODE PLOTS

magnitude phase

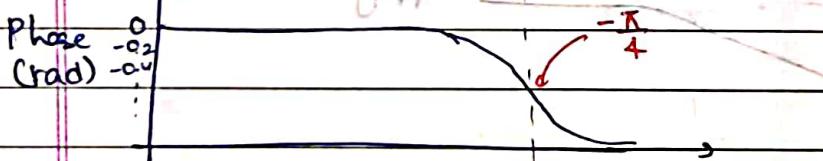


1st order low pass RC filter Transfer fⁿc

$$R = 10 \text{ k}\Omega \quad C = 20 \text{ pF}$$

$$f_{3\text{dB}} = \frac{1}{2\pi RC} = 796 \text{ kHz}$$

$$\text{dB} : (20 \log_{10} |H(j\omega)|)$$



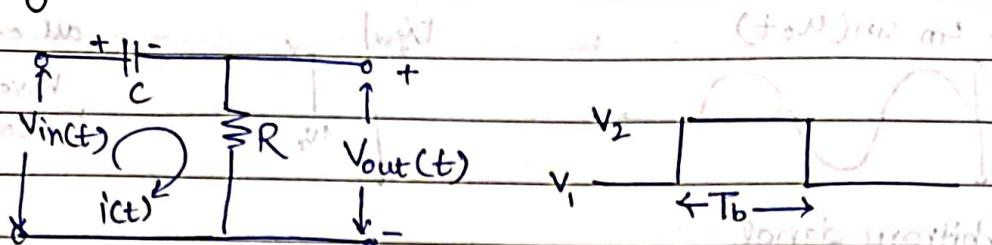
at very low frequency; $\omega \rightarrow 0 \Rightarrow \text{mag.} = 1$

$$\omega \rightarrow 1 \Rightarrow \text{mag.} = \sqrt{\frac{1}{1 + j2}} = \frac{1}{\sqrt{2}}$$

$$\therefore 20 \log_{10} |\sqrt{2}| = -3 \text{ dB}$$

$$\text{and } \phi = \frac{-\pi}{4} \text{ (phase)}$$

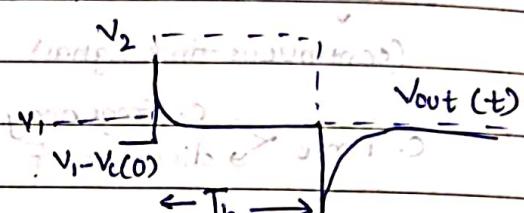
High Pass RC Filter (1st order)



Time Domain :- $RC \frac{dV_c(t)}{dt} + V_c(t) = V_{in}(t)$ (with any initial cond'n of V_{out})

$$\Rightarrow V_{out} = RC \left(\frac{dV_c(t)}{dt} \right)$$

High-pass RC circuit acts as a differentiator.



Frequency domain :- $H(s) = \frac{V_{out}(s)}{V_{in}(s)}$

$$H(s) = \frac{RCs}{1 + RCs}$$

with initial condition $V_{out}(0) = 0$
(1st order L.T.I.O system).

C2>

$$RC \gg T_b$$

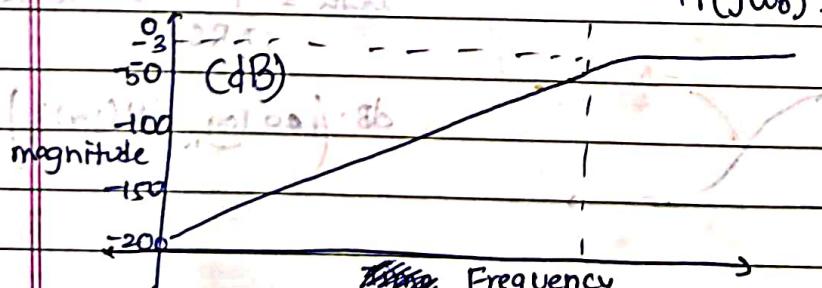
BODE PLOTS

$$s = j\omega$$

$$H(j\omega) = \frac{RCj\omega}{1 + RCj\omega}$$

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$H(j\omega_0) = \frac{1}{1 + j} \quad (\text{mag. } \uparrow \text{ as } \omega \uparrow)$$



$$f_{-3dB} = \frac{1}{2\pi RC} = 796 \text{ kHz}$$

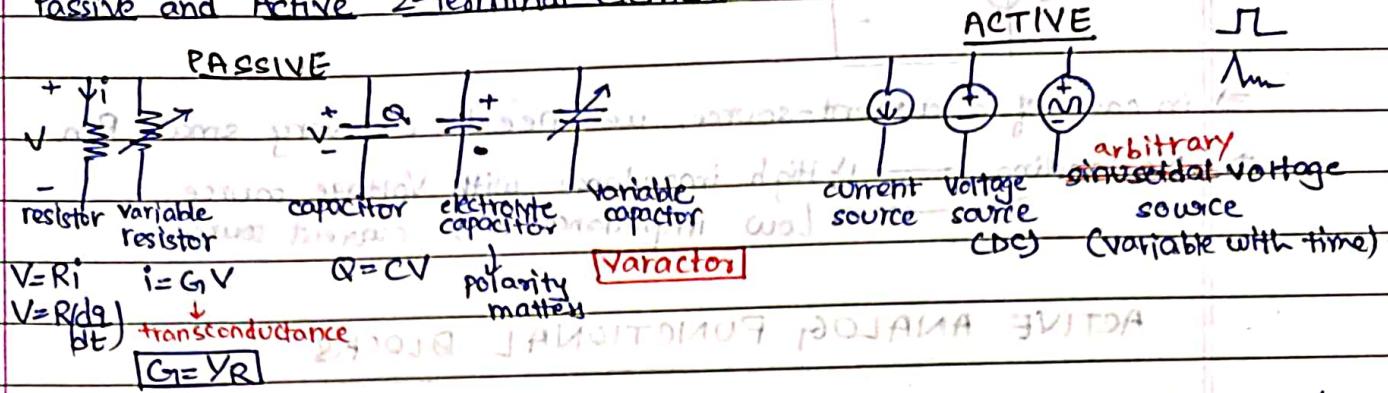
$$\Phi_{-3dB} = \left(\frac{\pi}{2}\right) - \left(\frac{\pi}{4}\right) = \frac{\pi}{4} \text{ rad}$$

(same as earlier)

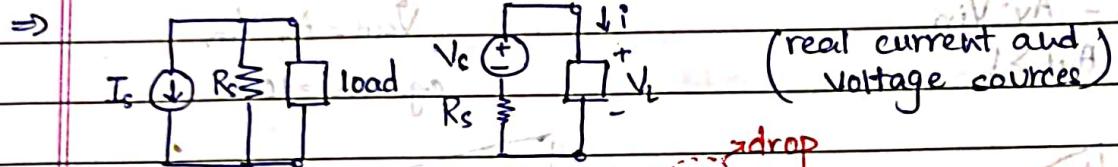
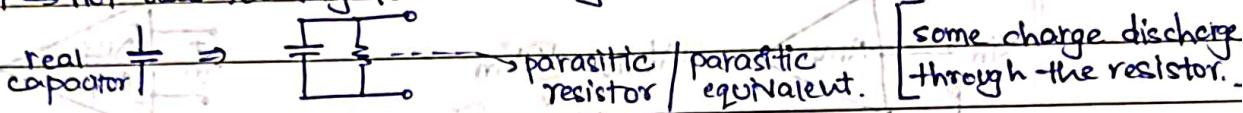
SOME APPLICATIONS OF ANALOG CIRCUITS

Voltage, current, charge, magnetic flux

⇒ Passive and Active 2-terminal elements

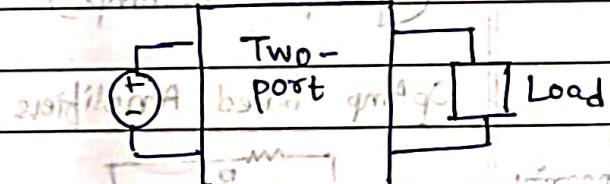
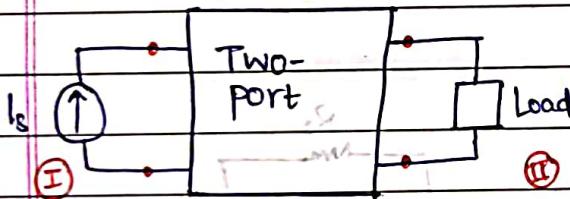


⇒ capacitor → not used for long-term memory due to some leakage current

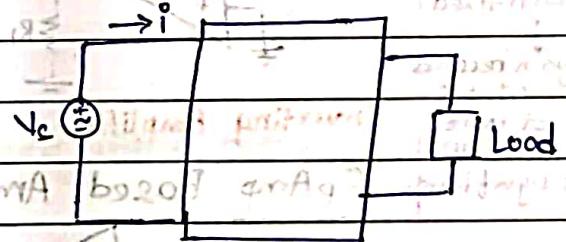
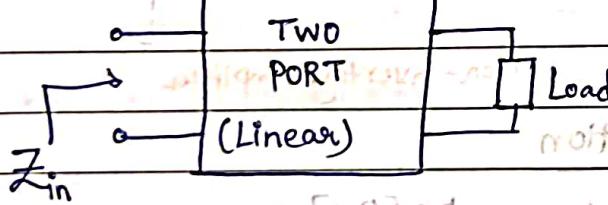


R_s : output resistance of the source (in II) $V_L = V_o - iR_s$

TWO-PORTS



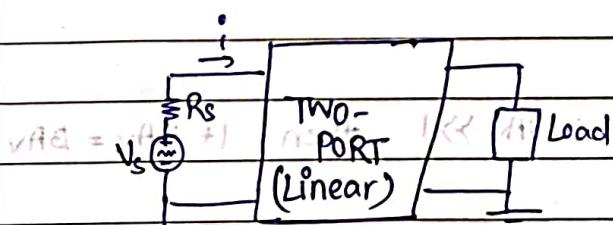
Input And Output Impedance



if we have a practical voltage source \Rightarrow

current depends on two-port characteristics and load.

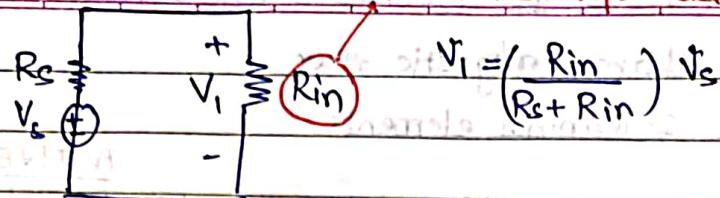
$$Z_{in} = V_s / i$$



$Z_{in} \rightarrow R_{in} \Rightarrow$ if $R_{in} \gg R_s$

(NO loading effect)
on the source

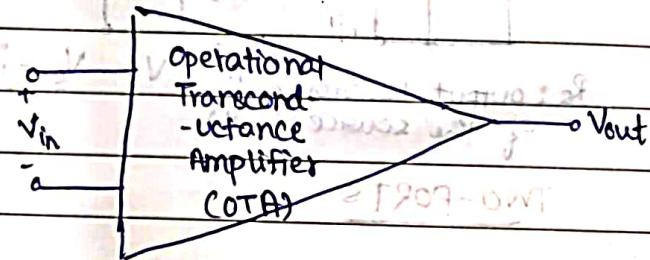
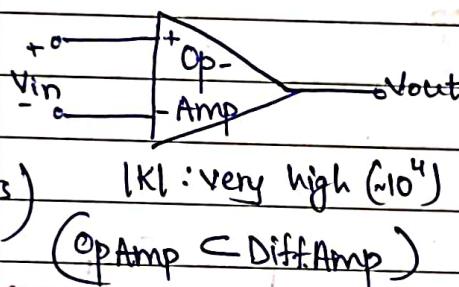
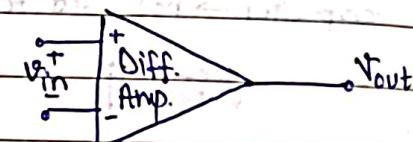
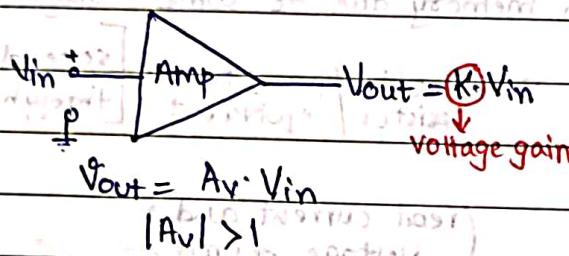
load + the two-port device



⇒ in case of a current-source, we need a very small R_{in}

- ⇒ No-loading → 1) High impedance with Voltage source.
→ 2) Low impedance with current source.

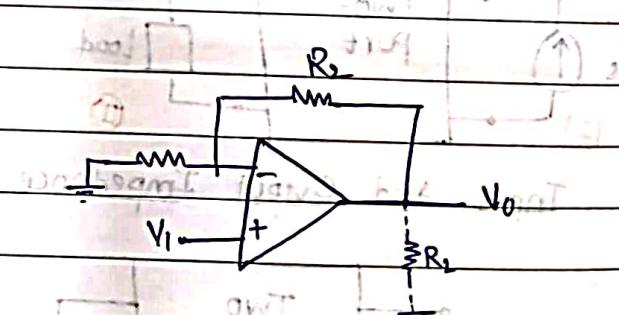
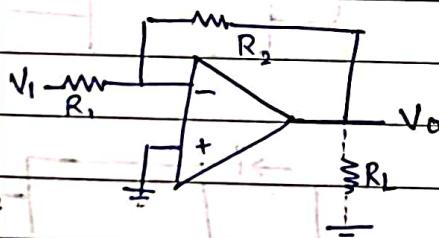
ACTIVE ANALOG FUNCTIONAL BLOCKS



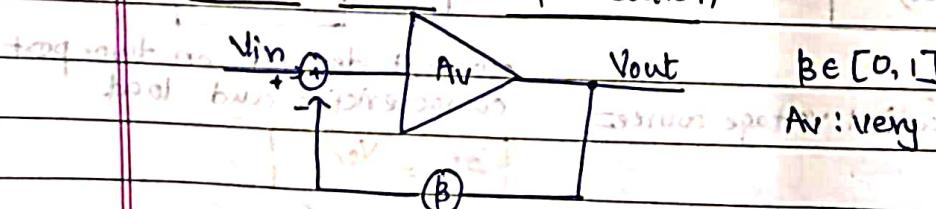
OpAmp based Amplifiers

due to non-linearity effects, gain does not remain fixed

once gain becomes high, $10^4, \pm 10$ does not matter, but around 10 , it is significant.



OpAmp Based Amplification



$$V_{out} = \frac{A_v - \beta}{1 + \beta A_v} V_{in}; \quad \beta A_v \gg 1 \quad \text{then} \quad 1 + \beta A_v = \beta A_v$$

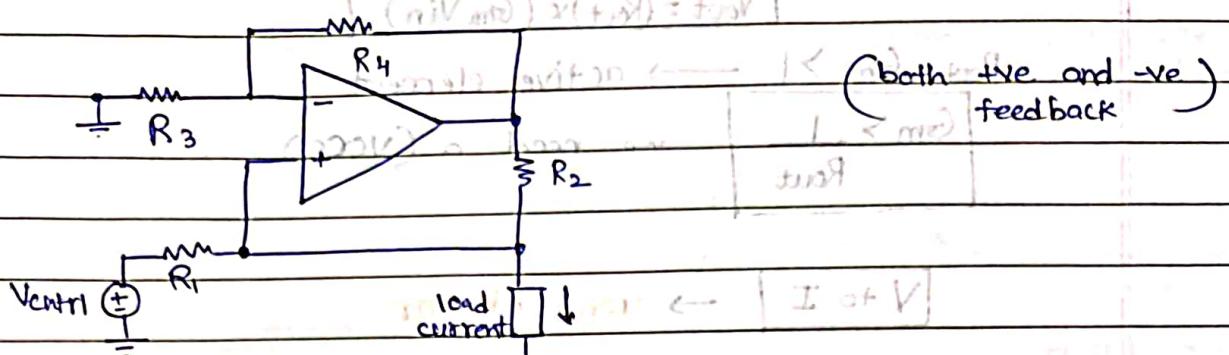
$$V_{in} = \beta V_{out} \Rightarrow V_{out} = \left(\frac{1}{\beta} \right) V_{in}$$

(It is hard to get a constant gain)

constant-gain amplifier

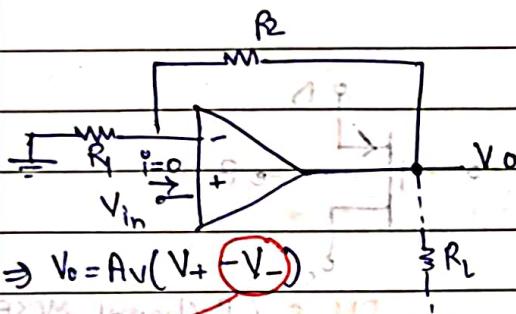
Voltage-to-current converter OR VCSC

Howland current source (V_{mid})



Voltage Comparator

(simple op-amp circuit)
used in ADC's



Non-inverting amplifier,

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{1}{1 + (R_2/R_1)}$$

$$V_o = A_v \times (V_i - \beta V_o) \rightarrow \text{fraction of output subtracted from the input.}$$

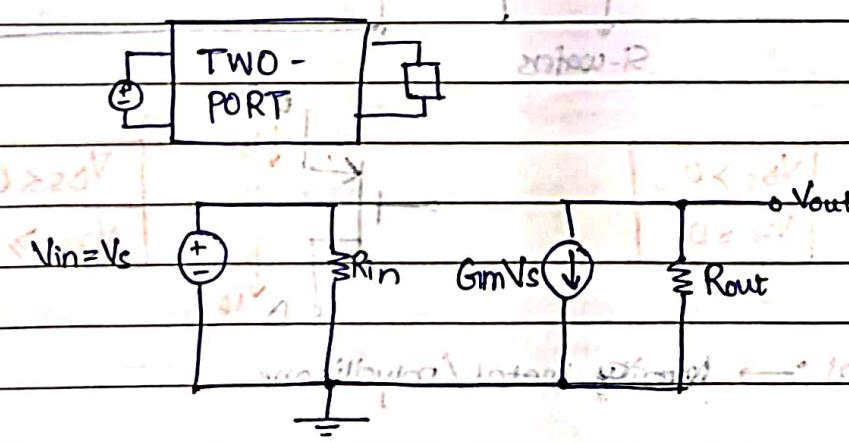
$$\frac{V_o}{V_i} = 1 + \frac{(R_2)}{(R_1)} \quad (\text{assuming } A_v \rightarrow \infty)$$

→ entire current flows only through the resistors to the ground.

→ -ve feedback → stabilizes the system

+ve feedback → destabilizes the system

⇒ Examples of realizing active two-ports using active elements



(no 3rd terminal ⇒ no control)

$(G_m V_s)$

$$V_{out} = (R_{out}) \times (G_m V_s)$$

$$V_{out} = (R_{out}) \times (G_m V_{in})$$

$R_{out} \times G_m > 1 \rightarrow$ active element
 additional

$$\frac{G_m}{R_{out}} > 1$$

we need a (VCCS)

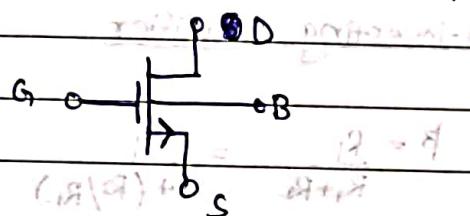
$V \rightarrow I \rightarrow$ transconductor

~~transistor~~ → transresistor = transistor

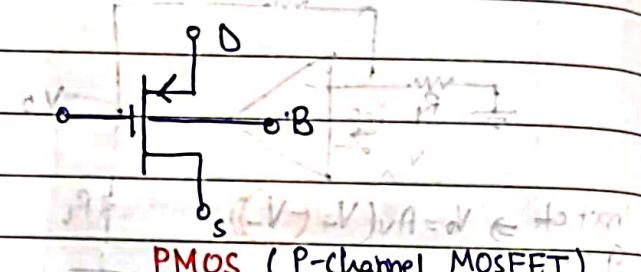
Transistor → use external supply → increase/amplify.

\downarrow
 gives enough current
 to the transistor.

MOSFET symbols



NMOS (N-channel MOSFET)

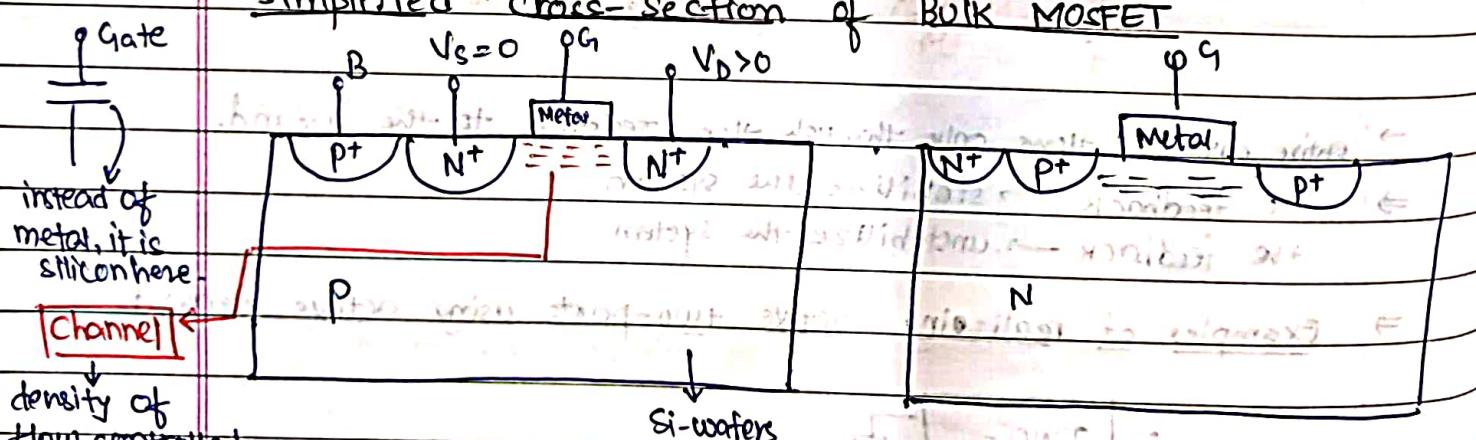


PMOS (P-channel MOSFET)

G: gate B: bulk D: drain S: source

BULK MOSFET (4-terminal device)

Simplified cross-section of BULK MOSFET



instead of metal, it is silicon here

channel
 density of flow controlled by gate

e: S → D

I: D → S

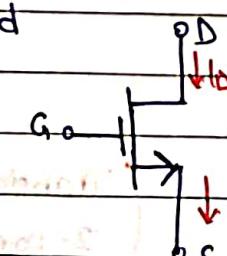
$v_D > 0$

$v_{BS} \leq 0$

$v_B < 0$

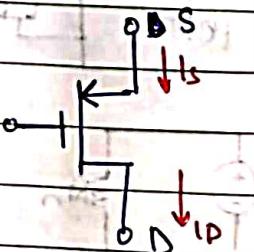
$v_D < 0$

$v_{BS} \geq 0$



$$v_{DS} > 0$$

$$v_{BS} \leq 0$$



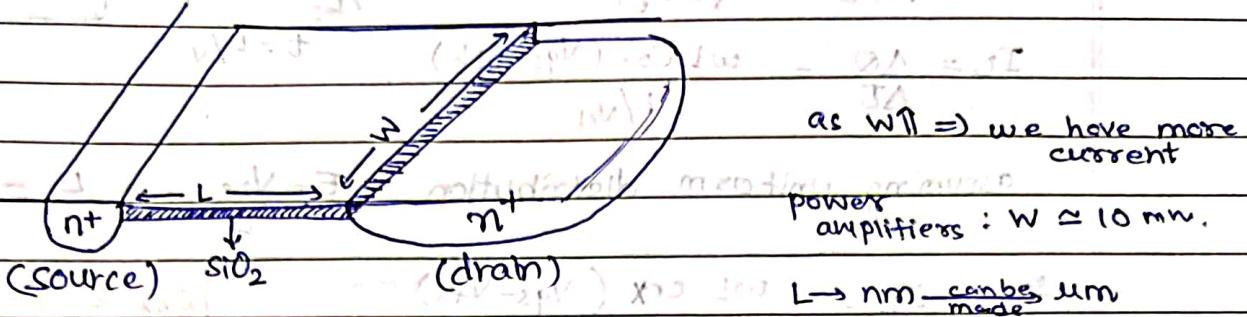
$$v_{DS} < 0$$

$$v_{BS} \geq 0$$

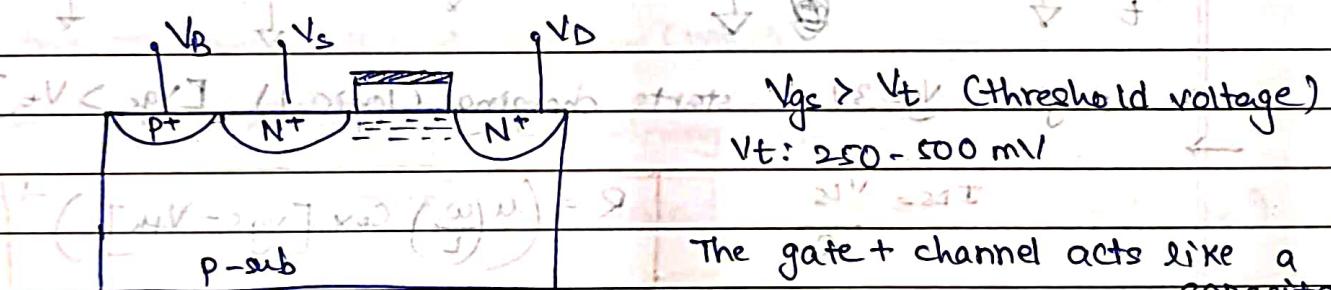
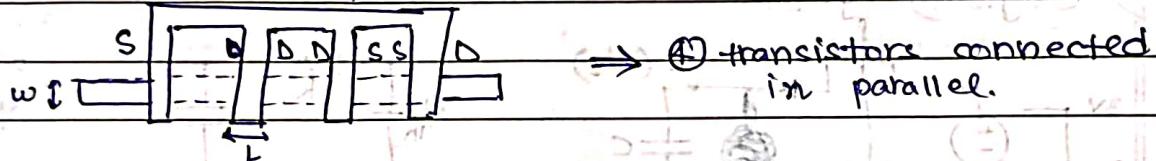
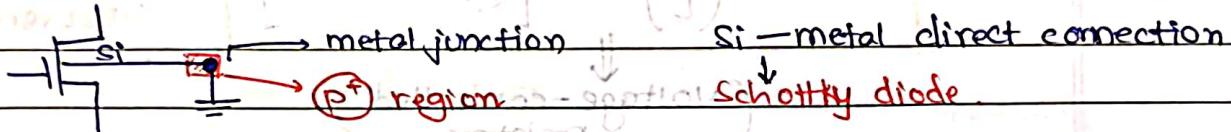
Gate material: → bonding metal/polysilicione.

REVERSE
→ bias the substrate → ~~reverse~~ bias → work with MOSFET.

rev. bias for all P-N junctions → so they do not act like parasitic diodes.



we need a p^+ region in a pMOS as



The gate + channel acts like a capacitance

$$\Delta Q = C_{ox} (V_{GS} - V_{th})$$

charge used to invert the channel (e^- excess)

$$\Delta Q = WL C_{ox} (V_{GS} - V_{th})$$

effective capacitance per unit area.

→ Capacitor C_L formed by gate and channel.

controlled

→ Assuming charge is uniformly distributed E is also uniform $\Rightarrow I_{DS} = \frac{dQ}{dt}$

$$C_{ox} (V_{GS} - V_{th})$$

IC designer Technology

$$\left(\frac{C = A \Sigma}{t} \right)$$

Date _____
Page _____

avg.

Velocity of e^- → determines the time

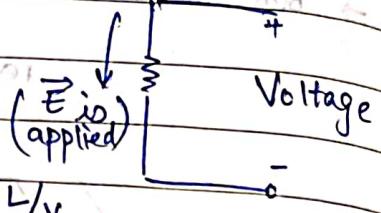
DRIFT velocity → $f^n c$ of \vec{E} .

$$V \propto E$$

$$V = \mu_e E$$

$$V = L/t$$

(E_{is})
applied



$$I_D = \frac{\Delta Q}{\Delta t} = \omega L C_{\text{ox}} (V_{gs} - V_{th})$$

L/v

$$t = L/v$$

assuming uniform distribution,

$$E = \frac{V_{ds}}{L}$$

$$\frac{L}{v} = \frac{L}{\mu V_{ds}/L}$$

$$\text{so, } I_D = \omega L C_{\text{ox}} (V_{gs} - V_{th})$$

$$L^2/\mu V_{ds}$$

$$C_{\text{ox}} = \epsilon_{\text{ox}}$$

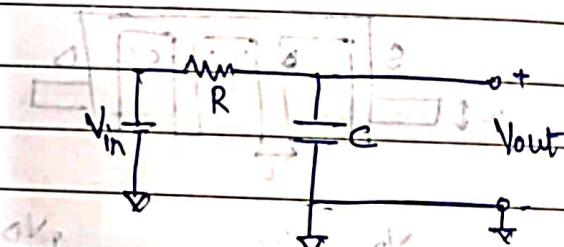
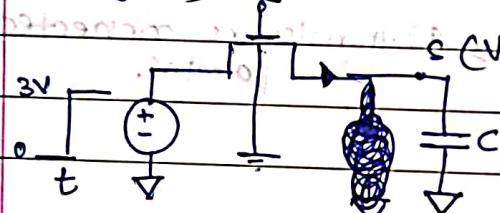
t_{oxide}

$$I_{DS} = \frac{\mu(w)}{L} C_{\text{ox}} [(V_{gs} - V_{th}) V_{ds}]$$

V_{ds} : very low $< 100\text{mV}$

(Voltage-controlled resistor)

($V_t = 400\text{mV}$) (logic 1) $V_g = 3\text{V}$



→ for gate, $V_g = 3\text{V}$, C starts charging (logic 1) [$V_{ge} > V_t$]

$$I_{DS} = \frac{V_{ds}}{R}$$

$$R = \left(\frac{\mu(w)}{L} C_{\text{ox}} [V_{gs} - V_{th}] \right)^{-1}$$

as we have, $V_{gs} > V_{th}$

$$3 - V_t > 0.4 \Rightarrow V_t < 2.6\text{V}$$

$$C_2 > V_{ds} > 100\text{mV}$$

$$V_{ge} > V_{gd}$$

$$\Rightarrow V_{gs} - V_t > V_{gd} - V_t \quad [\text{The entire channel is inverted.}]$$

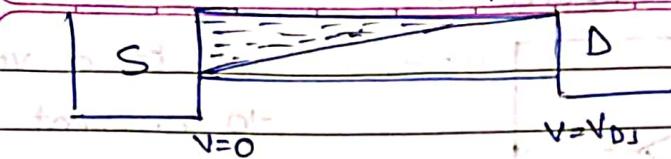
Q is not uniformly distributed everywhere.

If V_{ds} is not small

$$I_D = \mu C_{\text{ox}} \left(\frac{w}{L} \right) \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Under assumption, $\frac{V_{ds}}{2} \ll (V_{gs} - V_{th})$

channel

when $V_{DS} = V_g - V_t$,

Channel stops

For linear region \Rightarrow

$$\frac{V_{DS}}{2} \ll (V_{gs} - V_t)$$

and

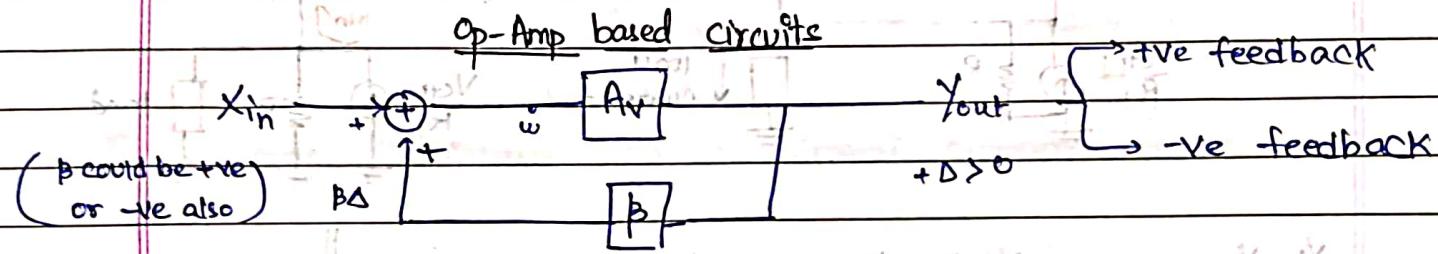
$$V_D > V_{g_s} - V_{th}$$

the channel doesn't stop.

 $V_g - V_t$: Gate overdrive voltage $V_D < V_{g_{sat}}$ \rightarrow the channel is ONwhen $V_{DS} > V_{g_{sat}}$ \rightarrow channel becomes OFF. (depletion layer)

LINEAR FEEDBACK SYSTEMS

Op-Amp based circuits



tries to control the disturbances (noise).

$$\omega \rightarrow (\omega Av) \cdot (\beta) \quad [\text{considering } x_m = 0]$$

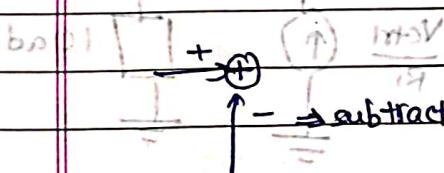
 $\Rightarrow \omega (Av \cdot \beta) \rightarrow \text{loop-gain}$ (appears in closed-loop)

transfer func

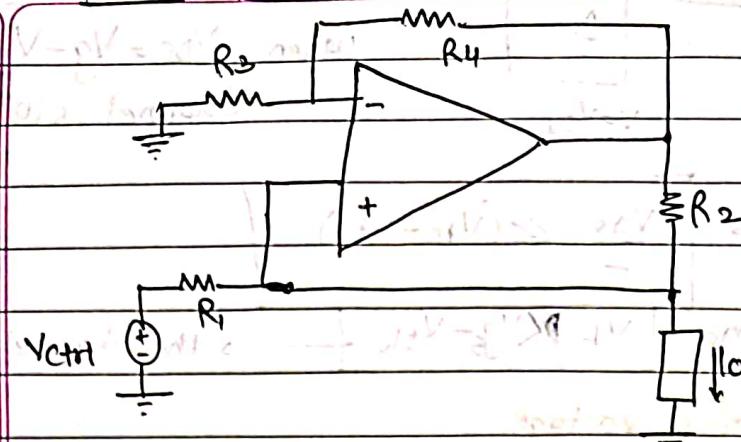
if $\beta < 0$ [Δ is +ve]
 $\Delta [Y_{out}] \Rightarrow \beta Y_{out} \downarrow \Rightarrow \text{summation} \downarrow \Rightarrow [Av] \downarrow$

increase (see note 12) \downarrow decrease
 decrease - the effect of disturbance

SUMMER \Rightarrow $\beta Av > 0$ (+ve) $\beta Av < 0$ (-ve)
 $\xrightarrow{+}$ circuit can be potentially unstable

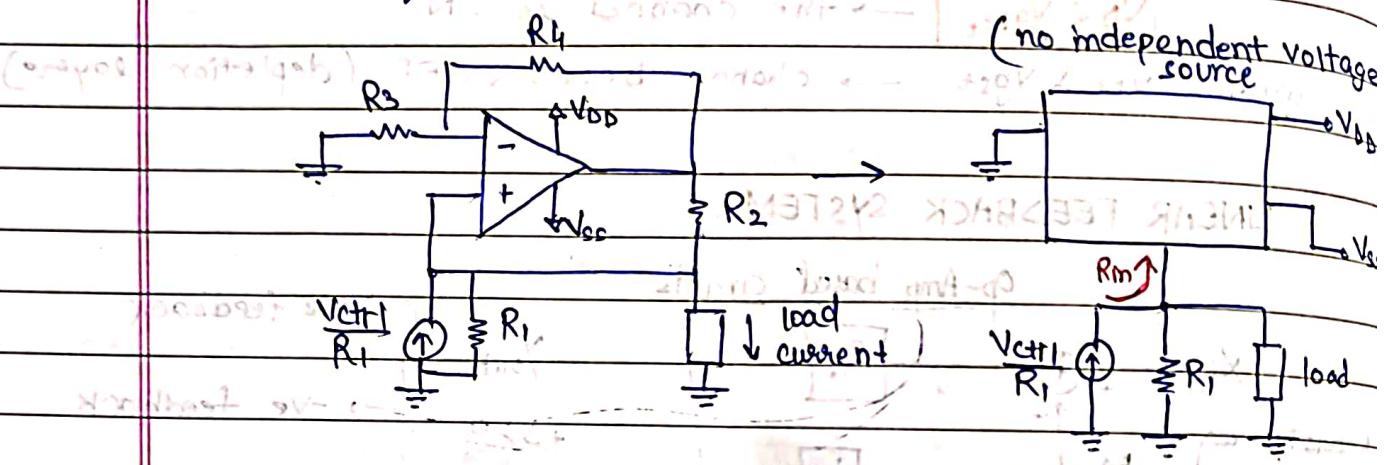
 $\beta Av = 0 \rightarrow$ No feedback at all.

 $\xrightarrow{-} \text{subtractor} \Rightarrow (\beta Av > 0 \Rightarrow \text{-ve feedback})$

Operation of OpAmp also depends on the frequency.

VCVS / Howland current source

it is a voltage
to current conv.

→ The value of I does not depend on the load.



$V_{DD}, V_{SS} \rightarrow$ no role in the circuit

$$R_1 \parallel R_m \rightarrow \infty$$

↓

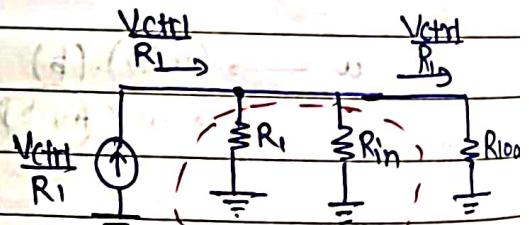
+ve FEEDBACK

⇒ passive element

(resistor)

active element

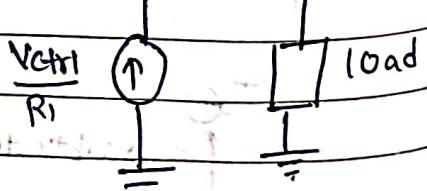
(negative resistor)



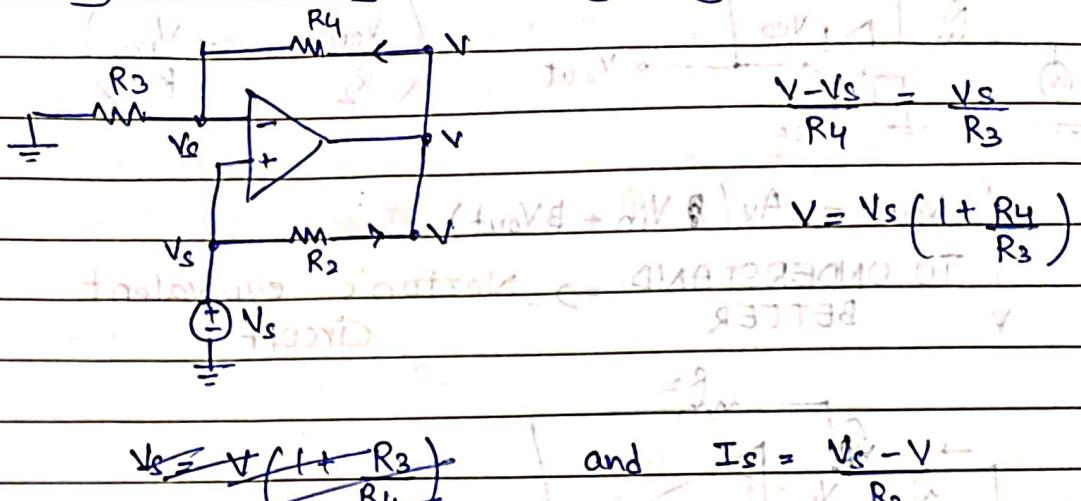
$$R_m = -R_1 \Rightarrow (R_1 \parallel R_m \rightarrow \infty)$$



equivalent resistance $\Rightarrow ?$



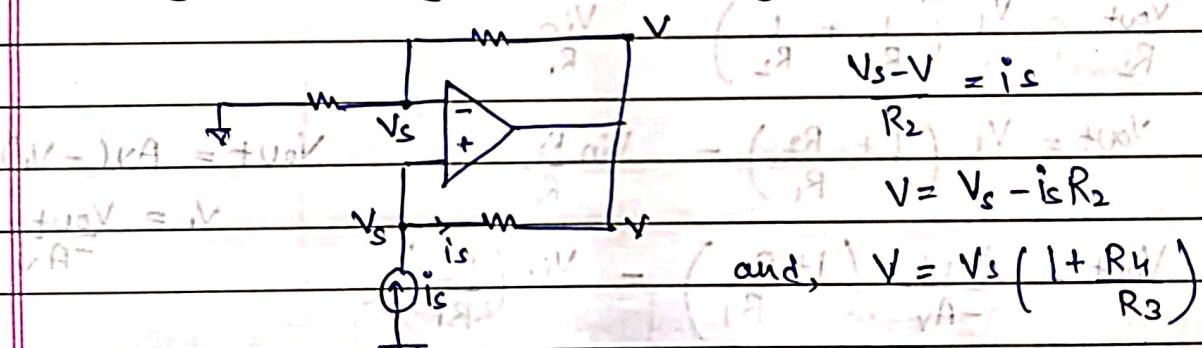
⇒ Finding R_{in} using an imaginary voltage source



$$I_s = \frac{V_s - V}{R_2} = V_s \left(1 - \left(1 + \frac{R_4}{R_3} \right) \right)$$

$$\frac{V_s}{I_s} = -R_2 R_3 \quad | \quad R_{in} = -(R_2 R_3)$$

⇒ Finding R_{in} using an imaginary current source



$$\text{So, } \frac{V_s}{i_s} = -R_2 R_3 = R_{in} \quad | \quad \frac{V_s + V}{R_4} = \frac{V_s - i_s R_2}{R_3}$$

$$\text{For } R_{in} \parallel R_1 \rightarrow \infty \Rightarrow R_{in} + R_1 = 0$$

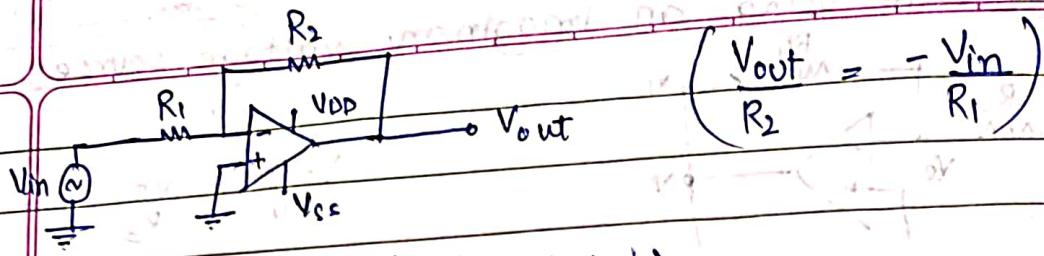
$$\Rightarrow R_{in} = -R_1$$

$$\text{So, } R_1 R_4 = R_2 R_3$$

i.e.

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

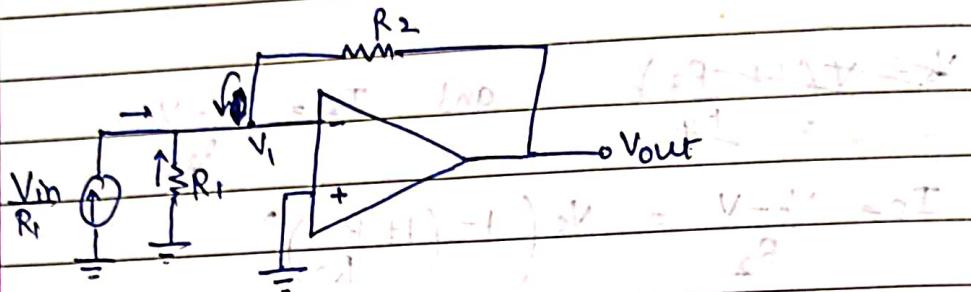
→ (acts as a ideal current source)



$$\frac{V_{out}}{R_2} = -\frac{V_{in}}{R_1}$$

$V_{out} = A_v (V_{in} + \beta V_{out})$

TO UNDERSTAND BETTER \rightarrow Norton's equivalent circuit



$$\frac{V_{in}}{R_1} = \frac{V_1}{R_1} + \left(\frac{V_1 - V_{out}}{R_2} \right)$$

$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_2} + V_1 \left(\frac{1}{R_1} + \frac{1}{R_2} \right)$$

$$\frac{V_{out}}{R_2} = V_1 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) = \frac{V_{in}}{R_1}$$

$$V_{out} = V_1 \left(1 + \frac{R_2}{R_1} \right) - \frac{V_{in} R_2}{R_1} \quad V_{out} = A_v (-V_{in})$$

$$V_{out} = \frac{V_{out}}{-A_v} \left(1 + \frac{R_2}{R_1} \right) - V_{in} \left(\frac{R_2}{R_1} \right) \quad V_1 = \frac{V_{out}}{-A_v}$$

$$A_v V_{out} = \left(1 + \frac{R_2}{R_1} \right) (-V_{out}) - \left(A_v \frac{R_2}{R_1} \right) V_{in}$$

$$V_{out} \left(1 + \frac{R_2}{R_1} \right) = -A_v V_{out} - \left(A_v \frac{R_2}{R_1} \right) V_{in}$$

$$V_{out} \left(\frac{R_1 + R_2}{R_1} \right) = -A_v \left[V_{out} + \left(\frac{R_2}{R_1} \right) V_{in} \right]$$

$$V_{out} = -A_v \left(\frac{R_1}{R_1 + R_2} \right) \left[V_{out} + \left(\frac{R_2}{R_1} \right) V_{in} \right]$$

$$= -A_v \left(\frac{R_1}{R_1 + R_2} \right) \left[\frac{R_2}{B_f} \right] \left[V_{in} + \left(\frac{R_1}{R_2} \right) V_{out} \right]$$

$$-V_{out} = A_v \left(\frac{R_2}{R_1 + R_2} \right) \left[V_{in} + \left(\frac{R_1}{R_2} \right) V_{out} \right]$$

$$V_{out} = \left(-\frac{A_v R_2}{R_1 + R_2} \right) \left[V_{in} + \left(\frac{+R_1}{R_2} \right) V_{out} \right] \quad (B = \frac{R_1}{R_2})$$

\downarrow
equivalent A_v is just a fraction of A_v \rightarrow not imp. if $(A_v \rightarrow \infty)$

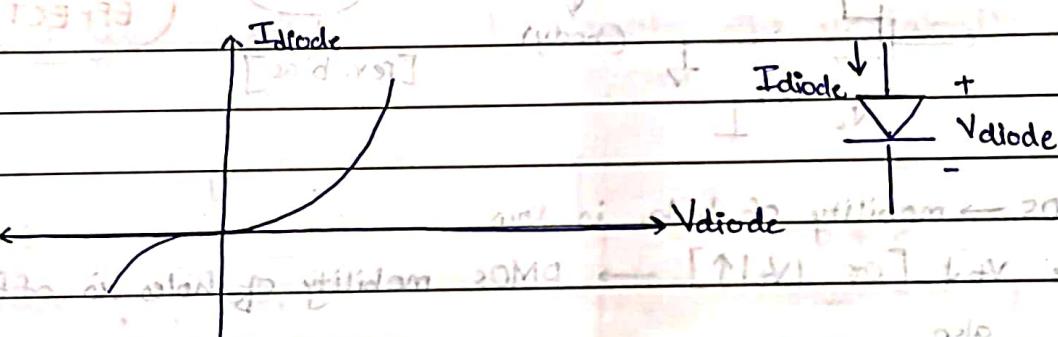
$$V_{out} = (A_v)_{eq.} \left[\left(\frac{R_1}{R_2} \right) V_{out} + V_{in} \right]$$

$$\frac{V_{out}}{V_{in}} = \frac{(A_v)_{eq.}}{1 - \frac{R_1}{R_2} (A_v)_{eq.}} \approx \frac{-1}{B} = -\frac{R_2}{R_1} \rightarrow A_{v,eq.} \gg 10^3$$

$$V_{out} = A_v (V_{in} + B V_{out})$$

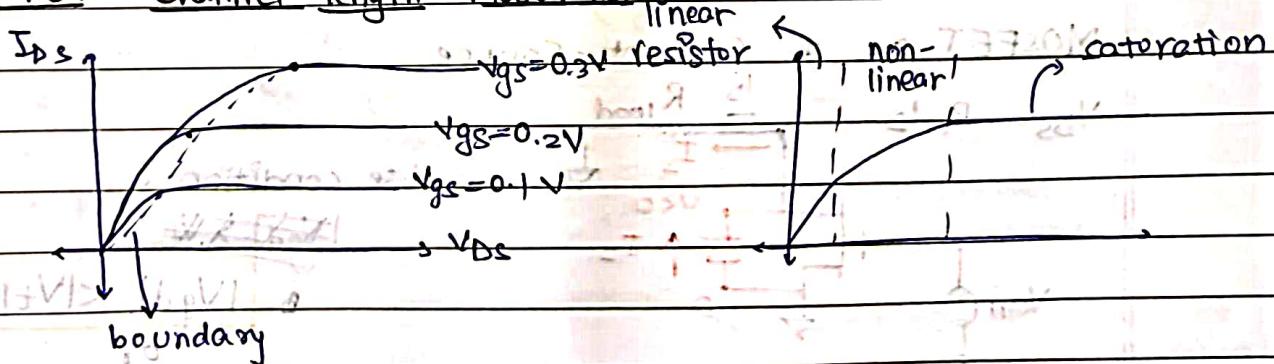
\downarrow $(A_v)_{eq.}$ \rightarrow loading effect

Diode Characteristics



$$I_{diode} = I_s \left[e^{\frac{V_{diode}}{nV_T}} - 1 \right] \quad V_T = \frac{kT}{q} \approx 25.9 \text{ mV at room temperature}$$

MOSFET - Channel length Modulation



$$N_{GD} = V_t \quad i.e. \quad V_{GS} - V_{DS} = V_t \quad \text{or} \quad V_{DS} = V_{GS} - V_t = V_{OV}$$

\hookrightarrow saturation point

$V_{GD} < V_t$: pinched-off channel

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) \left[\frac{V_{GS}^2}{V_T} \right] \rightarrow (\text{low-field long-channel approxim.})$$

$$L_{\text{eff}} = L - \Delta L = L \left(1 - \frac{\Delta L}{L}\right)$$

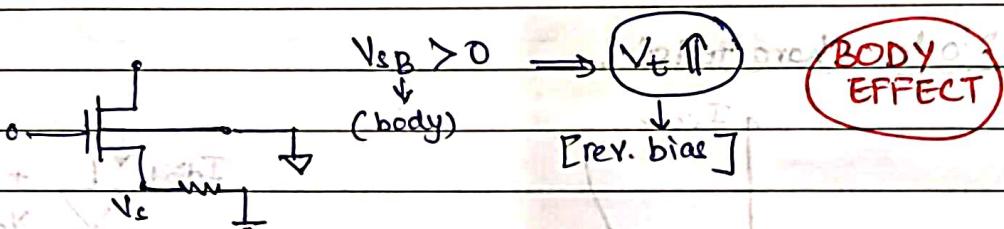
$$\frac{w}{L_{\text{eff}}} = \frac{w}{L(1 - \Delta L/L)} = \frac{w}{L} \left(1 + \frac{\Delta L}{L}\right)$$

and as $\frac{\Delta L}{L} = \lambda V_{DS}$ $\Rightarrow \frac{w}{L} (1 + \lambda V_{DS})$ [⊗: model]

$$I_{DS} = \frac{1}{2} \mu_n C_{Ox} \frac{w}{L} [V_{GSt}^2] (1 + \lambda V_{DS})$$

↓ ↓ ↓ ↓
technical designer empirical parameter
(technology)

→ If you have a reverse bias b/w the drain-body / source-body P-N junctions, then the threshold voltage increases.



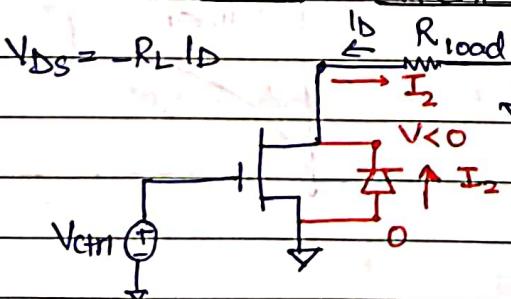
p-MOS → mobility of holes is low

as $V_t \downarrow$ [or $|V_t| \uparrow$] → PMOS mobility of holes is affected highly also,

$\mu_p < \mu_n$ → ONLY IN PLANAR DEVICES

in 3-D technologies → they can be adjusted.

MOSFET as a Current-Source



Use condition :

$$|V_{Gd}| < |V_{t1}|$$

strong inversion
or

$$|V_{DS}| > |V_{GS}|$$

$V_{DS} < 0 \Rightarrow$ Drain-body junction is forward bias

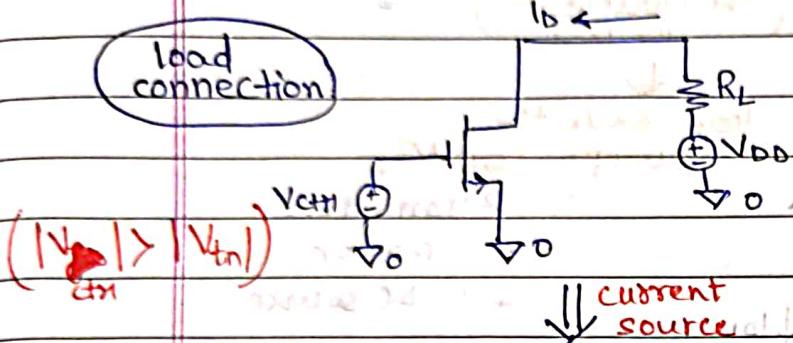
↳ DIODE

I_2 increases as long as it opposes I_D , and finally, it will make $I_D + I_2 = 0$

$\rightarrow I_{DS} = 0 \rightarrow$ MOSFET is not operating.

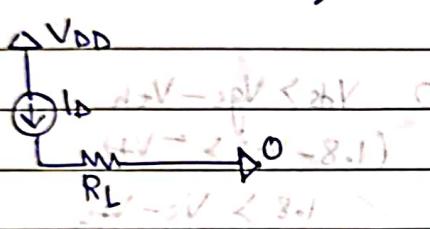
\rightarrow So, we need to add a voltage on R.H.S. \rightarrow

MOSFET needs two voltage sources to operate!

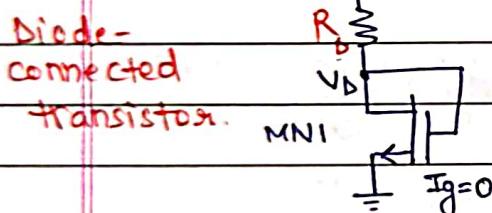


The load here isn't grounded

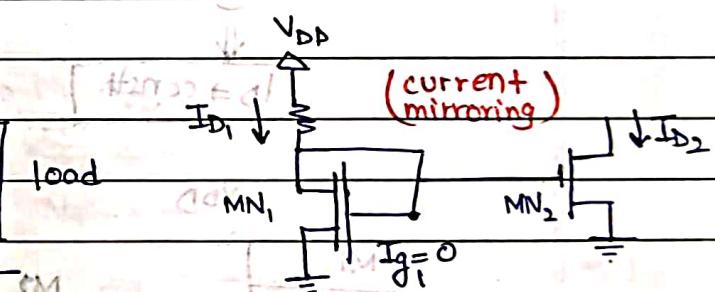
Howland current source has a load b/w node 2 & ground.



If W and L are large keeping (W/L) const., the variability of the system reduces.



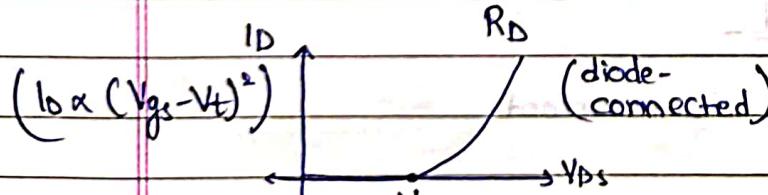
The gate current is 0 $\rightarrow I_g = 0$



$$I_D = V_{DD} - V_D$$

(assuming MN_2 in saturation)

$$I_{D2} = (\frac{W}{L})_2 \cdot I_{D1}$$



proportional factor

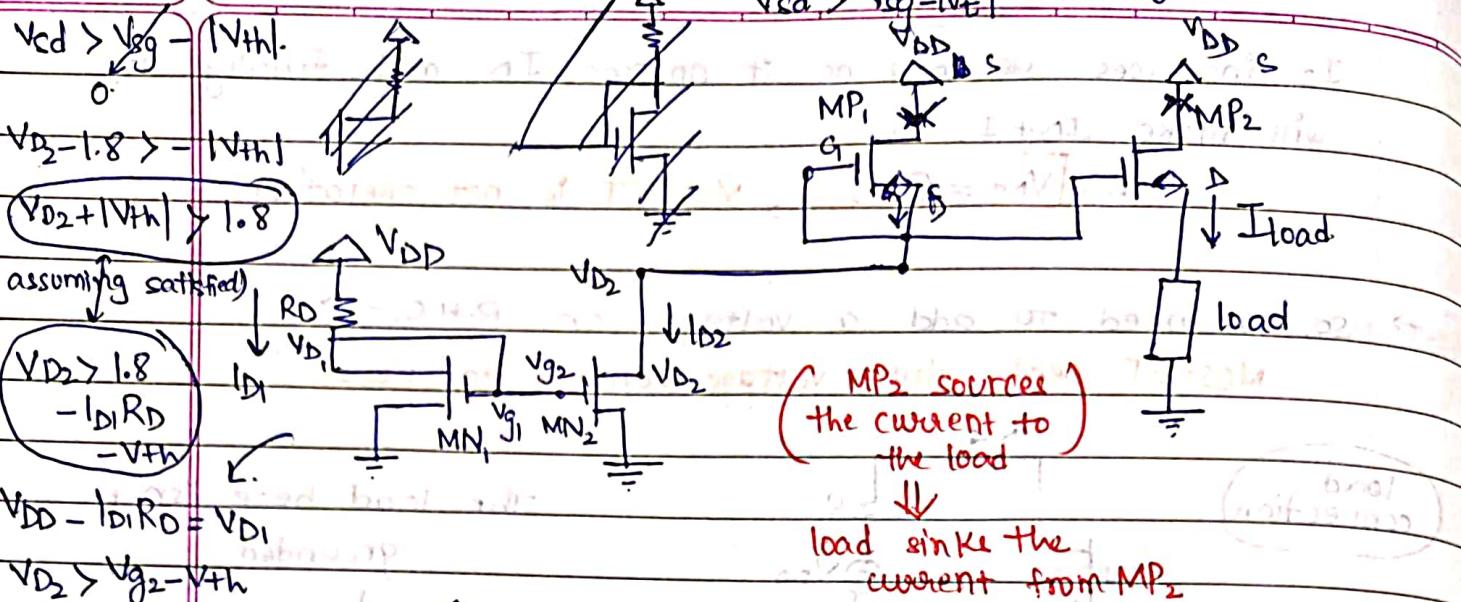
current mirroring using one nMOS and another pMOS.

The problem of load not being grounded isn't solved here, as still it is b/w V_{DD} and drain

$$\frac{I_{D2}}{(W/L)_2} = \frac{I_D}{(W/L)}$$

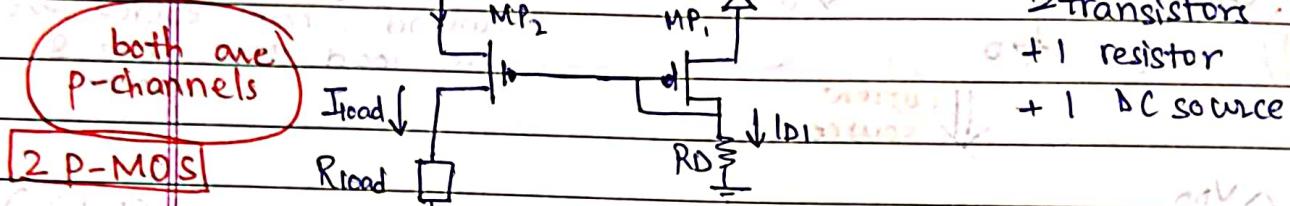
PMOS: $|V_{Gd} - V_{th}| < |V_{ds}|$

i.e. $V_{ds} > (V_{gs} - V_{th})$



(MP₂ sources
the current to
the load)

load sink the
current from MP₂



2 P-MOS

both are
p-channels

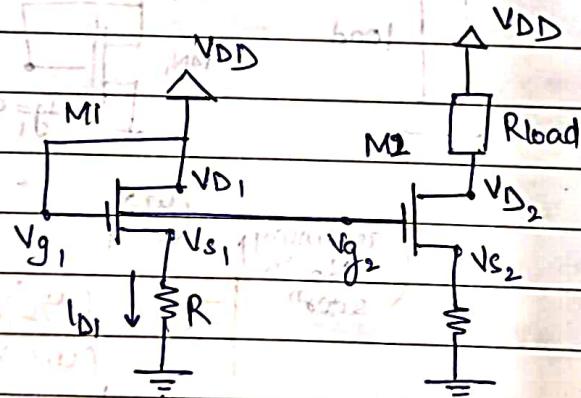
2 transistors
+ 1 resistor
+ 1 DC source

$$V_{ds} = 0 \quad V_{ds} > V_{gs} - V_{th}$$

$$(1.8 - V_s) > -V_{th}$$

$$1.8 > V_s - V_{th}$$

$$\text{i.e. } V_{DD} > (I_D \cdot R_D) - V_{th}$$



M1 is in saturation $\Rightarrow I_D$ is constant

$$V_{S1} = R \cdot I_D$$

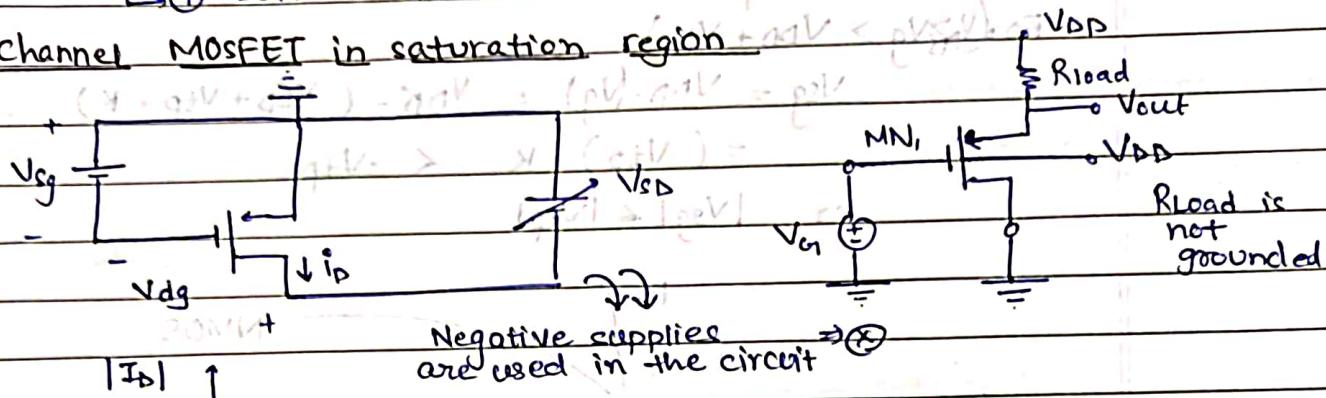
also, assuming M2 in saturⁿ, we get const. current for R_{load}

minib binar

⇒ Types of CMOS technology

- ① Regular V_t (regular transistor)
- ② I/O (thick oxide) transistor \Rightarrow higher $|V_t|$, V_{GS} , V_{DSmax}
- ③ Native devices
- ④ Low V_t devices

P-channel MOSFET in saturation region



$|I_D|$

strong inversion
(satn")

weak inversion

$V_g = 0$

$|V_{ds}| > |V_{gs}| - V_t$

$V_{ds} > V_{sg} - |V_t|$

$V_g - V_d > -V_t$

$V_g > -V_t$

$V_{DD} - |V_{tp}| < V_{DD}$

$(V_{DD} + V_{tp})$

$V_g > V_d > -V_t$

$V_g > -V_t$

$V_g > |V_t|$

$V_g > -V_t \Rightarrow |V_g| > |V_t|$ saturation

$$V_s = V_{out} = V_{DD} - (R_{load} \cdot I_D)$$

$$\text{condition : } |V_{ds}| > |V_{gs} - V_t| \Rightarrow |V_{ds}| > |V_{gs}|$$

saturation :-

$$V_{ds} \rightarrow V_{sg} + V_t \Rightarrow V_{ds} > V_t$$

$$V_{DD} - V_{sg} - |V_t| > V_t \Rightarrow V_{DD} - V_{sg} > 2|V_t|$$

N MOS : $V_{gd} < V_{tn}$

P MOS : $V_{gd} > V_{tp} \rightarrow$ drain is not inverted otherwise.

so, in general,

$$|V_{gd}| < |V_t|$$

note, $V_{DD} = R_{load} \cdot I_D + V_{SG} + V_g$

$$V_{DD} - V_g = V_{SG} + R_{load} \cdot I_D$$

$$\text{at } V_g = V_D \Rightarrow I_D = 0 \\ V_{SG} = 0$$

$$V_{g_p} > |V_{tp}| \quad \text{or} \quad V_{gs} < V_{tp} < 0$$

If $V_g = V_{DD} + V_{tp}$ (is -ve)

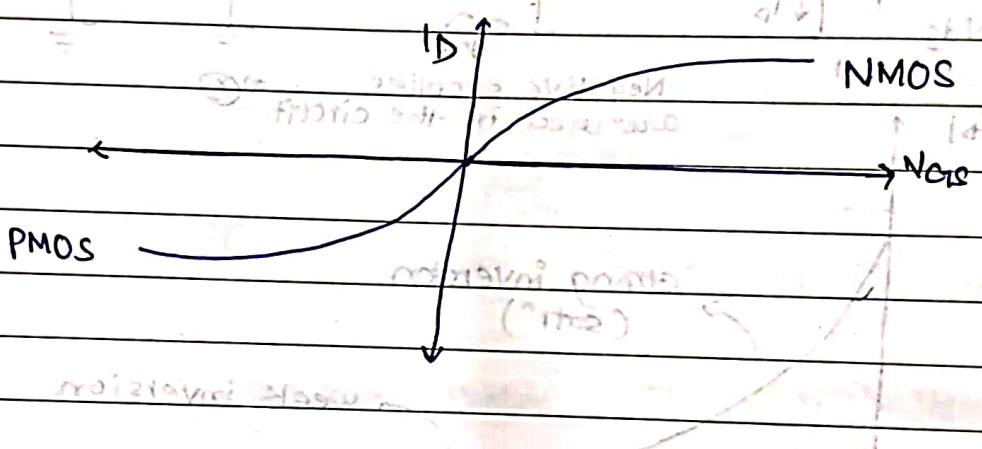
Then, $I_D = 0$ as V_{sg} has to be $< V_{tp}$ and R_{load} can't be

$$V_{sg} = -V_{tp} \quad (I_D = 0)$$

For ($V_g > V_{DD} + V_{tp}$)

$$\begin{aligned} V_{sg} &= V_{DD} - (V_g) = V_{DD} - (V_{DD} + V_{tp} + K) \\ &= (-V_{tp}) - K < -V_{tp} \end{aligned}$$

$$\text{or } |V_{sg}| < |V_{tp}|$$



$$AV = \frac{V_{out}}{V_{in}} = \frac{V_{DD} - V_{g1}}{V_{DD} - V_{g2}}$$

$$|V_{g1} - V_{g2}| < V_{DD}$$

$$0 = pV$$

$$|V_{g1} - V_{g2}| < V_{DD}$$

$$V_{DD} - V_{g1} < V_{DD} - V_{g2}$$

$$|V_{g1} - V_{g2}| < V_{DD}$$

$$|V_{g1} - V_{g2}| < V_{DD} \Rightarrow |V_{g1} - V_{g2}| < V_{DD} \rightarrow \text{condition}$$

$$(AV \cdot V_{DD}) - AV = pAV = 2V$$

~~Feedback mechanism~~ ~~Feedback mechanism~~

~~Feedback mechanism~~ ~~Feedback mechanism~~ ~~Feedback mechanism~~

~~Feedback mechanism~~ ~~Feedback mechanism~~