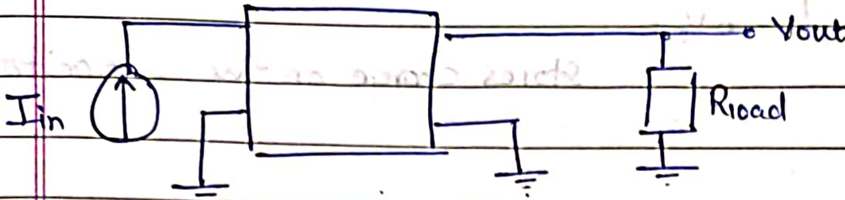
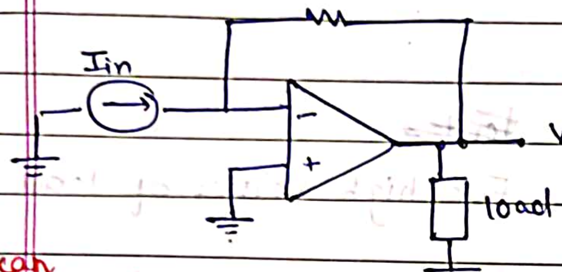
MORE OPAMP APPLICATION CIRCUITS

⇒ Current - To - Voltage - Converter



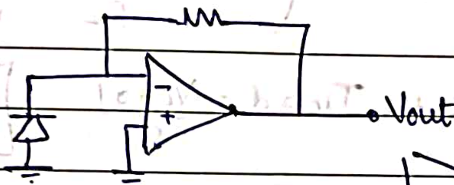


Problem ⇒ Voltage across the current-source = 0 ($R \to \infty$)

it may NOT work.

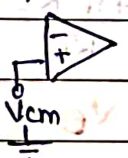
opamp can source/sink

(Radiation detector)

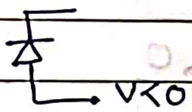


- The diode will be biased at 0
- If the diode is photovoltaic diode (cell)
  - ↳ it will work

To solve this problem,

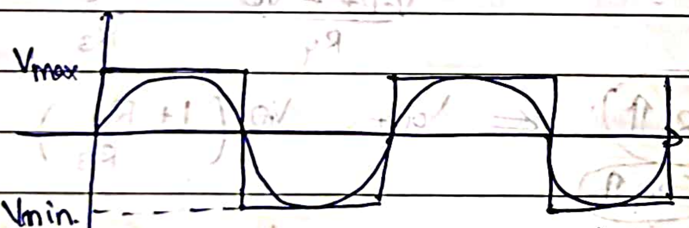


Or

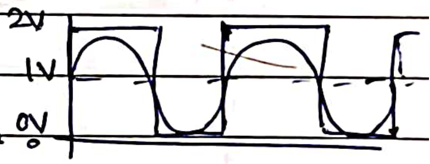


connect it to a -ve supply

⇒ if external supply is -ve, it is NOT a problem unless the voltage is +ve at all other points.



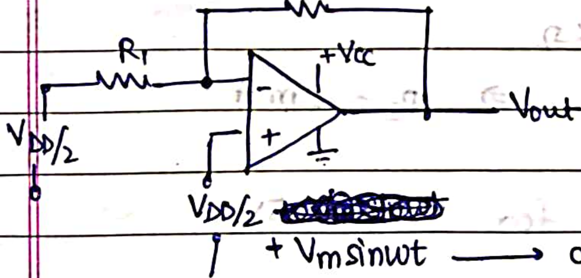
shift graph upwards ⟹



since we don't want -ve voltages

all signals have a DC value

used everywhere ex. supply ⟵ ($V_{DD}/2$) analog ground ⟸ DC output also increases

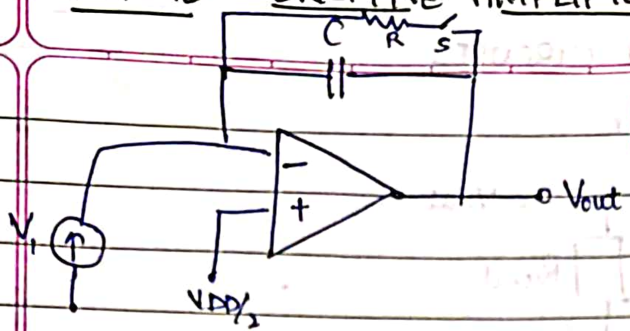


$I = 0 \to V_{out} = V_{DD}/2$

⟶ (DC does NOT change)

$+ V_m \sin \omega t$ ⟶ average doesn't change ⟹ $V_{out} = \frac{V_{DD}}{2} + \left(1 + \frac{R_2}{R_1}\right) V_m \sin \omega t$

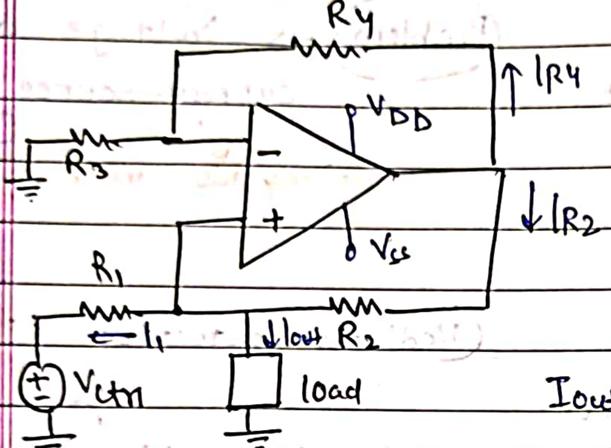
CHARGE SENSITIVE AMPLIFIER



(Integrator)

stores charge on the capacitor.

Voltage-To-Current Converter



~~Iout =~~

For high values of load,

(also: $\frac{R_1}{R_2} = \frac{R_3}{R_4}$)

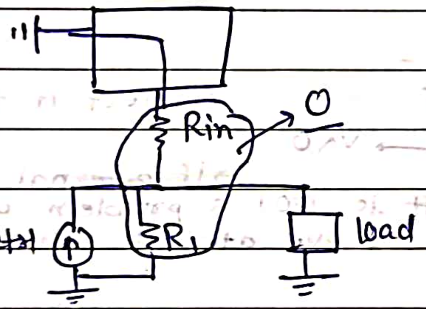
$I_{out} = I_{load} = \frac{V_{ctrl}}{R_1}$ [as $R_{in} = -R_1$].

⇓

$V_\oplus = I_{out} \times R_L$

$V_\oplus = \frac{V_{ctrl} R_L}{R_1}$

$\frac{V_{ctrl}}{R_1} = I_{ctrl}$



$\boxed{R_L \Uparrow \Rightarrow V_\oplus \Uparrow}$

↳ $I_{R_2} = I_{out} + I_1$

as $V_\oplus \Uparrow$ and

$\frac{V_{out} - V_\ominus}{R_4} = \frac{V_\oplus}{R_3}$

$I_{R_2} \Uparrow \Leftarrow V_{out} = V_\oplus \left(1 + \frac{R_4}{R_3}\right) \Uparrow$

also, $I_{R_4} \Uparrow$

↳ High current drawn from Op Amp supplies.

if $(I_{out})_{max.} = 1\ mA$

$(Load)_{max.} = 3\ K\Omega$ $\quad (V_\oplus)_{max.} = 3V.$

$V_{ctrl} = 1.5V \Rightarrow R_1 = 1.5\ K\Omega$

$I_1 = \frac{3 - 1.5}{1.5\ K\Omega} = 1\ mA \quad \Rightarrow I_{R_2} = 2\ mA$

assume $(V_{out})_{opamp,\ sat} = 4V$ for ~~VDD = 5V~~

$R_2 < \frac{4 - 3}{2\ mA} = 0.5\ K\Omega$

let's say $R_2 = 0.4k\Omega$ then $\frac{R_3}{R_4} = \frac{R_1}{R_2} = \frac{1.5}{0.4} = 3.75$

⇒ If the load is increased: $3k\Omega \rightarrow 5k\Omega$.

$(V_+)_{max.} = \frac{1.5 \times 5k\Omega}{1.5k\Omega} = 5V \rightarrow$ (V_{out} can't be 4V)

$I_1 = \frac{5-1.5}{1.5} = 2.3mA \Rightarrow I_{R_2} = 3.3mA$

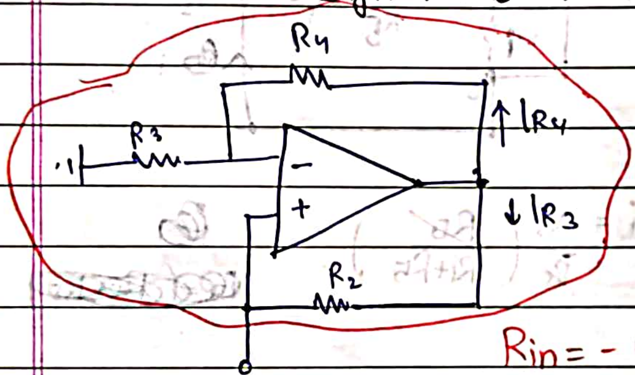
high current ; need higher VDD.

⇒ Assume $(V_{out})_{sat} = 7V$ for $V_{DD} = 8V$

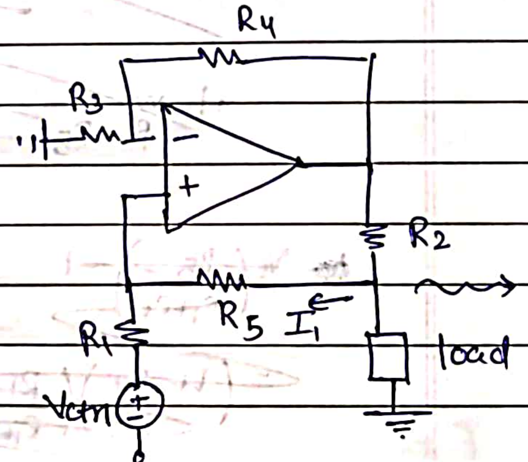
$R_2 < \frac{7-5}{3.3mA} = 0.6k\Omega \quad R_2 = 0.5k\Omega \Rightarrow \frac{R_3}{R_4} = 3$

MODIFIED HOWLAND CURRENT SOURCE

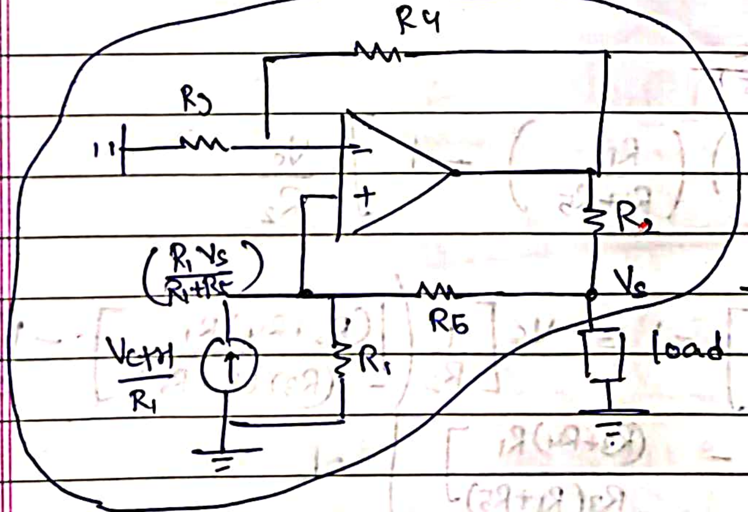
(High values of load)

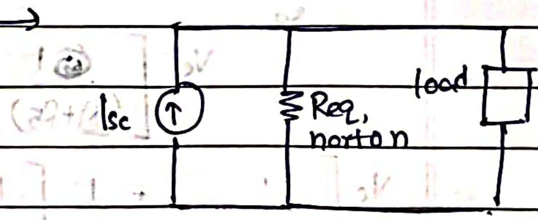


$R_{in} = -\frac{R_3 R_4}{R_2}$



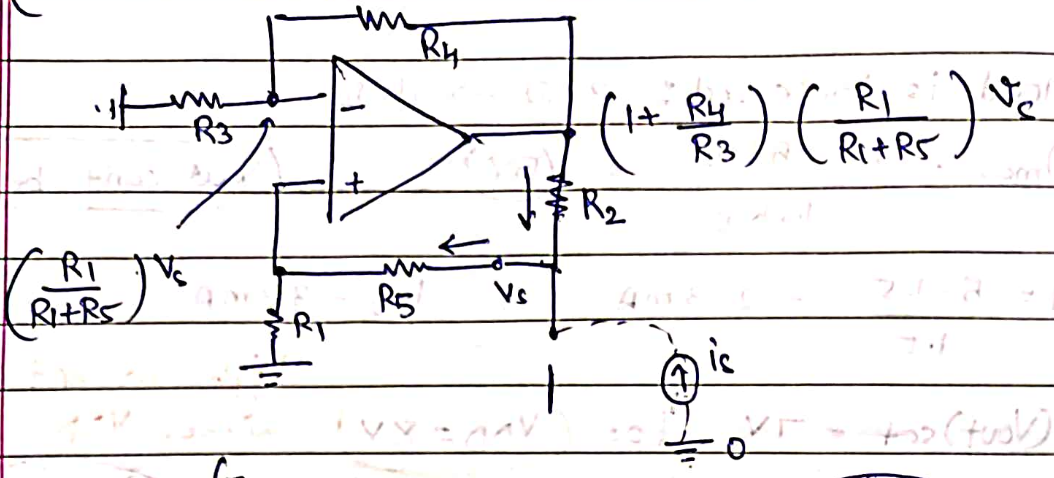
moving load away from + terminal of OpAmp reduces V_+ and also I_{R_2} and I_{R_4}.



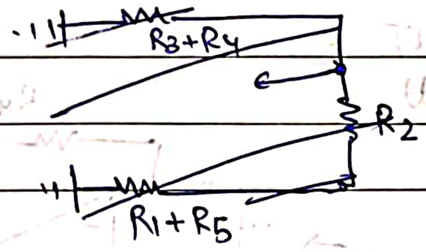


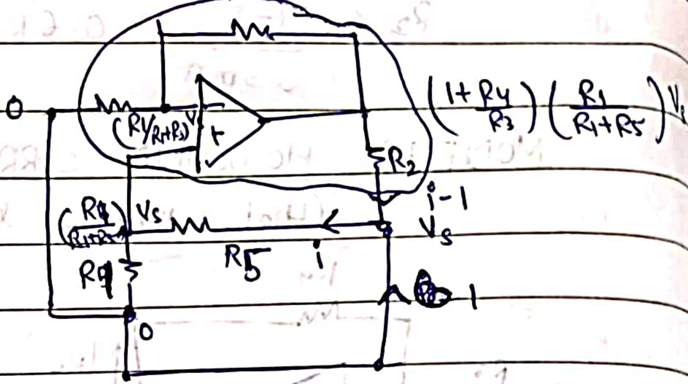
OPEN- CIRCUIT $\Rightarrow$

(and remove voltage sources)



$$G_{eq} = \frac{1}{R_{eq}} = 0$$





$$\cancel{V_s\left(\frac{R_5}{R_1+R_5}\right)-1}$$

$$i = \frac{V_s}{\cancel{R}}\left(\frac{\cancel{R_5}}{R_1+R_5}\right)$$

$$\cancel{=\left(1+\frac{R_4}{R_3}\right)\left(\frac{R_1}{R_1+R_5}\right)V_s}$$

$$\cancel{V_s\left(\frac{1}{(R_1+R_5)}\left(R_5-R_1\left(1+\frac{R_4}{R_3}\right)\right)\right)=1}$$

$$\cancel{\frac{i_s}{V_s} = R_{eq} = \frac{1}{(R_1+R_5)}}$$

$$i-1 = \left[\left(1+\frac{R_4}{R_3}\right)\left(\frac{R_1}{R_1+R_5}\right)-1\right]\frac{V_s}{R_2}$$

so,

$$V_s\left[\frac{1}{(R_1+R_5)}\right]-1 = V_s\left[\frac{1}{R_2}\left(\left[\frac{(R_3+R_4)R_1}{(R_3)(R_1+R_5)}\right]-1\right)\right]$$

$$V_s\left[\frac{1}{R_1+R_5}+\frac{1}{R_2}\left[1-\frac{(R_3+R_4)R_1}{R_3(R_1+R_5)}\right]\right]=1$$

$$G_{eq} = \frac{1}{R_1+R_5}+\frac{1}{R_2}\left[\frac{\cancel{R_3R_1}+R_3R_5-\cancel{R_3R_1}-R_4R_1}{R_3(R_1+R_5)}\right]$$

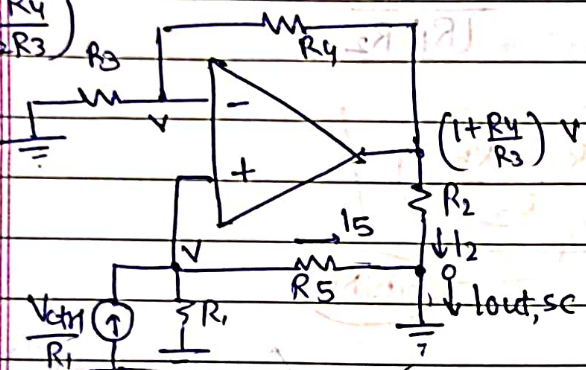
$$G_{eq} = \frac{1}{R_1+R_5} + \frac{1}{R_2}\left[\frac{(R_5/R_1) - (R_4/R_3)}{(1+R_5/R_1)}\right] = 0$$

so, $$\frac{1}{R_1} + \frac{1}{R_2}\left(\frac{R_5}{R_1}\right) = \frac{1}{R_2}\left(\frac{R_4}{R_3}\right)$$

$$R_2+R_5 = \frac{R_1R_4}{R_3} \qquad \frac{R_2}{R_1} + \frac{R_5}{R_1} = \frac{R_4}{R_3} \qquad \boxed{\frac{R_4}{R_3} = \frac{R_2+R_5}{R_1}}$$

$$\left(1+\frac{R_5}{R_2} = \frac{R_1R_4}{R_2R_3}\right)$$

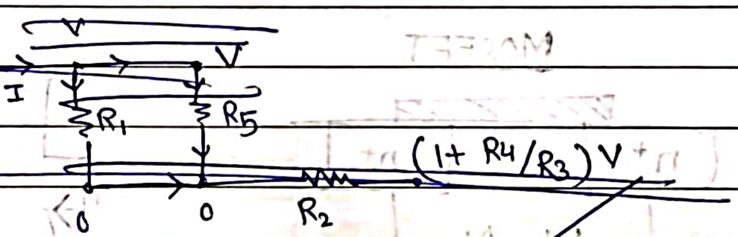
$(R_{eq} \to \infty)$



$$I_5 = \left(\frac{\cancel{R_1}}{R_1+R_5}\right)\cdot\frac{V_{ctrl}}{\cancel{R_1}}$$

$$I_2 = \left(\frac{V_{ctrl}}{R_1}\right)\left(\frac{R_1}{R_1+R_5}\right)R_5\left(1+\frac{R_4}{R_3}\right)\cdot\frac{1}{R_2}$$

$$I_2 = (R_1 \| R_5)\,\frac{V_{ctrl}}{R_1}\left(1+\frac{R_4}{R_3}\right)\left(\frac{1}{R_2}\right)$$



$$I = \frac{V}{R_1\|R_5}$$

$$V = I(R_1\|R_5)$$

and so $$I_2 = \left(1+\frac{R_4}{R_3}\right)\frac{V}{R_2} = \left(1+\frac{R_4}{R_3}\right)\frac{V_{ctrl}}{R_1R_2}(R_1\|R_5)$$

$$I_2 = \left(\frac{R_3+R_4}{R_3}\right)\left(\frac{V_{ctrl}}{R_2}\right)\left(\frac{R_5}{R_1+R_5}\right)$$

so, $$I_{sc} = \frac{\cancel{V_{ctrl}}}{(\cancel{R_1+R_5})}\;\frac{V_{ctrl}}{R_1}\left(\frac{R_1}{R_1+R_5} + \left(1+\frac{R_4}{R_3}\right)(R_1\|R_5)\cdot\frac{1}{R_2}\right)$$

Using $$\frac{R_4}{R_3} = \frac{R_2+R_5}{R_1}$$

$$\frac{R_1}{R_1+R_5} + \frac{R_1+R_2+R_5}{R_1}\left(\frac{R_1R_5}{R_1+R_5}\right)\cdot\frac{1}{R_2}$$

$$V = I(R_1\|R_5) \qquad \left(1+\frac{R_4}{R_3}\right)(R_1\|R_5)\,\frac{1}{R_2}\left(\frac{V_{ctrl}}{R_1}\right)$$

$$+\left(\frac{1}{R_2}+\frac{1}{R_1}+\frac{1}{R_2}\frac{R_5}{R_1}\right)\left(\frac{R_1R_5}{R_1+R_5}\right)\left(\frac{V_{ctrl}}{R_1}\right)$$

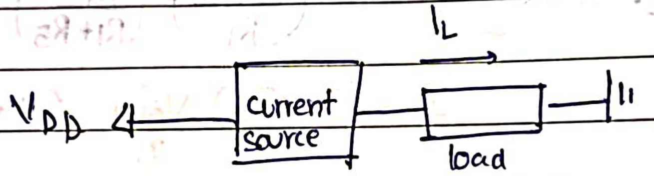
$$I_2 = \left(1+\frac{R_4}{R_3}\right)\left(\frac{R_1 R_5}{R_1+R_5}\right)\left(\frac{V_{ctrl}}{R_1}\right)\left(\frac{1}{R_2}\right).$$

$$I_{sc} = \frac{R_1}{R_1+R_5}\cdot\frac{V_{ctrl}}{R_1}\left[\frac{R_5}{R_2}\left(1+\frac{R_4}{R_3}\right)+1\right]$$

$$= \left(\frac{\cancel{R_1}}{R_1+R_5}\right)\frac{V_{ctrl}}{\cancel{R_1}}\left[\frac{R_5 R_4}{R_2 R_3}+\frac{R_1 R_4}{R_2 R_3}\right].$$

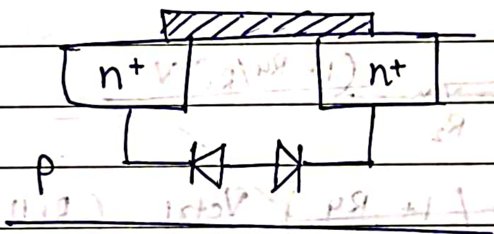
$$= \left(\frac{R_4}{R_2 R_3}\right)\left(\frac{V_{ctrl}}{\cancel{R_1}}\right) = \frac{R_2+R_5}{(R_1)R_2}\cdot V_{ctrl}$$

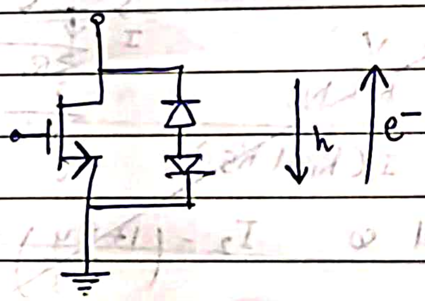
$$\boxed{I_{out,sc} = \left(\frac{V_{ctrl}}{R_1}\right)\left(\underbrace{\frac{R_2+R_5}{R_2}}_{GAIN}\right)}$$



(equivalent circuit)

MOSFET





$SiO_2 \rightarrow$ breakdown $\longrightarrow$ T reaches a max^m value

$\rightarrow$ SiO_2: $E_{max} \approx 0.5\ \frac{V}{nm}$

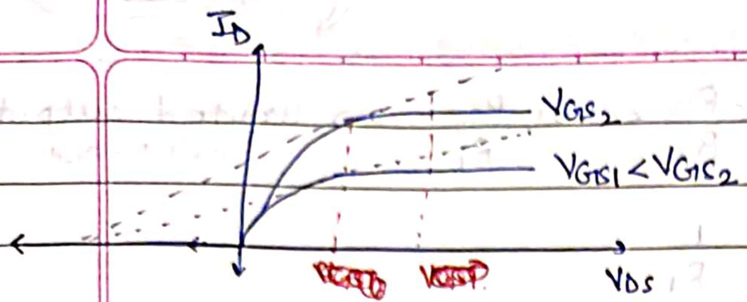
4nm oxide $\longrightarrow$ @ 2V $\rightarrow$ breakdown. $\Rightarrow$ $\boxed{\text{Not reversible}}$

$\rightarrow$ b/w gate and any part of channel, voltage shouldn't be more than 2

so, we have a $\boxed{(V_{gs})_{max} = (V_{gD})_{max} = (V_{gB})_{max} = 1.8V \text{ fore core devices in 180nm CMOS technology}}$

saturation:→

$\cancel{I_D = \mu_n C_{ox} \frac{W}{L} \cdot \frac{1}{2}(V_{GST}^2)(1+\lambda V_{DS})}$



$V_{DS} > V_{GST}$ $\quad I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{gst}^2)\left[1+\lambda[V_{DS}-V_{gst_i}]\right]$

$(i = 1/2 \ldots)$

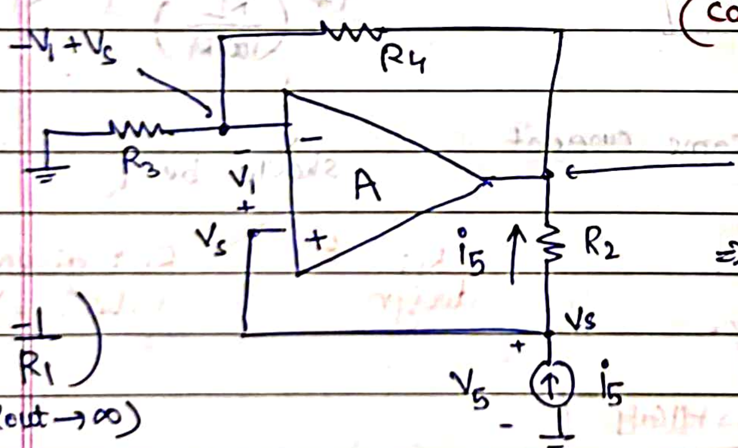
Saturation region ⇒ $\frac{\Delta I_D}{\Delta V_{DS}} = I_{D1}\cdot\lambda$ so, $\boxed{r_{out} = \frac{1}{\lambda I_D}}$

CMOS OpAmp Specifications

- → V_{DD} range
- → open-loop gain (AV)
- → unity gain frequency
- → input CM voltage range
- → output voltage range
- → input capacitance
- → output impedance
- → input offset voltage
- → output slew rate

OpAmp Gain Limitation

(condition for R1 depends on AV)



$AV_1 = \left(1+\frac{R_4}{R_3}\right)(V_s - V_1)$

$\Rightarrow AV_1 = \frac{A(1+R_4/R_3)}{(A+1+R_4/R_3)} \cdot V_s$

$V_{R_2} = V_s - AV_1 \Rightarrow i_s = \frac{V_s - AV_1}{R_2}$

$\left(\frac{i_s}{V_s} = \frac{-1}{R_1}\right)$ (for $R_{out}\to\infty$)

we get i_s as a function of V_s → Req → can be computed

i ⇒ function of a load

MISMATCH EFFECTS

eg.- $\frac{R_4}{R_3} = \frac{R_2}{R_1}(1-\varepsilon)$ $\quad\varepsilon$: small no.

↳ in a Howland VCCS.

Let $\varepsilon = \pm 1\%$ $\Rightarrow$ $0.99\frac{R_2}{R_1} \le \frac{R_4}{R_3} \le 1.01\frac{R_2}{R_1}$ $\longrightarrow$ limited output resistance

$$G_{out} = \frac{-R_4}{R_2R_3} + \frac{1}{R_1}$$
(output resistance)

$$= \frac{1}{R_1}\left[1 - \frac{R_1}{R_2}\cdot\frac{R_4}{R_3}\right]$$

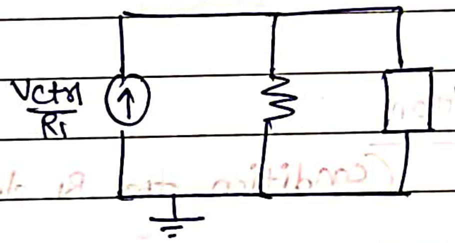
$$= \frac{1}{R_1}\left(1 - \frac{R_4/R_3}{R_2/R_1}\right) = \frac{1}{R_1}(\varepsilon) \rightarrow +0.01/R_1,\ -0.01/R_1$$

circuit may become unstable.

boundary values :-

$$G_{out} \Rightarrow \begin{cases} \frac{0.01}{R_1} \Rightarrow R_{out} = 100R_1 \\ \frac{-0.01}{R_1} \Rightarrow R_{out} = -100R_1 \end{cases}$$

stability output



$$I_{out} = \frac{100R_1}{100R_1 + R_L}\cdot\left(\frac{V_{ctrl}}{R_1}\right)$$

$$I_{out} = \frac{1}{1 + \left(\frac{R_L}{100R_1}\right)}\left(\frac{V_{ctrl}}{R_1}\right)$$

should be 1

R_1: design — R_L: given (change)

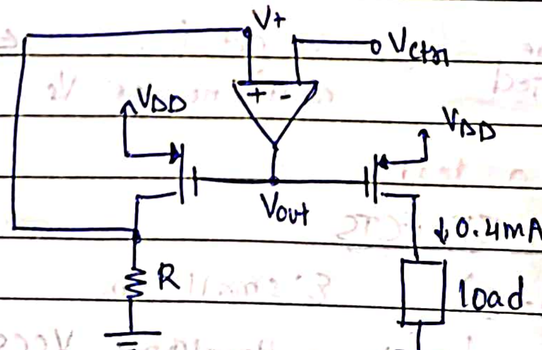
$R_1\uparrow \rightarrow V_{ctrl}\uparrow$ for same current

worst case error :

$\left(\frac{R_L}{100R_1}\right) \rightarrow$ max.

$\boxed{R_L \rightarrow \text{HIGH}}$

$\Rightarrow$



$\rightarrow$ it looks like +ve, BUT, it is -ve feedback

if $V_+ \Uparrow \Rightarrow V_D\uparrow$ of the pMOS

$I\uparrow \rightarrow$ Vgate should be lesser for I to be higher

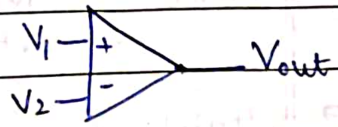
Hence, it is a -ve feedback

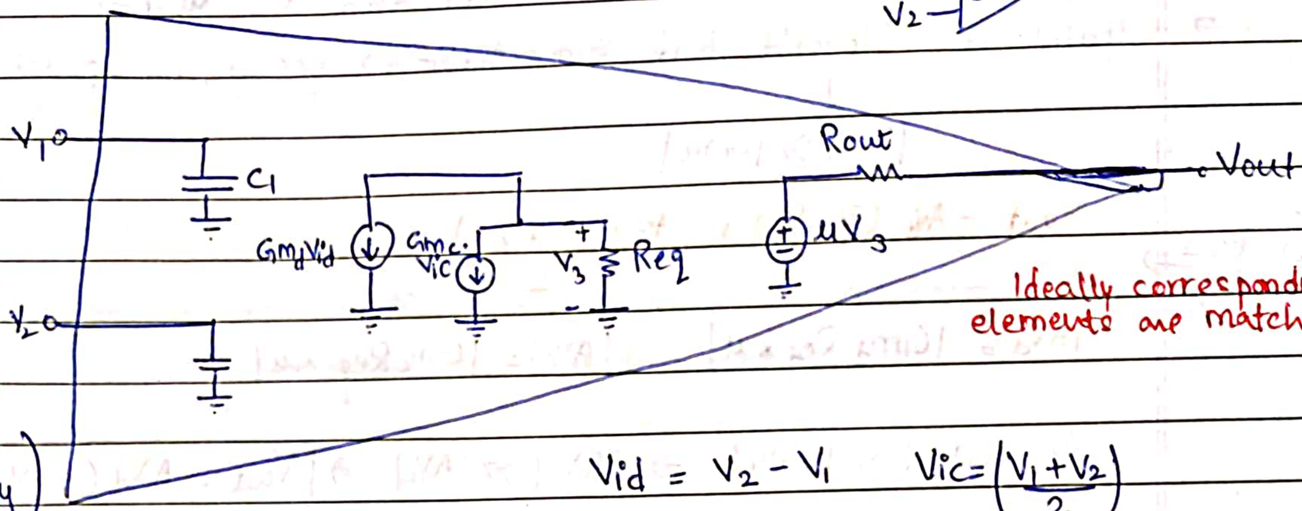
so, $V_g\downarrow$ $\leftarrow$ $V_{sg} = (V_{DD} - V_g)$

$I = K[V_{sg} - |V_{tp}|]^2$

MODEL AND ANALYSIS FOR SIGNAL AMPLIFICATION

CIRCUIT inside CMOS OpAmp





Ideally corresponding elements are matched.

(low frequency inputs)

$$V_{id} = V_2 - V_1 \qquad V_{ic} = \left(\frac{V_1 + V_2}{2}\right)$$

CMOS OpAmps are designed based on MOSFET's **biased** as signal amplific^n elements and other analog operations. ← (satur^n)

if $V_1 = V_2$
$V_{ic} = V_1 = V_2$; $V_{id} = 0$
if $V_1 = -V_2$
$V_{id} = 2V_1$; $V_{ic} = 0$

2 VCCS → respond to V_{id}, V_{ic} → currents added
↓
amplify the voltage.

① $|Gm_c| \ll |Gm_d|$
② Req : High, Rout : Low/Medium
⇒ 0° phase difference, $V_{ic} \simeq$ average ; 180° phase difference, $V_{ic} \simeq 0$.
③ Gm_c : very small

eg. $Gm_d = 1\ mA/V$ $\quad$ Req = 500 KΩ ; $\quad Gm_c = 0.1\ \mu A/V$

So, $\underbrace{|Gm_d\, Req| = 500}_{\text{diff. mode gain}}$ $\qquad \underbrace{|Gm_c\, Req| = 0.05}_{\text{common mode gain}}$

CMRR (common-mode rejection ratio) $= \left|\dfrac{Gm_D \cdot Req}{Gm_c \cdot Req}\right|$.

$$CMRR = \left(\frac{500}{500 \times 10^{-4}}\right) \rightarrow 20 \log\left(\frac{500}{500 \times 10^{-4}}\right)$$

$$\boxed{CMRR = 80\ dB}$$

both the currents are added & flowing together.

Date
Page

⇒ MOSFET is a non-linear element → how to get a linear OpAmp behavior from the MOSFET

⇒ Special model doesn't have $V_{out} = A_V(V_1 - V_2)$ except in special condit…
↓
$|G_{md}| \gg |G_{mc}|$.

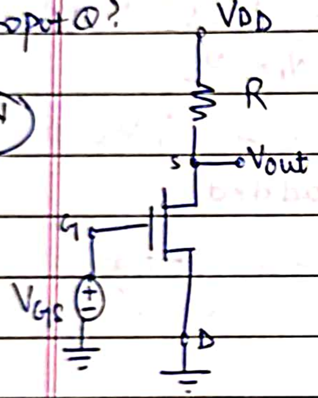
realistic model ⇒ $V_{out} = A_{Vd}(V_1 - V_2) + A_{Vc}\left(\frac{V_1 + V_2}{2}\right)$

$|A_{Vd}| = |G_{md} R_{eq} \times \mu|$ $|A_{Vc}| = |G_{mc} R_{eq} \times \mu|$

If $|G_{md}| \gg |G_{mc}|$ ⇒ $|A_{Vd}| \gg |A_{Vc}|$ ⇒ $\boxed{V_{out} = A_{Vd}(V_1 - V_2)}$

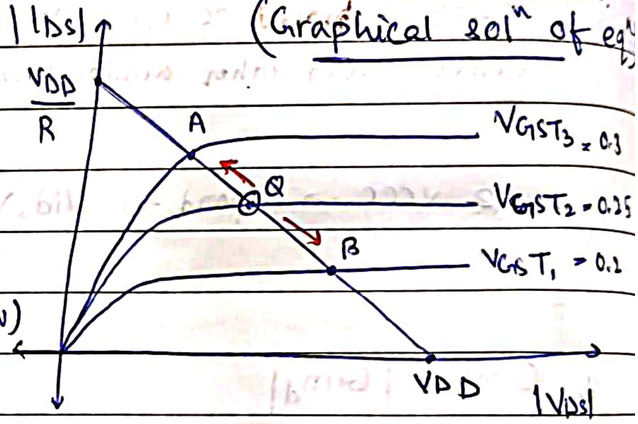
Approximate Linear Amplificat^n from a Transistor circuit

where to put Q?
↓
GAIN



$\boxed{Q}$
(Quiscent Point)
↓
somewhere in b/w)

(Graphical sol^n of eq^n)



$|V_{DS}| > |V_{gs} - V_T|$
i.e. $|V_{DS}| > |V_{gst}|$ $V_{DD} = RI_D + V_{DS}$

$$\boxed{I_{DS} = \frac{V_{DD}}{R} - \frac{V_{DS}}{R}}$$

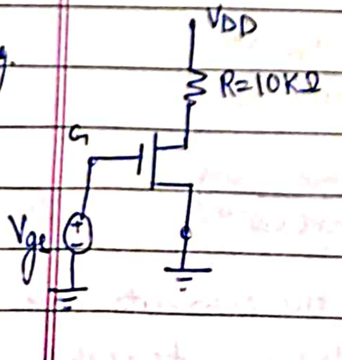
$V_{gs} = 0.25 \pm \Delta V_{gs}$

$\Delta V_{gs} = \begin{cases} +50mV & (A) \\ 0 & \\ -50mV & (B) \end{cases}$

as we ↑ V_{gst}, threshold moves to Right [Don't consider linear region]

⇒ As, $V_{gsT} \Downarrow$ ⇒ $I_D \downarrow$ as $V_{DS} \uparrow$ or $\boxed{V_{DS} \downarrow \Rightarrow I_D \uparrow}$
(on changing V_{gst} also)

eg.



λ: negligible, $\mu_n C_{ox} = 400\,\mu A/V^2$, $W/L = 10$, $V_{DD} = 3V$

$\left.\begin{array}{l} V_{gsTA} = 0.3 \\ V_{gsT}B = 0.25 \\ V_{gsT}C = 0.2 \end{array}\right\} \rightarrow \left.\begin{array}{l} I_D = 180\mu A \\ I_D = 125\mu A \\ I_D = 80\mu A \end{array}\right\} \Rightarrow \begin{array}{l} V_{DS} = 1.2\ V \\ = 1.78\ V \\ = 2.2\ V \end{array}$

↓
(using line eq^n)

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NOT THE SAME → limit of ΔV_{gsT} → more than 50mV, the diff is lesser.

$\frac{\Delta V_{DSA}}{\Delta V_{gsTA}} = \frac{-0.58}{0.05} = -11.6$

$\frac{\Delta V_{DSB}}{\Delta V_{gsTB}} = \frac{0.42}{0.05} = +8.4$

$\Delta V_{DST} \simeq$ (10 times) ΔV_{gsT}

(Amplification of incremental Values.)

⇒ we get an almost linear behavior for incremental values from MOSFET.

⇒ all the variables in Vout are incremental variables.
e.g. - Voice - incremental change in the signal.
↳ amplifier → increases the incremental values.

⇒ $\Delta V_{gst} = 10\,mV \;/\; 20\,mV \;/\; 30\,mV$ (linear → nonlinear)

→ Voltage and current compliance
⇒ Voltage and current rating

V_1, V_2 → [box] → Vout

$V_{id} = V_1 - V_2$

NOISE ⊗

if $V_1 = V_2$ ($V_{id} = 0$)
↳ Vout = 0

entire info. is blocked

$V_{out} = A(V_1 - V_2) = AV_{id}$

(Difference Amplifier)

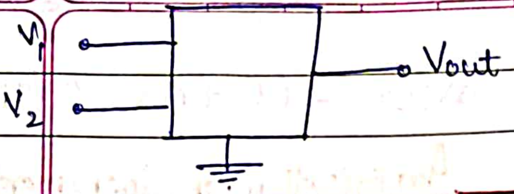
$V_1 = -V_2 \Rightarrow V_1 - V_2 = 2V_1 = -2V_2$ ⇒ $\boxed{V_1 = \frac{V_{id}}{2} \quad V_2 = -\frac{V_{id}}{2}}$ → ideal condition

$\boxed{\text{entire info. is passed}}$

reality) $V_1 = \frac{V_{id}}{2} + x \quad V_2 = -\frac{V_{id}}{2} + y$ → $\boxed{x = y = \frac{V_1 + V_2}{2}}$

and $V_1 = -V_2$ $\left(\begin{array}{l} V_1 - x = y - V_2 \\ x + y = V_1 + V_2 \end{array} \right)$

(common-mode.)
(shows up)



$V_{id} = V_1 - V_2$

$V_{ic} = \dfrac{V_1 + V_2}{2}$

$$\boxed{V_1 = \frac{V_{id}}{2} + V_{ic}} \quad \boxed{V_2 = \frac{-V_{id}}{2} + V_{ic}}$$

as long as the circuit is linear $\rightarrow$ $\boxed{\text{superposition}}$

see effect of V_{id} $\oplus$ see effect of V_{ic}

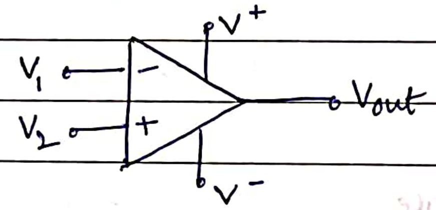
For some linear circuit, $y = aV_{id} + bV_{ic}$,

$$a = \left.\frac{y}{V_{id}}\right|_{V_{ic}=0} \qquad b = \left.\frac{y}{V_{ic}}\right|_{V_{id}=0}$$

[superposition principle]

Also note :- $\boxed{|bV_{ic}| \ll |aV_{id}|}$

in real conditions $\rightarrow$ $|V_{ic}| \gg |V_{id}|$ $\rightarrow$ 1mV signal and 1V noise is NOT



CMRR > 100 dB

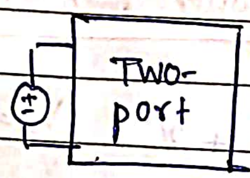
i.e. $\left|\dfrac{A_d}{A_c}\right| > 100\,dB$ [20log(

$\Rightarrow$ if the signal has a +ve swing only $\Rightarrow$ pull Q down ; -ve swing $\Rightarrow$ pull Q up

$V_{GS} = V_{GS,Q} + \Delta V_{GS}$

$$\boxed{\Delta I_D = \left(\frac{\partial I_D}{\partial V_{GS}}\right)\Delta V_{GS} + \left(\frac{\partial I_D}{\partial V_{DS}}\right)\Delta V_{DS}}$$

find (ΔI_D) at Q

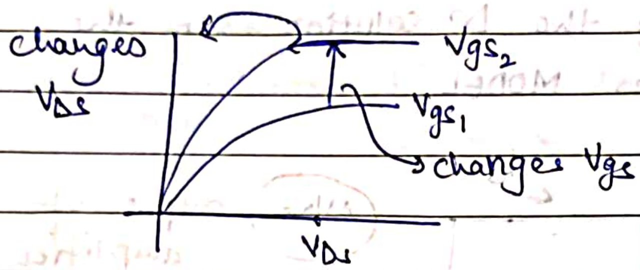


Q

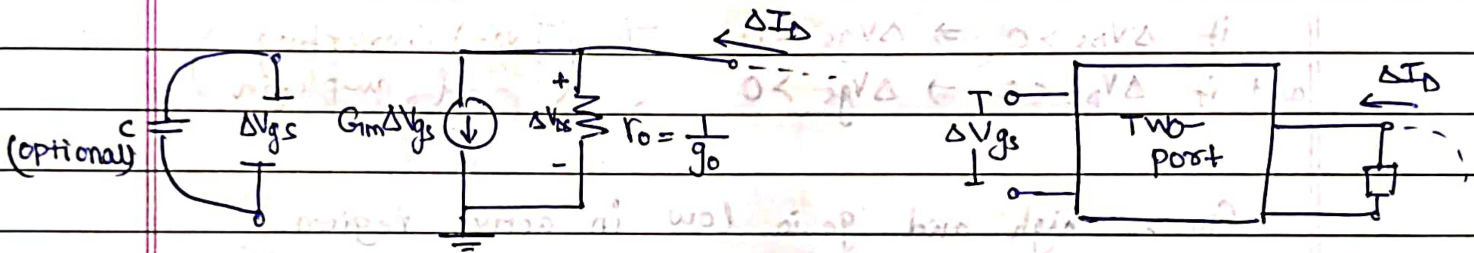
$V_{GS} = V_{GSQ} + \Delta V_{GS}$

$I_D = f(V_{GS}, V_{DS})$

$$\Delta I_D = \frac{\partial f}{\partial V_{GS}}\Bigg|_{\substack{V_{GS}=V_{GSQ}\\ V_{DS}=V_{DSQ}}} \overbrace{(V_{GS}-V_{GSQ})}^{\Delta V_{GS}} + \frac{\partial f}{\partial V_{DS}}\Bigg|_{\substack{V_{GS}=V_{GSQ}\\ V_{DS}=V_{DSQ}}} \overbrace{(V_{DS}-V_{DSQ})}^{\Delta V_{DS}}$$

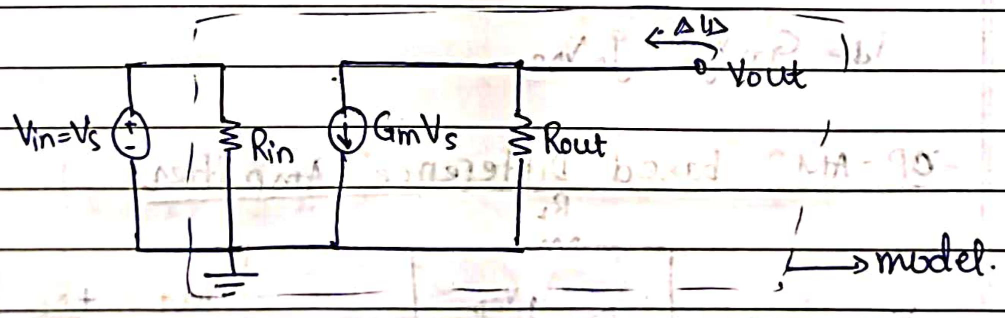


So, $\Delta I_D = G_m \Delta V_{GS}\Big|_{V_{DS}:\text{ constant}} + g_o \Delta V_{DS}\Big|_{V_{GS}:\text{ constant.}}$

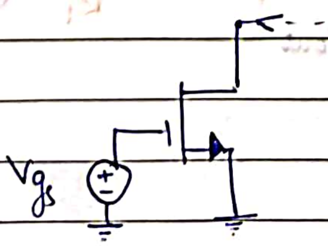


Assumptions:- 1) ΔV_{gs} is small
2) $I_g = 0$

(SMALL SIGNAL MODEL) ⇒



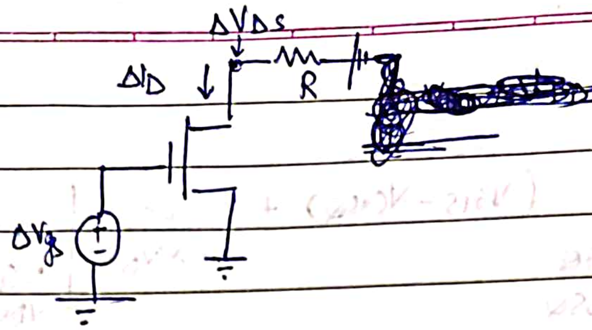
$V_{gs} = V_{gsQ} + \Delta V_{gs}$



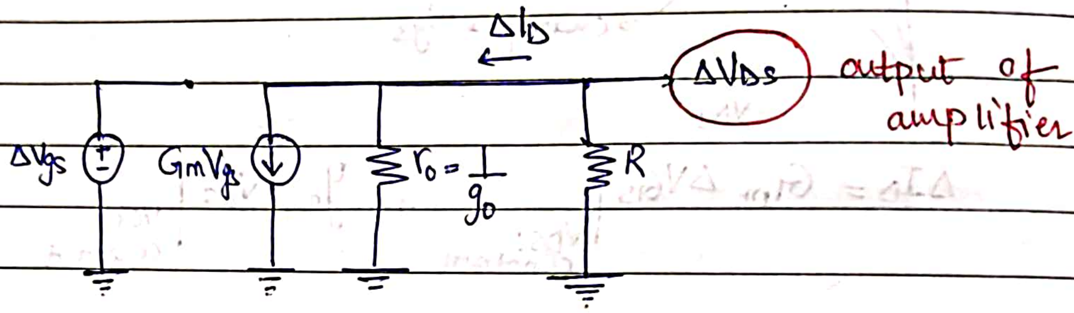
$\Delta I_D = G_m \Delta V_{gs}\Big|_{V_{DS}} + g_o \Delta V_{DS}\Big|_{V_{GS}}$

DC value of V_{gs} i.e. V_{gsQ} won't appear here

(Model only for small-signals)



⇒ We are decoupling the DC solution from the incremental changes MODEL.



if $\Delta V_{DS} > 0 \Rightarrow \Delta V_{gs} < 0$
and, if $\Delta V_{DS} < 0 \Rightarrow \Delta V_{gs} > 0$ → (Two-port) (inverting amplifier)

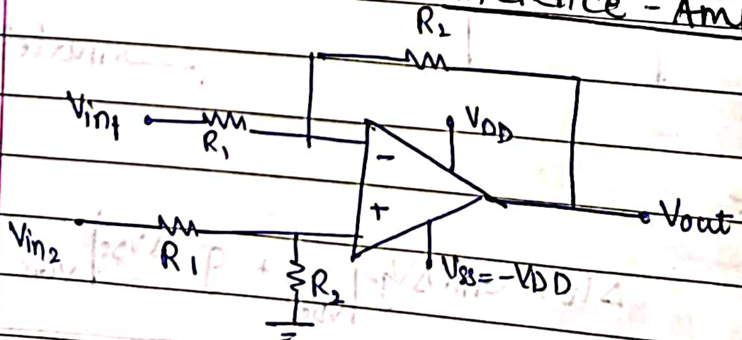
Gm is high and go is low in active region.

e.g. – $G_m = 0.5\ mA/V$ $\quad R_{out} = \frac{1}{g_o} = 100\,k\Omega$

$G_m R_{out} = 50$ → intrinsic gain of transistor

$i_d = G_m V_{gs} + g_o V_{DS}$

OP-AMP based Difference-Amplifier



$$\boxed{V_{out} = +\frac{R_2}{R_1}\left(V_{in_2} - V_{in_1}\right)}$$

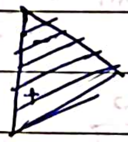
Input impedance → Differential mode input impedance.
→ Common mode input impedance.

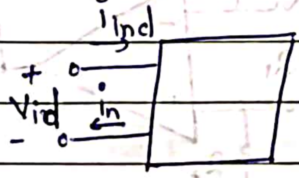
$$\boxed{V_{in1} = \frac{V_{id}}{2} + V_{ic}} \langle + \rangle \boxed{V_{in2} = -\frac{V_{id}}{2} + V_{ic}} \rightarrow \text{superposit}^n \text{ (linear)}$$

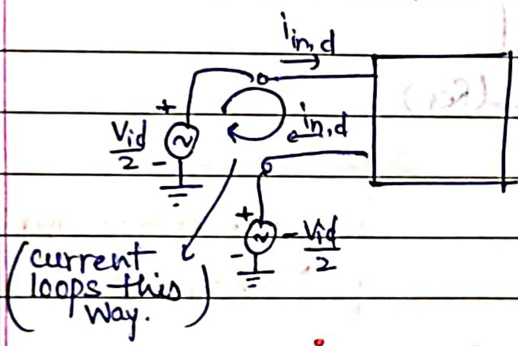
$$V_{id} = V_{in1} - V_{in2} \qquad V_{ic} = \frac{V_{in1} + V_{in2}}{2}$$

(Solve in differential mode) + (solve in common-mode)

$$R_d = \frac{V_{id}}{i_{in,d}}$$

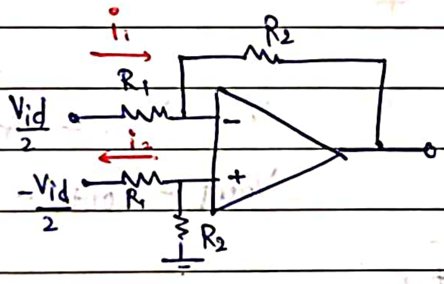






$\cancel{R_{in} = V_{id}/2}$

$$\boxed{R_{ind} = \frac{V_{id}}{i_{ind}}}$$



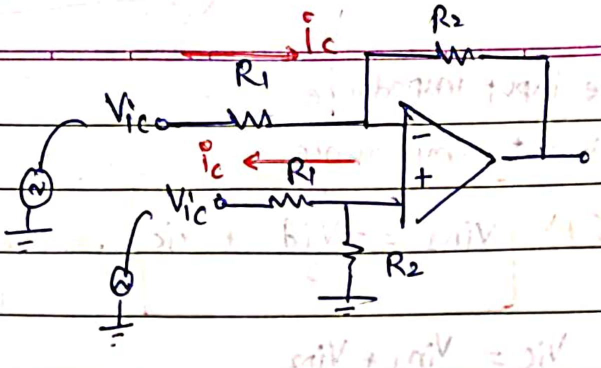
(⊖ ⊕ terminals are virtually shorted)

$$i_2 = \frac{+(V_{id}/2)}{(R_1+R_2)}$$

$$V_+ = \left(\frac{R_2}{R_1+R_2}\right)\left(-\frac{V_{id}}{2}\right)$$

$$i_1 = \frac{V_{id}/2 + \left(\frac{R_2}{R_1+R_2}\right)\left(+\frac{V_{id}}{2}\right)}{R_1} = \left(\frac{V_{id}}{2}\right)\left[\frac{R_1+2R_2}{(R_1+R_2)R_1}\right]$$

$$R_{ind}\Big|_{\frac{V_{id}}{2}} = \frac{V_{id}/2}{i_1} = \frac{R_1(R_1+R_2)}{R_1+2R_2} \qquad R_{in}\Big|_{-\frac{V_{id}}{2}} = (R_1+R_2)$$



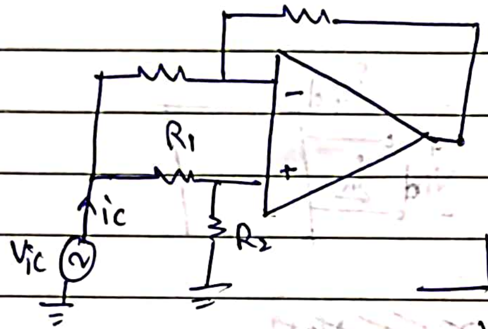
$$\frac{V_{ic}}{R_1}\left[1-\frac{R_2}{R_1+R_2}\right]$$

$$= \frac{V_{ic}}{R_1+R_2}$$

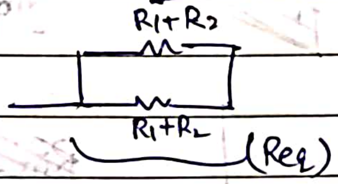
$\boxed{R_{inc} = R_1+R_2}$

So, we can say that $\boxed{V_{out} = 0}$ as $i_c = \frac{V_{ic}}{R_1+R_2}$,

R_1 & R_2 are in series..



$\boxed{R_{inc} = \frac{1}{2}(R_1+R_2)}$

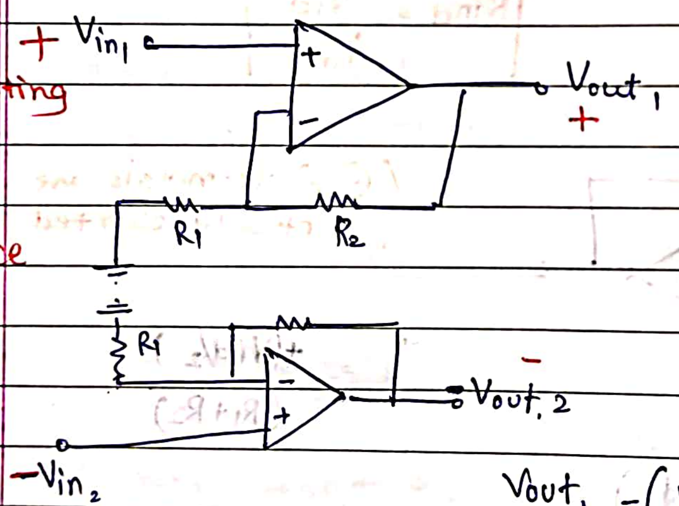


CONFIGURATION - II

Non-inverting

↓

∞ input impedance



Differential Input, Differential Output.

$$V_{in} = V_{in_1} - V_{in_2}$$

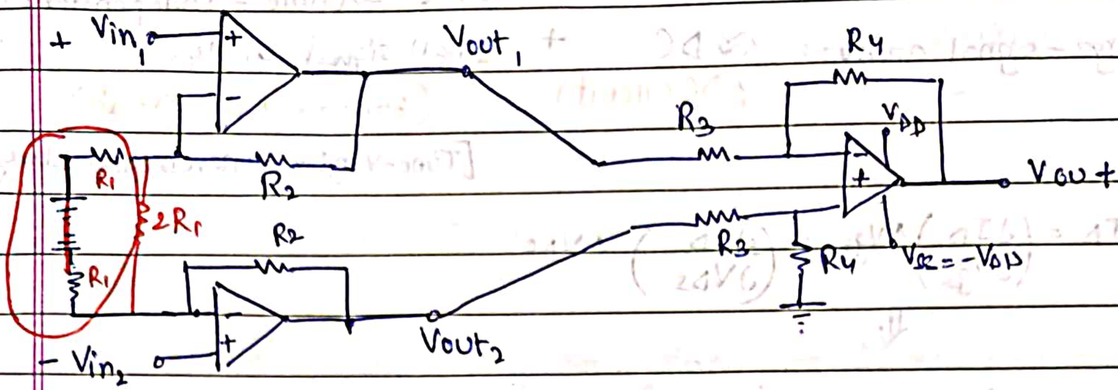
$$V_{out} = V_{out_1} - V_{out_2}$$

$$V_{out_1} = \left(1+\frac{R_2}{R_1}\right)V_{in_1}$$

$$+V_{out_2} = (1+R_2/R_1)(+V_{in_2})$$

$$\underbrace{V_{out_1} - V_{out_2}}_{\text{differential output}} = \left(1+\frac{R_2}{R_1}\right)\underbrace{\left[V_{in_1} - V_{in_2}\right]}_{\text{differential input}}$$

INSTRUMENTATION AMPLIFIER



(NOTE :- We practically analyze opAmp circuits in small-signal mode)

⇒ Common-mode gain ⇒ $\frac{V_{out}}{V_{ic}} = ?$ $V_{in_1} = V_{in_2} = V_{ic}$

$V_{out_1} = V_{out_2} = V_{ic}$

$V_{out} = 0$

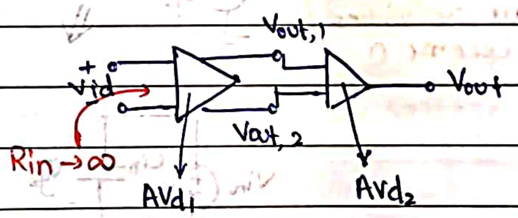
CM → | stage-1 G = 1 | → | stage-2 G = 0 |

$A_{VC_1} = 1 \, (0 \, dB)$

$A_{VC_2} = 0$

⇒ CMRR : High, Rin : High (inverting amplifier), Avd : High → (~ ideal)

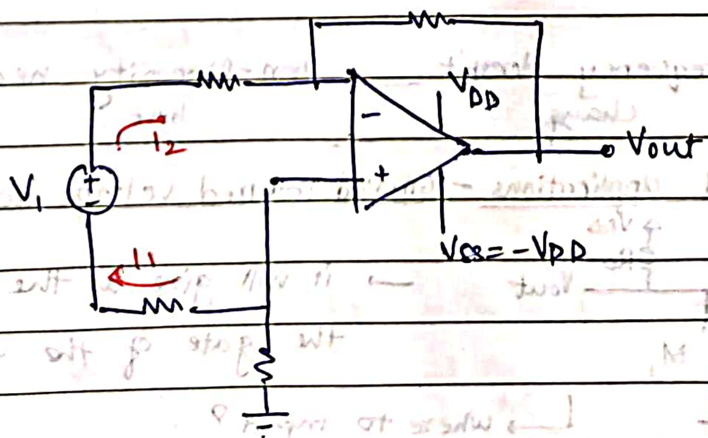
Block diagram :→



(signal) S → mV ⟶ $\left(\frac{V}{\mu V}\right)$ (amplify) at the output (rejected)

(noise) N_{CM} → V

$(10^{-3}) \rightsquigarrow (10^{6})$



We have imposed a condition → $I_1 = I_2$

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(DC)

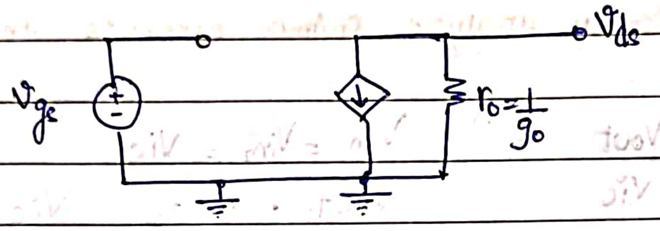
⇒ Input-Output Transfer characteristics ⇒ (time-independent)

⇒ large-signal analysis ≈ DC + small signal analysis
(DC circuit) (small-signal circuit)
[Time-varying / incremental change]

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{gs}}\right)\Delta V_{gs} + \left(\frac{\partial I_D}{\partial V_{DS}}\right)\Delta V_{DS}$$

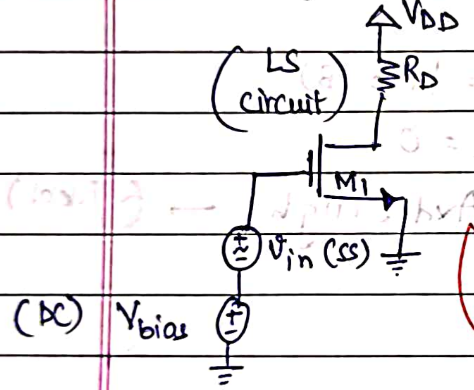
$$\Downarrow$$

$$i_d = G_m v_{gs} + G_o v_{ds}$$

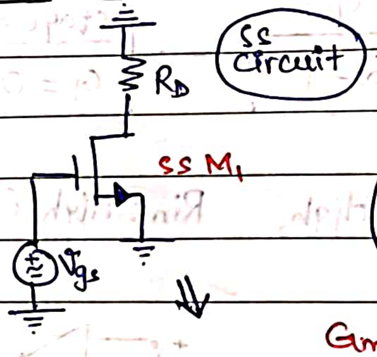


⇒ UNIVERSAL model [NMOS/PMOS]

Large Signal (LS) to small signal (SS) conversion

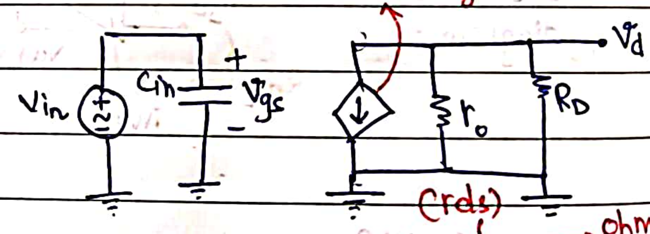


since we take derivatives, all incremental values remain, all DC values become 0



(C_{in} → comes from gate of the transistor (w+low))

$$\Downarrow$$



→ ohmic resistance

I_{DQ}, $\Delta I_D (i_d)$, I_D

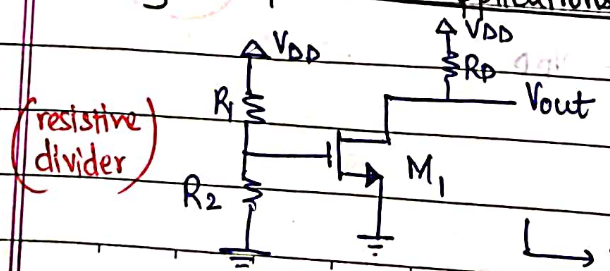
I_D at Q — incremental change — DC current

$$\boxed{I_D = I_{DQ} + \Delta I_D\,(i_d)}$$

$$\boxed{\underset{\text{(large signal)}}{Y} = \underset{\text{(DC)}}{Y} + \Delta Y}$$ → (small-signal)

linear system → frequency doesn't change → non-linearity needed here.

eg.- Biasing for practical applications - Ground-referred voltage sources



→ it will give us the bias at the gate of the transistor.

↳ where to input?

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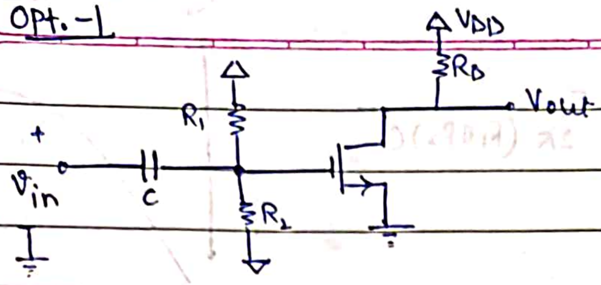
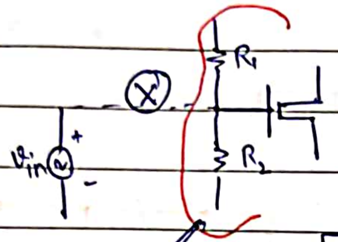
Opt.-I



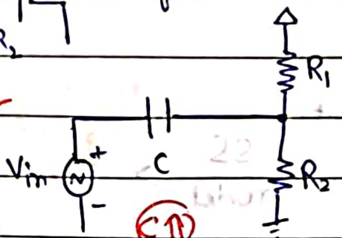
→ Capacitor is high enough to be consider ~shorted at frequencies of signal v_{in}

(Assume v_{in} does NOT have DC signal information)



DC circuit

if v_{in} = sine ⟶ DC value = 0 ⇒ $V_g = 0$



C: decouples the DC signal on both of its sides

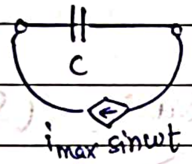
$(V_{GS})_Q = \boxed{V_g = V_{DD}\left(\frac{R_2}{R_1+R_2}\right)}$

C⇑

(C≈100uF)

⇒ Small signal part

$Z = \frac{1}{j\omega C⇑}$ ↓ ⇒ acts like a short even at low frequencies.

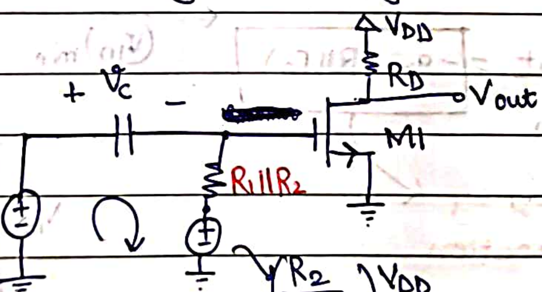


⇒ reactance ⇓ as capacitance ⇑

$\boxed{V_c = \frac{i_{max}}{\omega C}(\cos\omega t)}$ $V = \int \frac{1}{C} i \cdot dt$

capacitance ⇑ ⟶ can't change its voltage as fast as the current.

⇒ equivalent circuit ⇒



$\frac{1}{2\pi(R_1||R_2)C} \ll (f_{in})_{min.}$

[C: high]

Vin= ($V_{DC} + v_{max}\sin\omega t$)

$\left(\frac{R_2}{R_1+R_2}\right)V_{DD}$

DC component

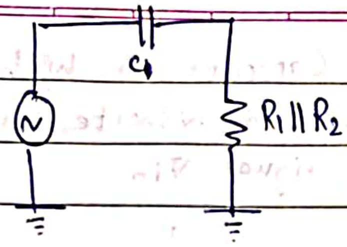
AC component ⇓ creates a current in the capacitor

$V_C = v_{in} - \frac{R_2}{R_1+R_2}V_{DD} \mp v_m \sin\omega t$

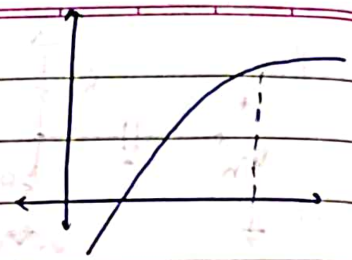
Small signal ⟶ short the capacitor and block DC

$V_c = V_{in} - \underbrace{\left(\frac{R_2}{R_1+R_2}\right)V_{DD}}_{\text{DC signal part } (i=0 \text{ as } \omega\to 0)} - \underbrace{v_m \sin\omega t}_{\text{AC signal part } (i \Rightarrow c \text{ is s.c})}$ ⇒ $\boxed{V_c = (V_{in})_{DC} - \left(\frac{R_2}{R_1+R_2}\right)V_{DD}}$

AC signal part → voltage across $R_1||R_2$

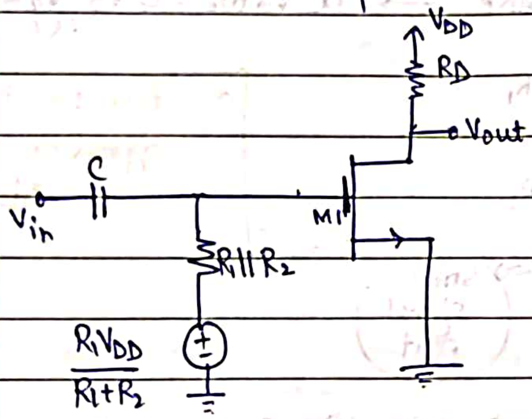


$$f_{cut\ off} = \frac{1}{2\pi (R_1 \| R_2) C}$$

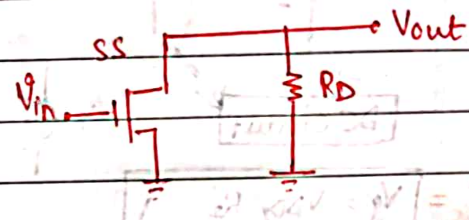


$$H(s) = \frac{s/p}{1 + s/p}$$

⇒



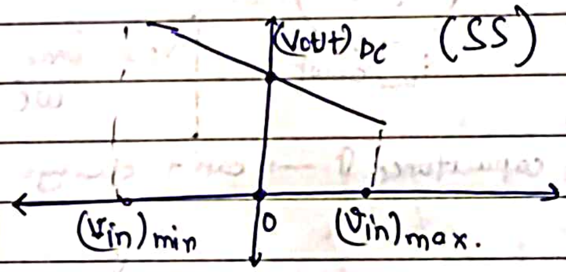
SS model



$R_1 // R_2$ is removed as it is simply a resistance ∥ to the voltage source

$$\boxed{\frac{1}{2\pi (R_1 \| R_2) C} \ll f_{min}}$$

capacitor will be shorted

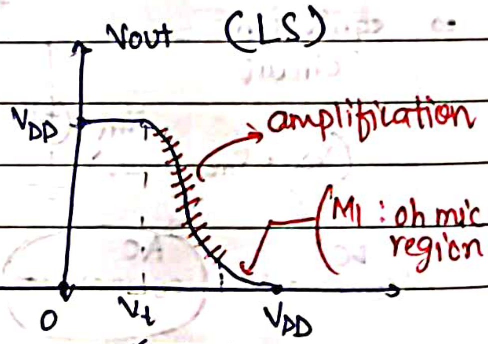


$$v_{out} = -g_m (R \| r_o) v_{in}$$

$$\text{slope} = \frac{v_{out}}{v_{in}} = \boxed{-g_m (R \| r_o)}$$

⇓

low frequency transfer function



Note :- The relⁿ b/w parameters are

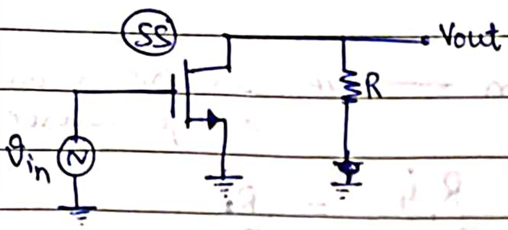
$$I_{DS} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) \left[(V_{gst})^2\right] \left[1 + \lambda (V_{DS} - V_{DSI})\right]$$ corresponds to active region

For active region ONLY, $V_{DS_1} = V_{GST}$

$$g_m = \left(\frac{\partial I_D}{\partial V_{gs}}\right)_{const.\ V_{DS}} = \boxed{\frac{2 I_{DQ}}{V_{GST,Q}}}$$ *

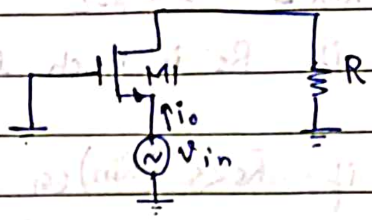
$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{const.\ V_{GS}} \Rightarrow r_o = \frac{1}{\lambda I_D}, \quad I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) \left[V_{GST,Q}^2\right]$$

CONFIGURATIONS

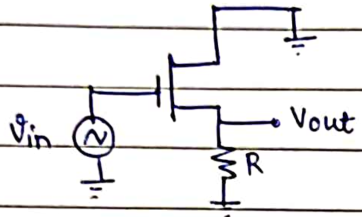


CS Amplifier

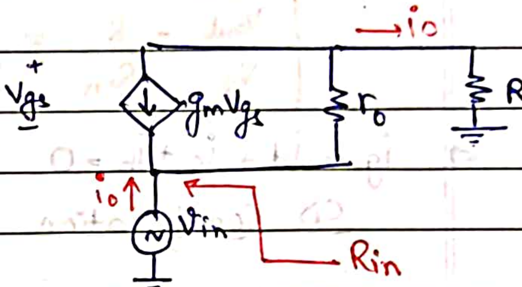
$R_{in} \to \infty$



CG Amplifier



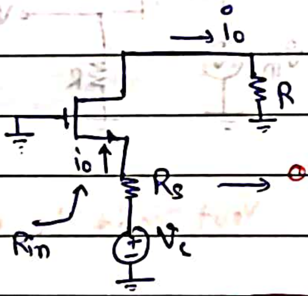
CD config.



CG MODE is NOT good as a voltage amplifier.

attenuates voltage at input itself

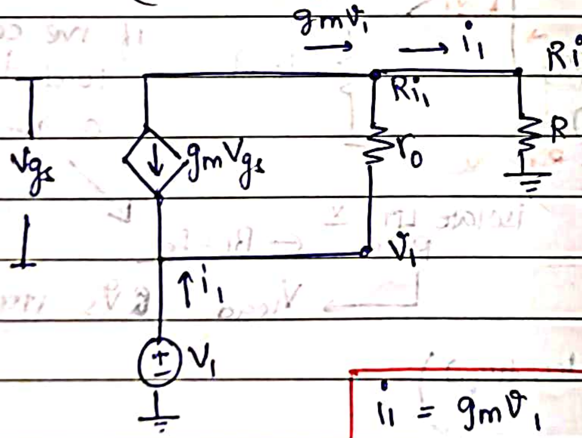
voltage at the input drops, not V_s anymore ← r_o, R_s : resistive division of voltage ←



→ output resistance of V_c

$$V_s = \left(\frac{R_{in}}{R_{in}+R_s}\right) v_s$$

$$\boxed{V_s = R_{in} i_1}$$



$$R_{in} = \frac{V_1}{i_1}$$

$$v_{gs} = -V_1$$

$$g_m V_{gs} = -g_m v_1$$

$$\boxed{i_1 = g_m v_1 + \frac{v_1 - Ri_1}{r_o}}$$

$$\left(1 + \frac{R}{r_o}\right) i_1 = \left(g_m + \underbrace{\frac{1}{r_o}}_{g_o}\right) v_1 \qquad g_m \gg \frac{1}{r_o}$$

$$1/R_{in} = \left(\frac{v_1}{i_1}\right)^{-1} = \frac{g_m + \frac{1}{r_o}}{1 + R/r_o} \qquad 1/R_{in} = \frac{g_m + 1/r_o}{1 + R/r_o} = \boxed{\frac{g_m}{1 + R/r_o}}$$

Eg.- $g_m = 0.4\ mA/V$ $R = 10\ K\Omega$ $r_o = 200\ K\Omega$ $R/r_o \to 0$ $1/R_{in} = g_m$ (CG) $\Rightarrow R_{in} = \frac{1}{g_m}$ $= 2.5 K\Omega$

$R_{in} \simeq 2.5\,k\Omega$

if R_s is much less that R_{in} ⟶ we can use it as a voltage source.

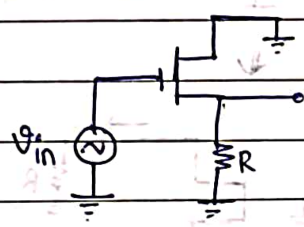
if $R_s \ll (R_{in})_{CG} \Rightarrow \frac{V_{out}}{V_s} = \frac{R \cdot i_1}{R_{in} \cdot i_1} = \frac{R}{R_{in}}$

as $R_{in} \simeq \frac{1}{g_m}$

$$\boxed{\frac{V_{out}}{V_s} = \frac{R}{R_{in}} = g_m R}$$

⇒ $i_g + i_d + i_c + i_b = 0$ (always)

CD Configuration



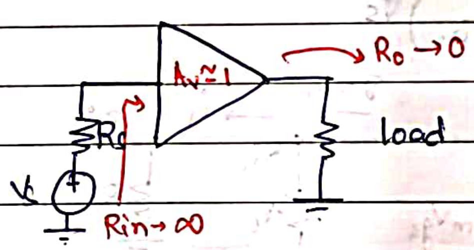
$V_{out} = (v_{in} - v_{gs})$

Source follower

v_{in} and v_{gs} have the same sign ⇒ $v_{in} - v_{gs} < v_{in}$

Vout can't be more than Vin ⇒ can't be used as a voltage amplifier.

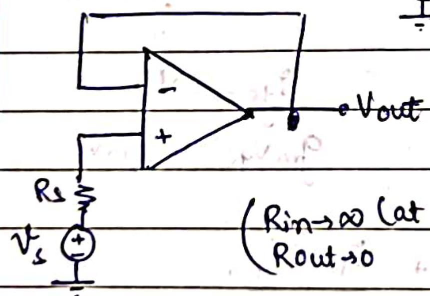
Buffer



if we connect R_s to load directly, there is a resistive division

isolate LHS & RHS ← Buffer

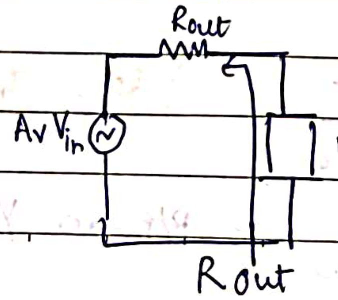
└→ $V_{load} = v_s$ itself



($R_{in} \to \infty$ (at low freq.)
$R_{out} \to 0$)

$V_{out} = V_s$ (buffer)

(CD Amplifier): $V_{in} > 0 \Rightarrow V_{gs} > 0$ and $V_{in} < 0 \Rightarrow V_{gs} < 0$



(MOSFET is symmetric about D and S)

$\Uparrow$

input resistance of CG $\Longleftrightarrow$ output resistance of CD SAME.

$(R_{out})_{CD} = \frac{1}{g_m}$ we want $R_{out} \to 0$ as we want it to be a source follower.

so, ($g_m \Rightarrow$ as high as possible)