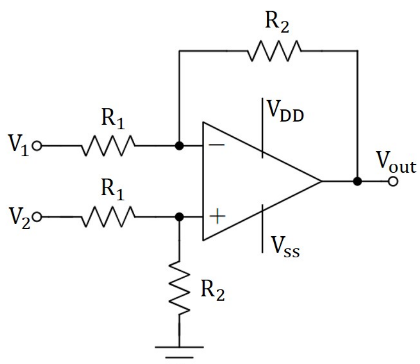
EE204 - Analog Circuits
Electrical Engineering Department
IIT-Bombay
Autumn 2023

Quiz 1

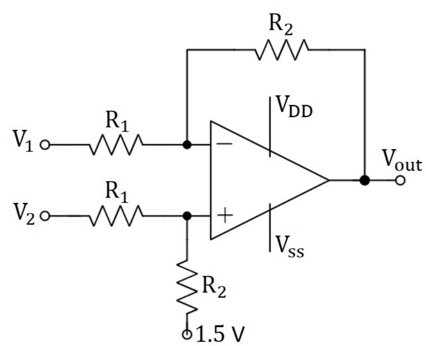
Total Marks : 10

Date: 2^{th} **September 2023**, **Time: 9.30 am to 10.30 am**.

Q1)



(a) Q1(a) circuit diagram



(b) Q1(b) circuit diagram

In the circuit shown in figure 1(a): $R_1 = 1k\Omega$, $R_2 = 9k\Omega$. **OpAmp is ideal**.

(a) Derive V_{out} as a function of V_1 and V_2 if V_{DD} = -V_{SS} = 2V. [2 marks]

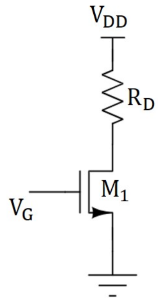
(b) In the circuit diagram shown in figure 1(b), V_{DD} = 3V and V_{SS} = 0V. $V_1 = 1.5 + V_x$, $V_2 = 1.5 + V_y$. Derive an expression for V_{out} as a function of V_x and V_y. [2 marks]

(c) In the question 1(b), if $V_1 = V_2 = 1.5$V and resistors R_1 and R_2 are 5% tolerance resistors, i.e. $R_1 \rightarrow R_1(1 \pm \epsilon)$ and $R_2 \rightarrow R_2(1 \pm \epsilon)$ where $\epsilon = 0.05$, determine the value of V_{out}. [1 mark]

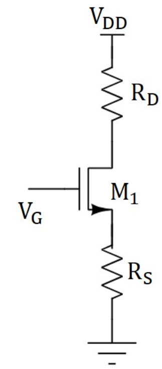
Q2)

(a) In the circuit diagram shown in figure 2(a), R_D = 15kΩ, V_{GST} = 0.3V, I_D = 0.1mA. Find minimum value of V_{DD} for which transistor M_1 will be in saturation (pinch-off) region. [1 mark]

(b) Repeat (a) if resistor as $R_S = 2k\Omega$ is added to the circuit as shown in circuit shown in figure 2(b). (Rest of the values will be same as the corresponding values in (a).) [1 mark]



(a) Q2(a) circuit diagram



(b) Q2(b) circuit diagram

Q3)

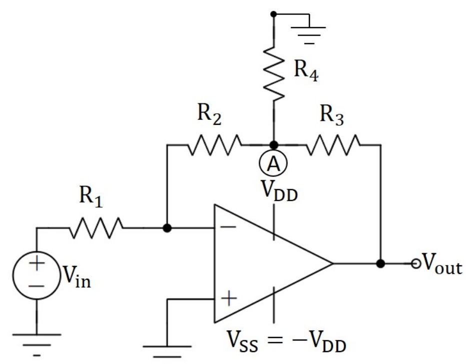


Figure 3: Q3 circuit diagram

In the circuit diagram shown in figure 3, **OpAmp is ideal**.

(a) Use left side of the circuit, i.e. V_{in}, R_1 and R_2 to derive V_A as a function of V_{in}. [1 mark]

(b) Use right side of the circuit, i.e. V_{out}, R_3, R_4 and R_2 to derive V_A as a function of V_{out}. [1 mark]

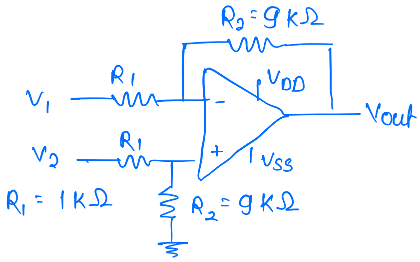
(c) Use (a) and (b) to derive V_{out} as function of V_{in}. [0.5 mark]

(d) In your opinion, what is the feature of the circuit? [0.5 mark]

All the Best!

EE 204 Quiz 1 Solution.

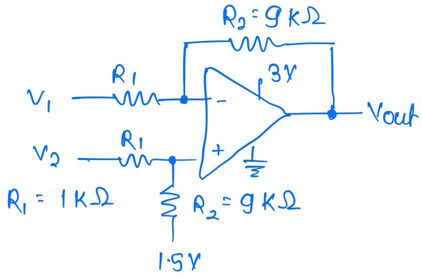
Q1)(a)



$$V_{out} = \left(\frac{R_2}{R_1+R_2}\right)\left(1+\frac{R_2}{R_1}\right)V_2 + \left(\frac{-R_2}{R_1}\right)\cdot V_1 = \frac{R_2}{R_1}(V_2 - V_1)$$ — ⟨1 mark⟩

$V_{out} = 9(V_2 - V_1)$ — ⟨1 mark⟩

(b)



$V_1 = V_x + 1.5$

$V_2 = V_y + 1.5$

$V_{cm} = \frac{V_{DD} - V_{SS}}{2} = \frac{3-0}{2} = 1.5V$ — ⟨0.5 mark⟩

$\therefore V_{out} = V_{cm} + \frac{R_2}{R_1}(V_2 - V_1)$

$= V_{cm} + \frac{R_2}{R_1}(V_y - V_x)$ — ⟨0.5 mark⟩

$V_{out} = 1.5 + 9(V_y - V_x)$ — ⟨1 mark⟩

c) $R_1 \to R_1 \pm 0.05 R_1$ & $R_2 \to R_2 \pm 0.05 R_2$

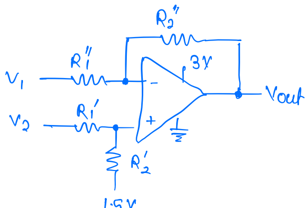
We have

$$V_{out} = \left(\frac{R_2'}{R_1'+R_2'}\right)\left(1+\frac{R_2''}{R_1''}\right)V_2 + \left(\frac{-R_2''}{R_1''}\right)\cdot V_1 + V_{cm}$$

Lets consider worst case mismatch $R_2' = (1+\varepsilon)R_2$, $R_1' = (1-\varepsilon)R_1$, $R_2'' = (1+\varepsilon)R_2$ & $R_1'' = (1-\varepsilon)R_1$

$$V_{out} = \frac{(1+\varepsilon)}{R_1+R_2} \times \frac{(R_1+R_2)}{(1-\varepsilon)} V_2 - \frac{(1+\varepsilon)R_2}{(1-\varepsilon)R_1}\cdot V_1 + V_{cm}$$

$$= \left(\frac{1+\varepsilon}{1-\varepsilon}\right)(V_2 - V_1) + V_{cm}$$



Note*
The consideration of specific worst case is optional, students can directly write that Vout will remain at Vcm irrespective of mismatch

Thus Vout due to mismatch is

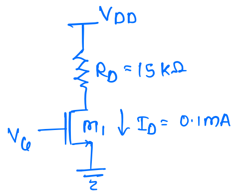
$V_{out} = \left(\frac{1\pm\varepsilon}{1\mp\varepsilon}\right)(V_1 - V_2) + V_{cm}$ — ⟨0.5 mark⟩

We have $V_1 = V_2 = 1.5V$ Hence

No matter how mismatched the resistors are, the output voltage remains the same value of Vcm

$V_{out} = V_{cm} = 1.5V$ — ⟨0.5 mark⟩

Q2) (a)



$V_{GS_T} = 0.3V$

For M_1 to remain in Saturation region

$V_{DS} \geq V_{GS_T}$

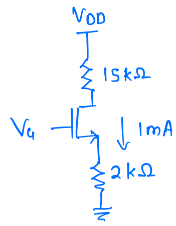
i.e $V_{DD} - I_D \cdot R_D \geq V_{GS_T}$ — <0.5 mark>

$V_{DD} - 0.1mA \times 15k\Omega \geq 0.3V$

$\therefore V_{DD} \geq 1.8V$

$V_{DD_{min}} = 1.8V$ — <0.5 mark>

(b)



$V_{DS} = V_{DD} - I_D \cdot R_D - I_D \cdot R_S$ — <0.5 mark>

For M_1 to remain in Saturation

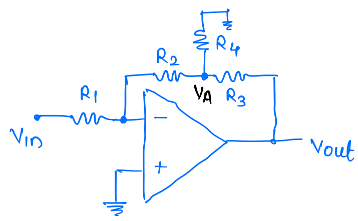
$V_{DS} \geq V_{GS_T}$

$\therefore V_{DD} - 0.1mA \cdot 15k\Omega - 0.1mA \times 2k\Omega \geq 0.3V$

$V_{DD} \geq 2V$

$V_{DD_{min}} = 2V$ — <0.5 mark>

Q3)



(a) $V_A = -\frac{R_2}{R_1} V_{in}$ — <1 mark>

(b) $V_{out} = \left(1 + \frac{R_3}{R_4 \| R_2}\right) V_A$ — <1 mark>

(c) $V_{out} = -\left(\frac{R_2}{R_1}\right)\left(1 + \frac{R_3}{R_4 \| R_2}\right) V_{in}$ — <0.5 mark>

<0.25 mark>

(d) As $R_4 \| R_2 < R_2$, adding R_4 improves the gain of the inverting amplifiet without the need of using wide range of resistanse values. ← <0.25 mark>

Alternate Answer

Adding R_4, amplifies the current flowing into R_3 branch without adding too small or large resistors

<0.25 mark> <0.25 mark>