EE204 : Analog Circuits
Dept of Electrical Engineering
IIT Bombay
Autumn Semester 2023

Assignment 1
Total Marks: 10
Submission Deadline: 11:59 p.m., 19-08-2023
Mode of Submission: Scan your assignment and upload on Moodle as a single pdf file.

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1. For the circuit shown in Figure 1, use $A_v = 10^4$ for the OpAmp. Choose $10k\Omega < R1 < 20k\Omega$, and $1k\Omega < R2 < 5k\Omega$, such that the feedback factor $\beta = 0.1$.
   (a) Calculate the $Gain = \frac{V_{out}}{V_{in}}$. [1 Mark]
   (b) Calculate V_{out} for $V_{in} = 0.15$V. [1 Mark]
   (c) Calculate the voltage at negative terminal of OpAmp for $V_{in} = 0.15$V. [1 Mark]

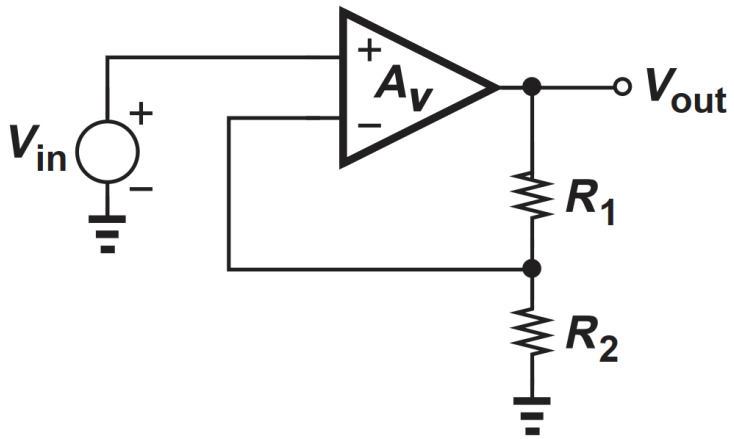

Figure 1: Circuit for Q1

2. For the circuit in Figure 2, use $W/L = 3\mu m/1\mu m$ for transistor M1. For M1 fabricated in 180nm CMOS technology, use $V_t = 0.4$V, and $\mu C_{ox} = 260\mu A/V^2$. Voltage limits for V_{GS} and V_{DS} are the following: $0 < V_{GS} < 1.8V$ and $0 < V_{DS} < 1.8V$.

(a) Specify the range of V_{GS} and V_{DS} such that,

(i) transistor M1 is in OFF region [0.5 Marks]

(ii) transistor M1 is in Ohmic region [0.5 Marks]

(iii) transistor M1 is in Saturation region [0.5 Marks]

(b) Choose two values for V_{GS} and V_{DS} in Ohmic and Saturation regions of operation, calculate I_D and fill in the Table 1. [4 Marks]

Table 1

	Set1 V_{GS}=...		**Set2** V_{GS}=...	
	V_{DS}	I_D	V_{DS}	I_D
Ohmic Region				
Saturation Region				

(d) Sketch the plot of I_D vs. V_{DS} for all sets of V_{GS}. Mark the points calculated in Table 1 on the plot. [1.5 Marks]

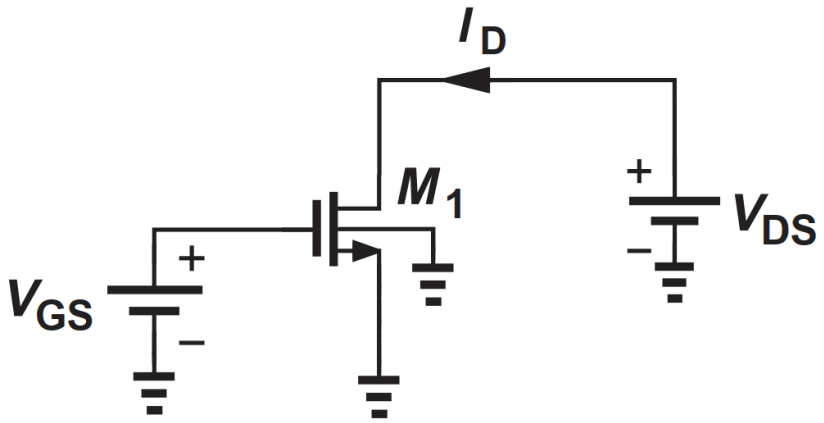

Figure 2: Circuit for Q2