EE230: Analog Circuits Lab
Lab - 4

Nimay Shah, 22B1232

January 31, 2024

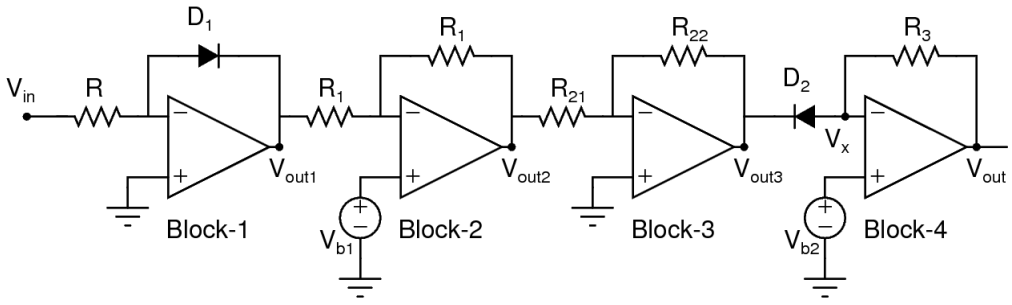
1 Square-Root Amplifier

1.1 Aim of the experiment

The aim of this experiment is to design a square-root amplifier, by employing a logarithm and an anti-logarithm amplifier, and using a pn junction diode. We simulate the designed circuit on LTspice and record our observations.

1.2 Design

The block diagram of the Square-Root Amplifier is shown here:

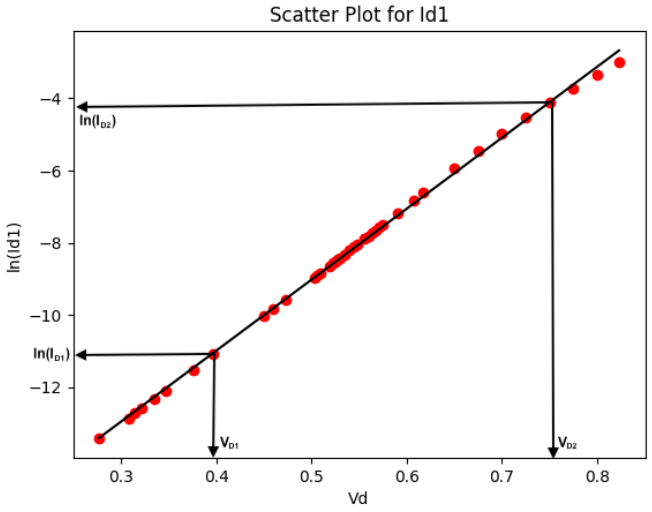


Block-1 represents a Logarithm Amplifier
Block-2 is used to remove the offset from the output of Block-1
Block-3 is employed to scale the output appropriately to $\frac{1}{2}$
Block-4 is an Anti-Log Amplifier
TL084 is used as the OpAmp for the design

Given to us are the diode characteristics (V_D, I_D) for two diodes D1 and D2.

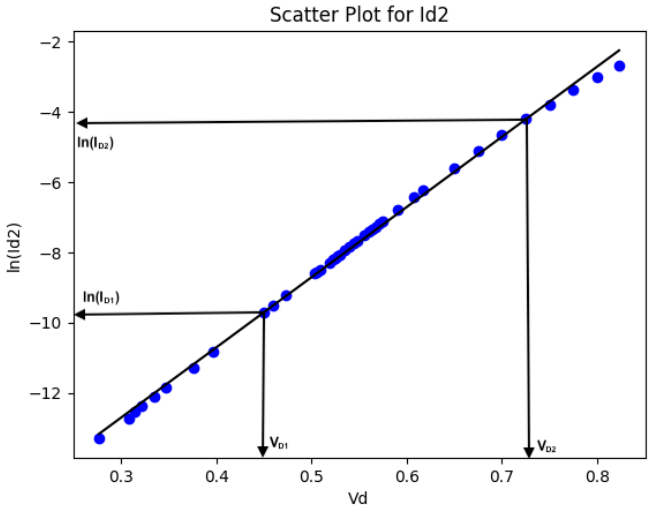
The plots of $ln(I_D)$ v/s V_D along with the best fit line is drawn:

Figure 1: for Diode-1



$$slope = 19.6544 \tag{1}$$
$$intercept = -18.8507 \tag{2}$$

Figure 2: for Diode-2



$$slope = 19.9637 \tag{3}$$
$$intercept = -18.6934 \tag{4}$$

We know, for a pn junction diode, we can write:

$$I_D = I_S.e^{V_D/nV_T}$$

or

$$ln(I_D) = \frac{V_D}{nV_T} + ln(I_S)$$

Thus, for the above graphs

$$slope = \frac{1}{nV_T} \tag{5}$$

$$intercept = ln(I_S) \tag{6}$$

Given, the value of V_T at 27°C or 300 K, can be taken as 0.026 V.
Thus, using (1), (2), (3), (4), (5) and (6), we can calculate

for Diode-1	for Diode-2
$I_{S1} = 6.505$ nA	$I_{S2} = 7.613$ nA
$n_1 = 1.9569$	$n_2 = 1.9266$

now, Diode-1 is in linear region for

$$ln(I_D) = -9.70463669 \text{ to } -4.2131281$$
$$\text{or, } I_D = 0.000061A \text{ to } 0.01479A$$

similarly, Diode-2 is in linear region for

$$ln(I_D) = -11.07467053 \text{ to } -4.11475137$$
$$\text{or, } I_D = 0.0000155A \text{ to } 0.01633A$$

I chose Diode-1 as D1 in Block-1, and Diode-2 as D2 in Block-4.

Now, designing the Square-Root Amplifier
Assuming a maximum input voltage of $V = 15V$ to the amplifier,
we have $I_{D1min} = 0.000061A$, we have $R_{max} = \frac{15}{0.000061} = 2.45$ MΩ
we have $I_{D1max} = 0.01479A$, we have $R_{min} = \frac{15}{0.01479} = 1$ kΩ

Thus, we can take any value of R between these two values.
We take, $R = 10$ kΩ in Block-1.

Now,

$$V_{out1} = n_1 V_T ln(V_{in}) + n_1 V_T ln(I_S R)$$

or,

$$V_{out1} = 0.0509 ln(V_{in}) - 0.4905$$

Thus, we now need to set

$$V_{b2} = \frac{-0.4905}{2} = -0.24525V$$

in Block-2, to nullify the offset from Block-1.
However, I set $V_{b2} = -0.2440V$ on LTspice, fine tuning to remove the offset.

We could choose any value of R_1 in Block-2. Thus, I chose $R_1 = 5$ kΩ.

Voltage across the resistor R_3 will give us the Square-Root of V_{in}. We have,

$$V_{R3} = R_3 I_{S2} e^{\frac{V_{b2}}{n_2 V_T}} V_{in}^{\frac{n_1}{n_2}\beta}$$

here, $\beta = \frac{R_{22}}{R_{21}}$

For $V_{in} = 1V$, we must have $V_{R3} = 1V$.
Also, the diode D_2 must remain in the linear region of operation.
Thus, I chose to set $V_{b2} = 0.5V$.
So, for $V_{in} = 1V$, we have

$$1 = R_3 \times 7.6 \times 10^{-9} \times e^{\frac{0.5}{1.9266 \times 0.026}}$$

Thus, we have $R_3 = 6073.5\ \Omega$

For $V_{in} = 9V$, we must have $V_{R3} = 3V$.
This helps us calculate the gain in Block-3.
We must have

$$\frac{n_1}{n_2}\beta = \frac{1}{2}$$

or,

$$\beta = \frac{n_2}{2n_1} = \frac{1.9266}{2 \times 1.9569} = 0.4922$$

Thus,

$$\frac{R_{22}}{R_{21}} = 0.4922$$

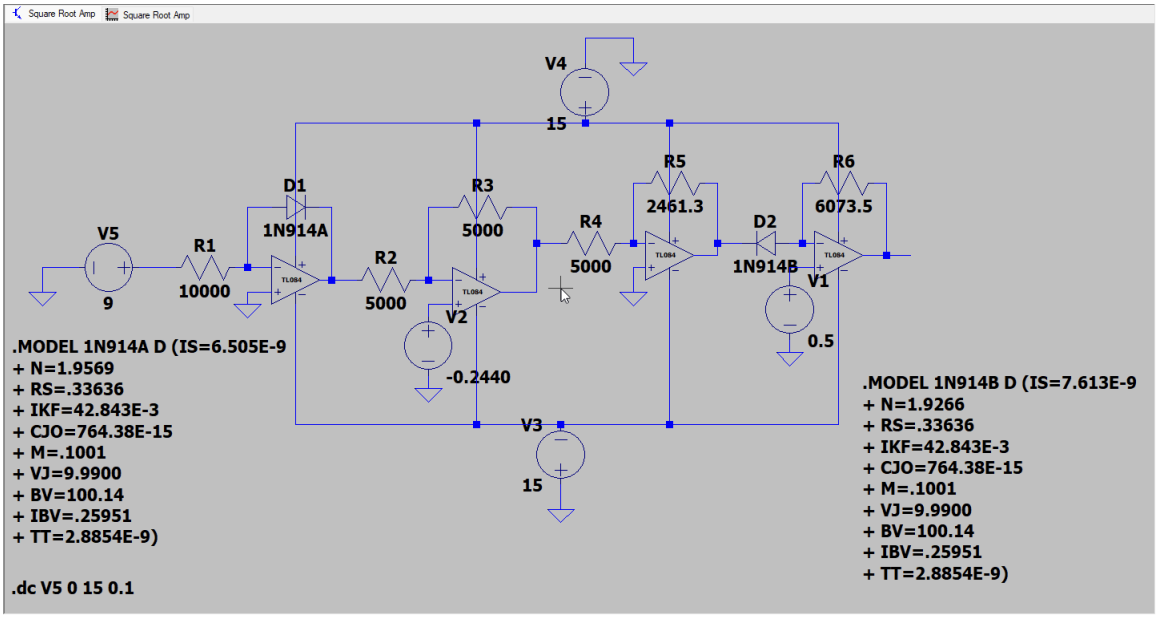
say, $R_{21} = 5k\Omega \implies \mathrm{R}_{22} = 2.4613k\Omega$

Thus, the design of the Square-Root Amplifier is now complete.

1.3 Simulation results

1.3.1 Circuit Schematics

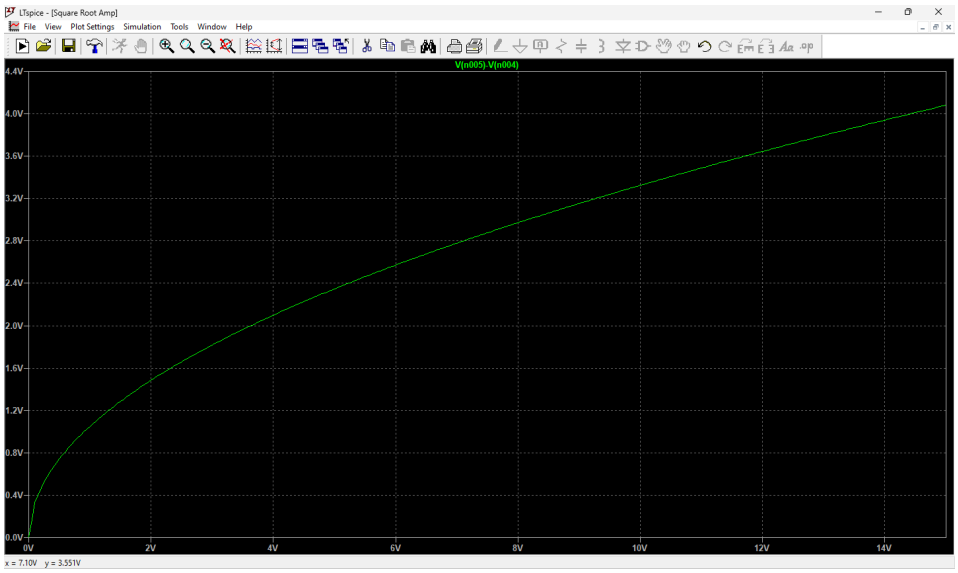
The circuit schematics drawn on LTspice is shown below.



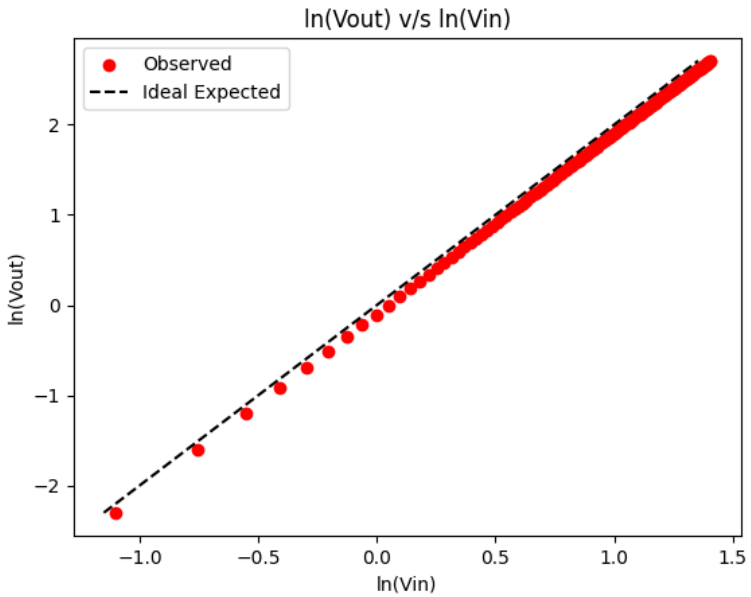
TL084 OpAmp has been used in the simulation
IN914 diodes with the calculated I_S and n have been used
a DC Sweep from 0 to $15V$, with $0.1V$ step size was applied

1.3.2 Simulation results

The below simulation plot shows the graph between V_{R3} and V_{in}.



The expected and the observed graph between $ln(V_{out})$ and $ln(V_{in})$ is also shown below:



1.4 Conclusion and Inference

Thus, we successfully designed and simulated a Square-Root Amplifier.
As can be inferred from the plot above, the observed graph
$ln(V_{out})$ v/s $ln(V_{in})$ is reasonably close to the ideal expected graph; thus verifying the correctness of our design.

1.5 Experiment completion status

All parts of this experiment were successfully designed and simulated in the lab.