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TEAM DETAILS

TEAM - I

DIGITAL SYSTEMS (EE224)
course Project

Members :-

NAME

ROLL NO.

NIMAY UPEN SHAH

22B1232

MANAV AGRAWAL

22B1253

HARSHIL SINGLA

22B1260

ANAY ARORA

22B3939

WORK DISTRIBUTION

DATE: / /

Nimay :- Design of the final circuit

Harehil :- Codes for reg-file, CPU, Memory, ALU

Manav :- codes for concatenators, sign-extenders, data-path (incl. control signals), ALU functions

Anay :- Codes for FSM, small parts eg. MUX

FSM design & logic :- Manav & Anay

Datapath & other codes :- Nimay, Harehil, Manav

ALU code & ideation :- Harehil

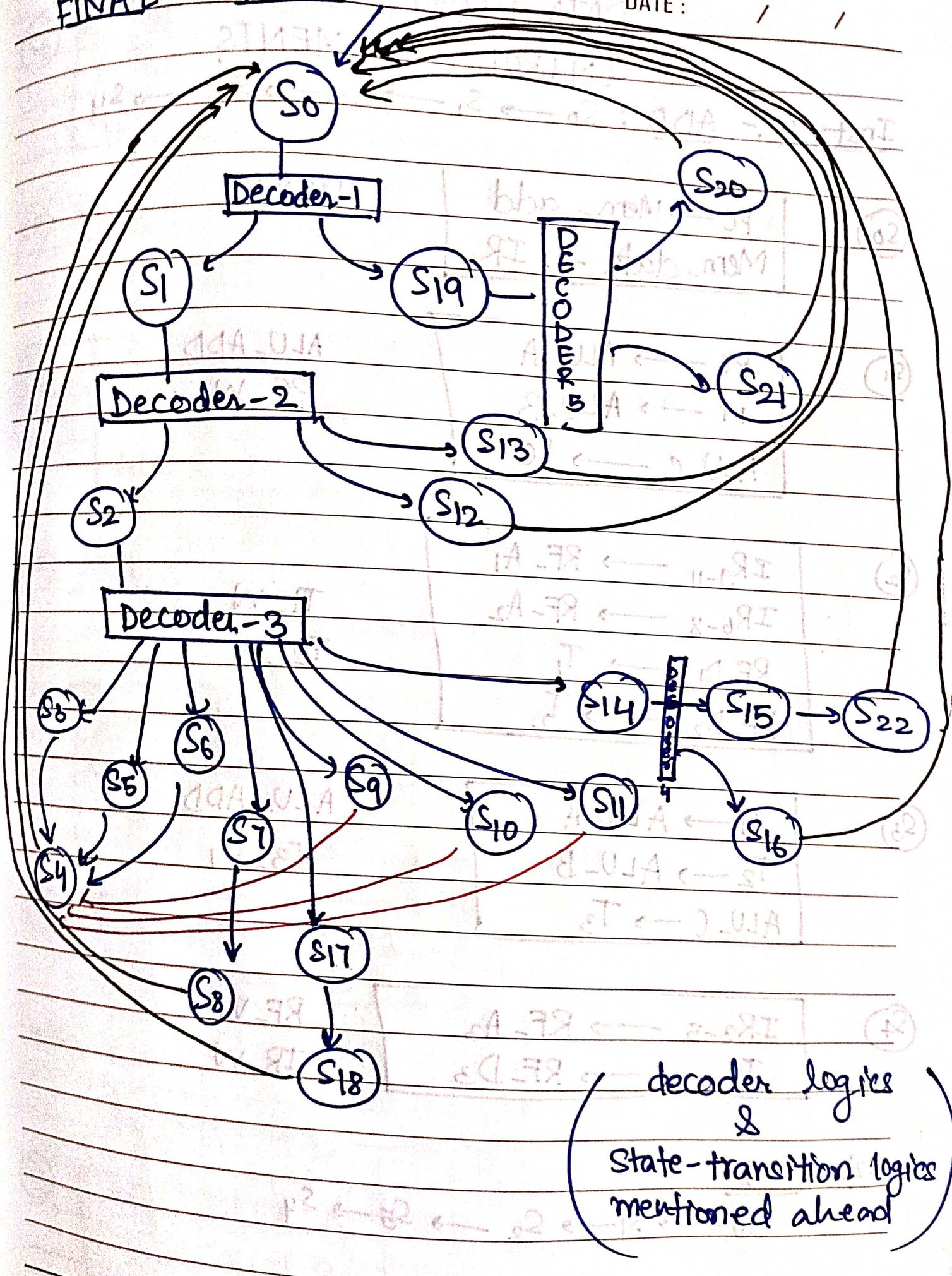
Circuit Verification :- Nimay & Harehil

Final Testing & Verification :- All 4 together



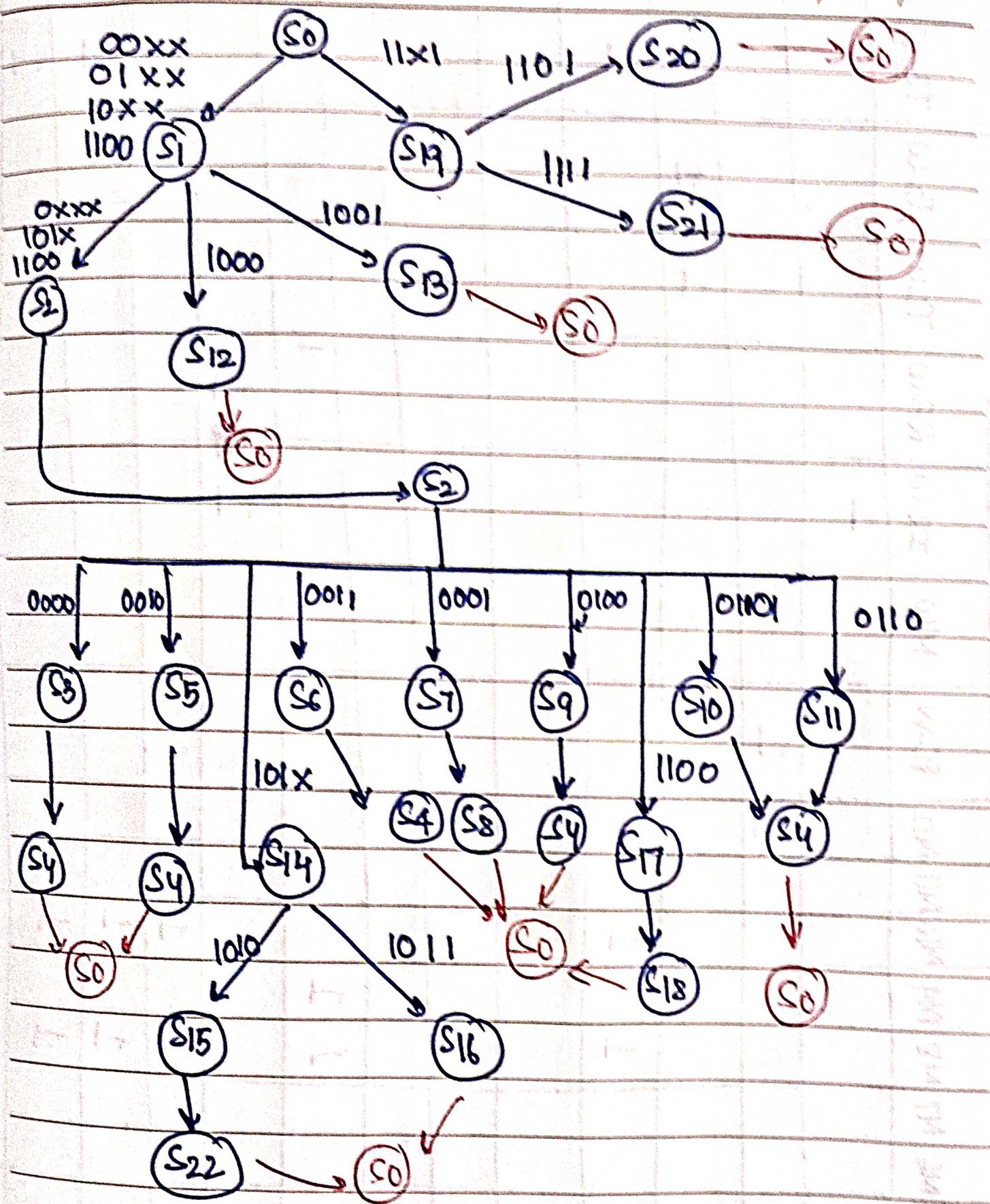
FINAL - FSM

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STATE-TRANSITIONS (FSM cont.)

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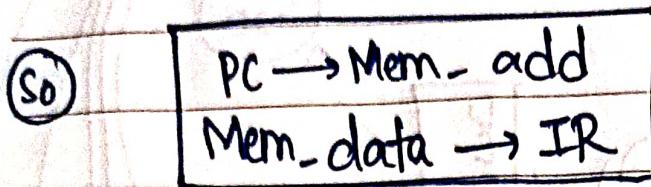
DATA-FLOW

DATE: 1/1/2011

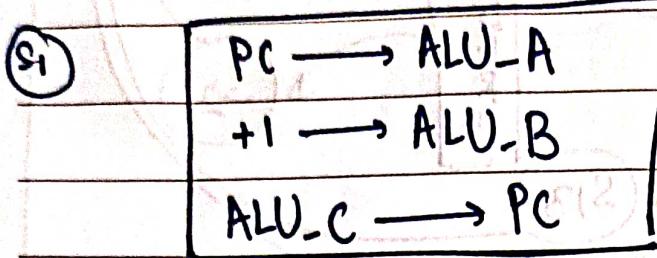
CONTROL STATEMENTS

Inst₁ :- ADD : S₀ → S₁ → S₂ → S₃ → S₄

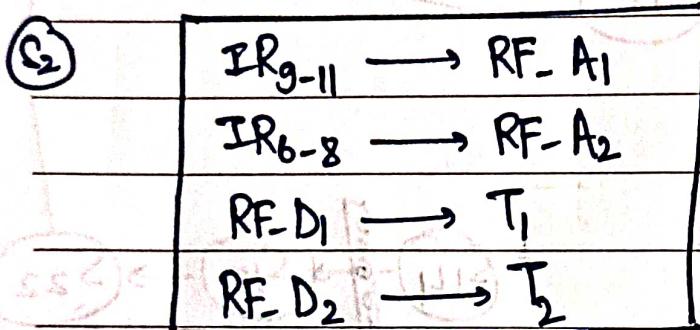
01



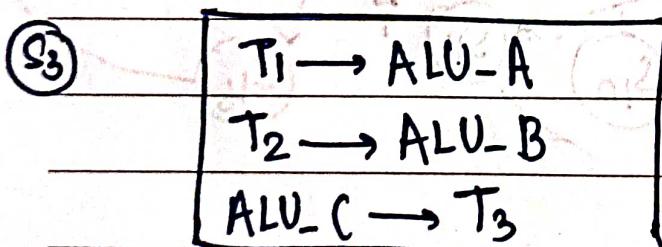
IR-W



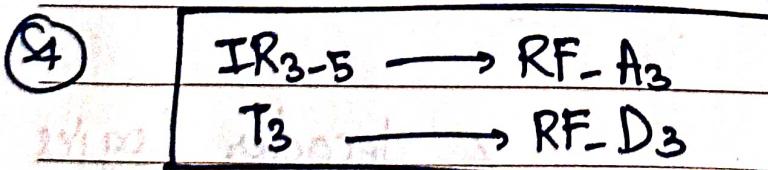
ALU-ADD
PC-W



T₁-W
T₂-W



ALU-ADD
T₃-W



RF-W
IR-W

I₂) SUB

S₀ → S₁ → S₂ → S₅ → S₄

>>

(S5)

 $T_1 \rightarrow ALU-A$ $T_2 \rightarrow ALU-B$ $ALU-C \rightarrow T_3$

ALU-SUB

T3-W

I3> MUL $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$

(S6)

 $T_1 \rightarrow ALU-A$ $T_2 \rightarrow ALU-B$ $ALU-C \rightarrow T_3$

ALU-MUL

T3-W

I4> ADI $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4 \rightarrow S_5$

(S7)

 $T_1 \rightarrow ALU-A$ $IR_{0-5} \rightarrow SE_{6-16} \rightarrow ALU-B$ $ALU-C \rightarrow T_3$

ALU-ADD

T3-W

(S8)

 $IR_{6-8} \rightarrow RF-A_3$ $T_3 \rightarrow RF-D_3$

RF-W

IR-W

I5> AND $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$

(S9)

 $T_1 \rightarrow ALU-A$ $T_2 \rightarrow ALU-B$ $ALU-C \rightarrow T_3$

ALU-AND

T3-W

I6 > ORA

$$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{10} \rightarrow S_4$$

(S₁₀)

$T_1 \rightarrow \text{ALU-A}$
$T_2 \rightarrow \text{ALU-B}$
$\text{ALU-C} \rightarrow T_3$

ALU-OR
T_3-W

I7 > IMP

$$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{11} \rightarrow S_4$$

(S₁₁)

$T_1 \rightarrow \text{ALU-A}$
$T_2 \rightarrow \text{ALU-B}$
$\text{ALU-C} \rightarrow T_3$

ALU-IMP
T_3-W

I8 > LHI

$$S_0 \rightarrow S_1 \rightarrow S_{12}$$

(S₁₂)

$\text{IR}_{0-7} \rightarrow \text{CONCAT-I} \rightarrow \text{RF-D}_3$
$\text{IR}_{9-11} \rightarrow \text{RF-A}_3$

RF-W
IR-W

I9 > LLI

$$S_0 \rightarrow S_1 \rightarrow S_{13}$$

(S₁₃)

$\text{IR}_{0-7} \rightarrow \text{CONCAT-II} \rightarrow \text{RF-D}_3$
$\text{IR}_{9-11} \rightarrow \text{RF-A}_3$

RF-W
IR-W

I10) LW

$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{14} \rightarrow S_{15} \rightarrow S_{22}$

(1=5) 31

(42)

(S14) $T_2 \rightarrow \text{ALU-A}$ $\text{IR}_{0-5} \rightarrow \text{SE}_{6-16} \rightarrow \text{ALU-B}$ $\text{ALU-C} \rightarrow T_3$

39 ← 12-1A

ALU-ADD

T3-W

(S15) $T_3 \rightarrow \text{Mem-Add}$ $\text{Mem Data} \rightarrow T_3$

(MR) T3-W

AT (41)

02 ← PR ← 02

(S22) $T_3 \rightarrow \text{RF-D}_3$ $\text{IR}_{9-11} \rightarrow \text{RF-A}_3$

RF-W

(PR)

EA IR-W

III) SW

$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{14} \rightarrow S_{16}$

ALU-A ← 39

(42)

(S15) $T_3 \rightarrow \text{Mem-Add}$ $T_1 \rightarrow \text{Mem-Data}$

MW

IR-W

I12) BEQ

$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{17} \rightarrow S_{18}$

W-RZ

39 ← C-Z

(42)

(S17) $T_1 \rightarrow \text{ALU-A}$ $T_2 \rightarrow \text{ALU-B}$ $\text{ALU-C} \rightarrow T_3$ $\text{ALU-Z} \rightarrow Z$

ALU-SUB

T3-W

>>

(S₁₈)

PC → ALU-A

IR₀₋₅ → SE_{g-16} → ALU-B

if (Z=1)

ALU-C → PC

else

PC → PC

ALU-ADD

PC-W

IR-W

I13>

JALS₀ → S₁₉ → S₂₀(S₁₉)PC → RF-D₃

RF-W

IR₉₋₁₁ → RF-A₃(S₂₀)

PC → ALU-A

ALU-ADD

IR₀₋₈ → SE_{g-16} → ALU-B

PC-W

ALU-C → PC

IR-W

I14>

JLRS₀ → S₁₉ → S₂₁(S₂₁)IR₆₋₈ → RF-A₂

PC-W

RF-D₂ → PC

IR-W

CONTROL SIGNALS FOR ALL STATES

	M1	M2	M3	M4	M5	M6	N7	M8	M9	M10	M11	M12	PC-W	MW	IR-W	RF-W	T1-W	T2-W	T3-W
S0															1				
S1														1	1				
S2																1	1		
S3																		1	
S4																			
S5																			
S6																			
S7																		1	
S8	1														1	1	1		
S9																		1	
S10																		1	
S11																		1	

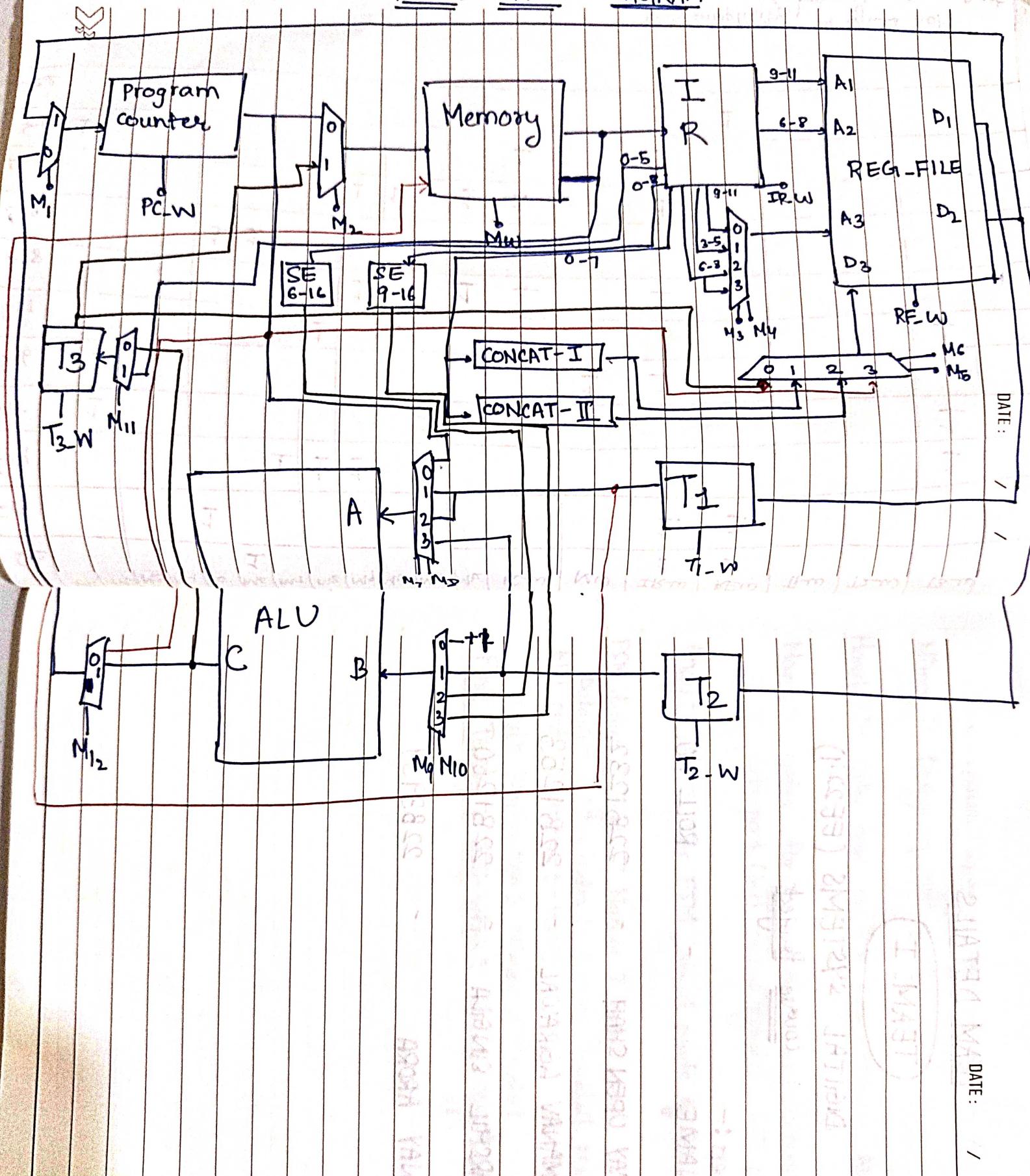
	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	PC-W	MW	IR-W	RF-W	T1-W	T2-W	T3-W
S12		M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	PC-W	MW	IR-W	RF-W	T1-W	T2-W	T3-W
S13															1	1			
S14																		1	
S15	1														1	1			
S16	1																		1
S17																			
S18																			
S19																			
S20																			
S21	1														1	1			
S22																			

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for simplicity, all signals not mentioned are Don't care.

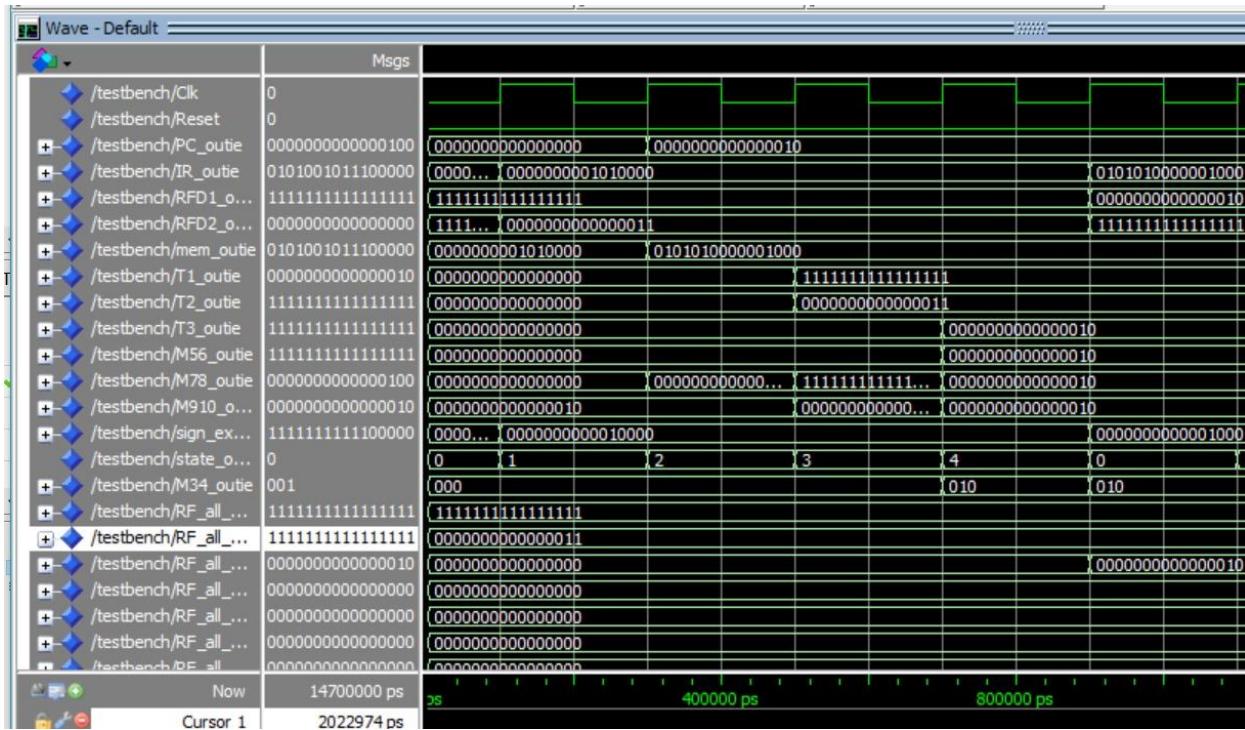
(they are 0 in our code.)

FINAL CIRCUIT DIAGRAM

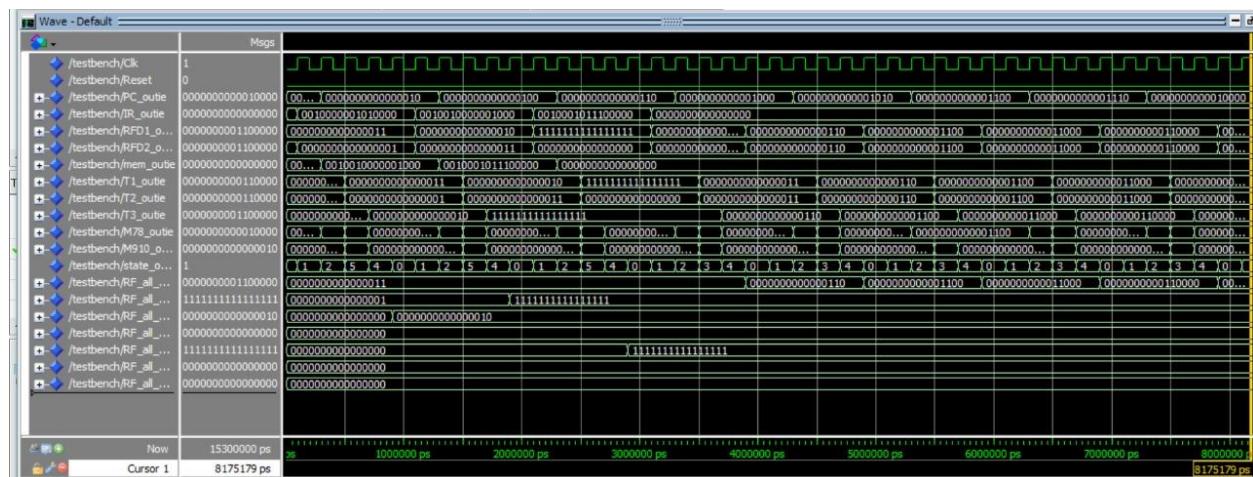


SCREENSHOTS OF WORKING SIMULATIONS

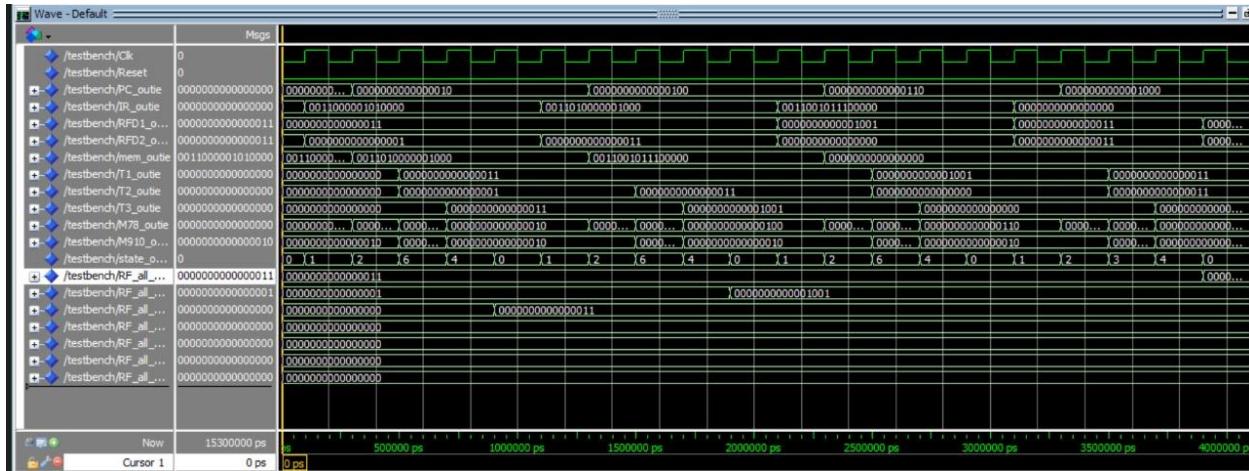
1. ADD



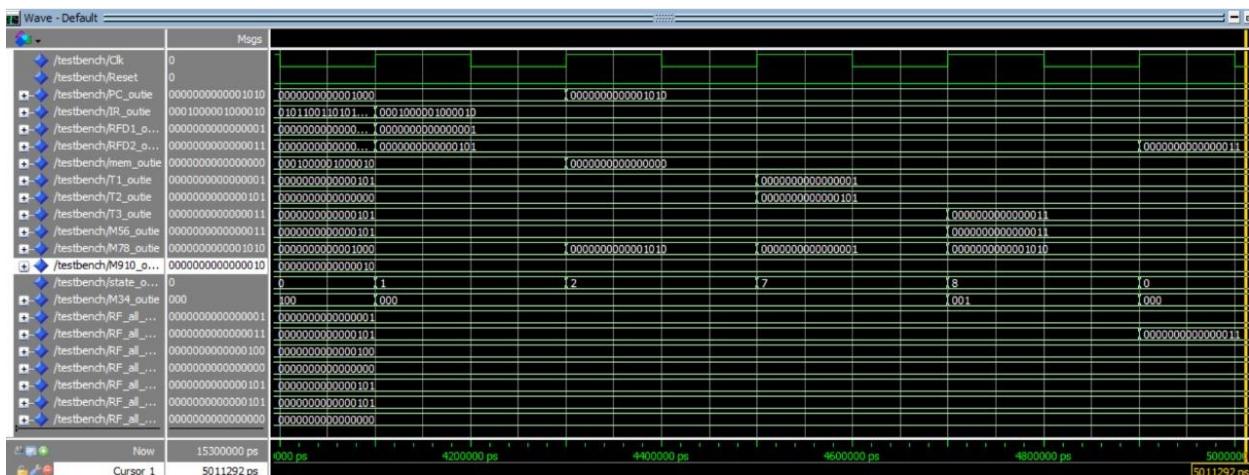
2. SUB



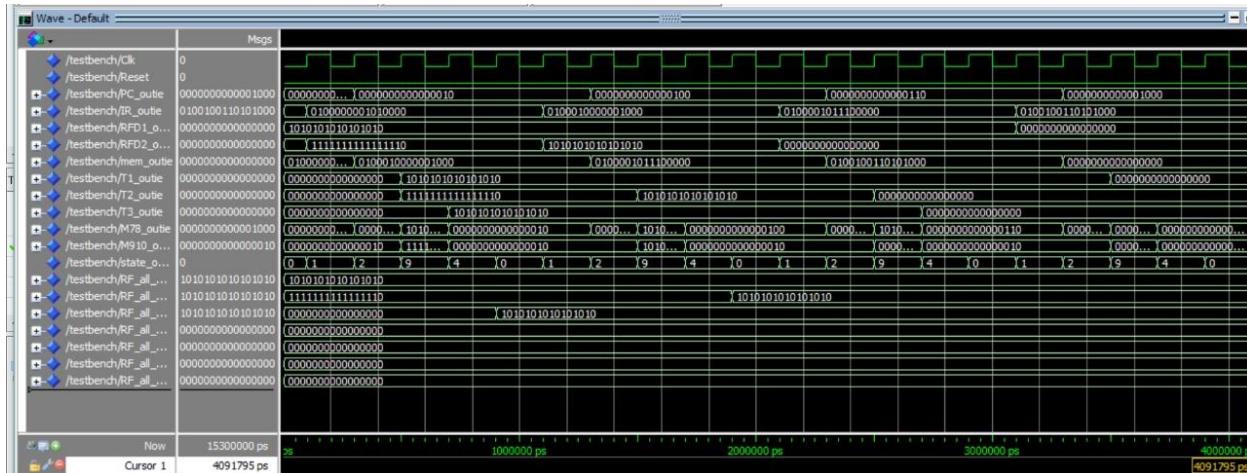
3. MUL



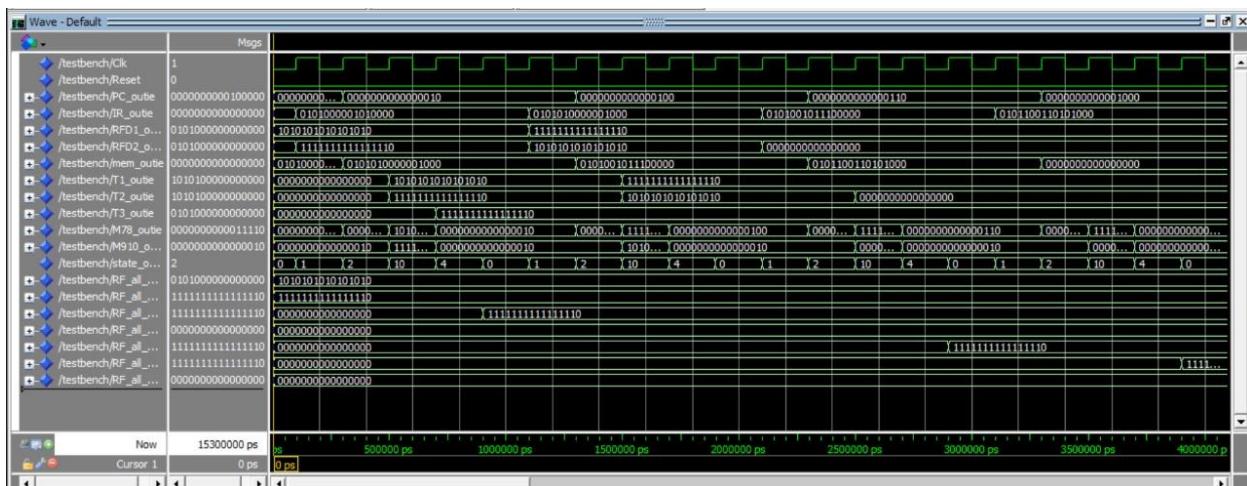
4. ADI



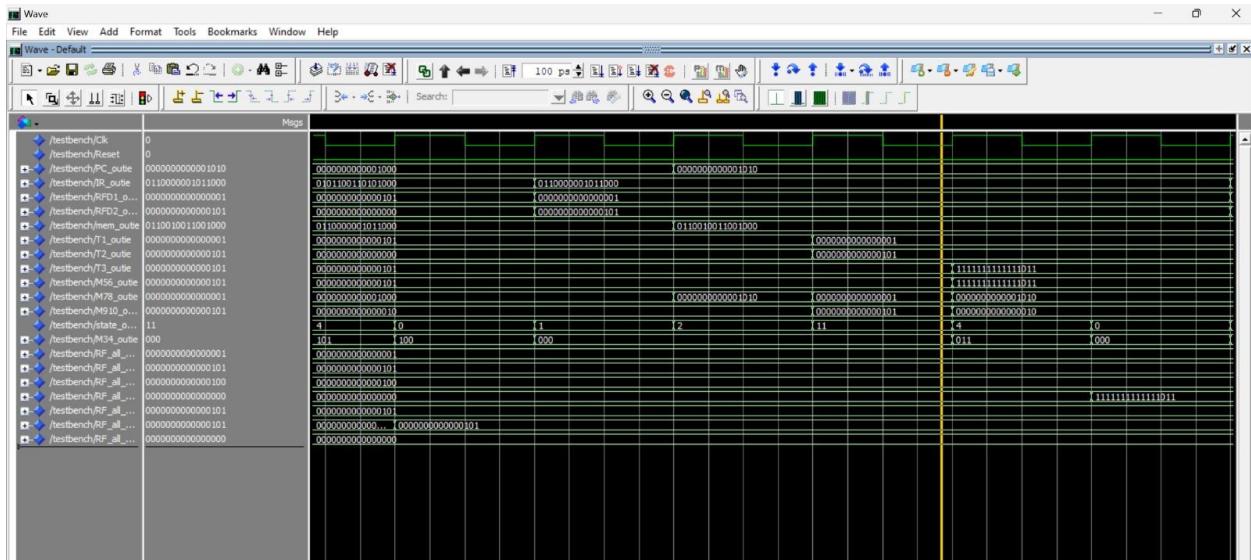
5. AND



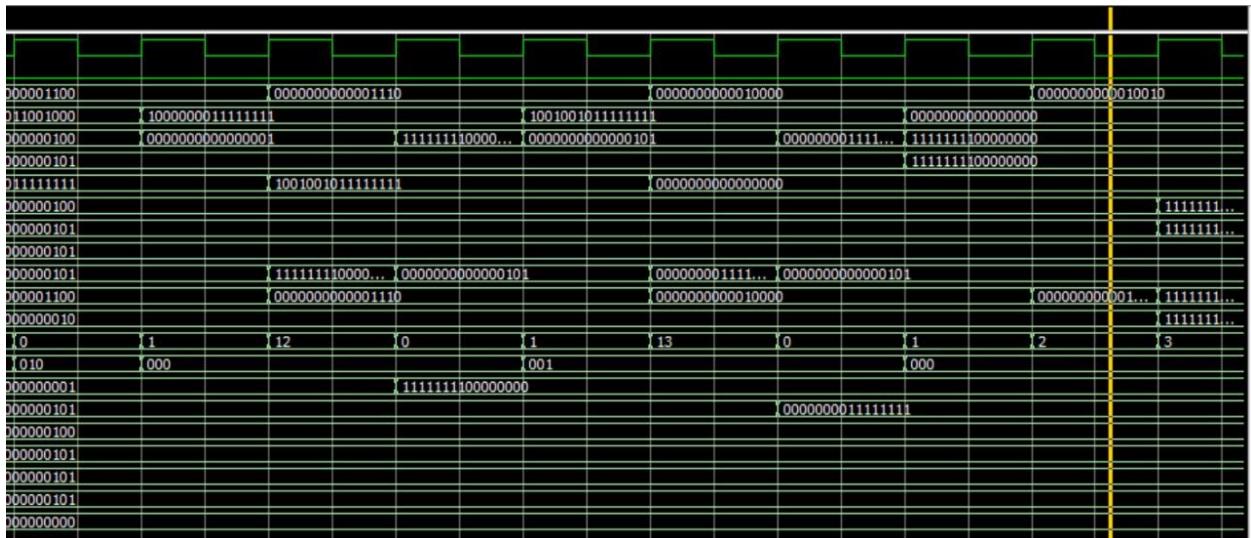
6. OR



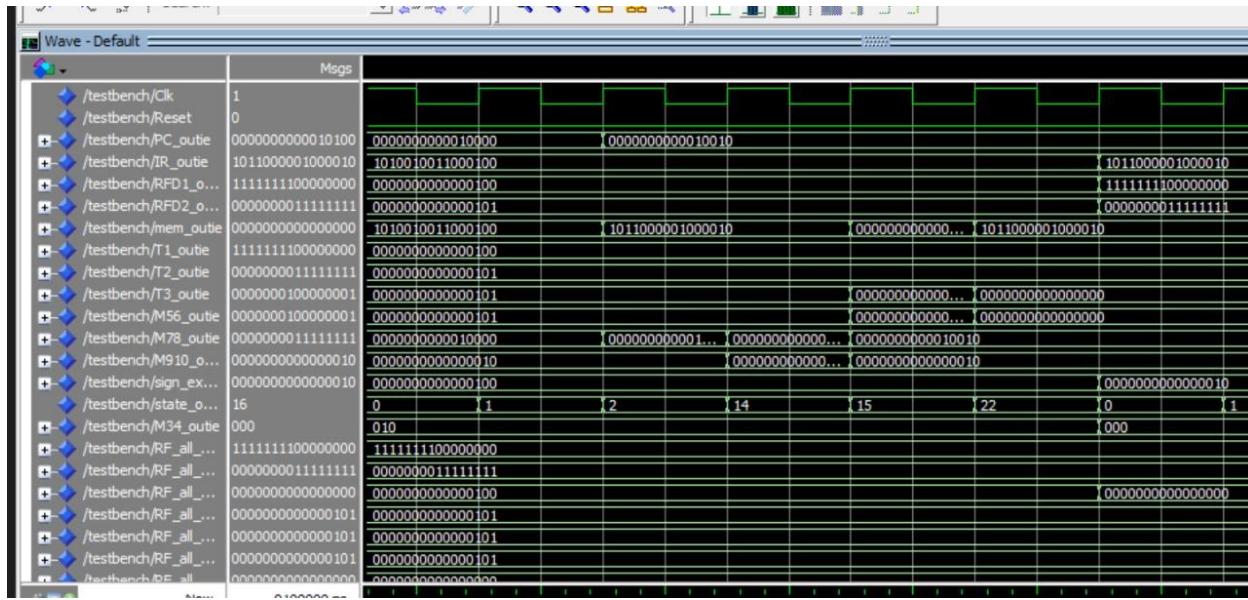
7. IMP



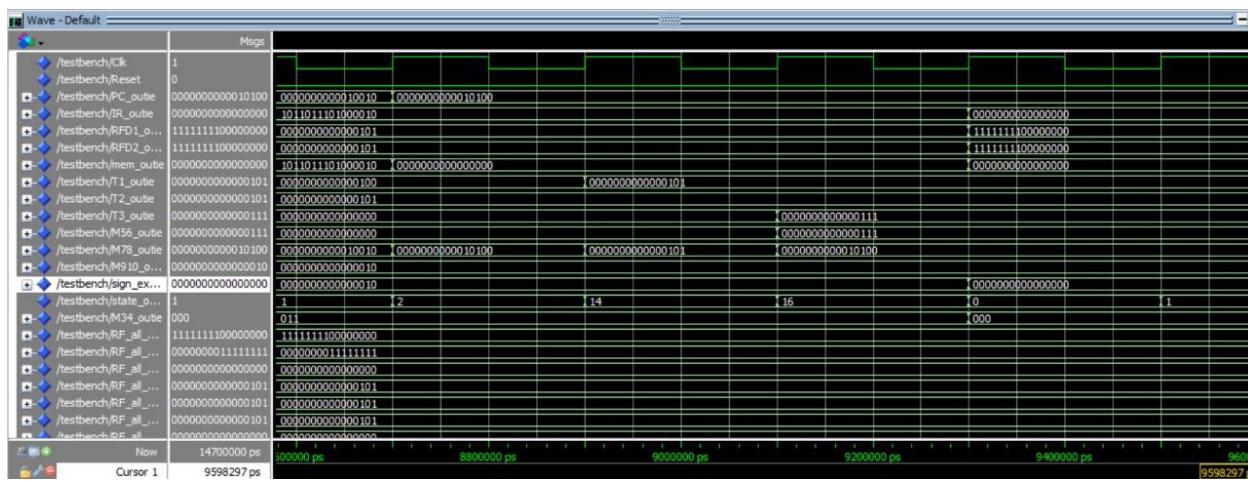
8. LHI and 9. LLI



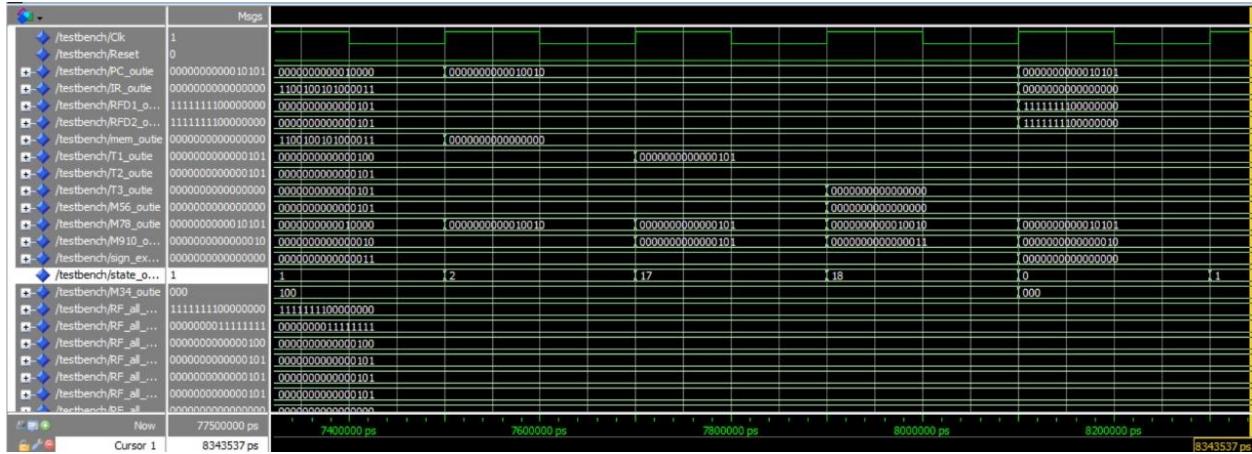
10. LW



11. SW



12. BEQ



13. JAL and 14. JLR

