

TEAM DETAILS

DATE:

TEAM - I

EE-309

DIGITAL SYSTEMS (EE224)
course Project - FPGA

Members :-

NAME

ROLL NO.

NIMAY OPEN SHAH - 22B1232

MANAV AGRAWAL - 22B1253

HARSHIL SINGLA - 22B1260

ANAY ARORA - 22B3939



	2	3	4	5	W	T	M
AVU					00-000		
					000000		

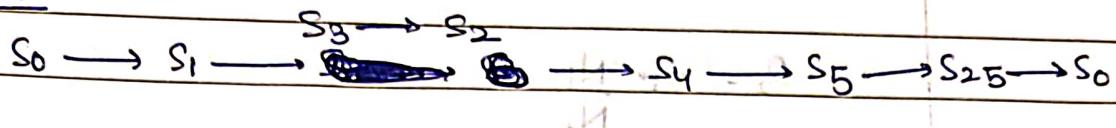
M	T	W	T	F	S	S
Page No.:					YOUVA	

FINAL STATE

Definitions

DATA-PATH

I17 ADD



(S0)

RF-D4 → Mem-Add
Mem-Data → IR

IR-W

(S1)

RF-D4 → ALU-A
+1 → ALU-B
ALU-C → T3

ALU-ADD

T3-W

(S2)

III → RF-A3
T3 → RF-D3

RF-W

(S3)

IR9-11 → RF-A1
IR6-8 → RF-A2
RF-D1 → T1
RF-D2 → T2

T1-W

T2-W

(S4)

T1 → ALU-A
T2 → ALU-B
ALU-C → T3

ALU-ADD

T3-W

(S5)

IR3-5 → RF-A3
T3 → RF-D3

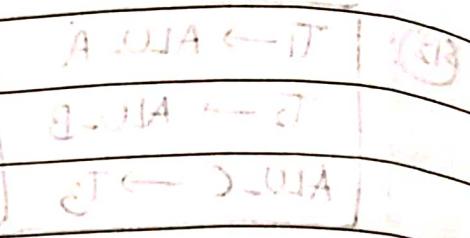
RF-W

(S25)

(do nothing, just
generate a delay of
1 clock cycle.)

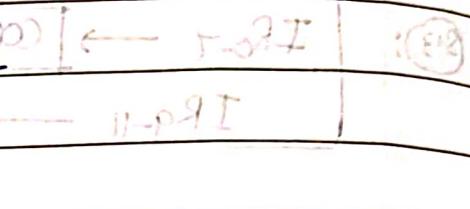
I2) SUB :- $S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_2 \rightarrow S_6 \rightarrow S_5 \rightarrow S_{25} \rightarrow S_0$

(S6):	$T_1 \rightarrow ALU-A$	$M1 \leftarrow ALU-SUB$
	$T_2 \rightarrow ALU-B$	$W-ET \quad T3-W$
	$ALU-C \rightarrow T_3$	$D-UJA \leftarrow T$



I3) MUL :- $S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_2 \rightarrow S_4 \rightarrow S_7 \rightarrow S_{25} \rightarrow S_0$

(S7):	$T_1 \rightarrow ALU-A$	$ALU-MUL$
	$T_2 \rightarrow ALU-B$	$T3-W \leftarrow H-PR$
	$ALU-C \rightarrow T_3$	



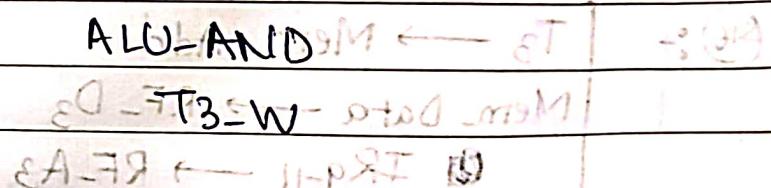
I4) ADI :- $S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_2 \rightarrow S_8 \rightarrow S_9$

(S8):	$T_1 \rightarrow ALU-A$	$ALU-ADD$
	$IR_0-5 \rightarrow SE_{6-16} \rightarrow ALU-B$	$T3-W$
	$ALU-C \rightarrow T_3$	$W \leftarrow RF-W$

(S9):	$IR_6-8 \rightarrow RF-A_3$
	$T_3 \rightarrow RF-D_3$

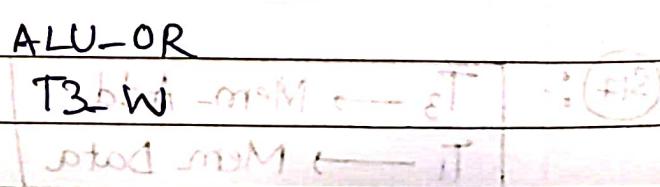
I5) AND :- $S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_2 \rightarrow S_{10} \rightarrow S_5 \rightarrow S_0$

(S10):	$T_1 \rightarrow ALU-A$
	$T_2 \rightarrow ALU-B$
	$ALU-C \rightarrow T_3$

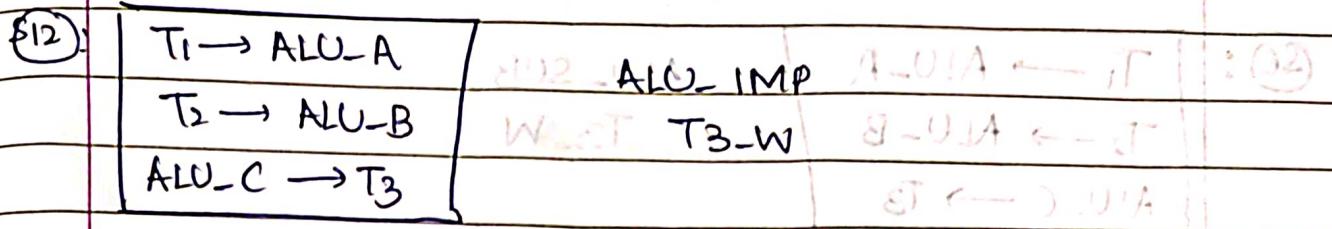


I6) IORA :- $S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_2 \rightarrow S_{12} \rightarrow S_5 \rightarrow S_0$

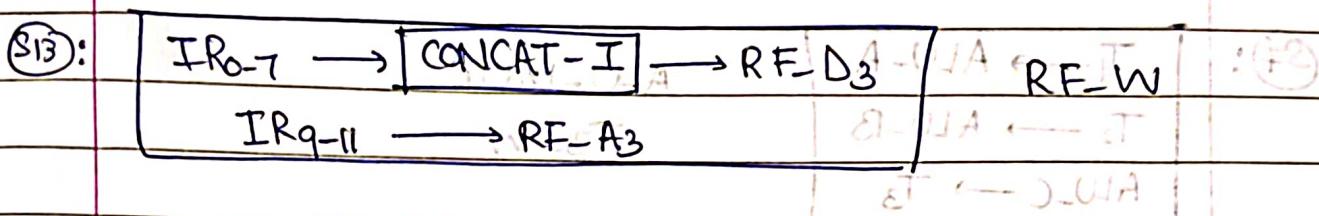
(S11):	$T_1 \rightarrow ALU-A$
	$T_2 \rightarrow ALU-B$
	$ALU-C \rightarrow T_3$



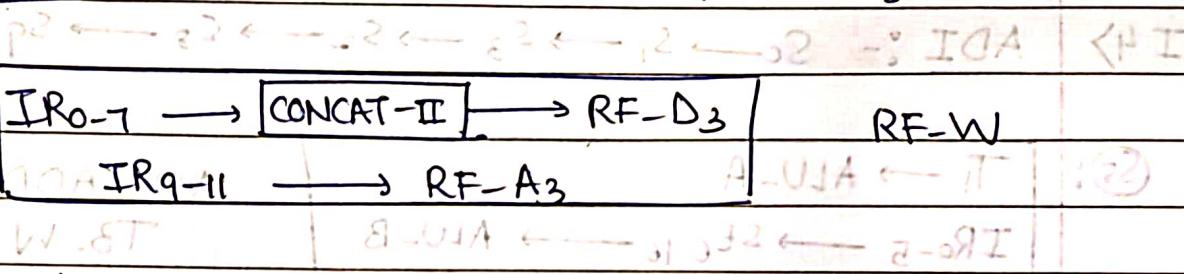
I7) IMP :- $S_0 \rightarrow S_1 \rightarrow S_3 \rightarrow S_2 \rightarrow S_{12} \rightarrow S_5 \rightarrow S_{25} \rightarrow S_0$



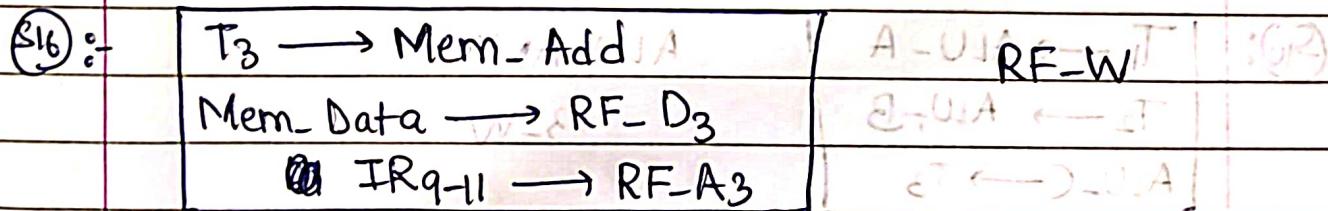
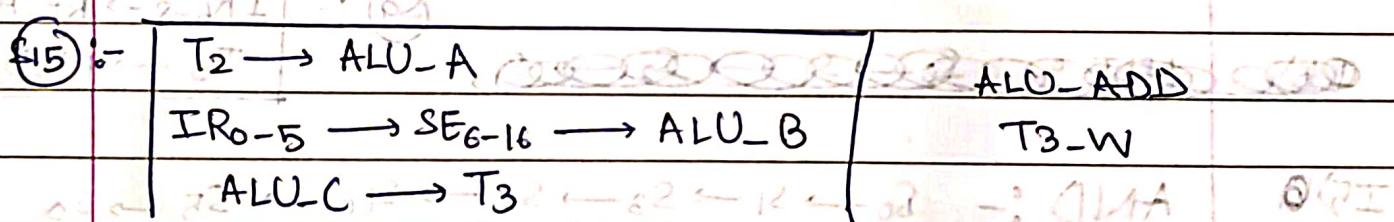
I8) LHI :- $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{12} \rightarrow S_{25} \rightarrow S_{01}$ (Q2)



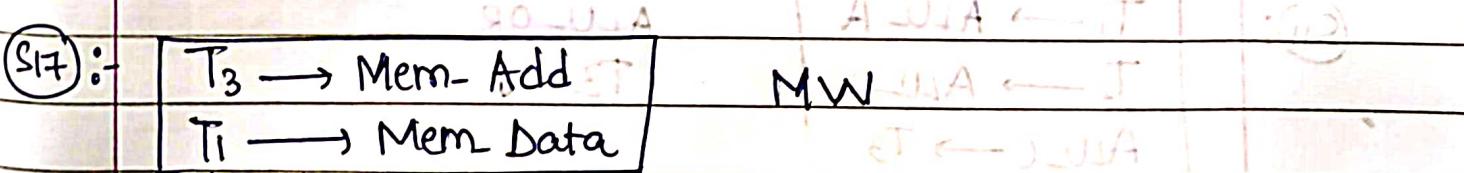
I9) LLI :- $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{14} \rightarrow S_{25} \rightarrow S_0$



I10) LW :- $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_8 \rightarrow S_{15} \rightarrow S_{16} \rightarrow S_{25} \rightarrow S_0$



I11) SW :- $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_{15} \rightarrow S_{17} \rightarrow S_{25} \rightarrow S_0$



I12) BEQ :- $S_0 \rightarrow S_3 \rightarrow S_6 \rightarrow S_{18} \rightarrow S_2 \rightarrow S_{25} \rightarrow S_0$
 ↓
 (zero flag
 sets here)

S18 :-

```

graph LR
    RF[RF-D4] --> ALU_A[ALU-A]
    RF --> ALU_B[ALU-B]
    IR[IR0-5] --> SE[SE6-16]
    SE --> ALU_B
    ALU_A --> SUM[ALU-C]
    ALU_B --> SUM
    SUM --> T3_W[T3-W]
    
```

I13) JAL :- $S_0 \rightarrow S_{21} \rightarrow S_{26} \rightarrow S_2 \rightarrow S_{25} \rightarrow S_0$

S21	$RF-D_4 \rightarrow ALU-A$	<u>ALU-ADD</u>
	$IR_{0-8} \rightarrow SEQ-16 \rightarrow ALU-B$	<u>T3-W</u>
	$ALU-C \rightarrow T_3$	

S26 :-	$IR_{9-11} \rightarrow RF\text{-}A_3$	$RF\text{-}W$
	$RF\text{-}D_4 \rightarrow RF\text{-}D_3$	

I14) JLR :- S₀ → S₁₉ → S₂₃ → S₂₂ → S₂ → S₀

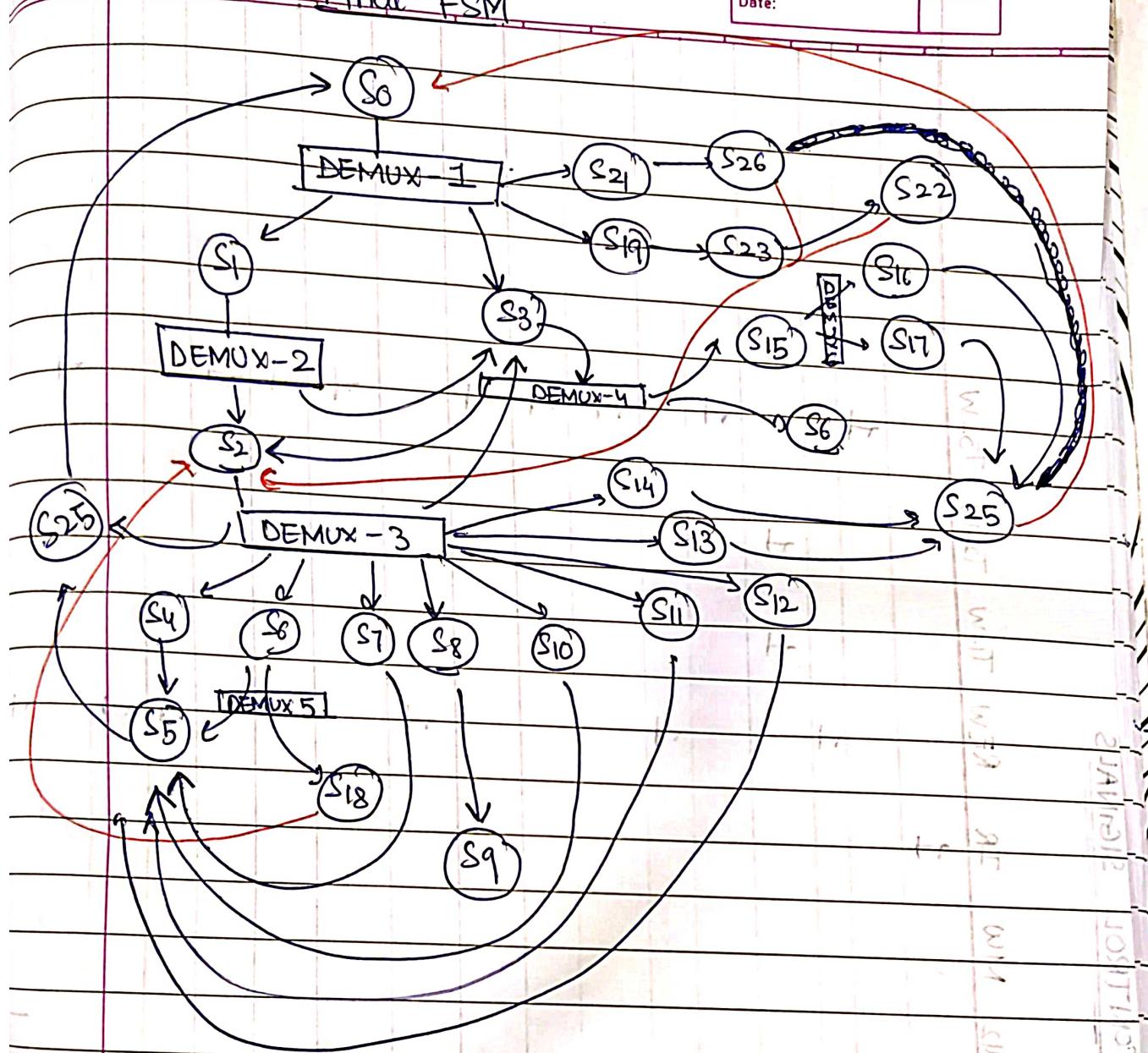
(519) :-

$\text{RF-D}_4 \longrightarrow \text{T}_3$	T_3-W
$\text{RF-A}_4 \longleftrightarrow \text{III}$	

S23) :-	$T_3 \longrightarrow RF_D_3$ $RF_A_3 \leftarrow IR_{9-11}$	RF-W
---------	---	------

$$\text{S}_{22} \text{: } \begin{array}{c} \text{IR}_{6-8} \longrightarrow \text{RF-A}_2 \\ \text{T}_3 \leftarrow \text{RF-D}_2 \end{array} \quad \text{T}_3 = \text{W}$$

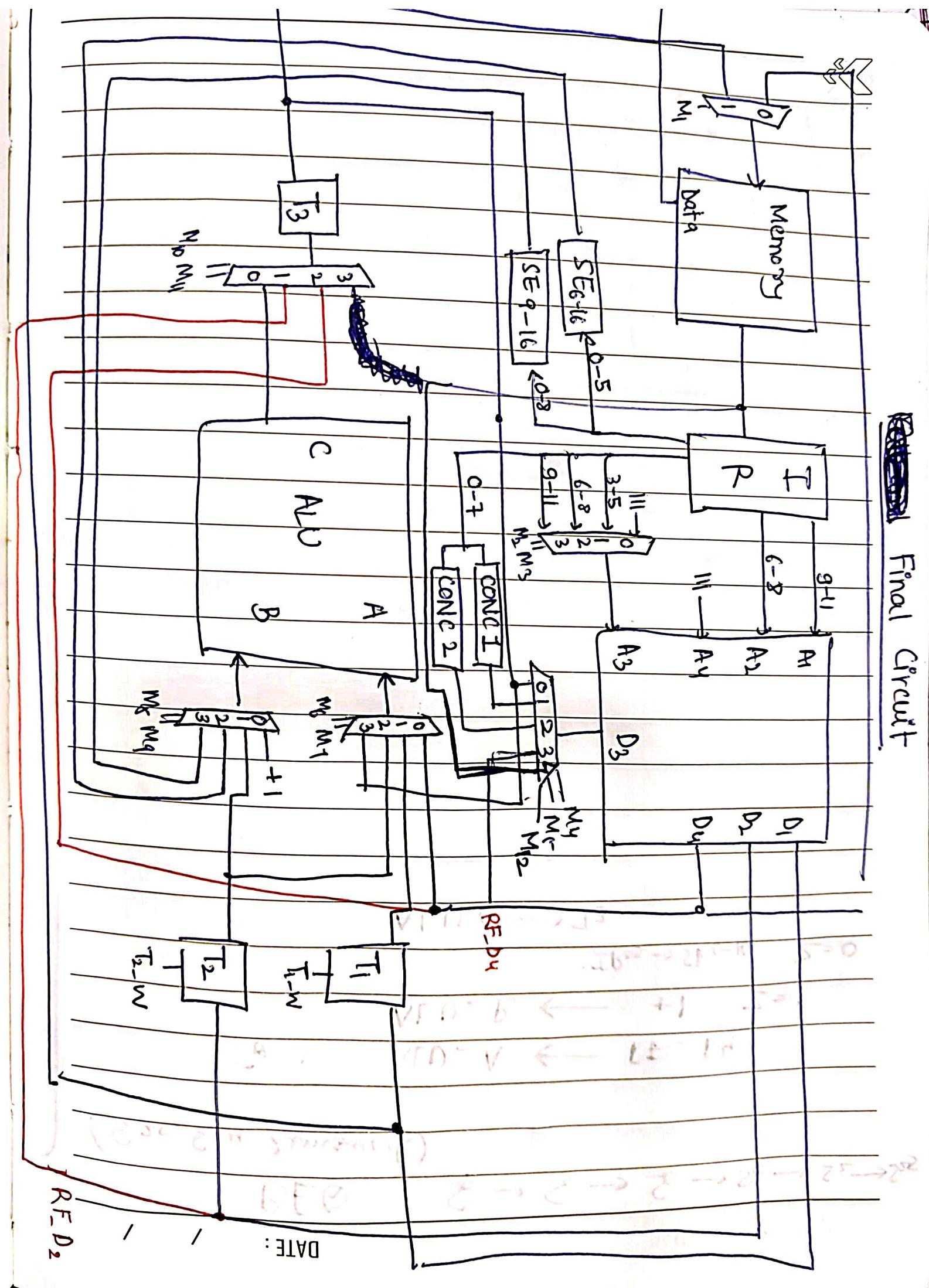
Final FSM



(Both S₂₅ are the same)

~~RECORDED~~

Final Circuit.



④ LIST of All Changes Done

- <1> Introduction of an extra FPGA-delay state (S_{25}) at the end of all instructions, so that IR can be updated in the previous instruction itself.
- <2> Removed external PC and stored it in site R_7 in register file. Read and wrote into R_7 using the register file itself.
- <3> Changed the FSM to make sure that the original PC is used for the instruction and not the updated PC ($PC+1$).
- <4> Changed the definitions of the states, and made the FSM such that $PC+1$ (for the next instruction) doesn't get updated right in the beginning, but after all of its values from the IR are taken into the temporary registers (T_1, T_2)
- <5> Modified the definition of BEQ statement, and changed control signals such that it itself chooses whether to add (+) or Immediate value to the PC, to jump or not jump.
- <6> Added a RESET pin, did all the pin-planning and other relevant SVF's etc. to upload the code on the FPGA. The reset pin is mapped to the push switch, while the

S	M	T	W	T	F	S
WORK						
HOME						

M	T	W	T	F	S	S
Page No.:					YOUVA	

8 switches are used to index the registers.

until A=277 there no to nothing

R0 → SW1, In R0 out to RESET → PB,

R1 → SW2, and out 2LSB/MSB → PB_Y

R2 → SW3, In R2 out to nothing

R3 → SW4, C1K → 1KHz (Pin 55)

R4 → SW5, For 4x8 memory

R5 → SW6, In R5 out to nothing

R6 → SW7, In R6 out to nothing

R7 → SW8

to R1, R12 work if M27 out binged

Changed the inputs and outputs of the CPU

INPUT :- reset, C1K, switches (██████)

OUTPUT :- All the 8 registers (in the programmer section)

→ VERIFIED! on FPGIA the working of all the 14 instructions by changing the memory accordingly and observing the outputs of the LED's. Also added the check to update R7 using any instruction and not PC.

All the instructions worked

dig out the bit pin T3239 → b6A

its → EVB + board with b6A minima

now out A3272 out to b6A out b6A

Now, adding this out b6A?

M	T	W	T	F	S	S
Page No.:	YOUVA					
Date:						

WORK DISTRIBUTION

Nimay :- re-designed FSM and datapath,
FPGA implementation.

Harsil :- updated code, signals etc., FPGA
implementation, made code FPGA-
ready.

Mahav !— FPGA implementation, ideation of
PC-R7 issue.

Anay :- FPGA implementation, ideation of
PC-R7 issue.