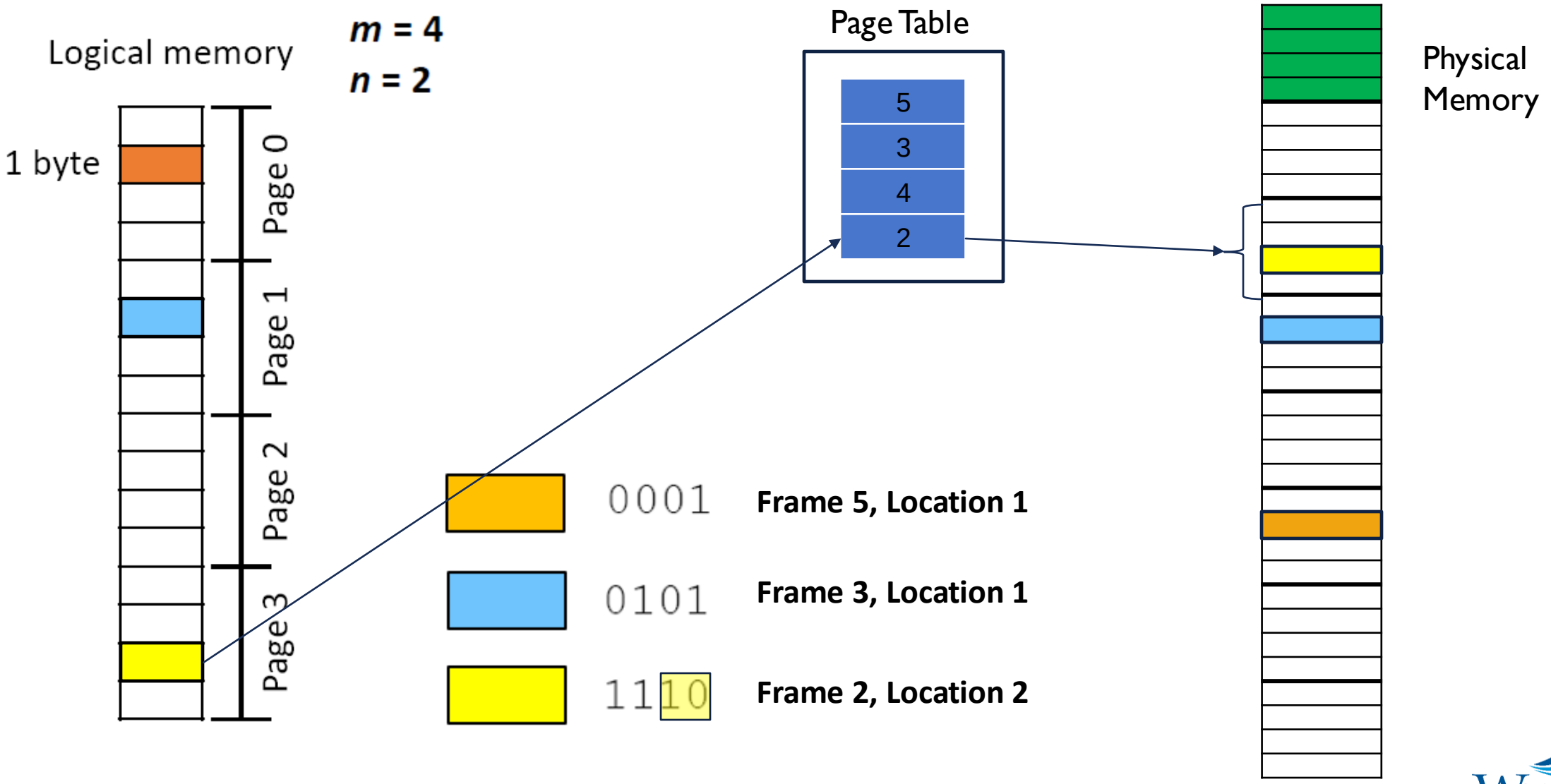
OPERATING SYSTEMS INTERNALS

CSCI 509

PAGING



FRAGMENTATION

Q: Can we have external Fragmentation?

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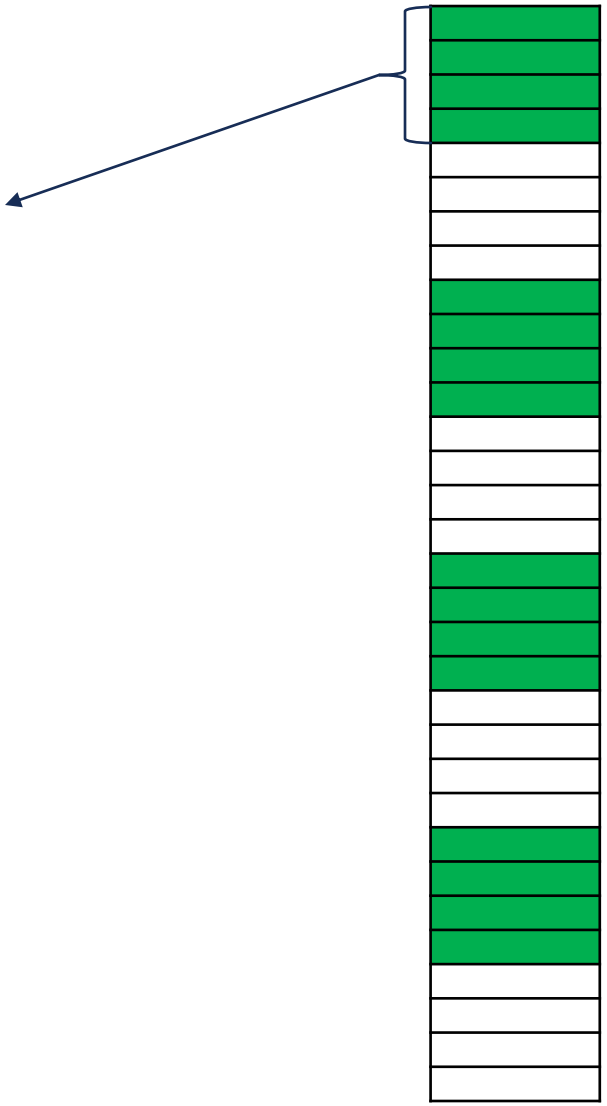
All memory holes are made up of a multiple of pages (1x , 2x , ..) since frame size = page size.

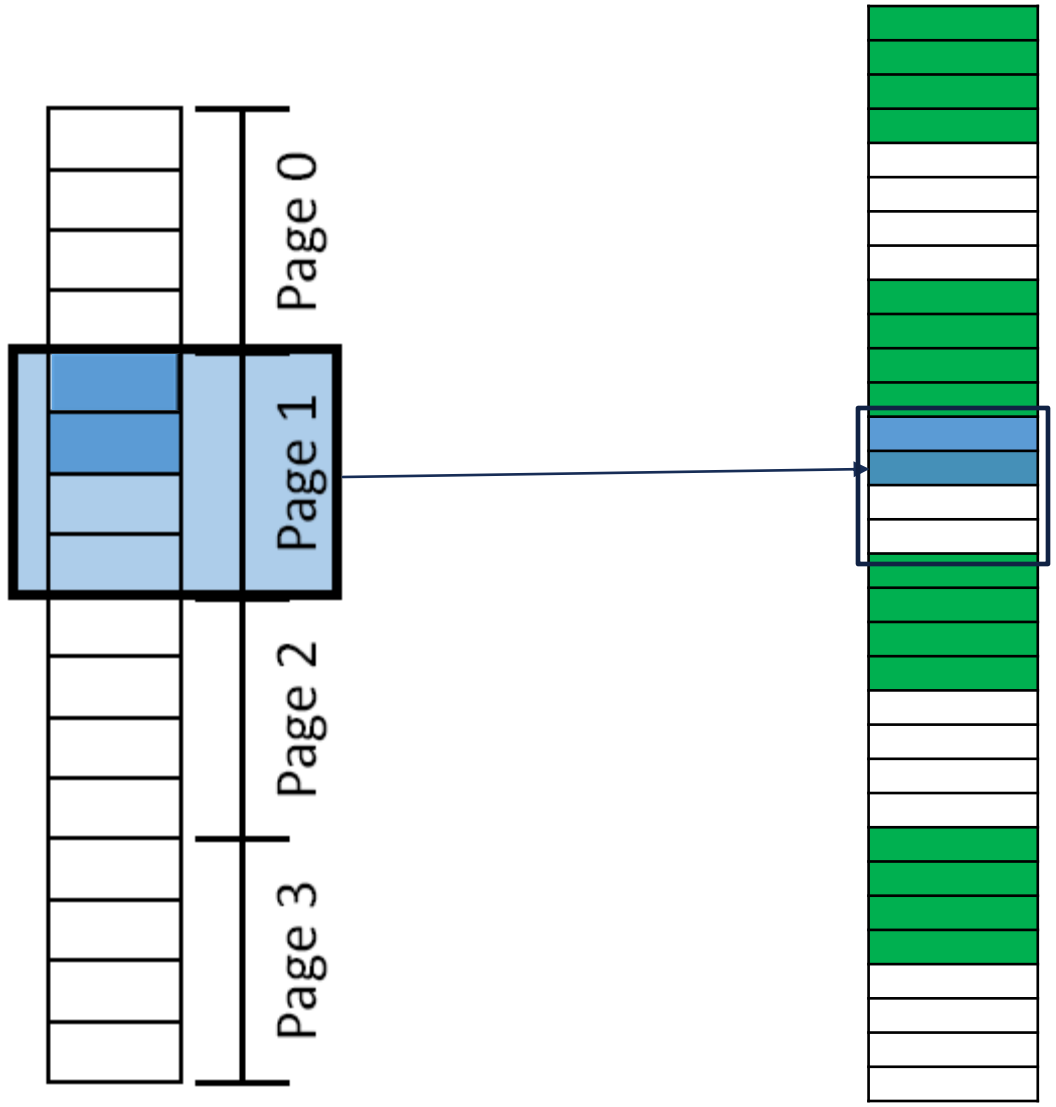
No External Fragmentation!



INTERNAL FRAGMENTATION

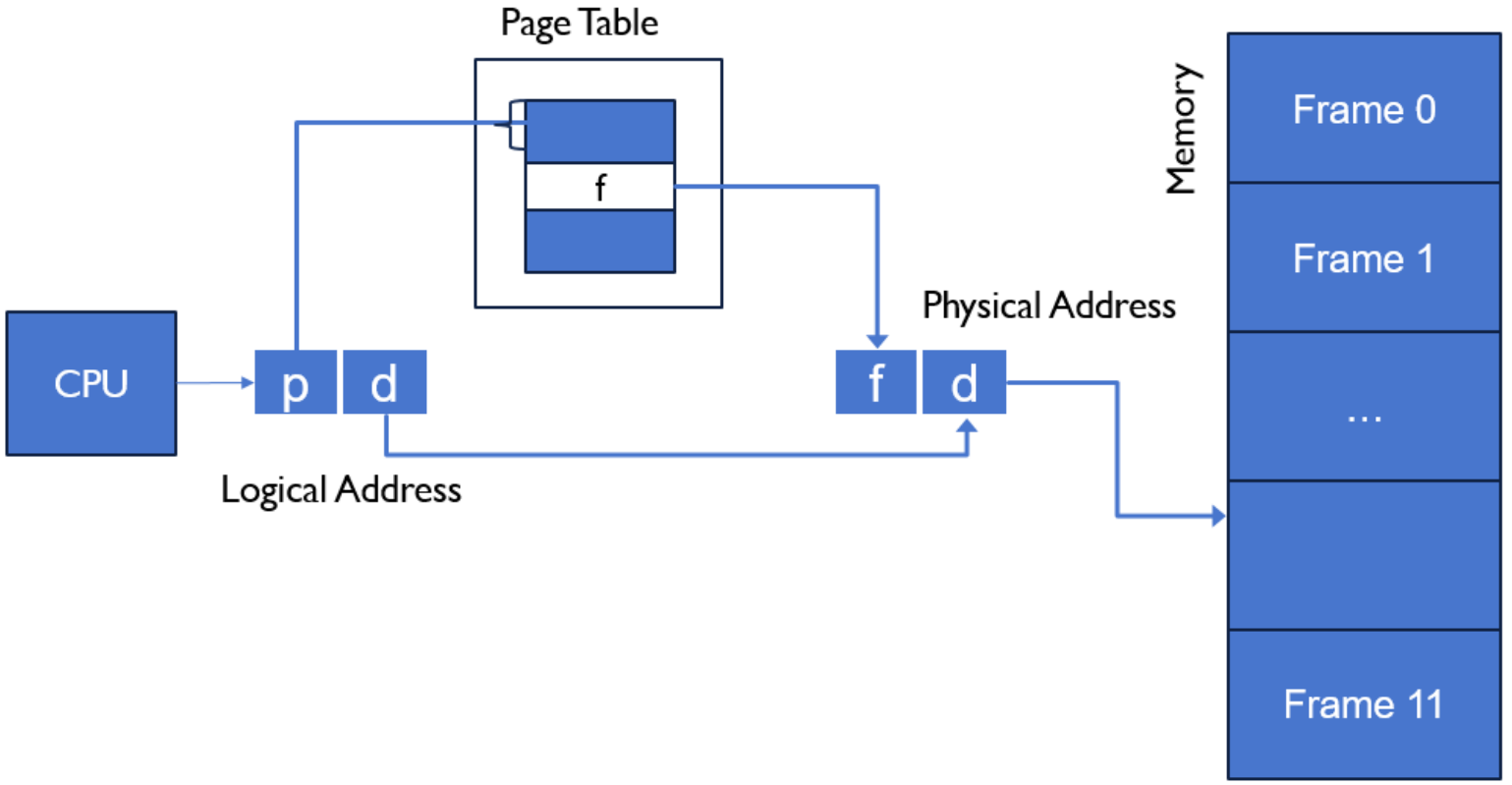
A process might not use its last page fully …

Internal fragmentation still exists.



PAGE TABLE

- Every address resolution needs to go through the Page Table.
- How large is the page table?



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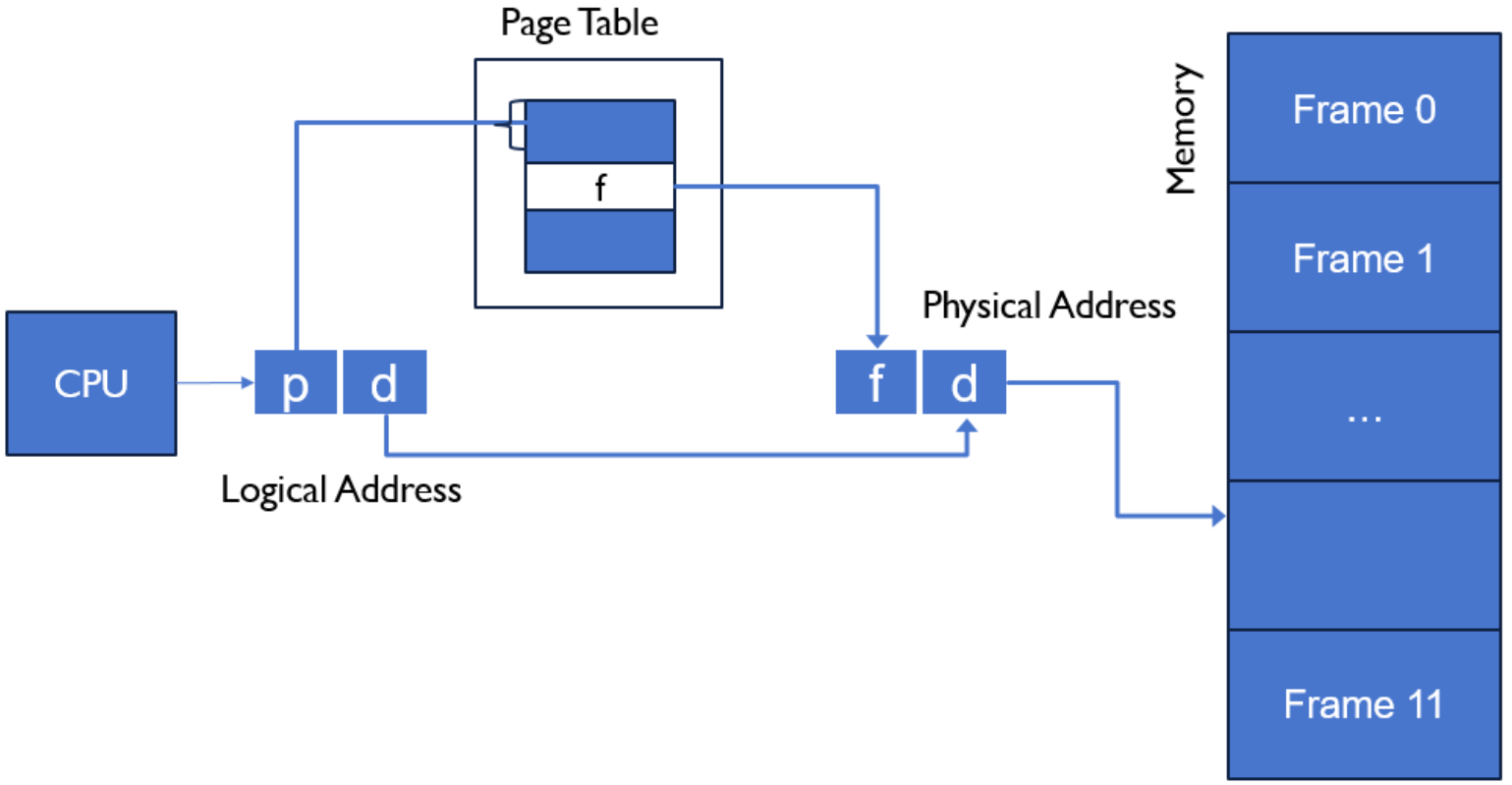

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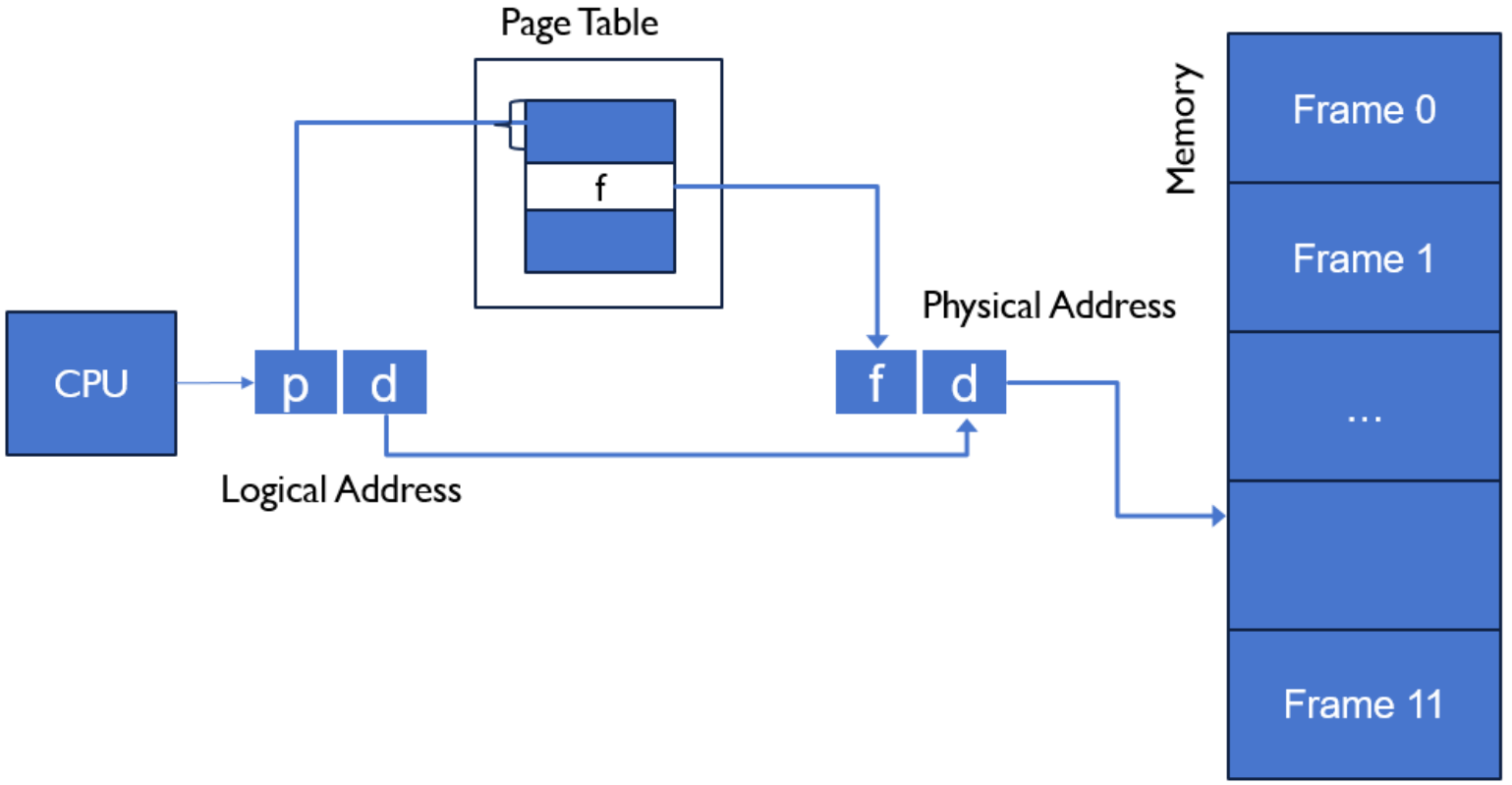

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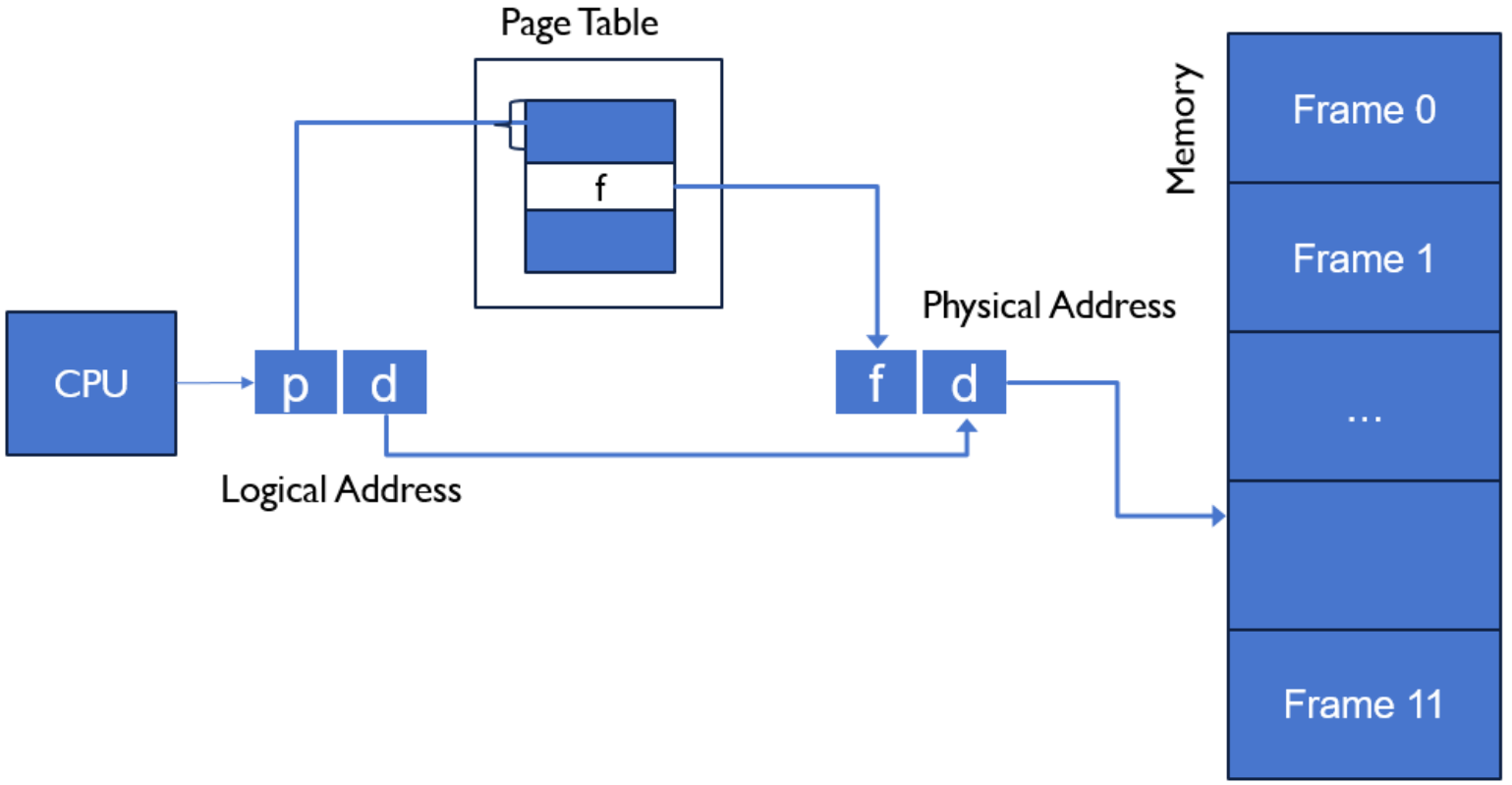

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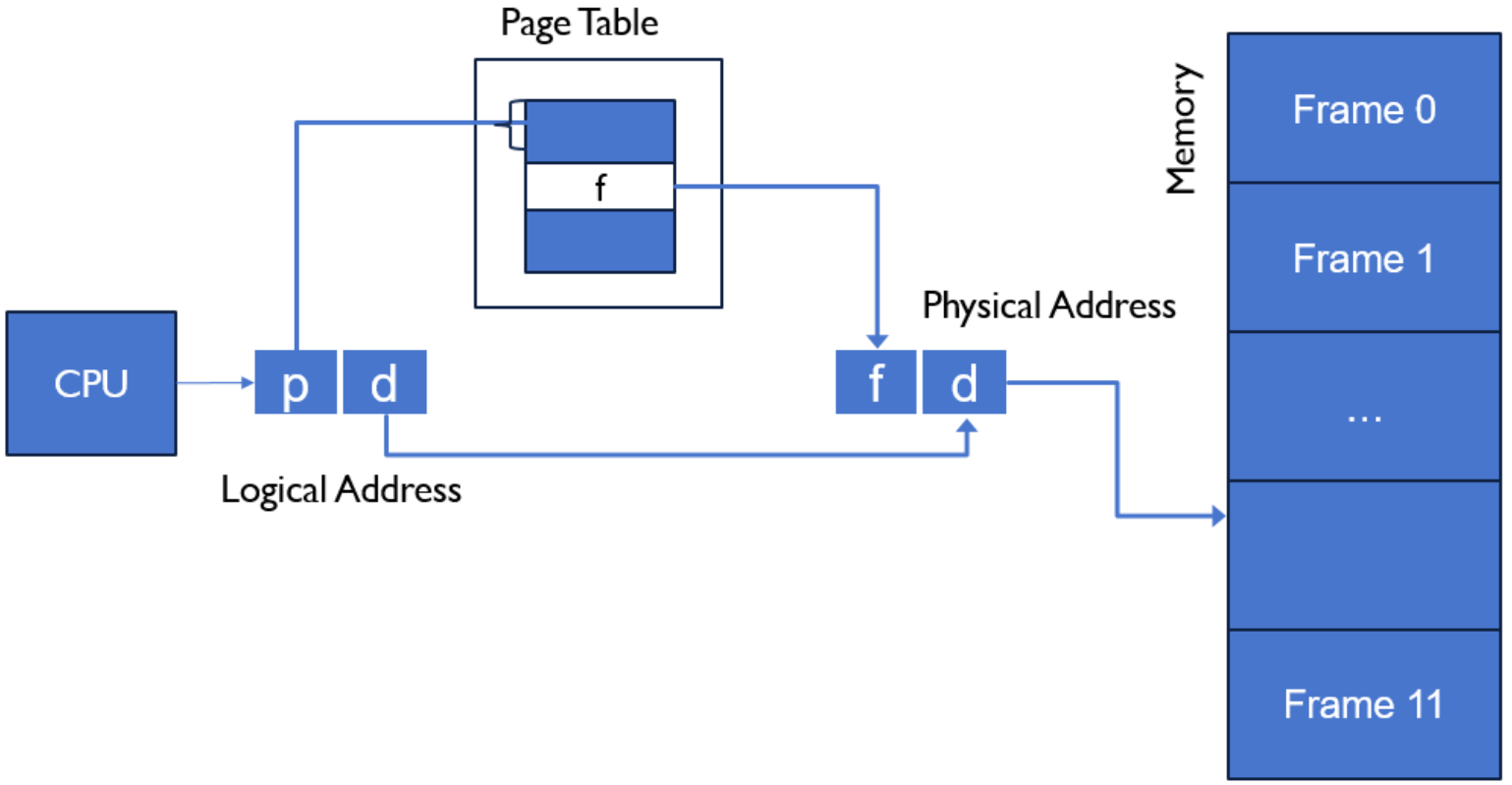

PAGE TABLE

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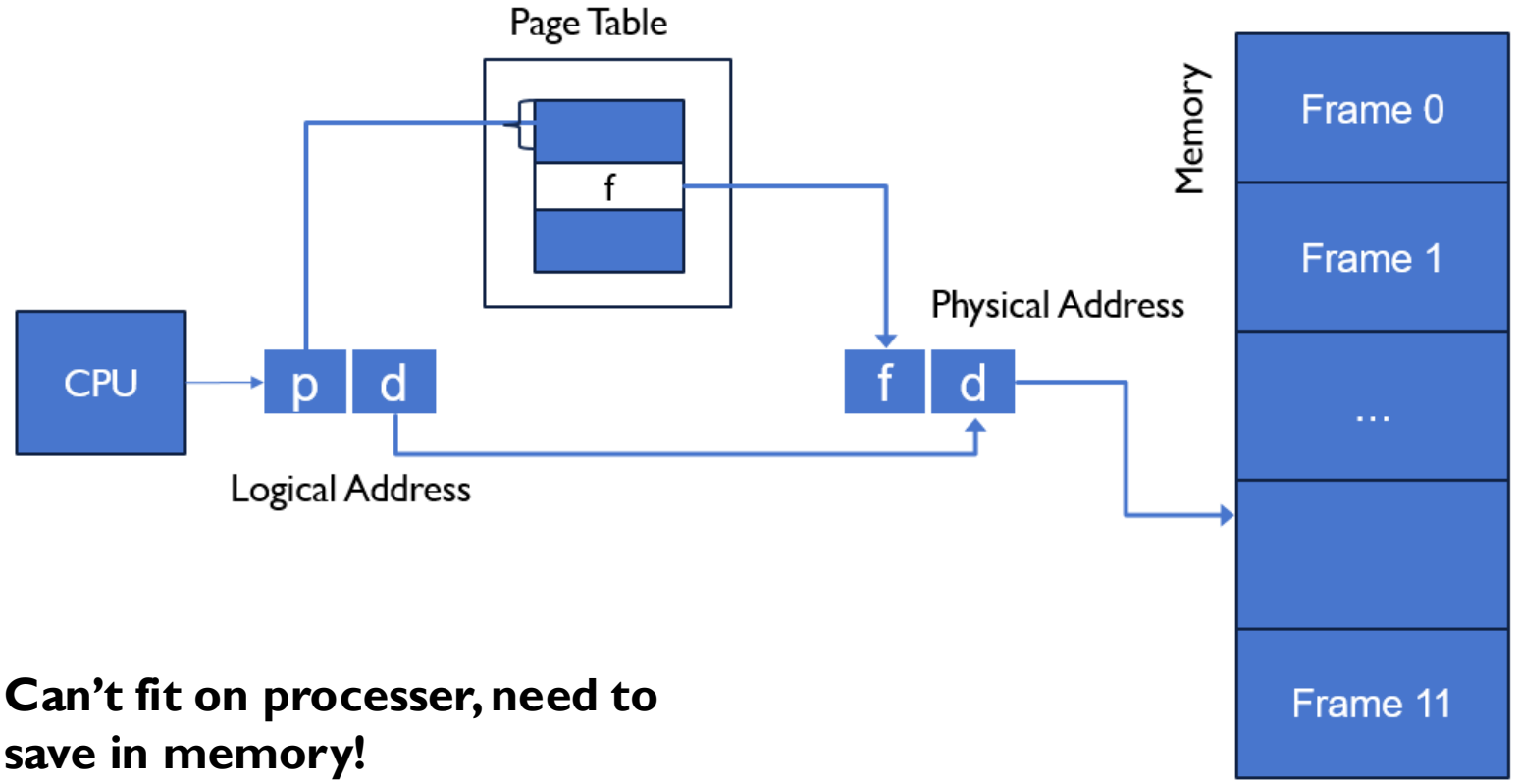
- Need to calculate m-n
- m = 32
- n = 10 = (2^10 = 1KB)
- m-n = 22
- # entries in table: 2^{22}
- Size of table 4 bytes (32-bites) x 2^{22} MB = 16 MB.



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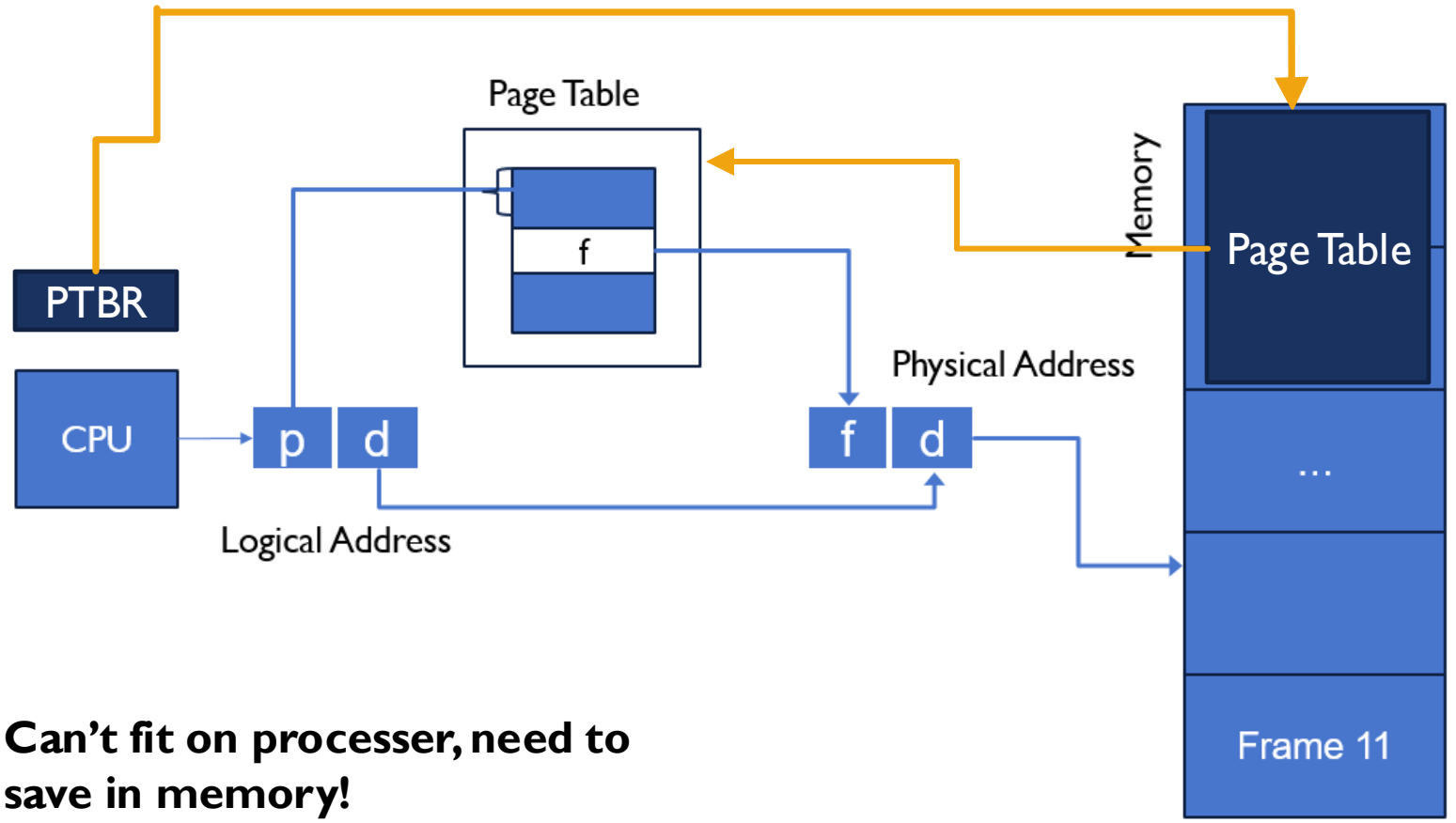

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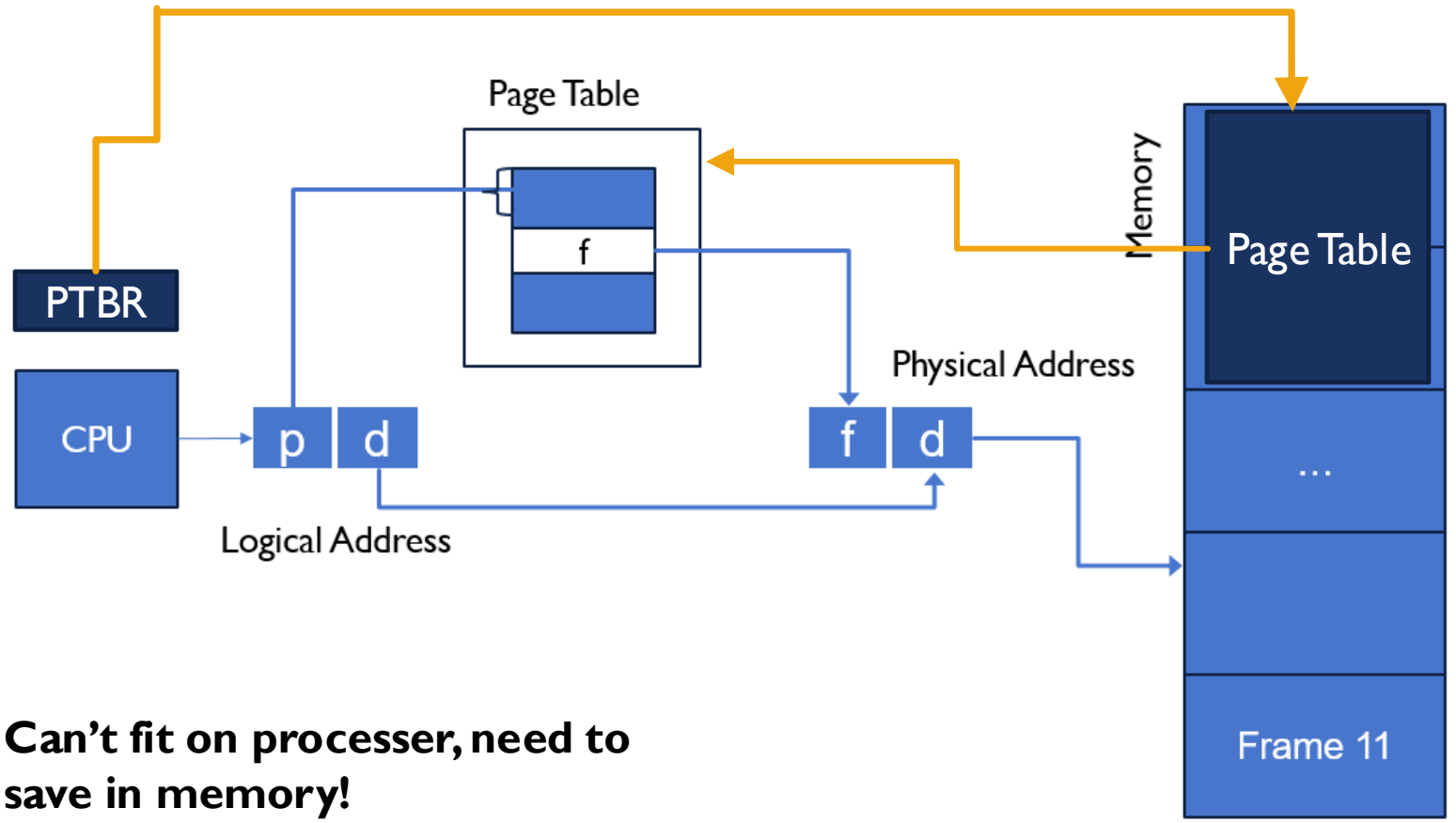

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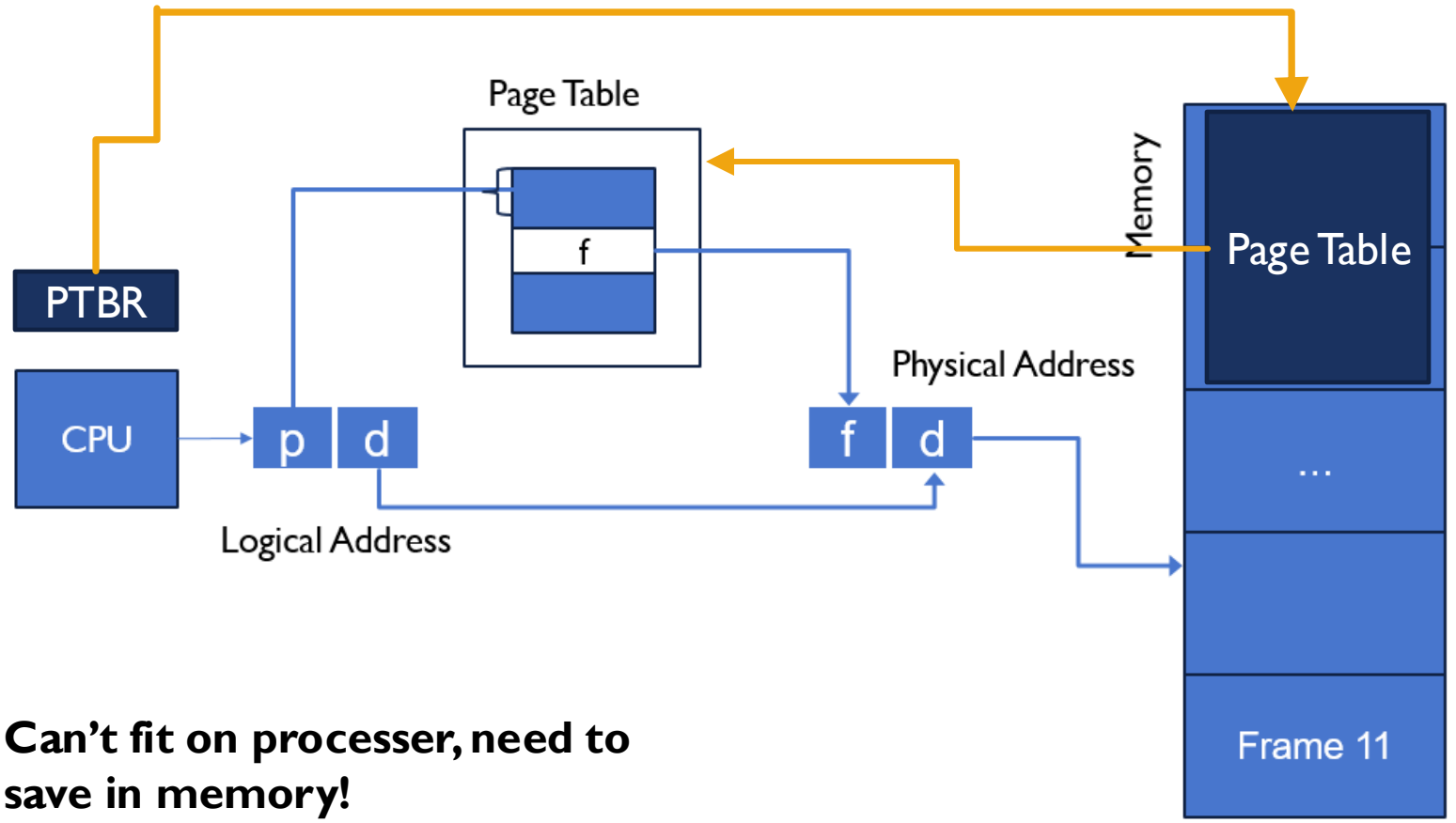
- **Extremely slow!**



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TRANSLATION LOOK ASIDE BUFFER

- TLB: A small table that resides on the CPU.
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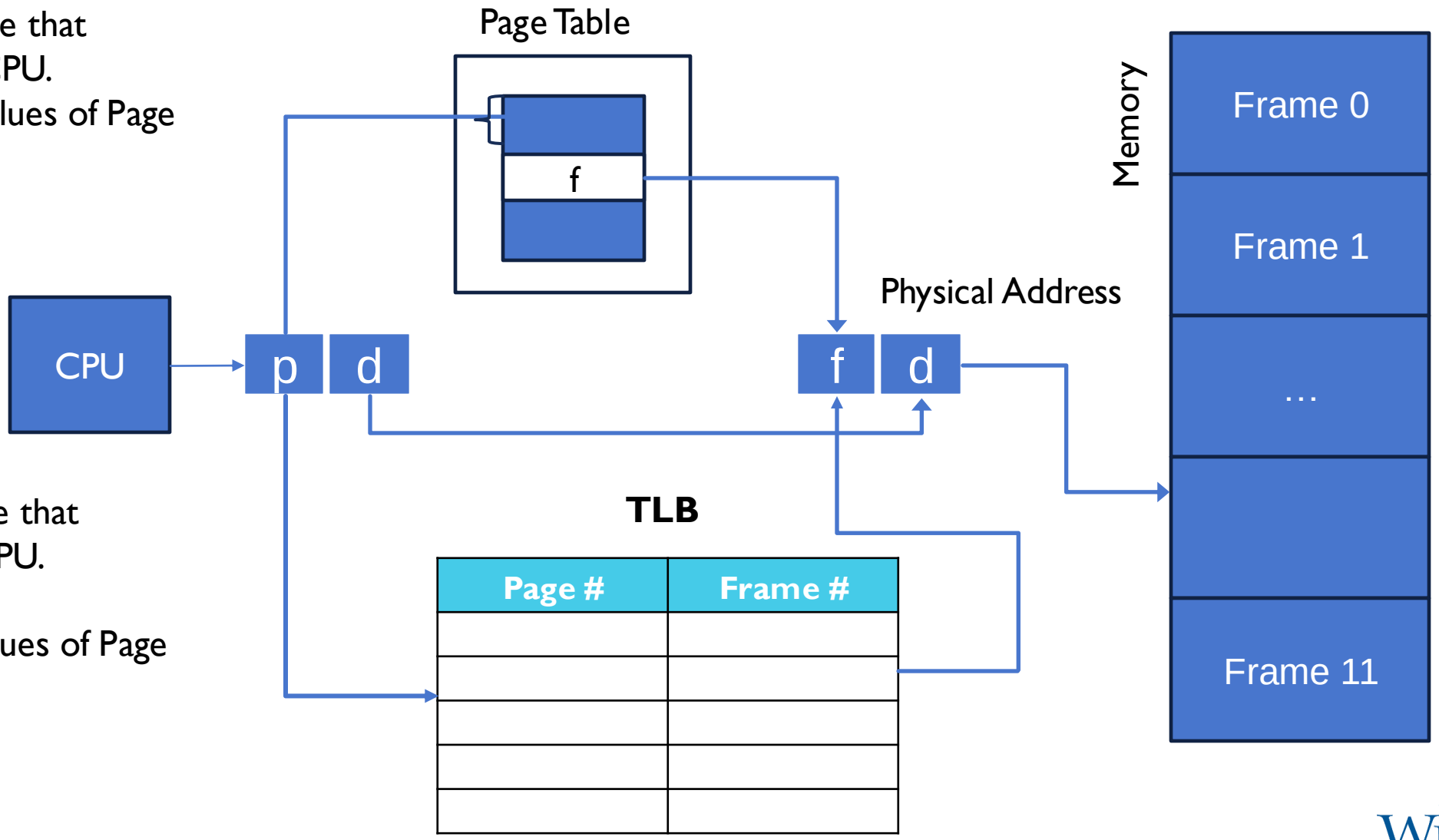

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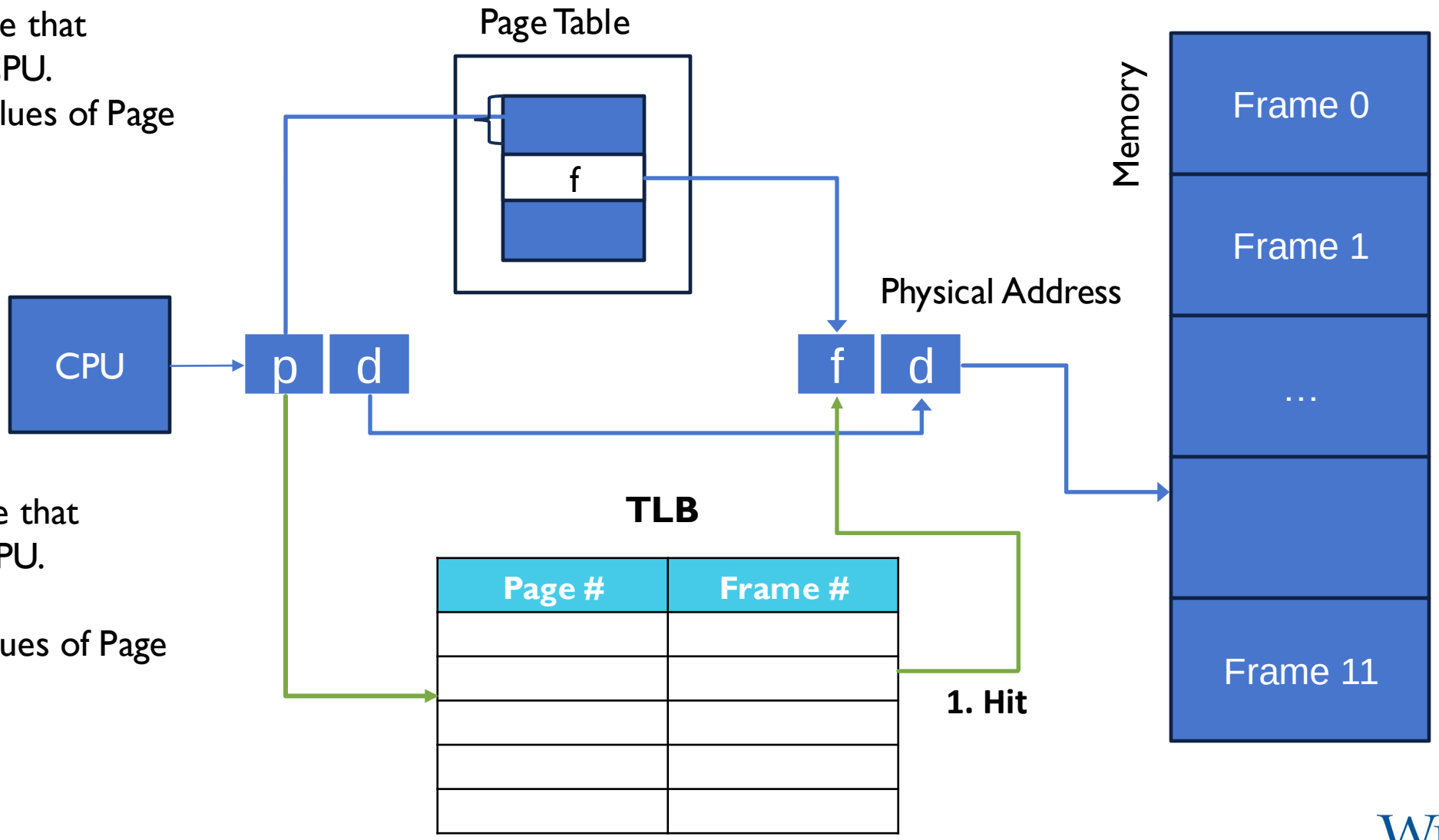

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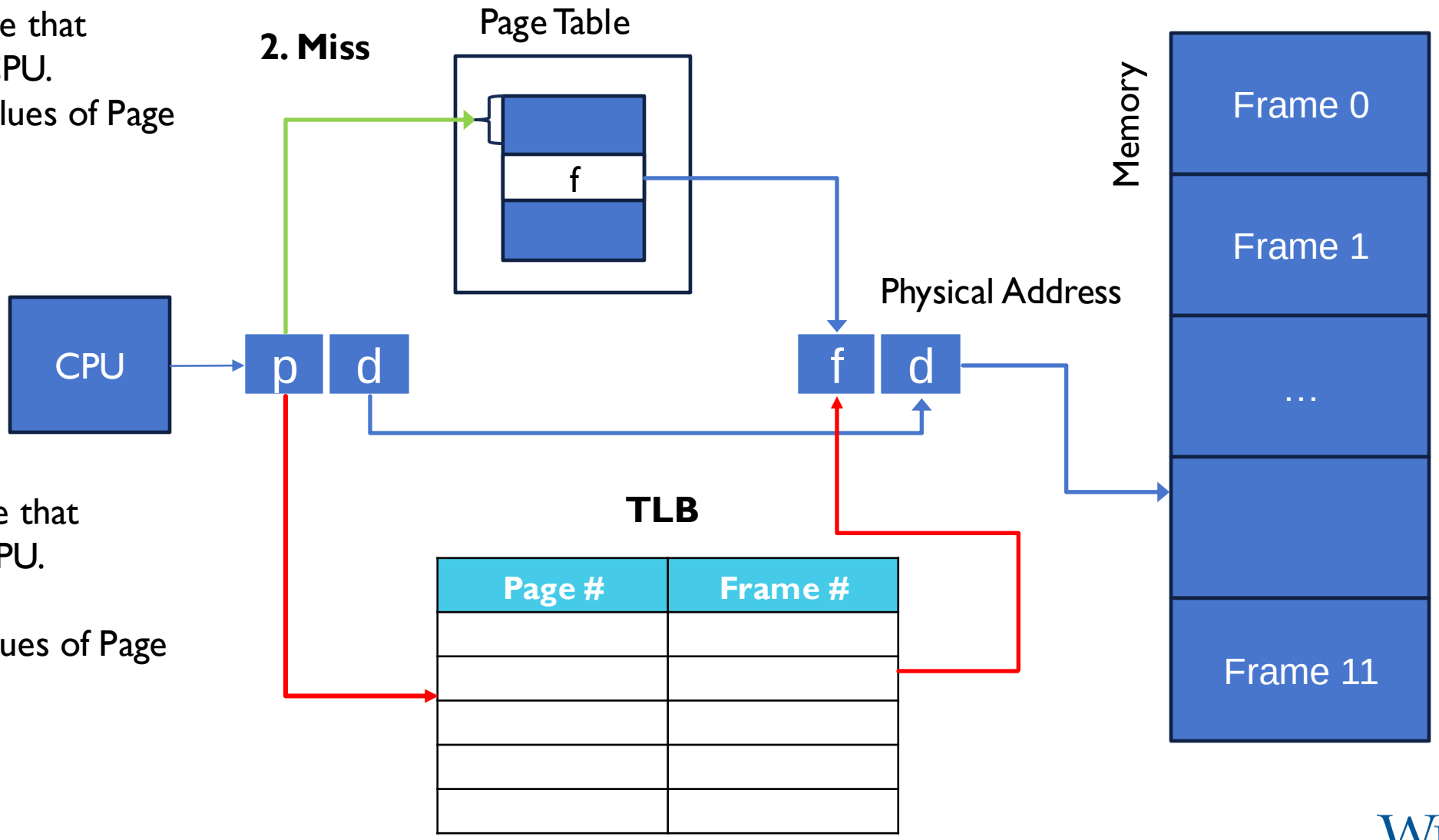

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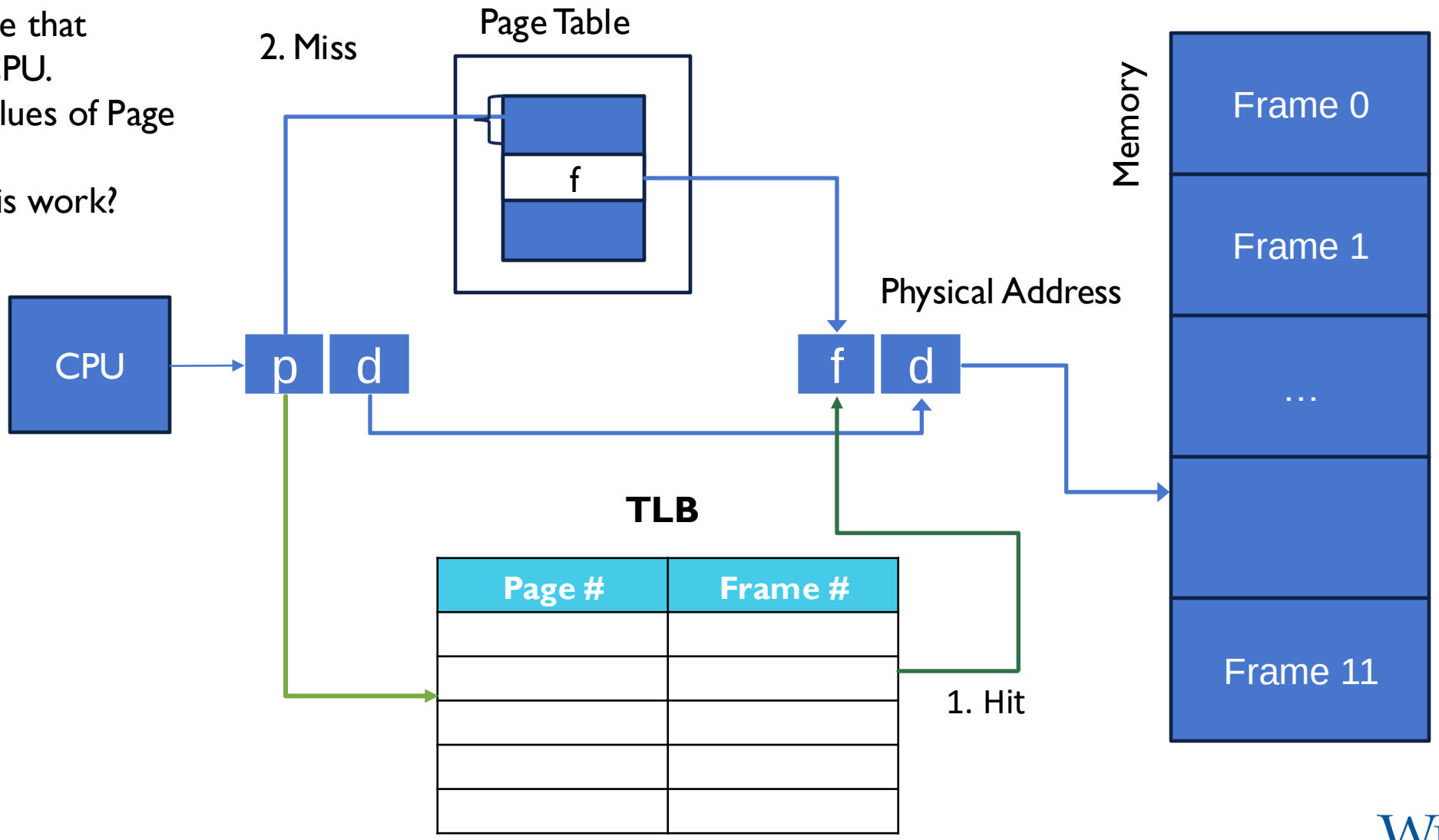

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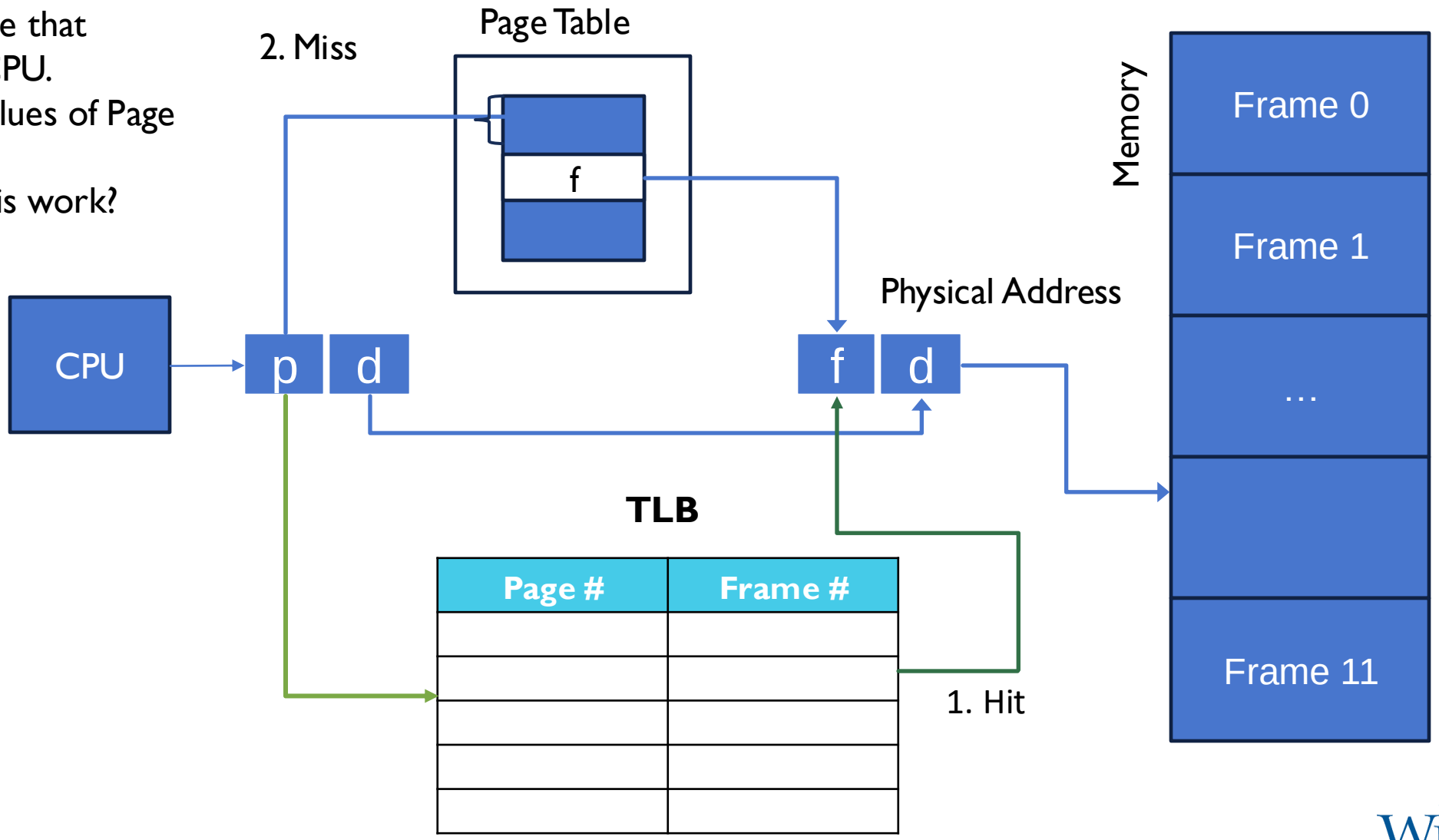

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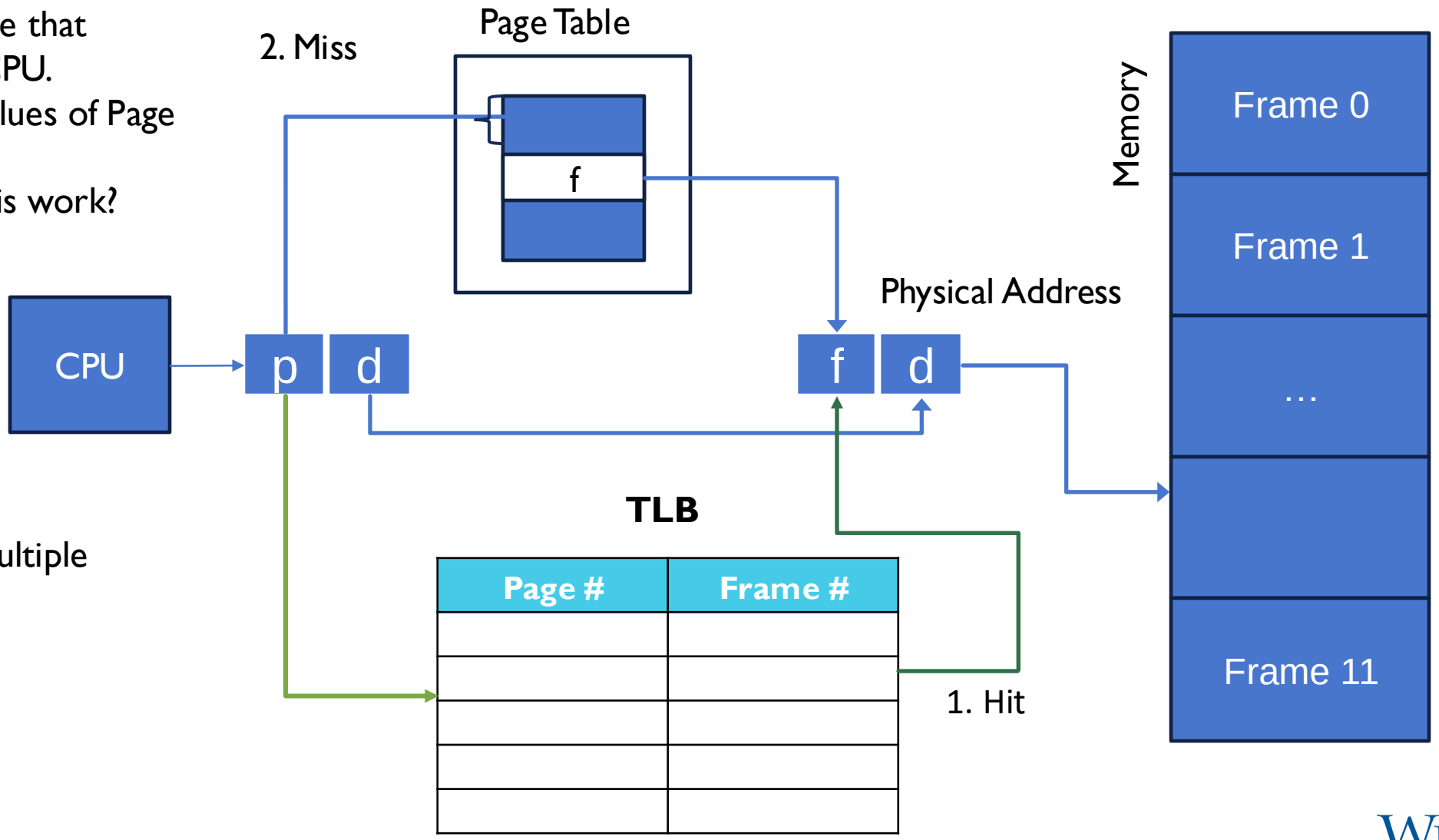

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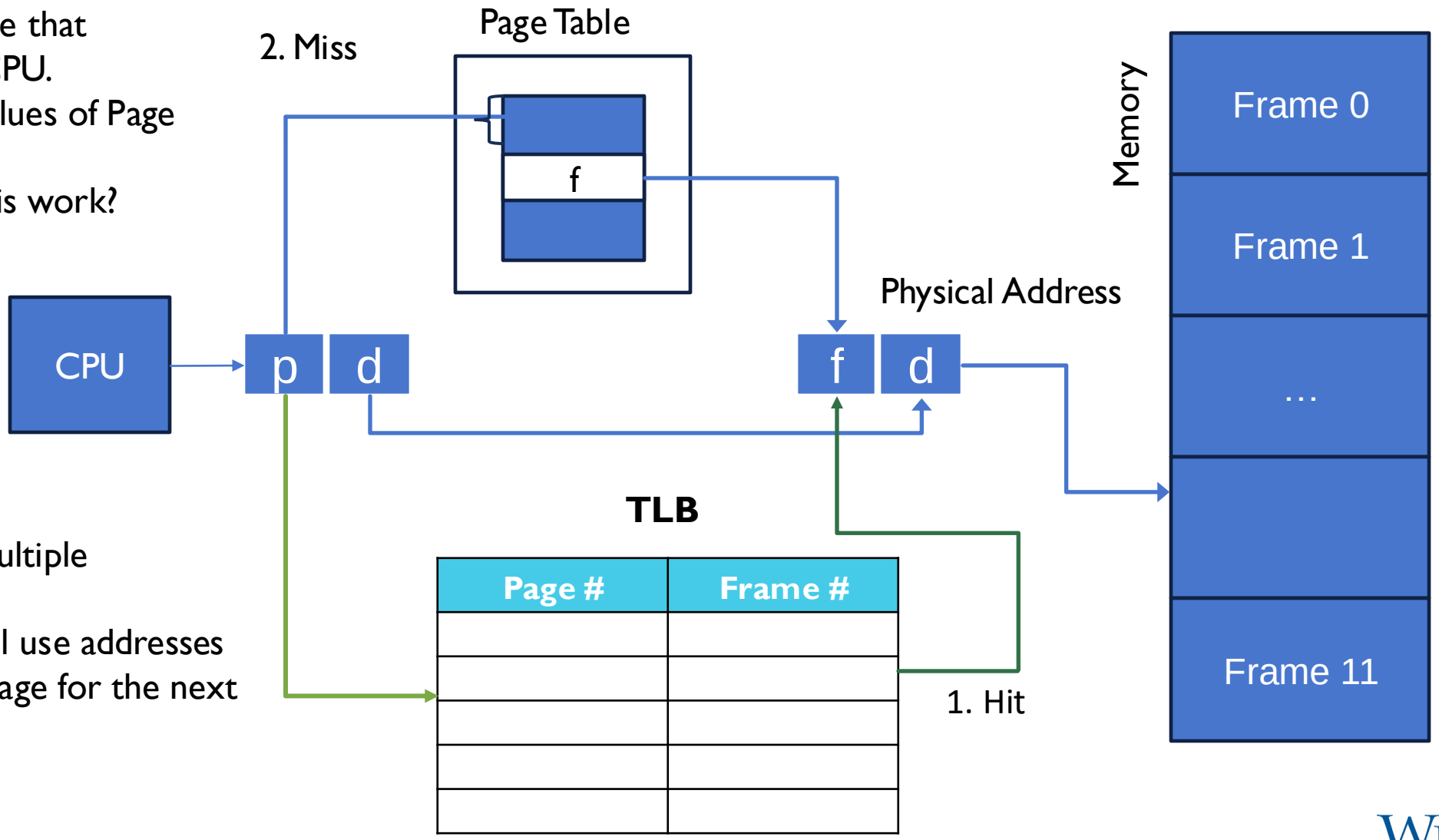

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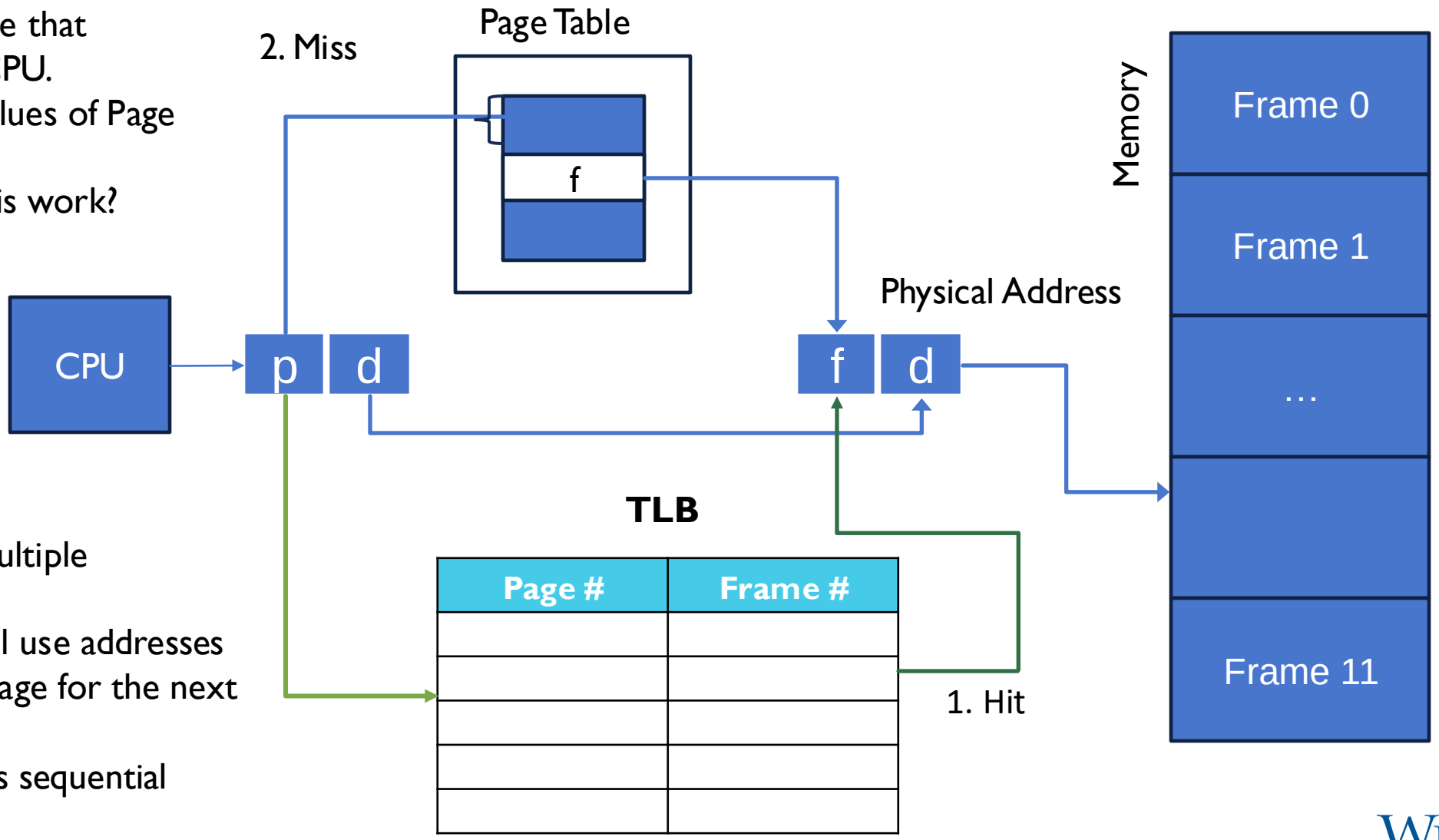

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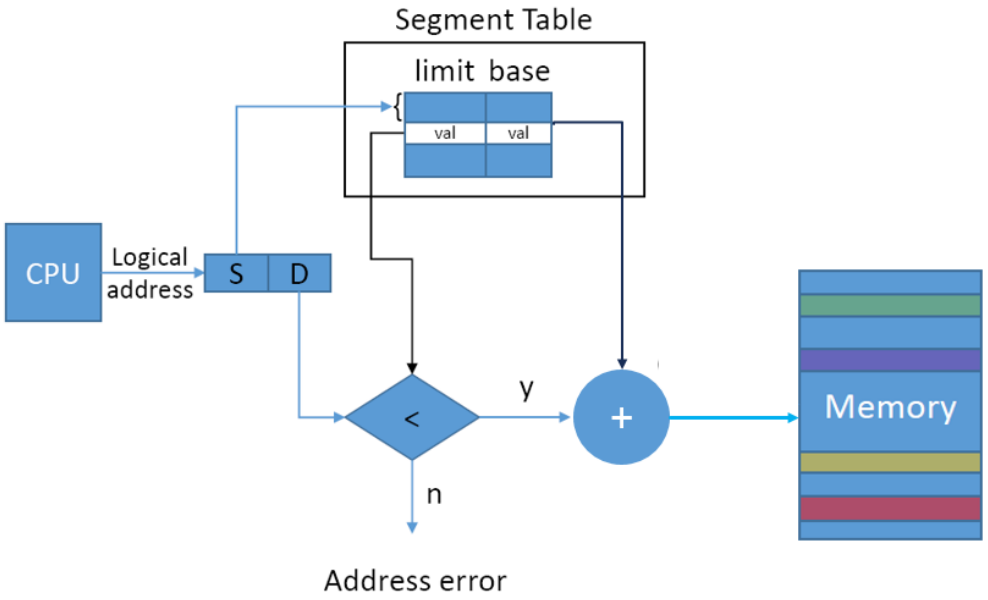
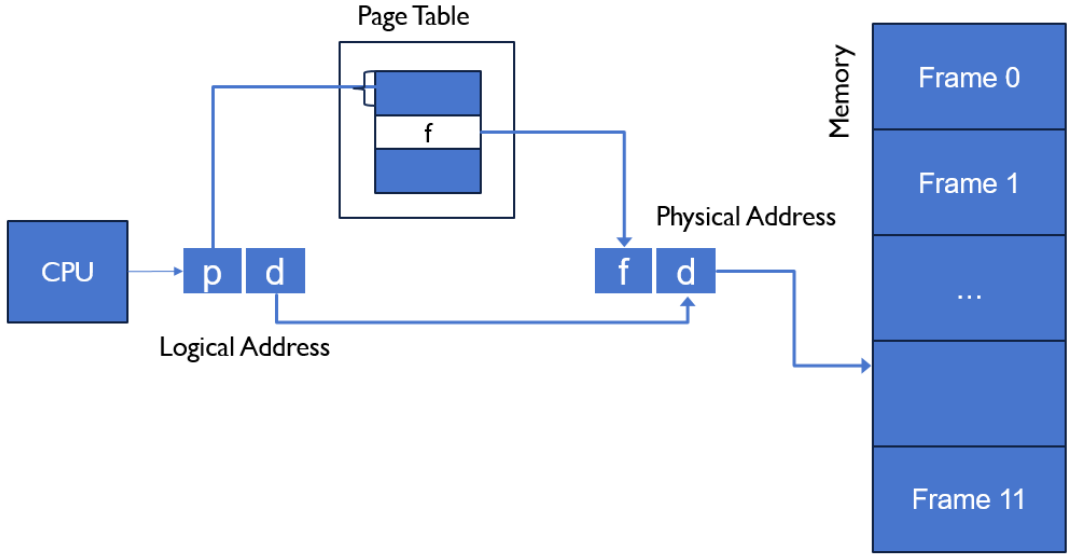
- Example: Code is sequential

PAGING VS SEGMENTATION





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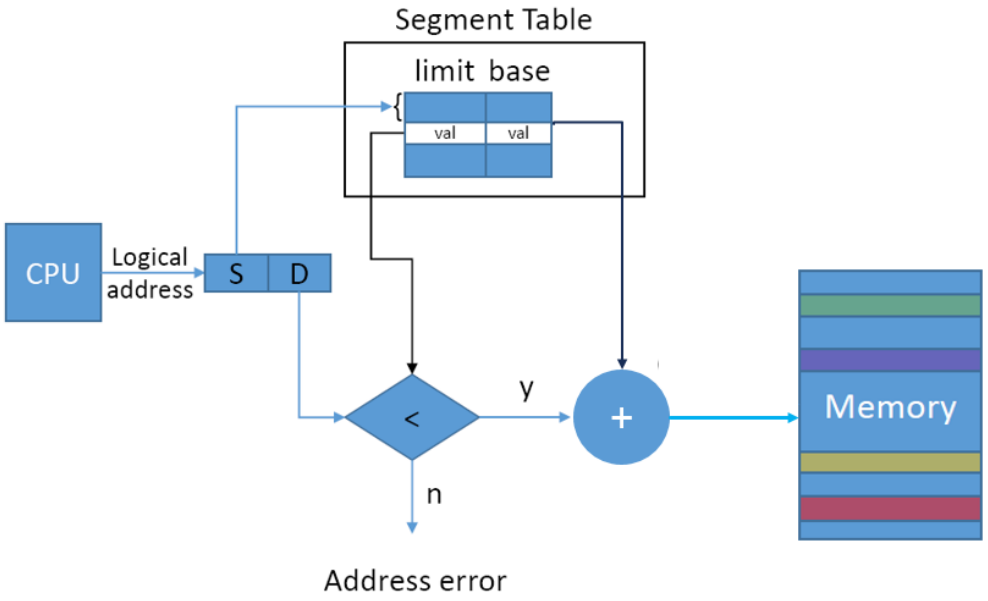

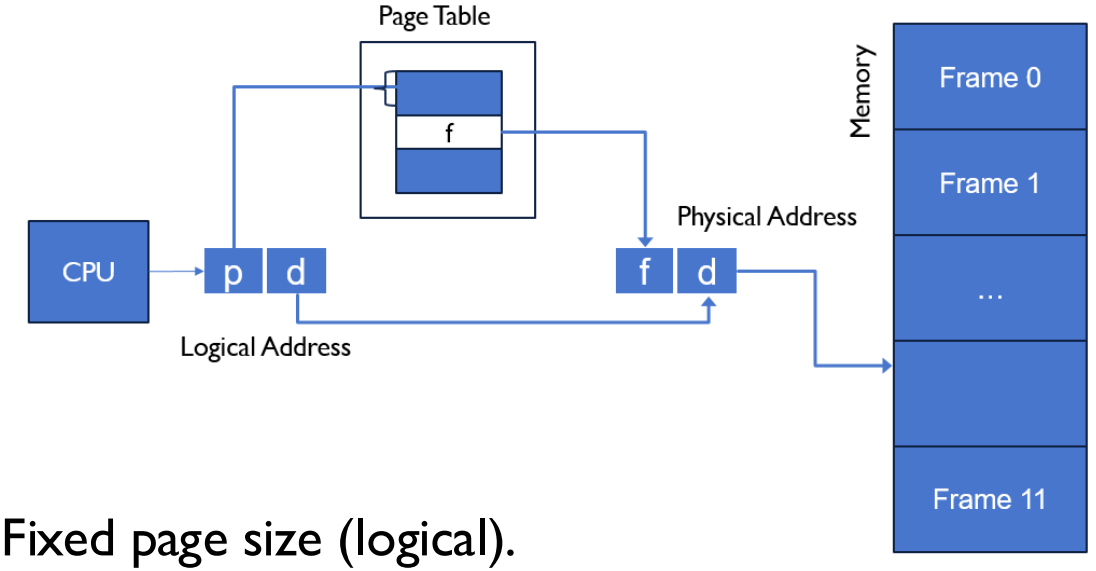

1. Fixed page size (logical).
2. Fixed frame size (physical) = page size.
3. Contiguous virtual (logical) address. Programmer doesn't see <p,d> but just an address.
4. Not all Pages need to be in memory!

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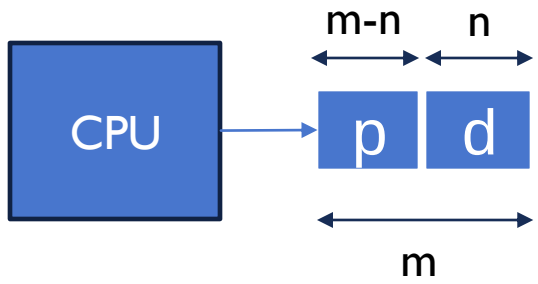

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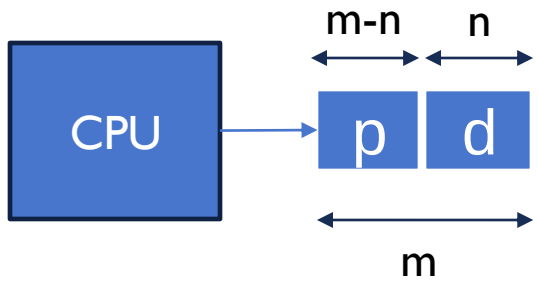

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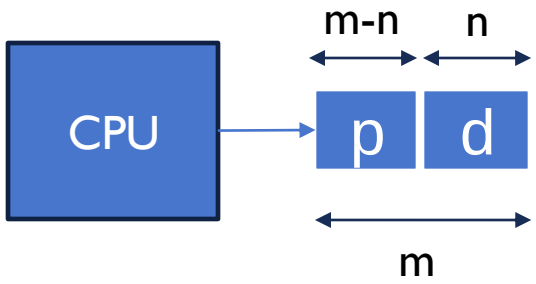

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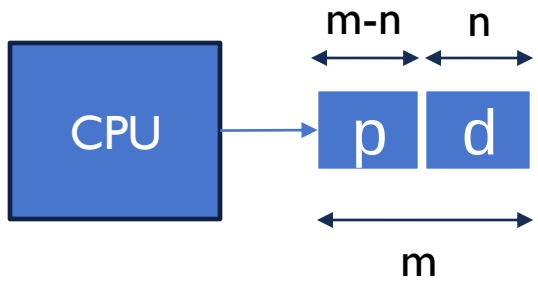

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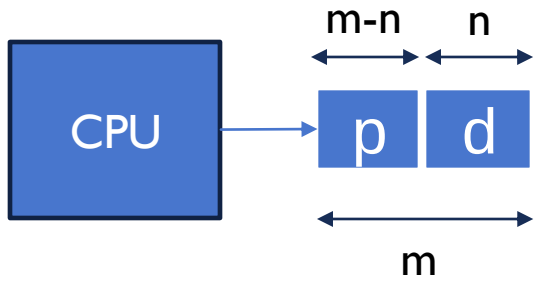

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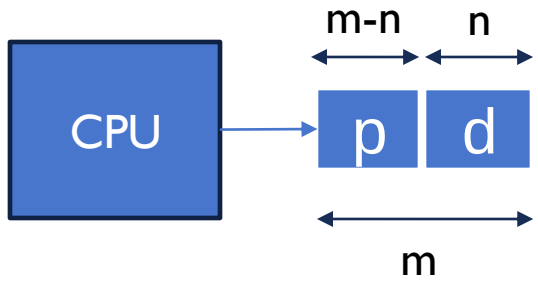

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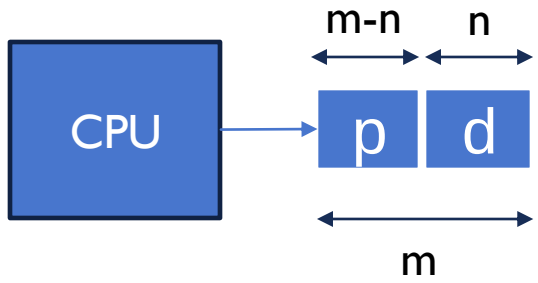

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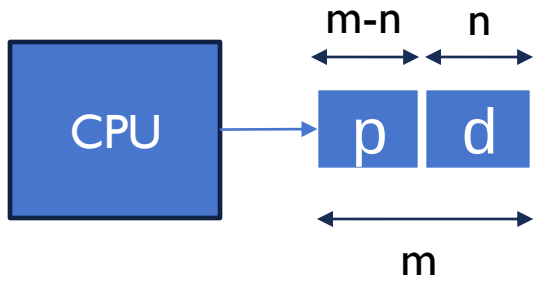
  4 bytes x 2^{23} = 2^{25} bytes= 32 MB.



PAGE TABLE LENGTH

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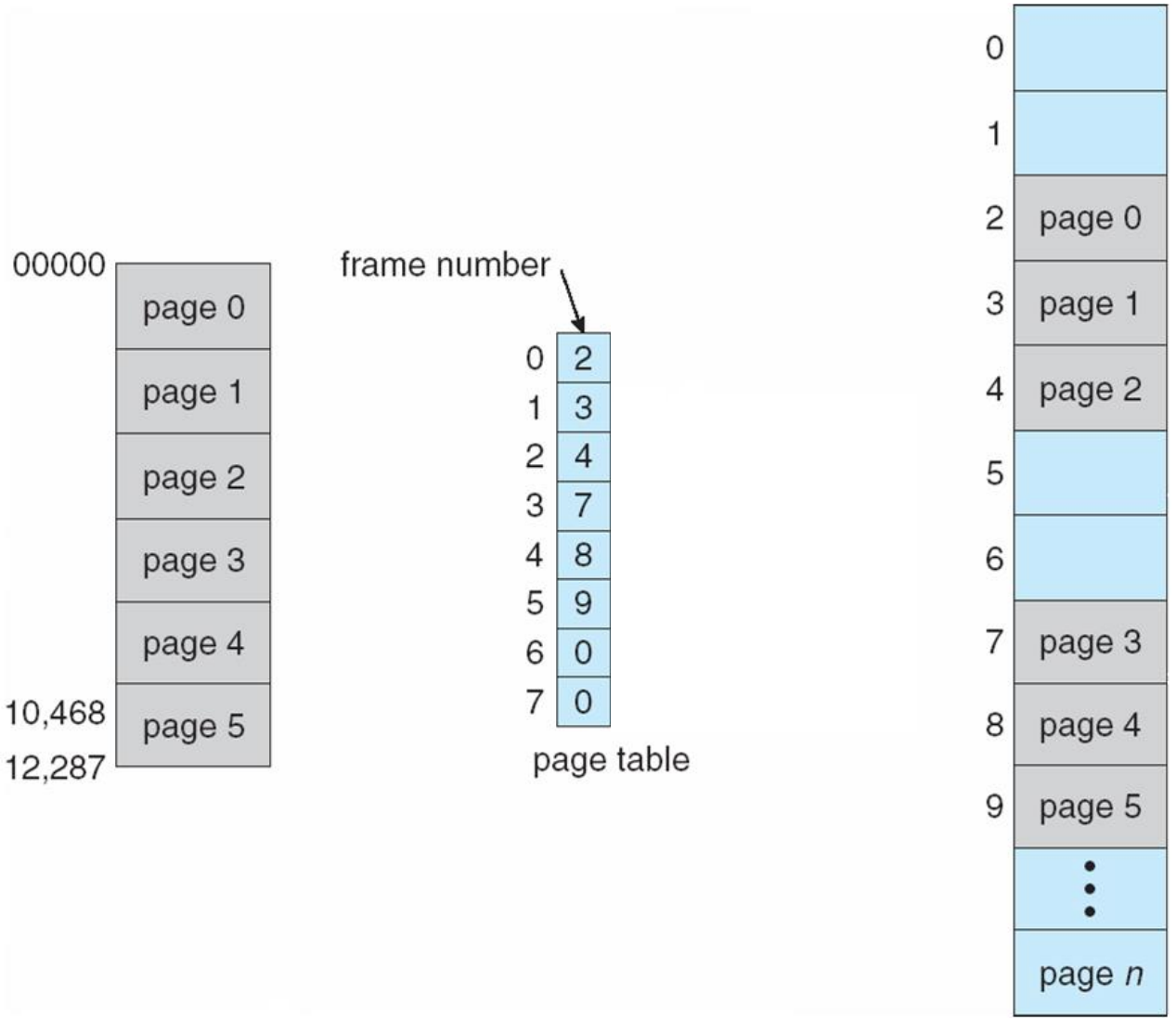
- Some page numbers in the page tables can thus be "empty".



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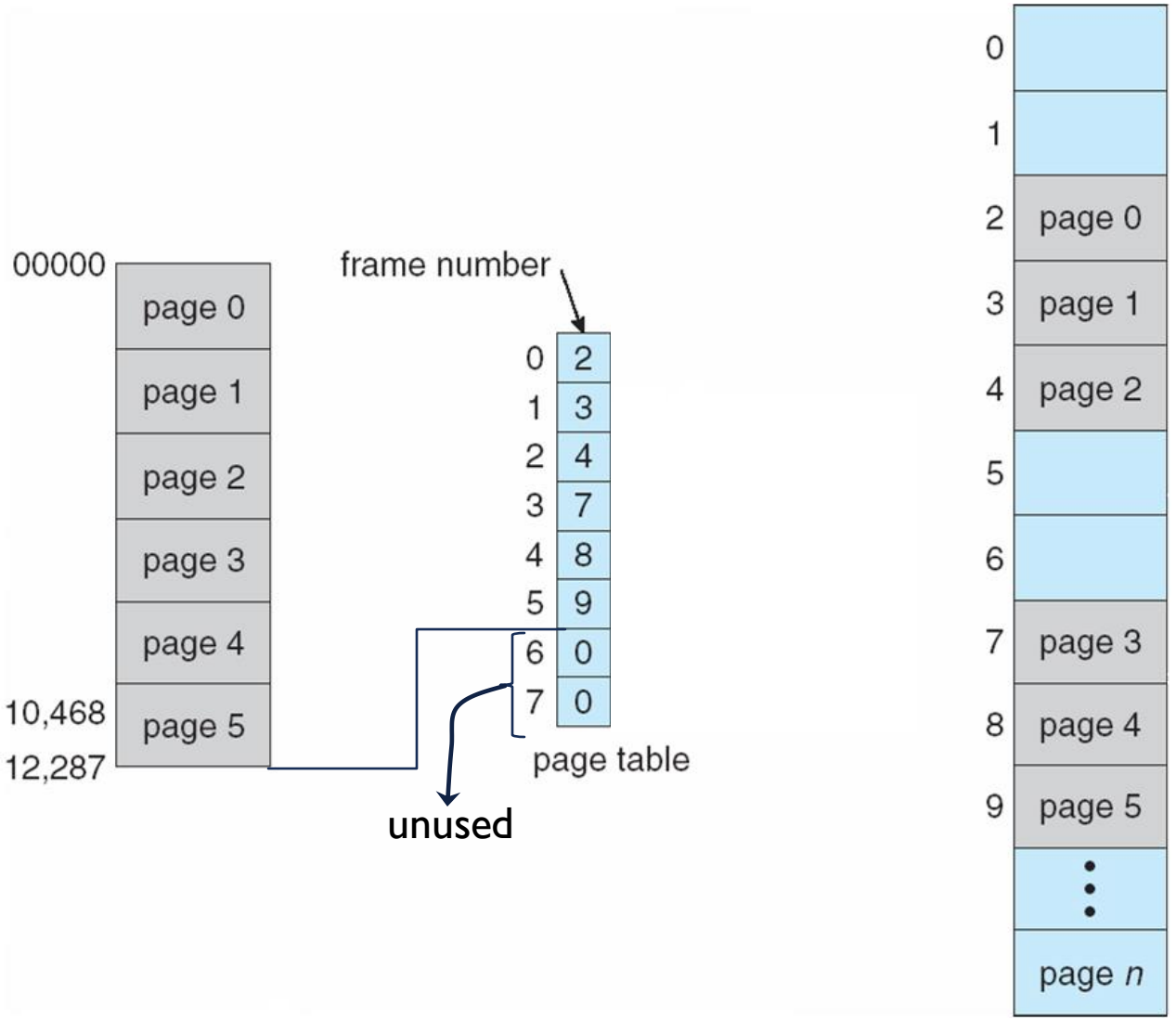

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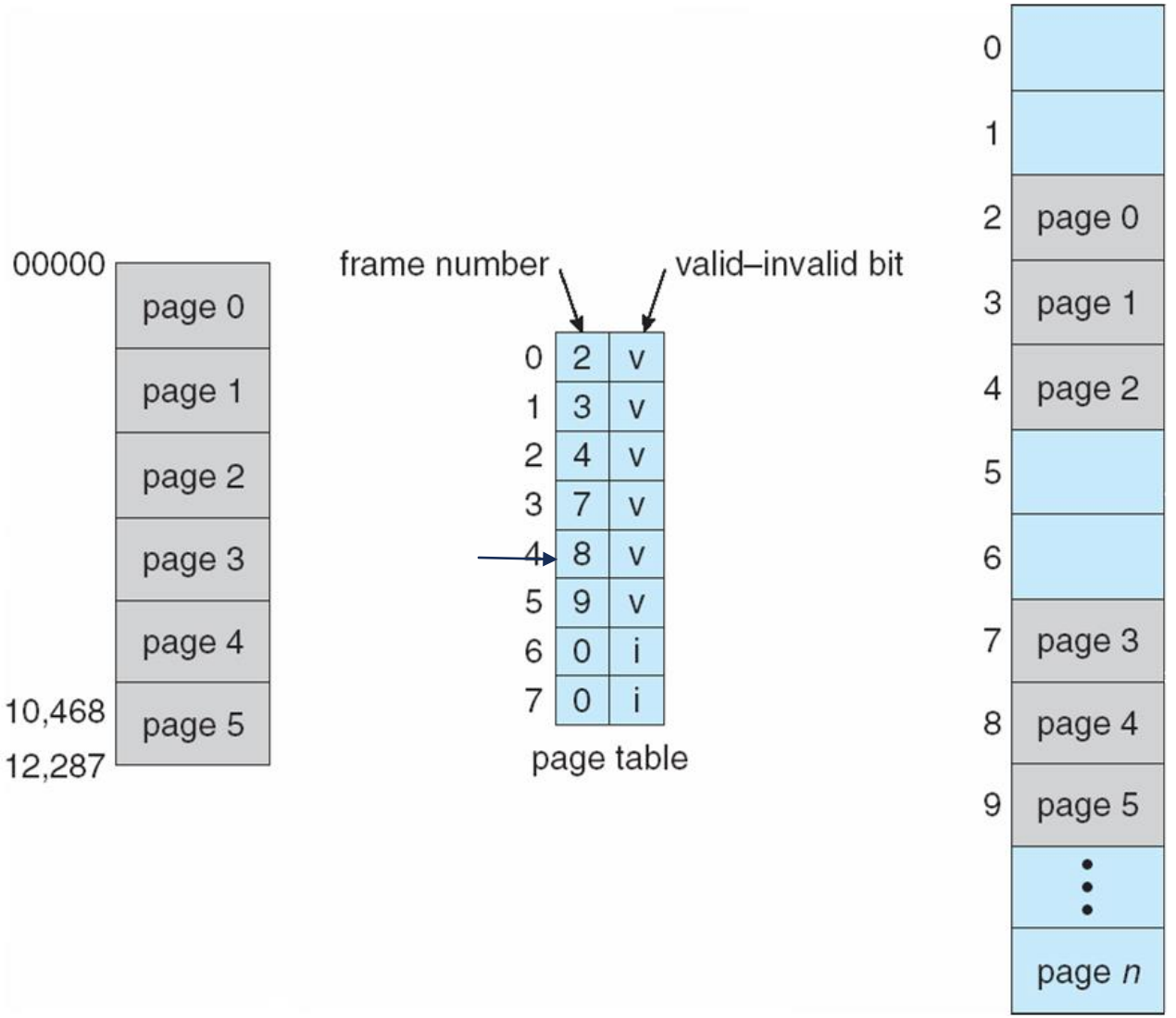

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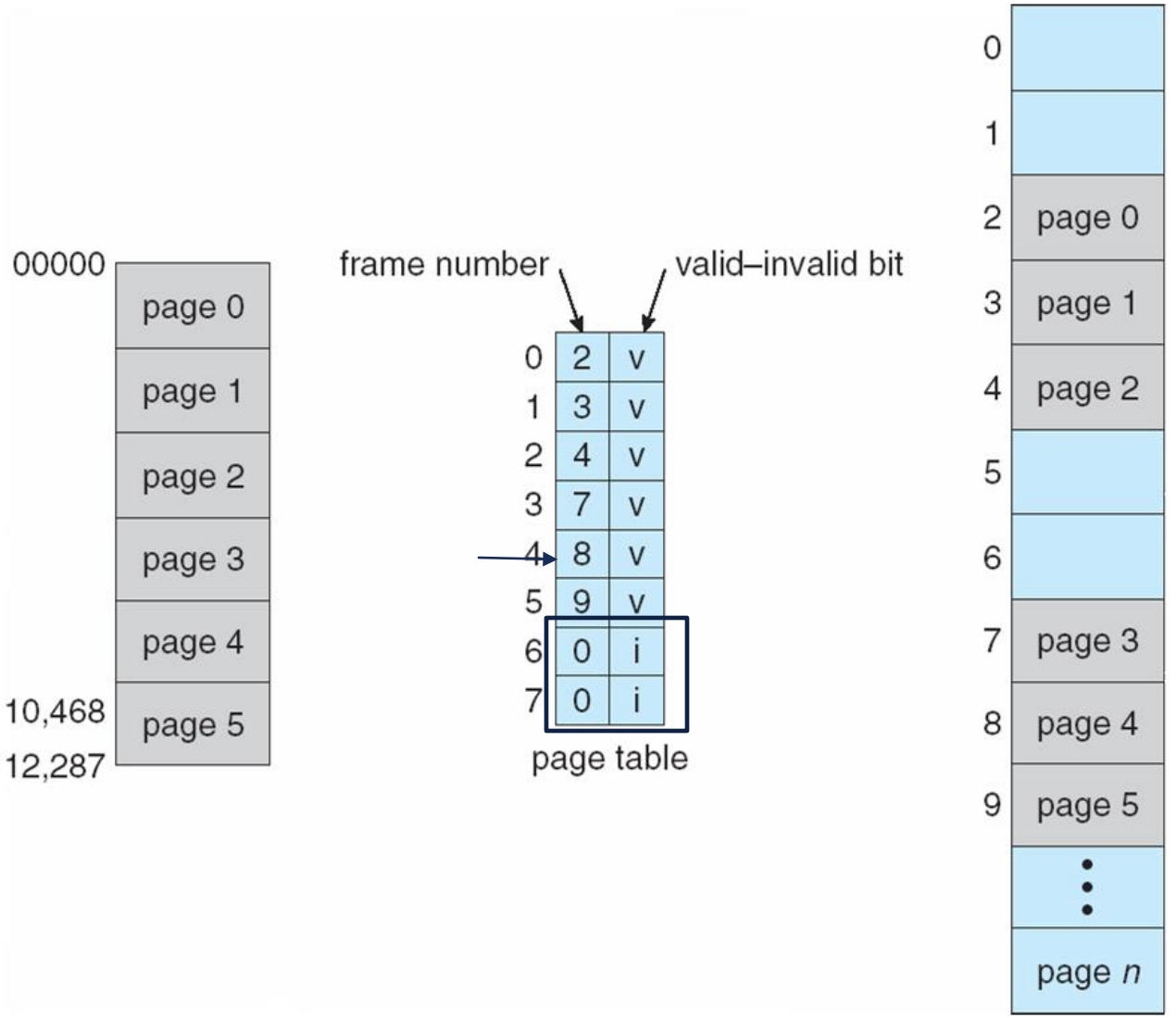

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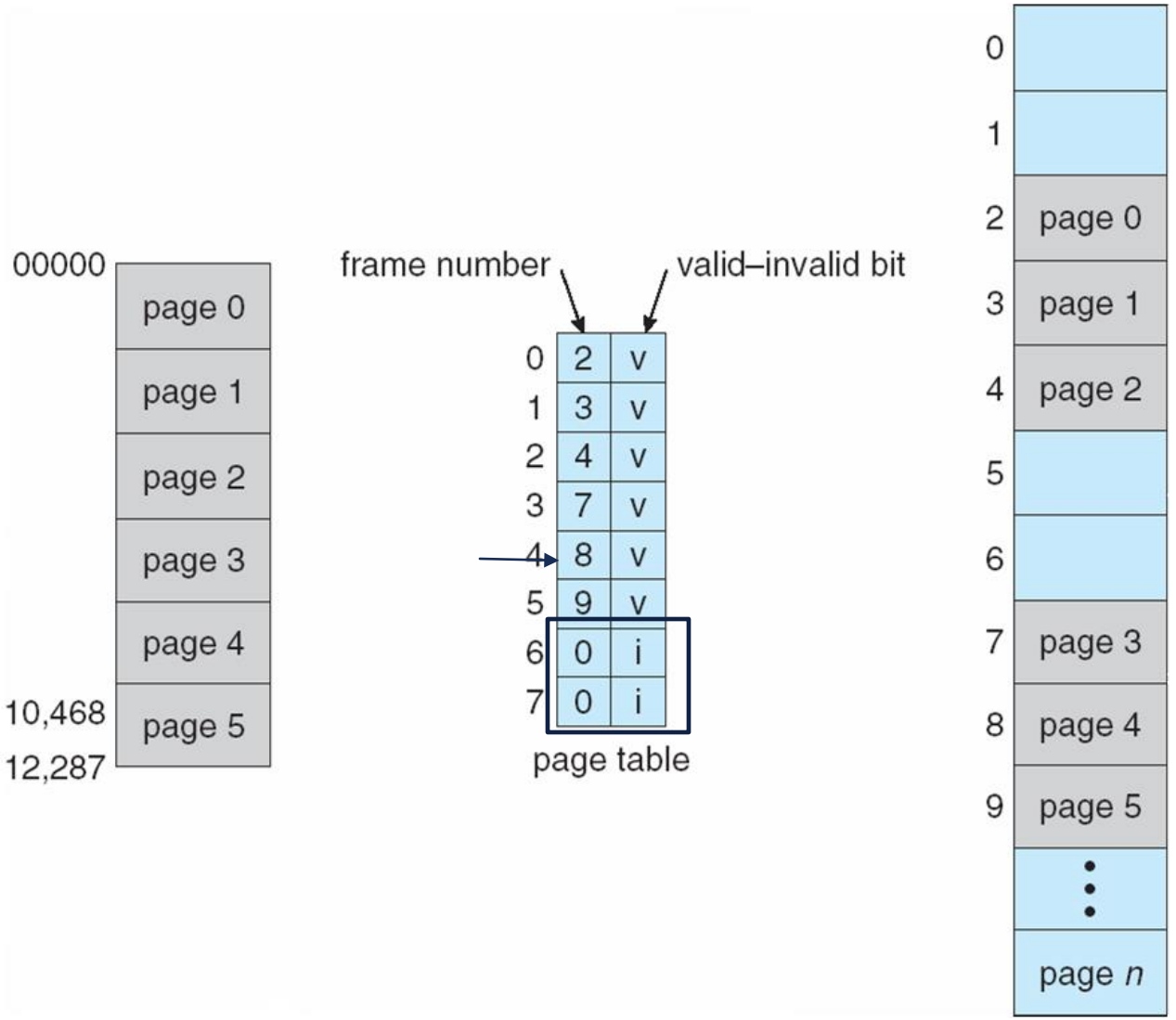
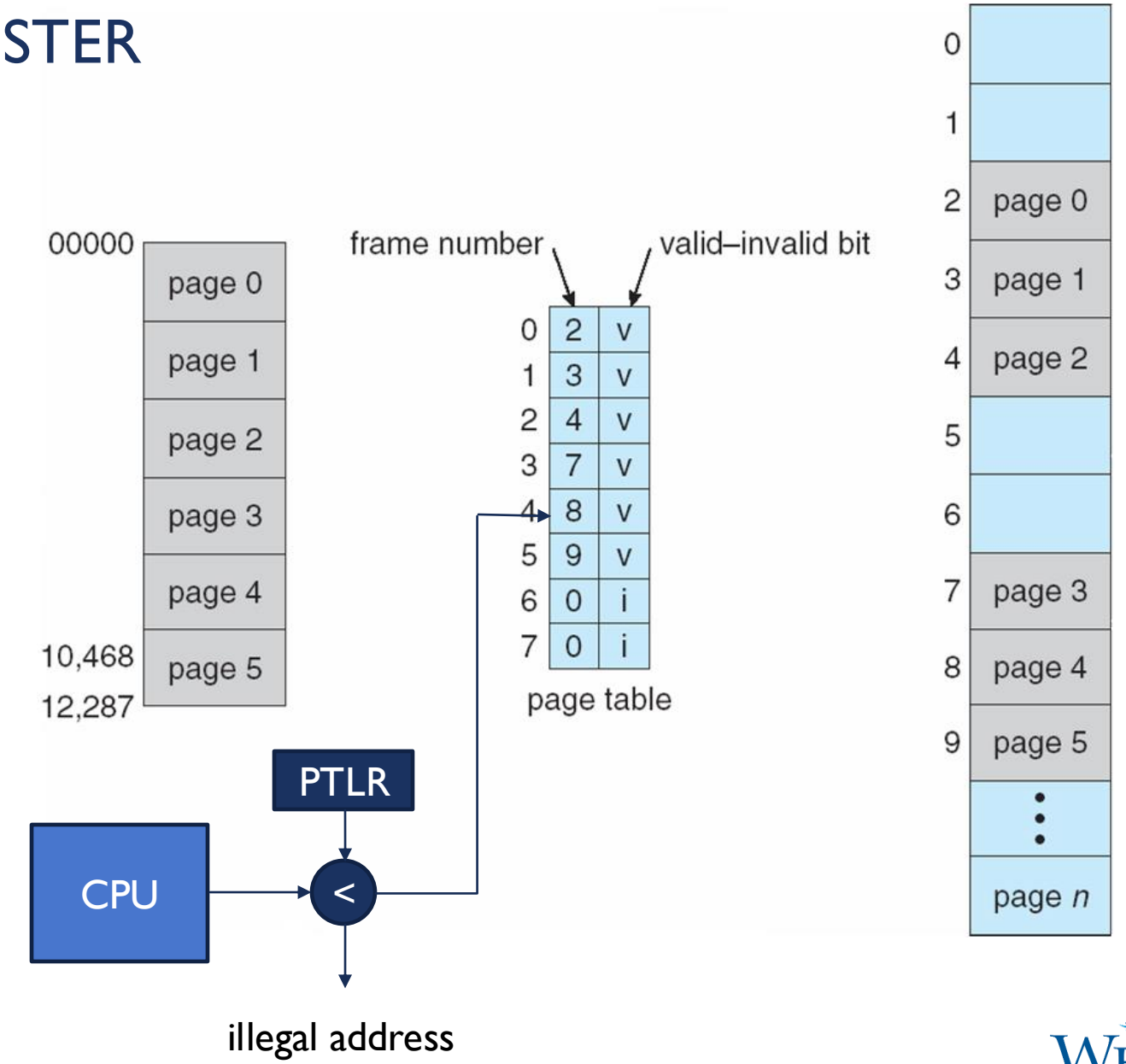
- An valid-invalid bit can be added to indicate whether a logical address is valid or not.
- Q: Disadvantage? We still have to store a table containing all the entries .. Which can be huge and wasteful.



PAGE TABLE LENGTH REGISTER

- Alternative: A Page Table Length Register (PTLR) can be used to store the length of the table instead.
- Any address issued will be compared to this register value.



PAGE TABLE LENGTH REGISTER

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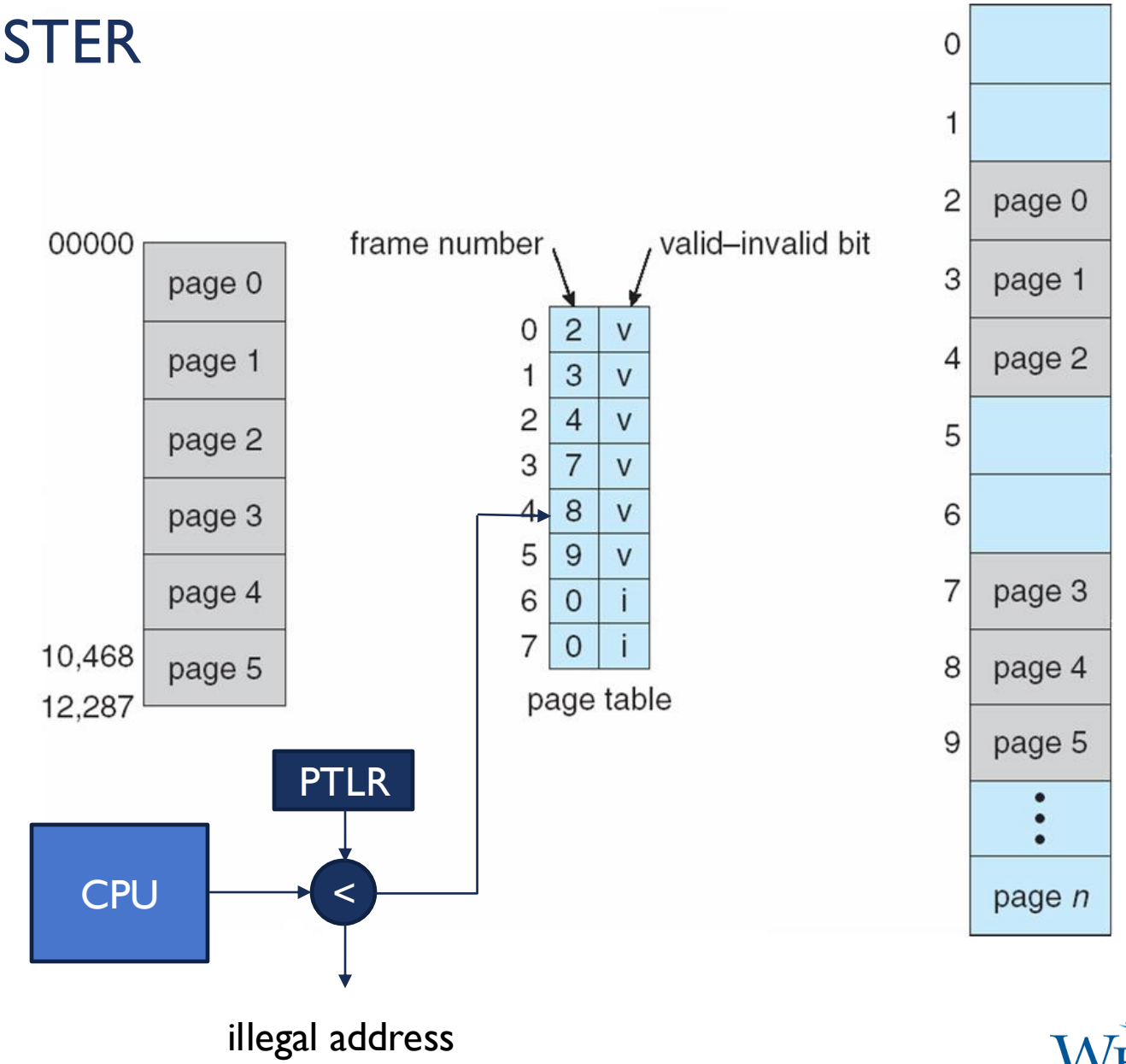
- Any address issued will be compared to this register value.
- Q: What should be the value of PTLR in this example?



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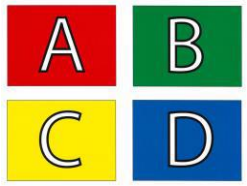
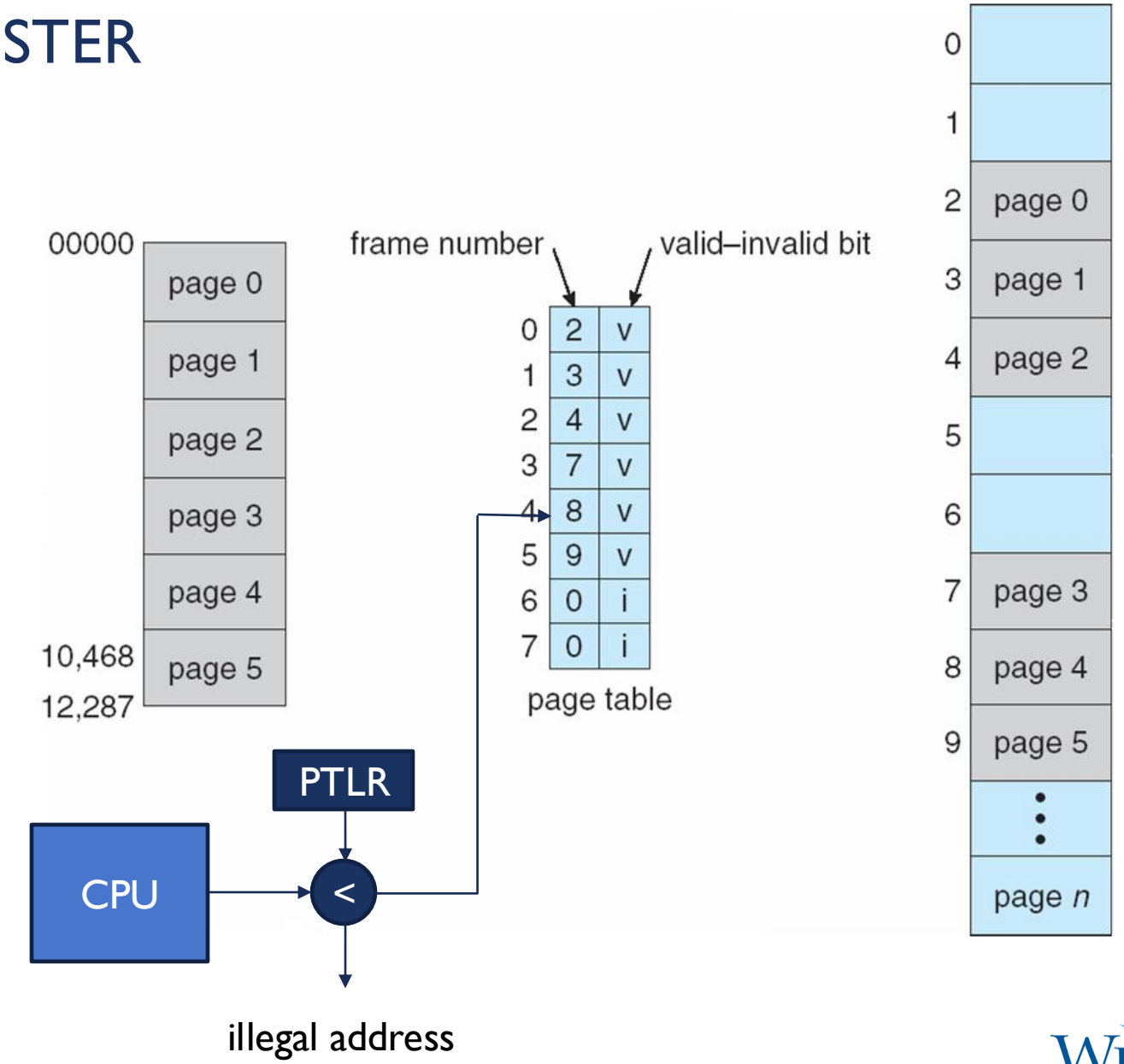


A: 5
B: 9
C: 7
D: 12,287



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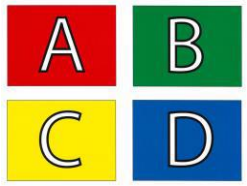

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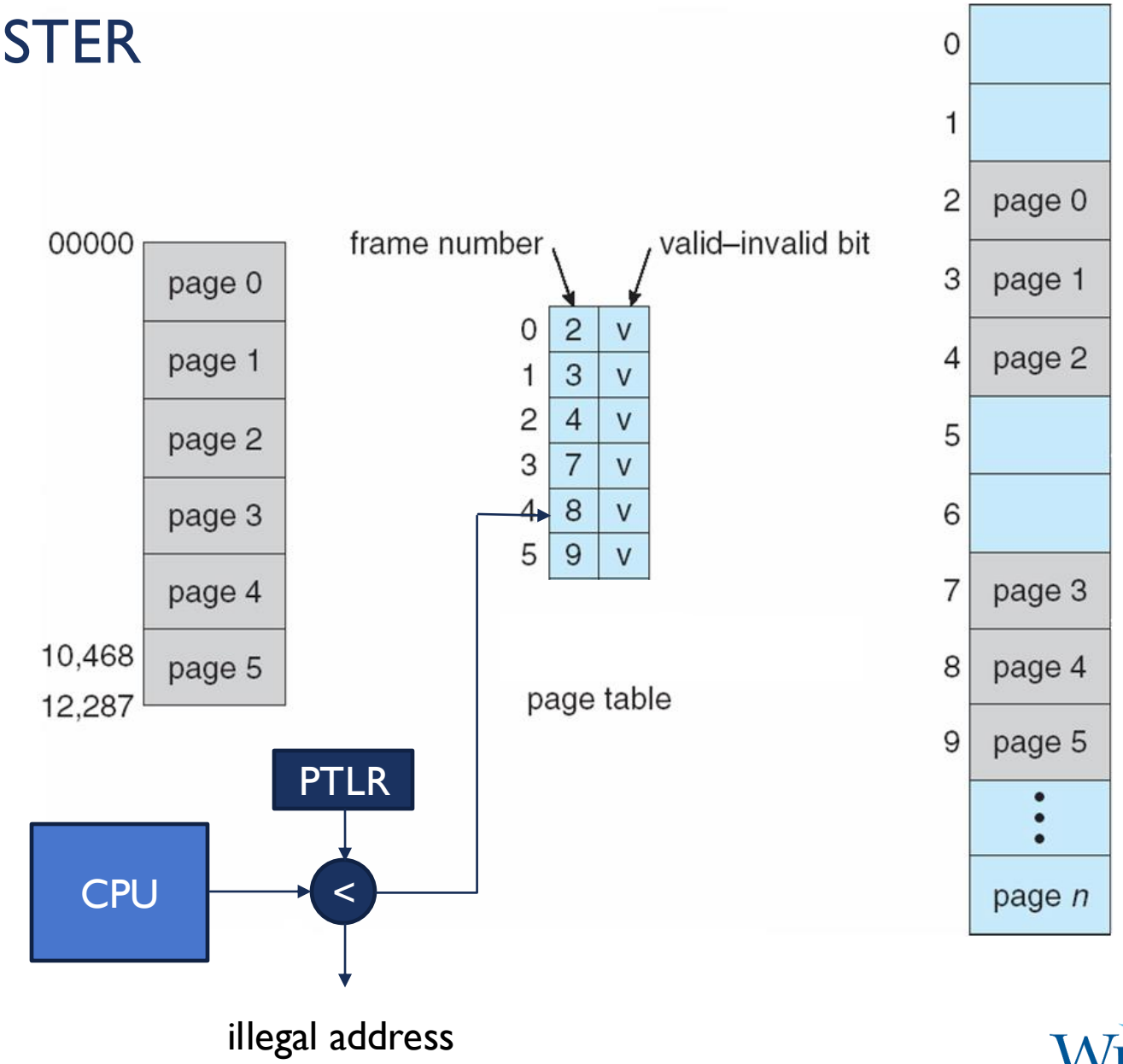
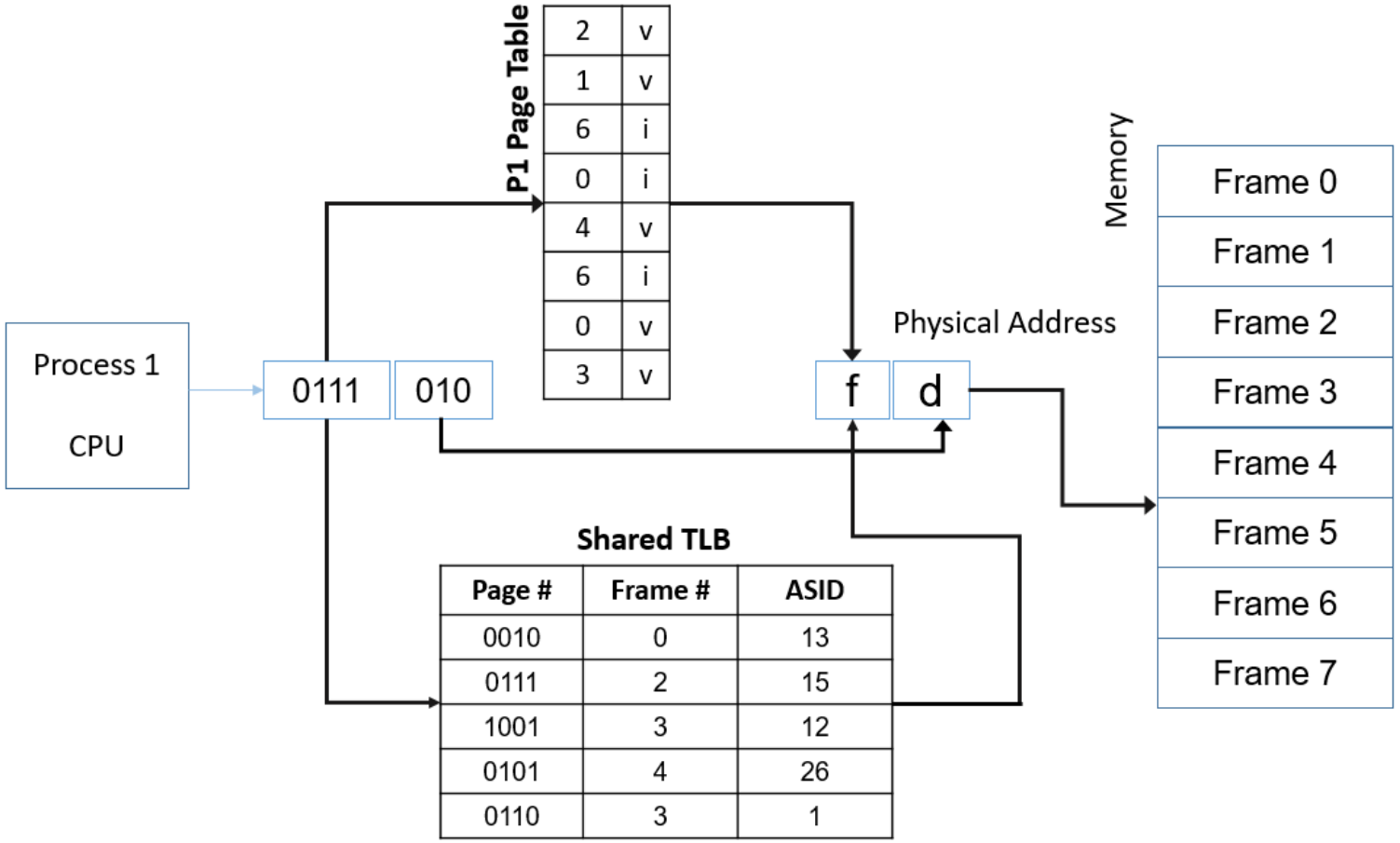


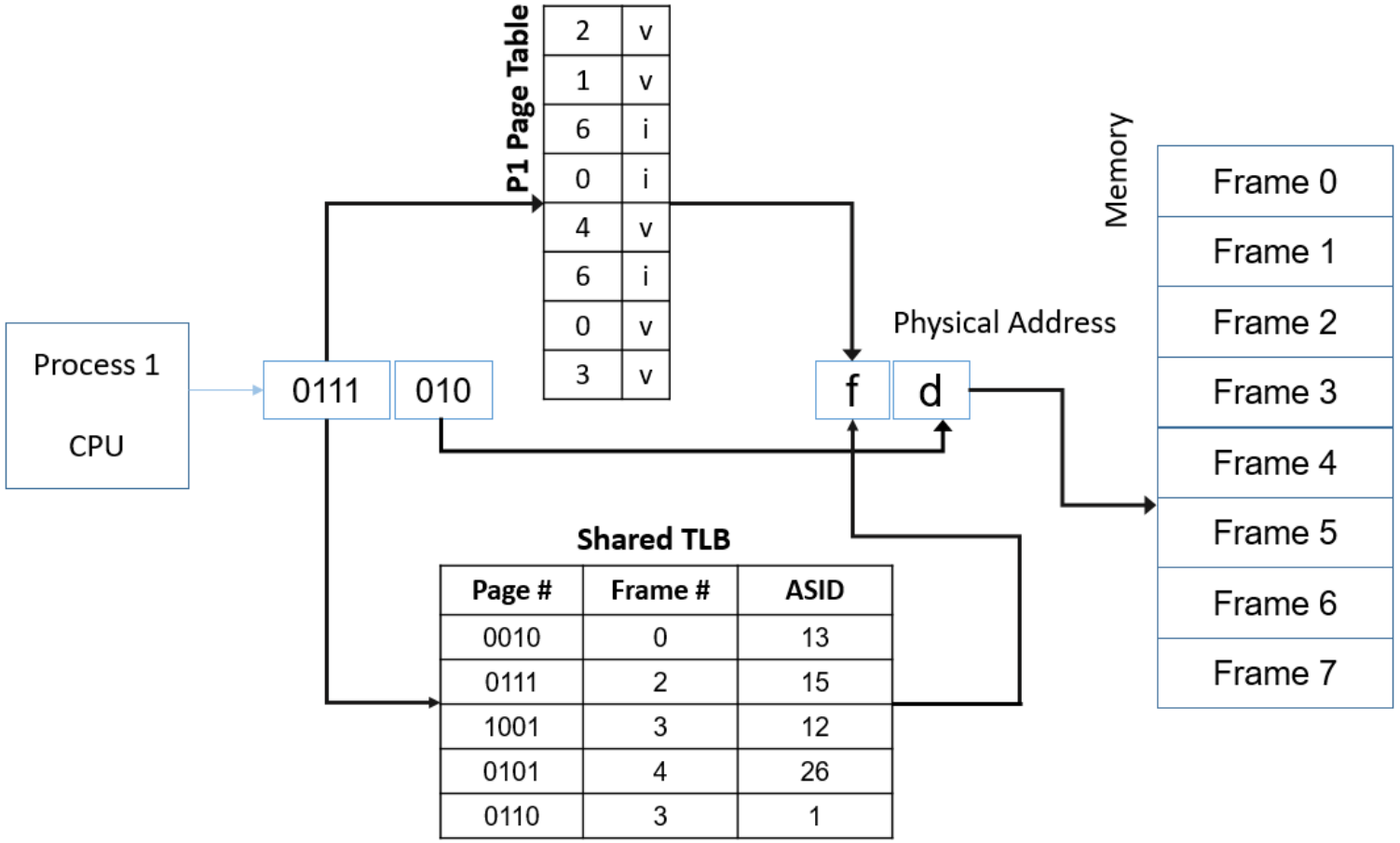
WORKSHEET Q2

- Will it cause a hit or miss at the TLB? Explain.
- Will this attempt cause a page fault? Explain.
- What is the frame number (physical frame address) retrieved? Explain.
- What byte address does the process attempt to access? Explain.



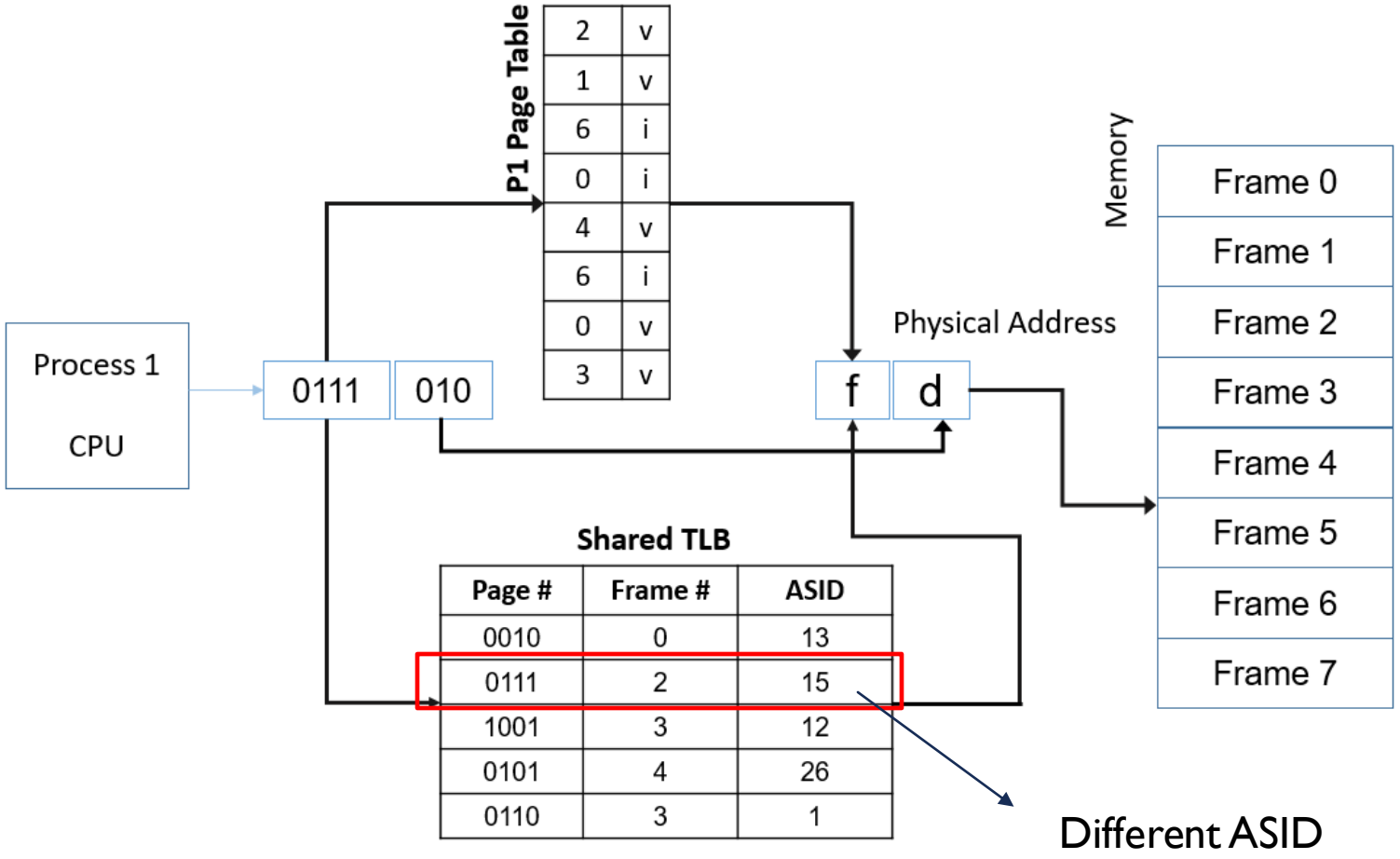
WORKSHEET Q2

- TLB Hit or Miss?



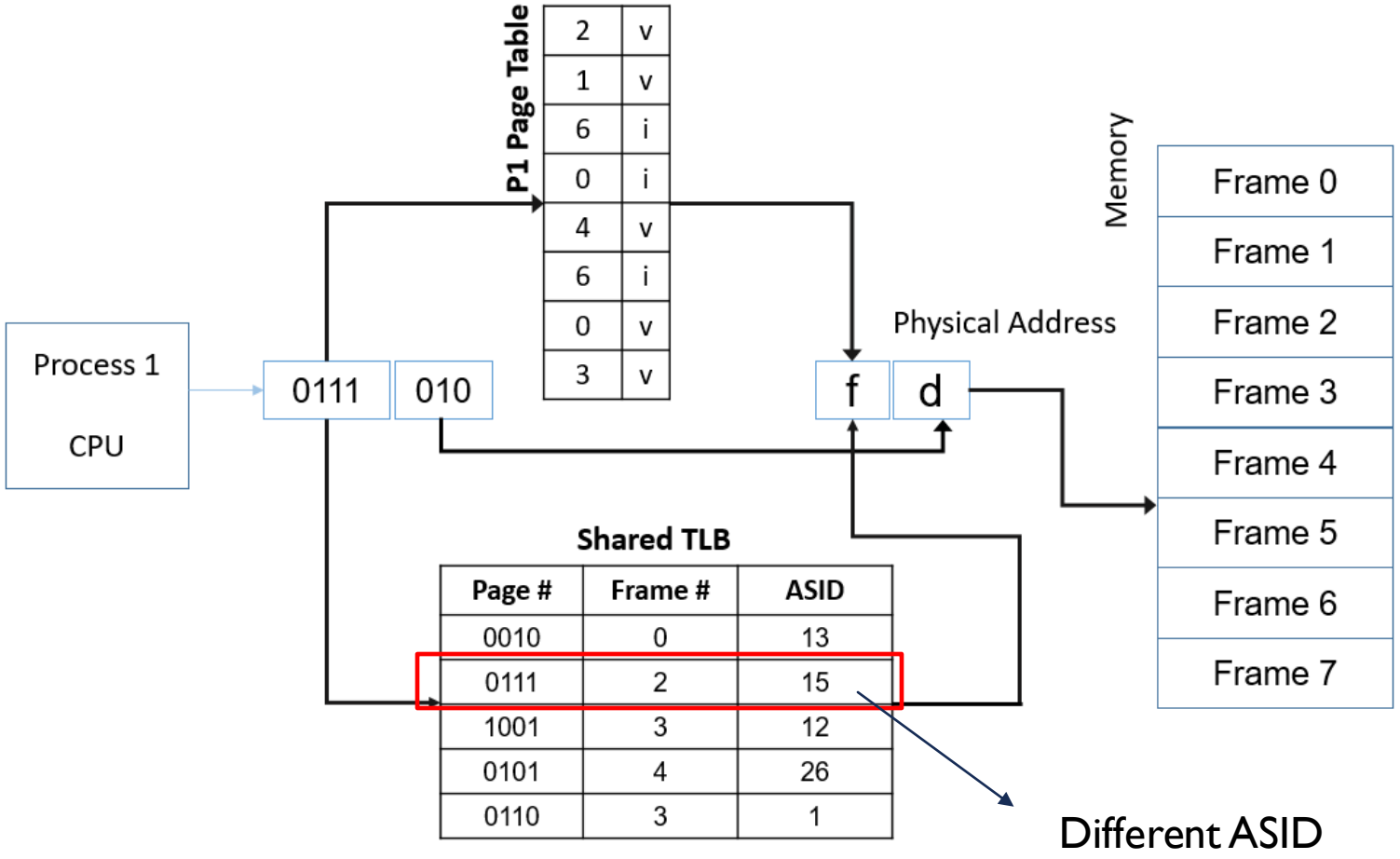
WORKSHEET Q2

- TLB Hit or Miss?



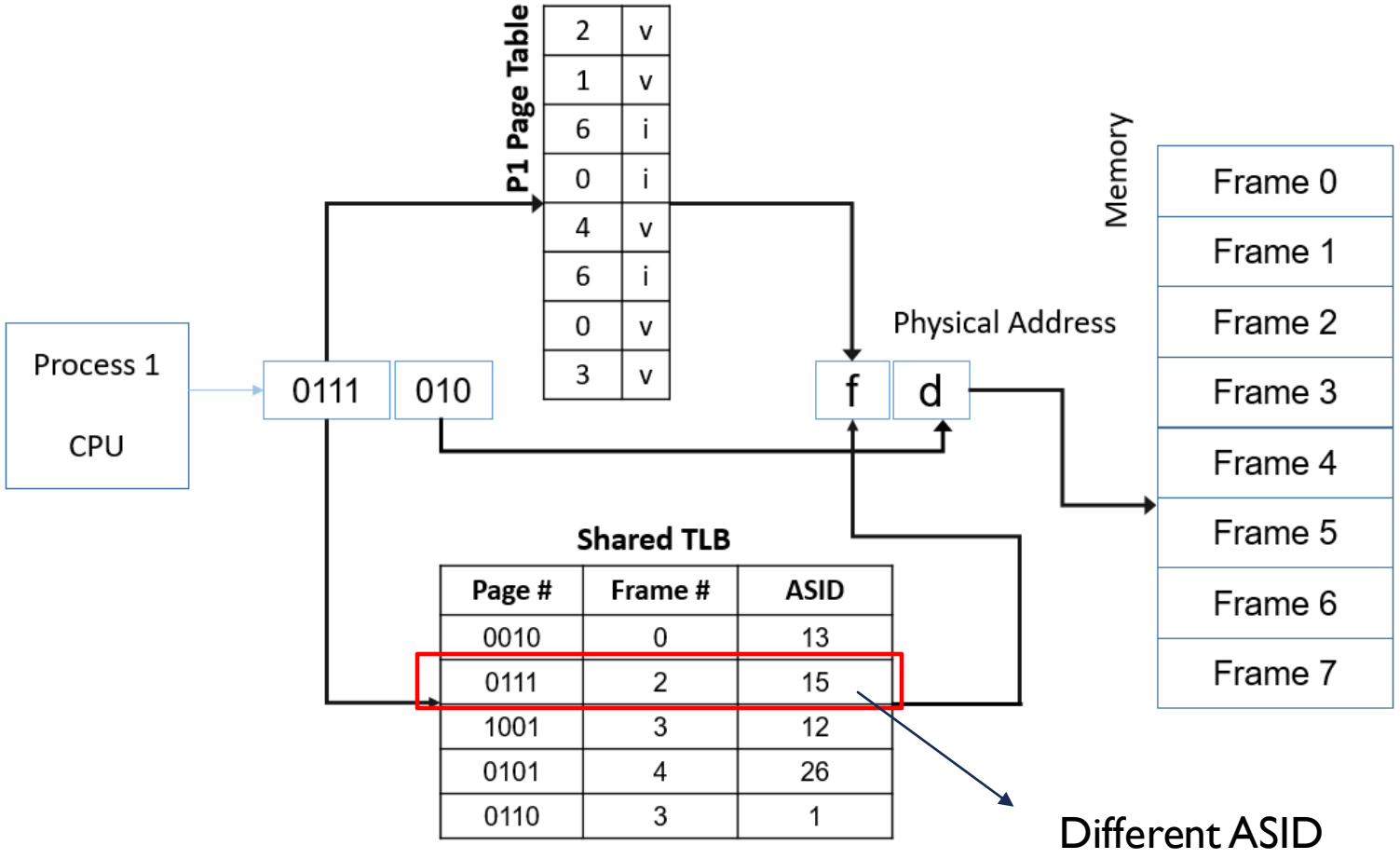
WORKSHEET Q2

- TLB Hit or Miss? Miss



WORKSHEET Q2

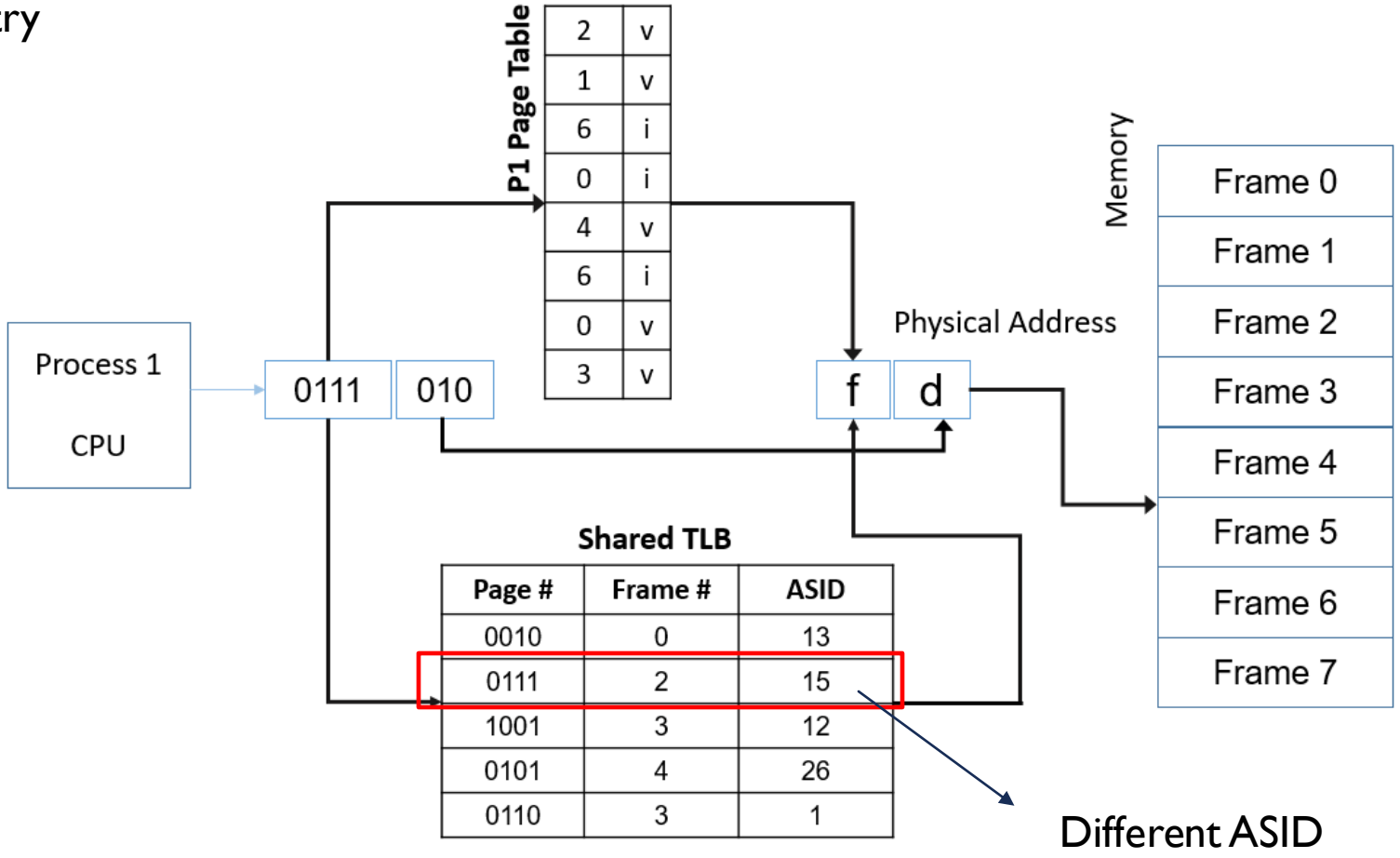
- Page Fault?



WORKSHEET Q2

0111 = 7 in decimal
Check 8th entry

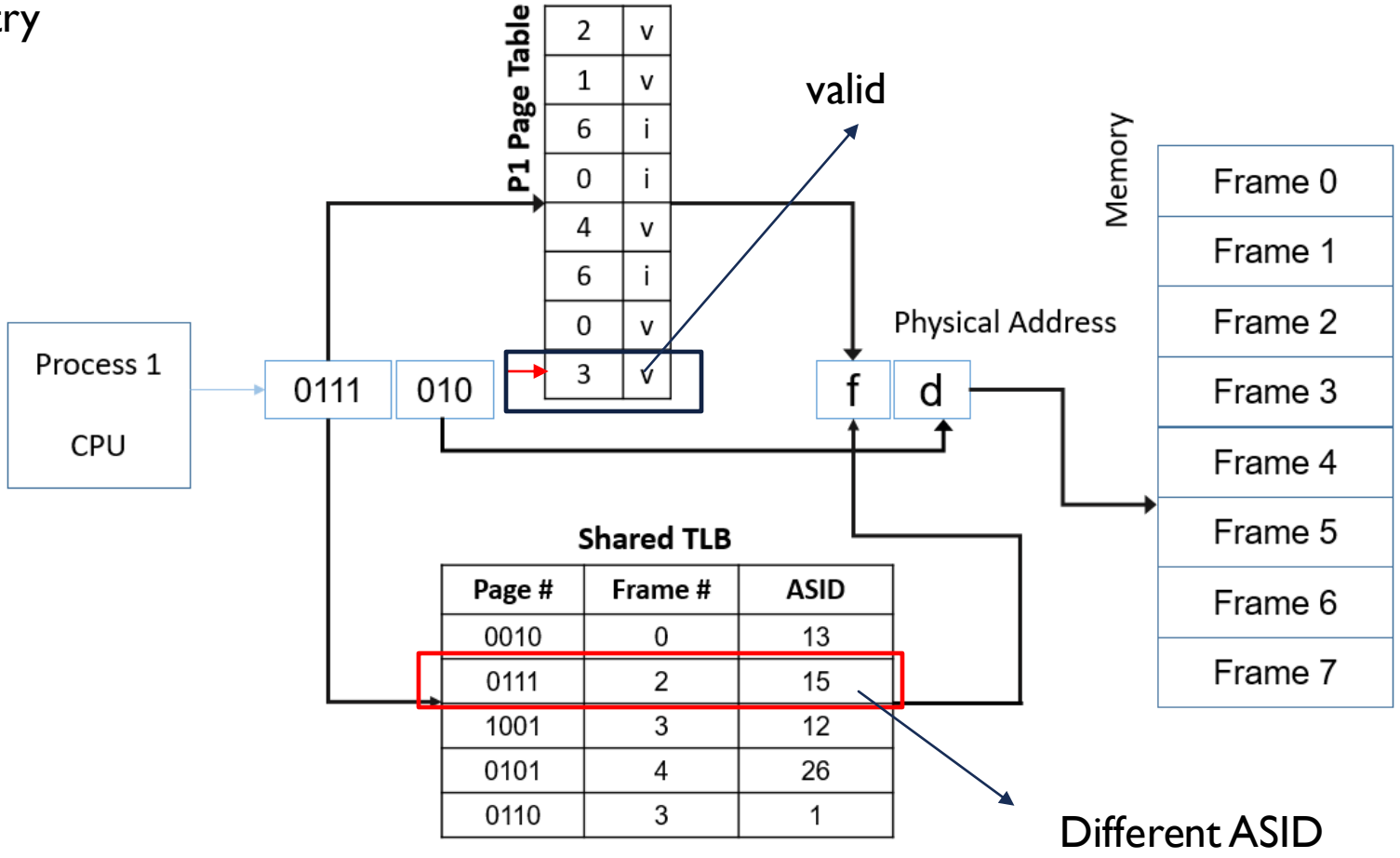
- Page Fault?



WORKSHEET Q2

0111 = 7 in decimal
Check 8th entry

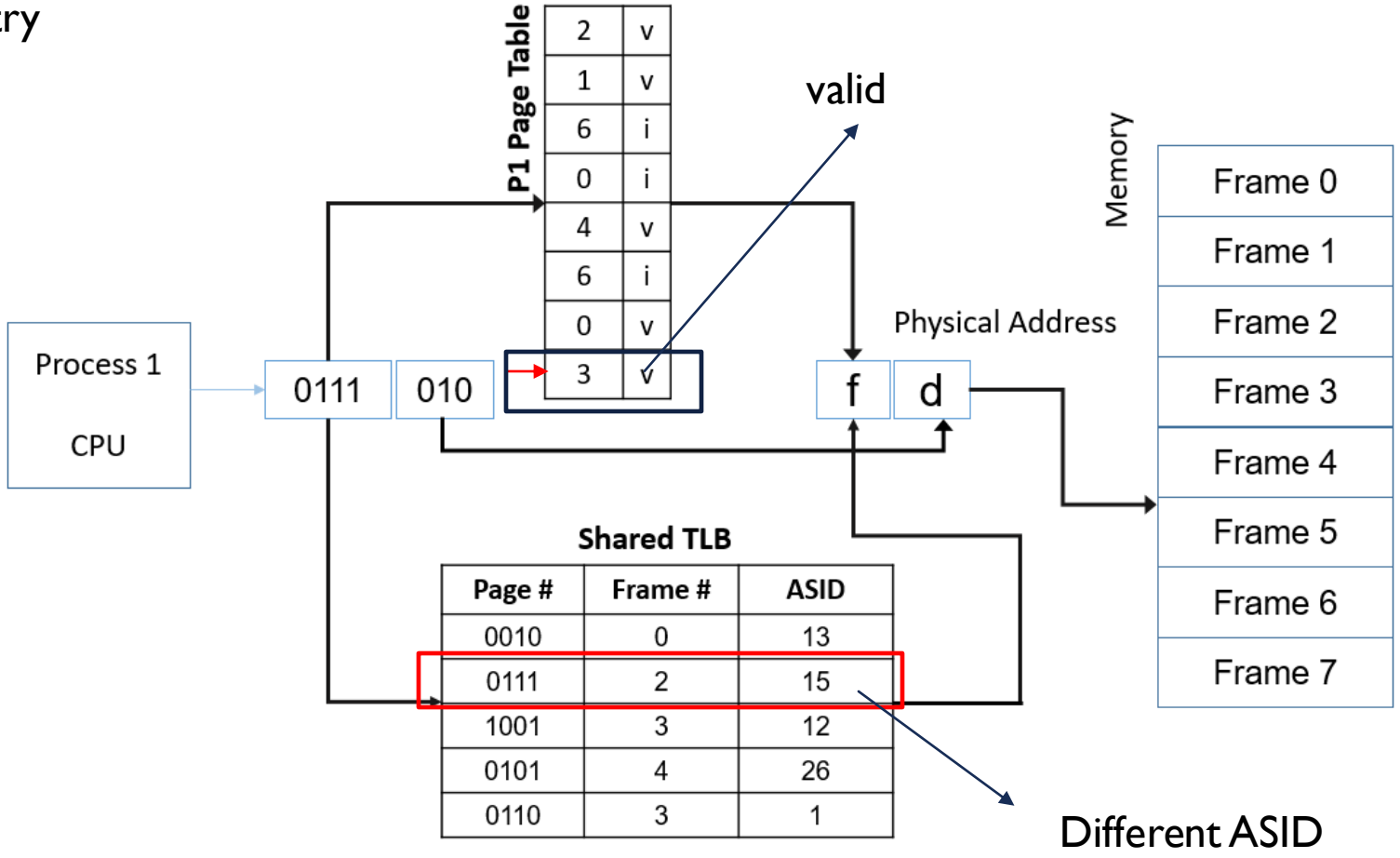
- Page Fault?



WORKSHEET Q2

0111 = 7 in decimal
Check 8th entry

- Page Fault? No page fault!



WORKSHEET Q2

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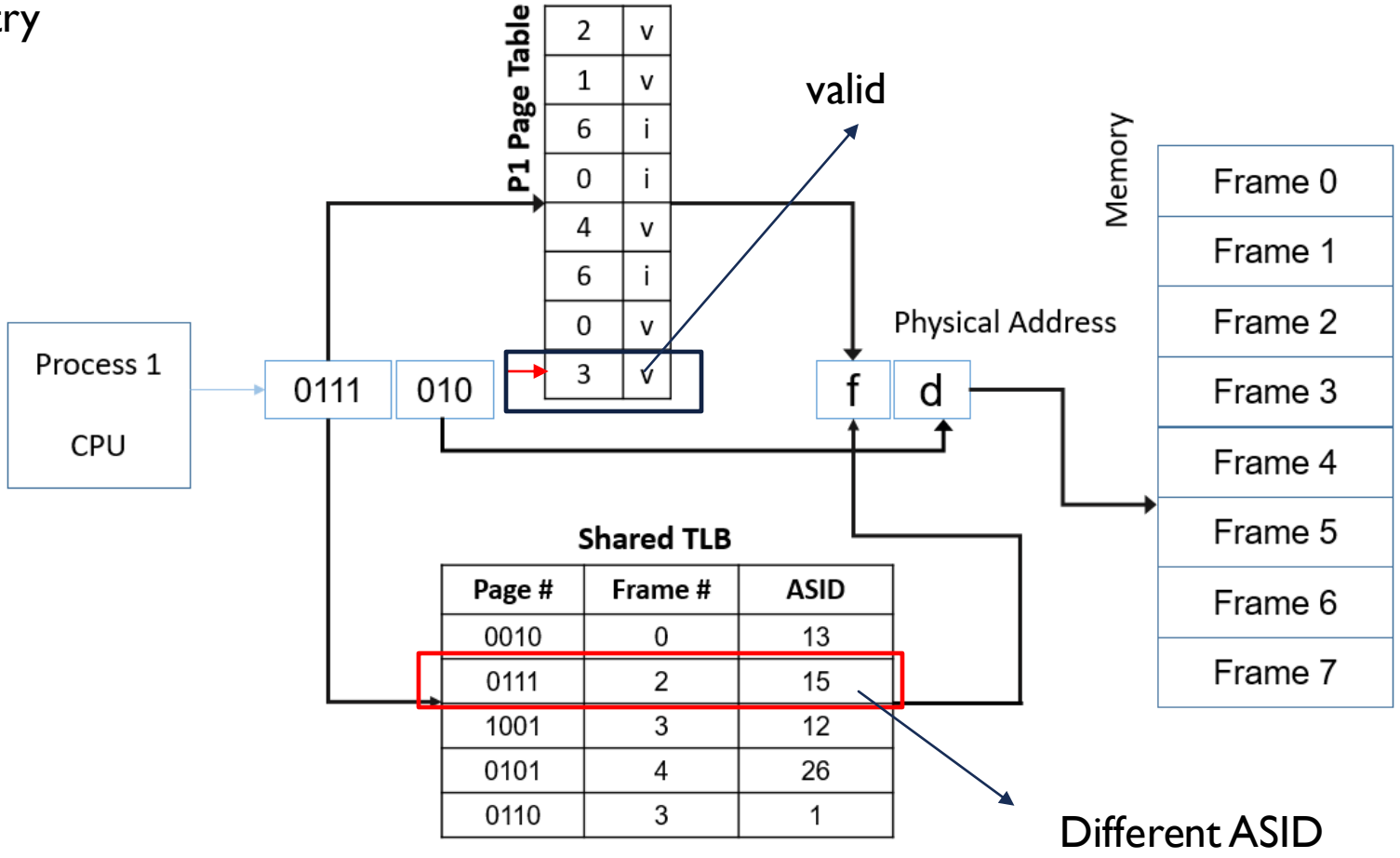
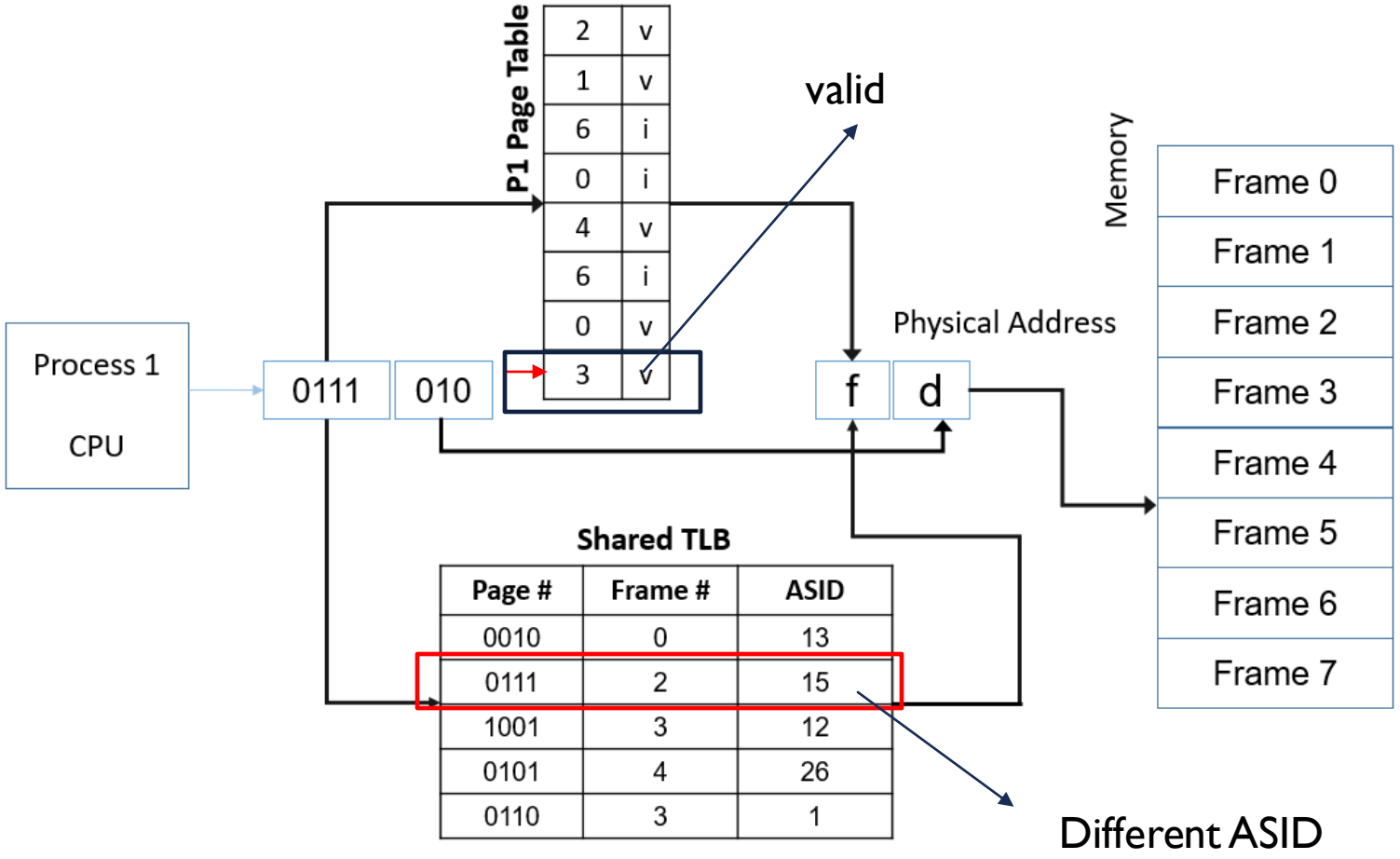


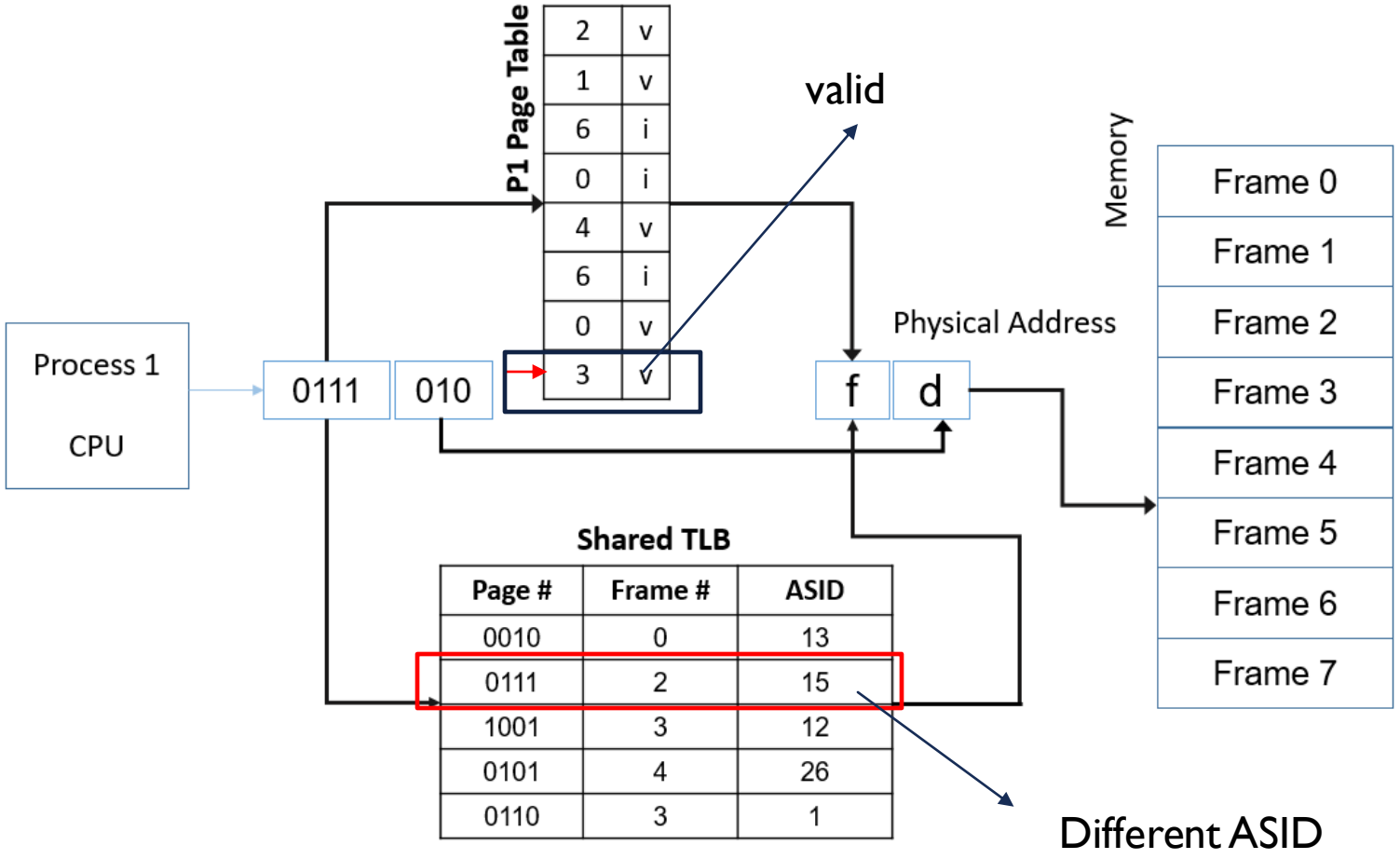
WORKSHEET Q2

- Frame retrieved?



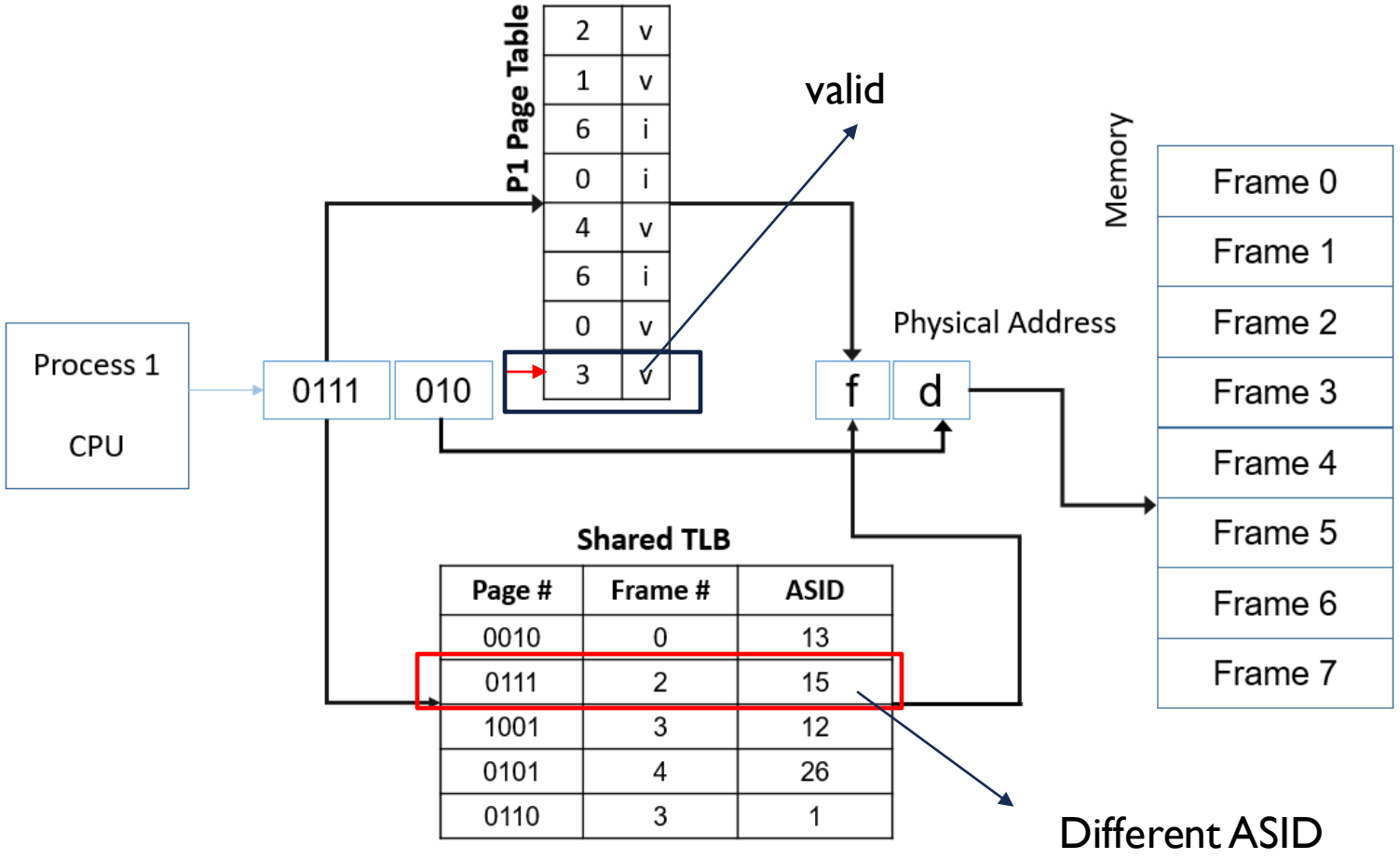
WORKSHEET Q2

- Frame retrieved? Frame #3



WORKSHEET Q2

- Byte offset in the physical address?



WORKSHEET Q2

- Byte offset in the physical address?
- Same as logical: 010