Documentation of PSpice Schematic Circuit

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Circuit Description

This document provides detailed information on the schematic circuit designed and simulated in PSpice. The schematic was created to analyze the behavior of a difference detector circuit which has an inbuilt difference amplifier as its key component. Assume a situation where, we have to analyze the behavior of 2 independent sensors which are sending data simultaneously in a noisy environment. So, both the signals must have a certain noise level added to them in form of an offset or low frequency jitter. Our circuit would be used to detect both of these noisy signals and compare them on a real time basis.

The primary components include:

- **Resistors:** 50k, 31.83k, 14k, 9k, 5k and 1k ohms.
- **Capacitors:** 0.1uF.
- **Operational Amplifiers/ICs:** TL084 and LM318.
- **Supply/Sources:** +15(VDD), -15(VSS) and 2 other sources have been kept to imitate the sensor output voltages.

Working of the Circuit

Let's understand how the circuit works. The first stage is a difference amplifier configuration of two operational amplifiers, commonly known as an Instrumentation Amplifier. The gain expression for an Instrumentation Amplifier is given by:

$$V_{\text{out}} = (V_2 - V_1)\left(1 + \frac{2R_2}{R_{\text{gain}}}\right)\frac{R_4}{R_3} \tag{1}$$

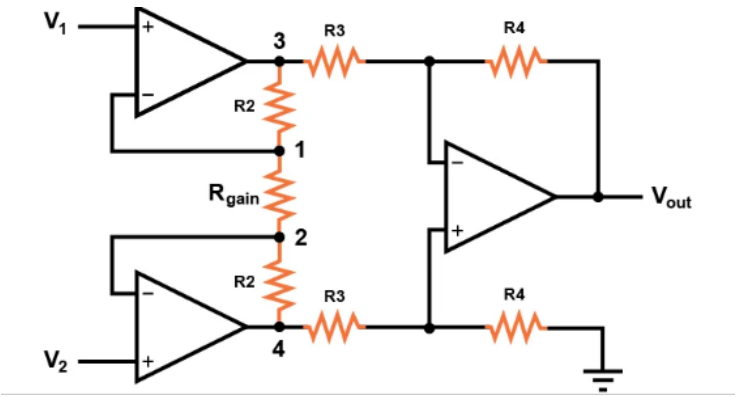

Figure 1: Instrumentation Amplifier

So, we find that R_2 is nothing but equal to R_{out1} and R_{out2}. Also, R_4 and R_3 are equal as per the schematic attached, so the gain expression reduces to:

$$V_{\text{out}} = (V_2 - V_1)\left(1 + \frac{2R_2}{R_{\text{gain}}}\right) \tag{2}$$

This simplifies further to:

$$V_{\text{out}} = (V_2 - V_1) \times 101 \tag{3}$$

Thus, the difference voltage is amplified by a factor of 101.

Then, a buffer stage has been used before the filter stage in order to prevent any loading. In the third stage, we have used an RC low-pass filter to limit the transmission to 50Hz only. In the fourth stage, a non-inverting amplifier with a gain of 10 has been installed to bring up the signal strength to a voltage level.

In the fifth and sixth stages, an inverting Schmitt trigger and an inverting amplifier have been used, with threshold limits of +1 and -1 volts, to indicate when the difference is positive and when the difference is negative.

Circuit Schematic

Below is the schematic of the circuit designed in PSpice:

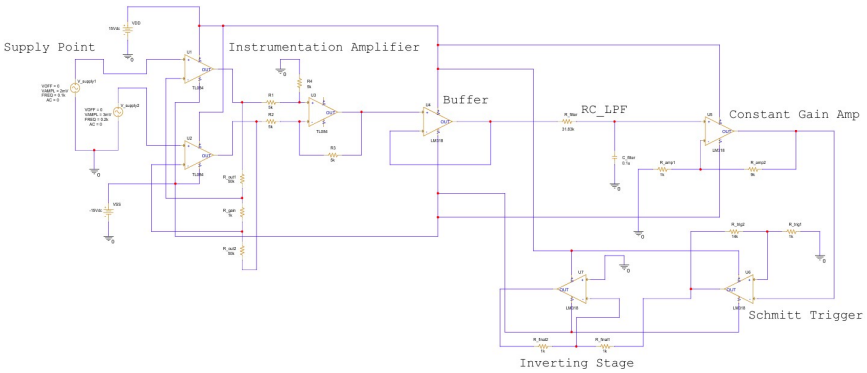

Figure 2: Schematic of the Circuit Designed in PSpice

Simulation Results

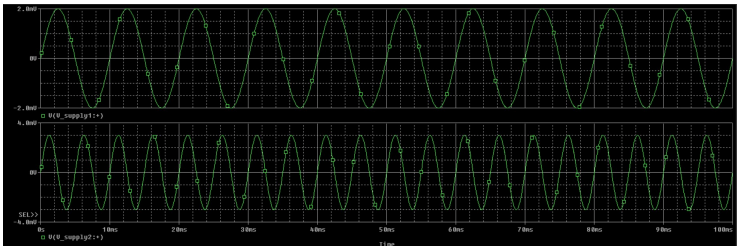

Figure 3: Input Signals

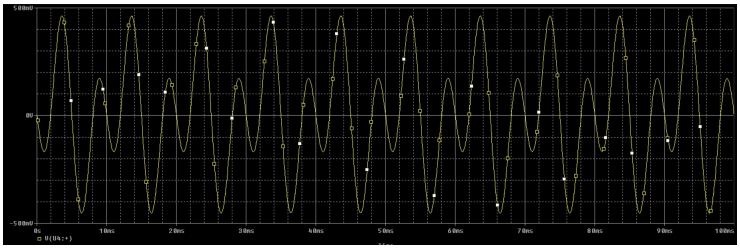

Figure 4: Title for Image 2

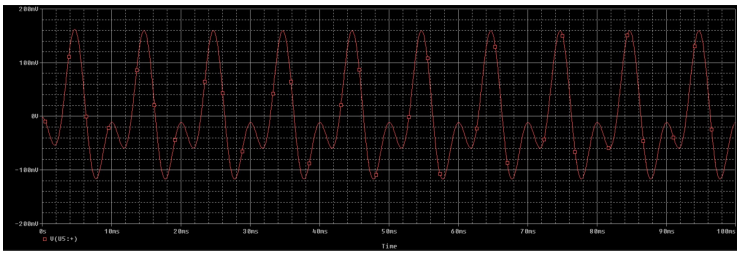

Figure 5: RC LPF Output

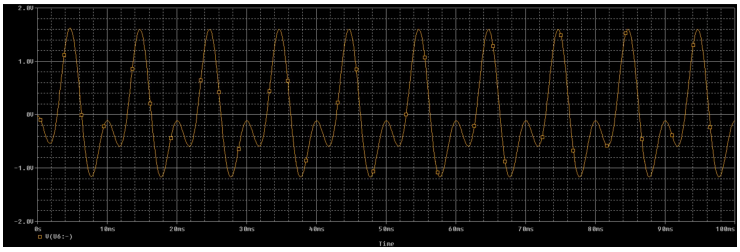

Figure 6: Schmitt Trigger Input

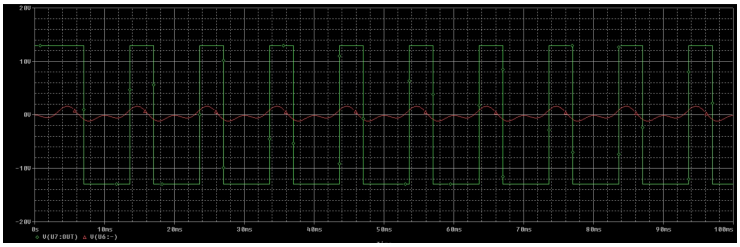

Figure 7: Final Triggered Input and Output

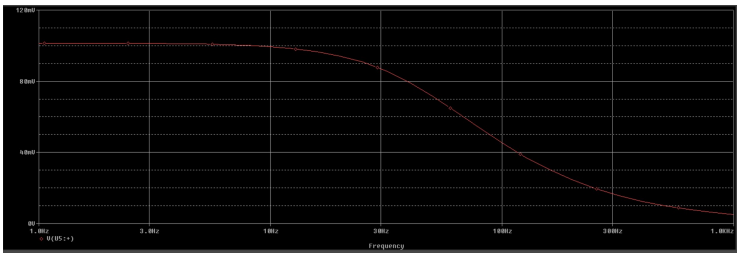

Figure 8: Frequency Response Analysis

Limitations

The circuit works well for any set of input signals where the offset is same or it is an equally noisy environment. However, if the noise levels added to the signal offset are un-equal, the final output may saturate heavily and the comparison can't be made. So, pls take a note of this before running the simulation.

Conclusion

In conclusion, the PSpice simulation validated the design, showing that the circuit operates within expected parameters