Features

- **Fast Read Access Time - 45 ns**
- **Low-Power CMOS Operation**
  - **100 µA max. Standby**
  - **25 mA max. Active at 5 MHz**
- **JEDEC Standard Packages**
  - **32-Lead 600-mil PDIP**
  - **32-Lead PLCC**
  - **32-Lead TSOP**
- **5V ± 10% Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial, Industrial and Automotive Temperature Ranges**

Description

The AT27C010 is a low-power, high-performance 1,048,576-bit one-time programmable read only memory (OTP EPROM) organized as 128K by 8 bits. They require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

In read mode, the AT27C010 typically consumes only 8 mA. Standby mode supply current is typically less than 10 µA.

(continued)

Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

PLCC Top View
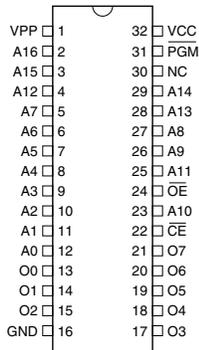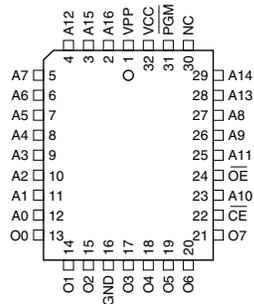
PDIP Top View

TSOP Top View

Type 1
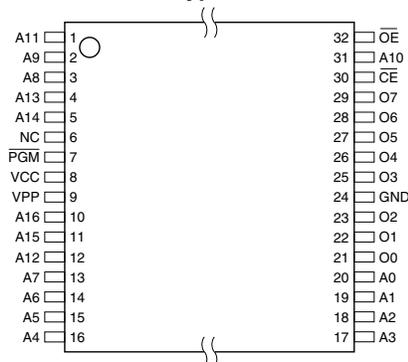
1-Megabit (128K x 8) OTP EPROM

AT27C010

The AT27C010 is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and TSOP packages. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With 128K byte storage capability, the AT27C010 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C010 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram
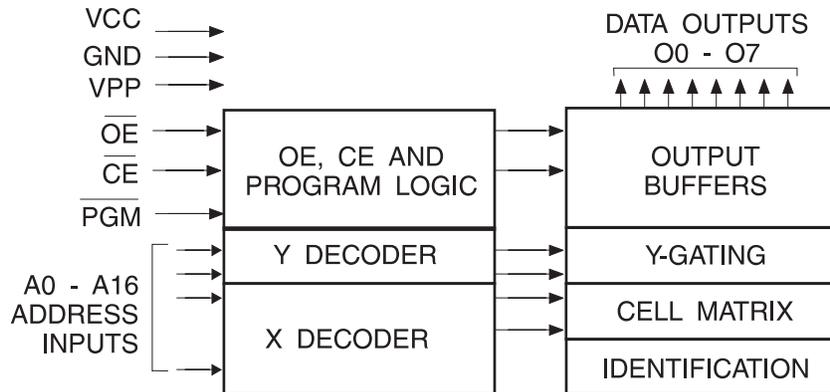
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V[1]
Voltage on A9 with Respect to Ground	-2.0V to +14.0V[1]
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

Mode\Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X[1]	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X	High Z
Rapid Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification[4]	V_{IL}	V_{IL}	X	A9 = V_H[3] A0 = V_{IH} or V_{IL} A1 - A16 = V_{IL}	X	Identification Code

Note: 1. X can be V_{IL} or V_{IH}.

2. Refer to Programming Characteristics.

3. V_H = 12.0 ± 0.5V.

4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C010		
		-45	**-70**	**-90**
Operating Temp. (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Auto.			-40°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}	Com., Ind.		± 1	µA
			Auto.		± 5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	Com., Ind.		± 5	µA
			Auto.		±10	µA
IPP1[2]	V_{PP}[1] Read/Standby Current	V_{PP} = V_{CC}			10	µA
I_{SB}	V_{CC}[1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}			25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C010						
			-45		**-70**		**-90**		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Units
t_{ACC}[3]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		45		70		90	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		70		90	ns
t_{OE}[2][3]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		30		35	ns
t_{DF}[4][5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		25		25	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		0		ns

Note: 1. 2,3,4,5. - see AC Waveforms for Read Operation.

AC Waveforms for Read Operation[(1)]
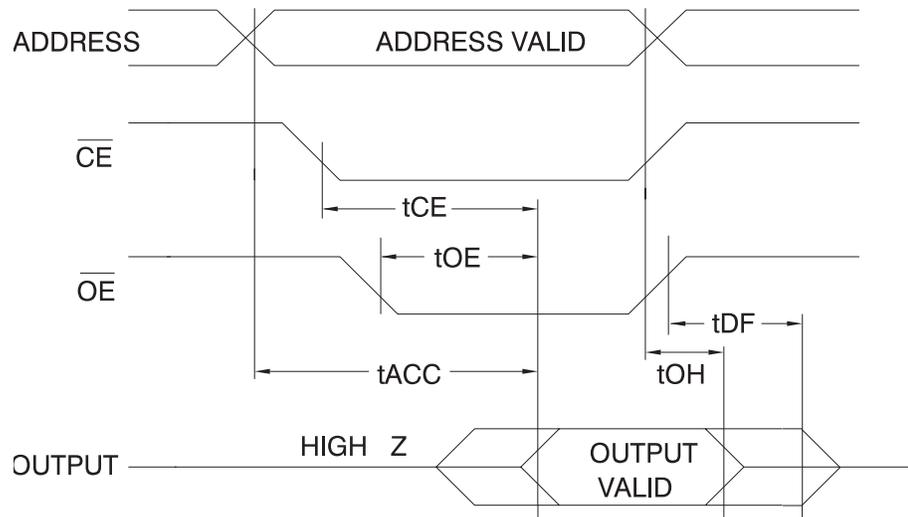

Note: 1. Timing measurement reference level is 1.5V for -45 devices. Input AC drive levels are $V_{IL} = 0.0V$ and $V_{IH} = 3.0V$. Timing measurement reference levels for all other speed grades are $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$. Input AC drive levels are $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$.

2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels

For -45 devices only:

t_R, t_F < 5 ns (10% to 90%)

For -70 and -90 devices:

t_R, t_F < 20 ns (10% to 90%)

Output Test Load

```
          1.3V

          ┬
          ▽  (1N914)

          ┴  3.3K
OUTPUT    ∿
 PIN      ┬  ▷
          ┴  CL
          │
          ▽
```
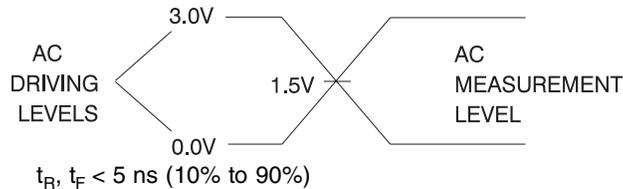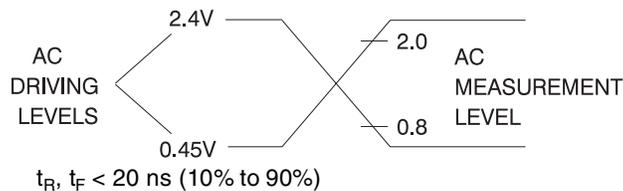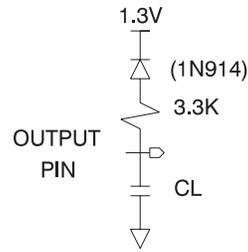
Note: C_L = 100 pF including jig capacitance, except for the -45 devices, where C_L = 30 pF.

Pin Capacitance

f = 1 MHz, T = 25°C[Note:]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms[1]
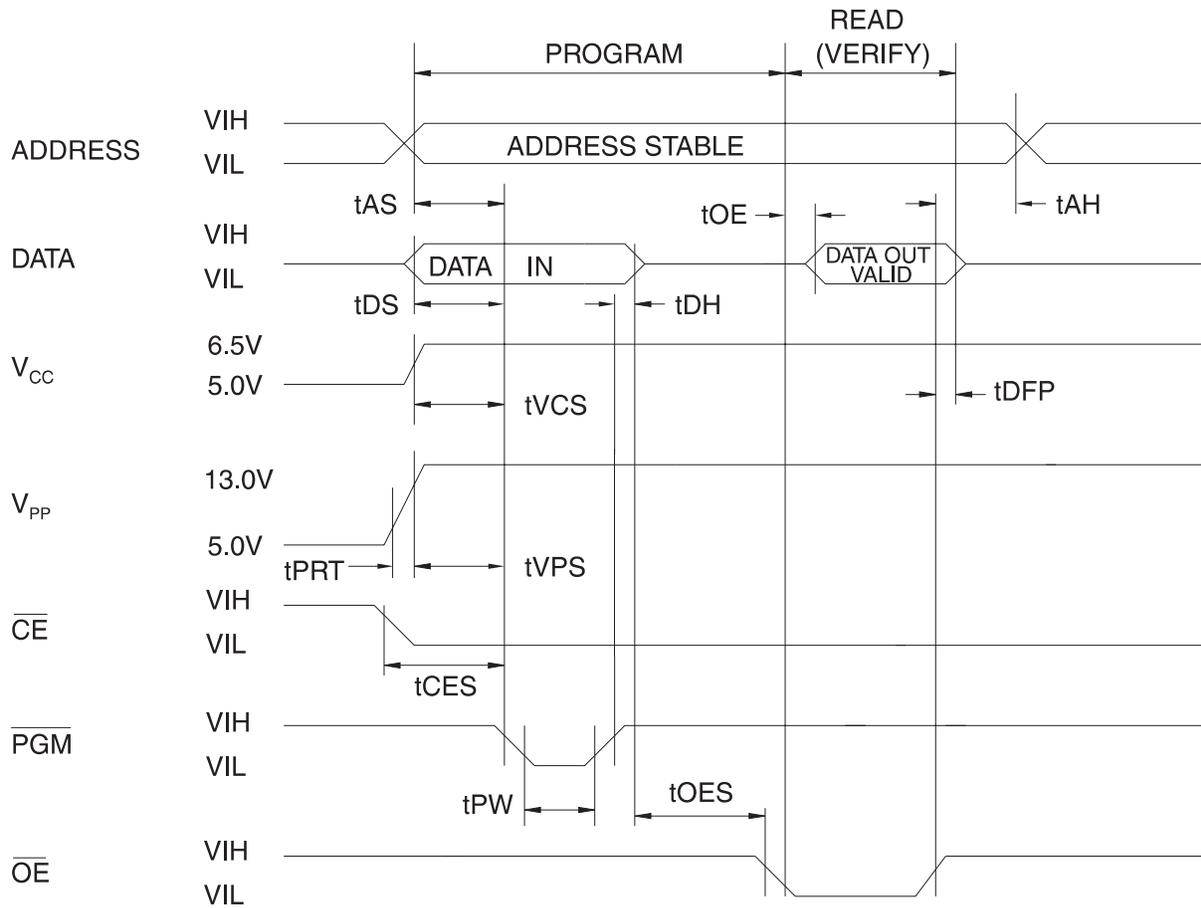
Note: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

3. When programming the AT27C010 at 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

			Limits		
Symbol	Parameter	Test Conditions	Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4		V

DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25V$

| Symbol	Parameter	Test Conditions[1]	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time	Input Rise and Fall Times	2		µs
t_{DS}	Data Setup Time	(10% to 90%) 20ns	2		µs
t_{AH}	Address Hold Time	Input Pulse Levels	0		µs
t_{DH}	Data Hold Time	0.45V to 2.4V	2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay [2]		0	130	ns
t_{VPS}	V_{PP} Setup Time	Input Timing Reference Level	2		µs
t_{VCS}	V_{CC} Setup Time	0.8V to 2.0V	2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width[3]	Output Timing Reference Level	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	0.8V to 2.0V		150	ns
t_{PRT}	V_{PP} Pulse Rise TIme During Programming		50		ns

Note:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven— see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C010 Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Rapid Programming Algorithm

A 100 μs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 μs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.
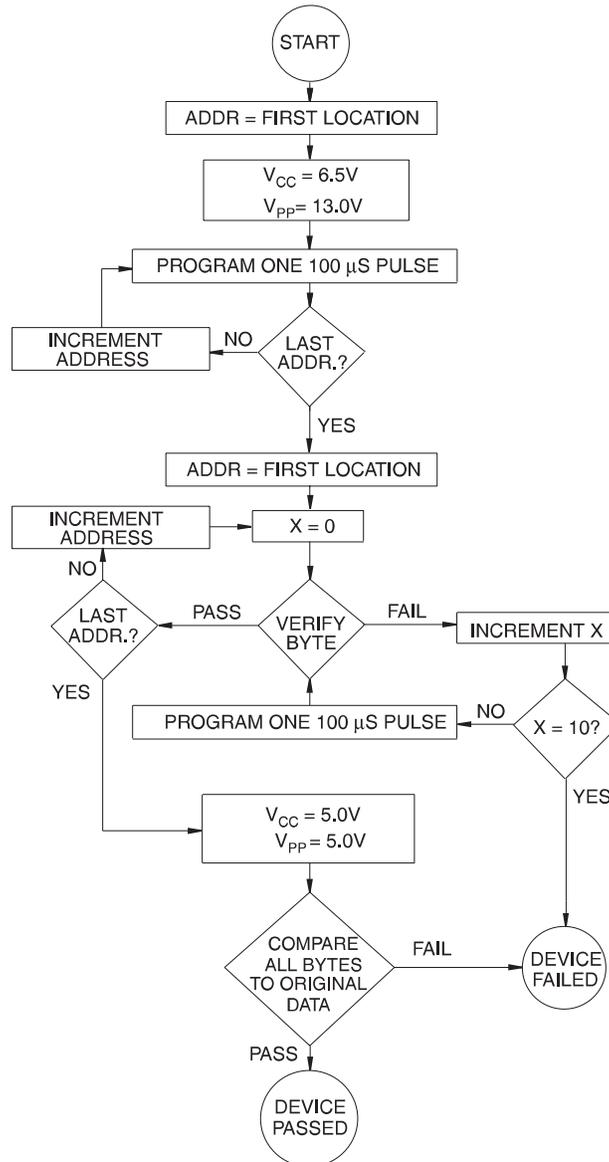
AT27C010 Ordering Information

t_ACC (ns)	I_CC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	25	0.1	AT27C010-45JC AT27C010-45PC AT27C010-45TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010-45JI AT27C010-45PI AT27C010-45TI	32J 32P6 32T	Industrial (-40°C to 85°C)
70	25	0.1	AT27C010-70JC AT27C010-70PC AT27C010-70TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010-70JI AT27C010-70PI AT27C010-70TI	32J 32P6 32T	Industrial (-40°C to 85°C)
90	25	0.1	AT27C010-90JC AT27C010-90PC AT27C010-90TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C010-90JI AT27C010-90PI AT27C010-90TI	32J 32P6 32T	Industrial (-40°C to 85°C)
	25	0.1	AT27C010-90JA AT27C010-90PA	32J 32P6	Automotive (-40°C to 125°C)

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Package Information

32J – PLCC

1.14(0.045) X 45°

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45°

0.318(0.0125)
0.191(0.0075)

E1   E

B

B1   E2

e

D1

A2
A1

D

A

0.51(0.020)MAX
45° MAX (3X)

D2

Notes: 1. This package conforms to JEDEC reference MS-016, Variation AE.
          2. Dimensions D1 and E1 do not include mold protrusion.
             Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
             and E1 include mold mismatch and are measured at the extreme
             material condition at the upper or lower parting line.
          3. Lead coplanarity is 0.004" (0.102 mm) maximum.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e		1.270 TYP		

10/04/01

	TITLE	DRAWING NO.	REV.
AMEL 2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

32P6 – PDIP
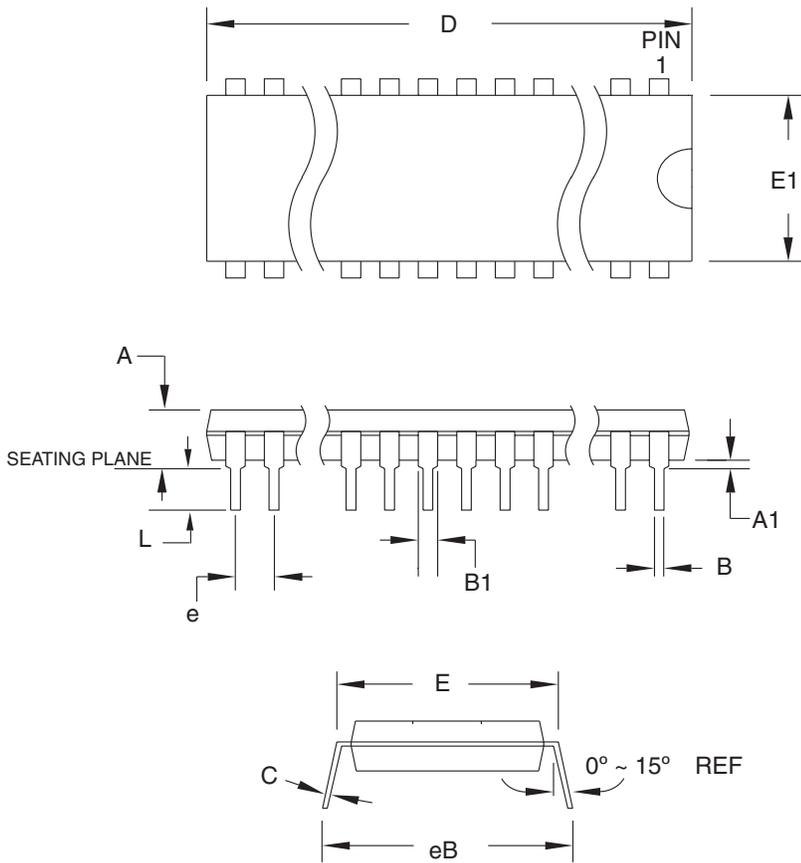
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	41.783	–	42.291	Note 1
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 1
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
![Atmel] 2325 Orchard Parkway San Jose, CA 95131	**32P6**, 32-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	32P6	B

32T – TSOP

PIN 1

0º ~ 8º

c

Pin 1 Identifier

D1 D

L

e   b

L1

E   A2   A

SEATING PLANE   GAGE PLANE

A1

Notes: 1. This package conforms to JEDEC reference MO-142, Variation BD.
          2. Dimensions D1 and E do not include mold protrusion. Allowable
             protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
          3. Lead coplanarity is 0.10 mm maximum.
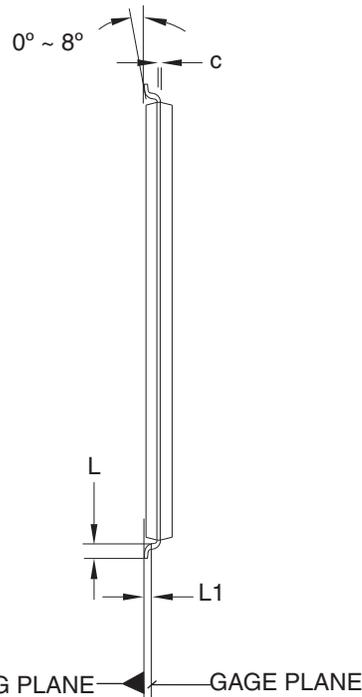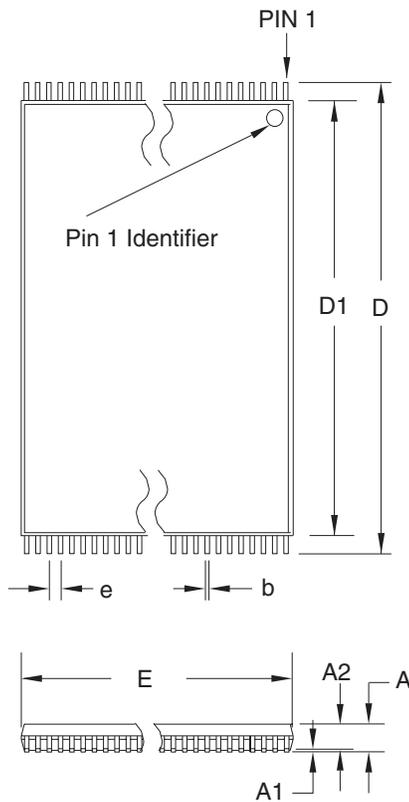
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

10/18/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

Printed on recycled paper.