CXD3400N

6-channel CCD Vertical Clock Driver

Description

The CXD3400N is a vertical clock driver for CCD image sensor. This IC is composed of 6 channels which supports high frame rate readout mode.

Features

Composition

Vertical transfer output 3 levels driver × 4

2 levels driver × 2

Electronic shutter output 2 levels driver × 1

- Suitable drive capability for high-pixel CCD (40% improved compared to current device)
- Small package (20-pin SSOP)
- 2.7 to 5.5V supported input interface

Applications

Digital still camera

Structure

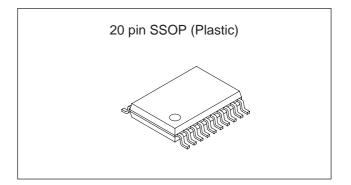
CMOS

Absolute Maximum Ratings

 Supply voltage 	Vdd	GND - 0.3 to +7.0	V
 Supply voltage 	V_L	GND to −10	V
 Supply voltage 	Vн	V∟ + 26	V
 Input voltage 	VIN	GND - 0.3V to $VDD + 0.3$	V
Operating temperature	Topr	-20 to +75	°C
Storage temperature	Tstg	-55 to +150	°C

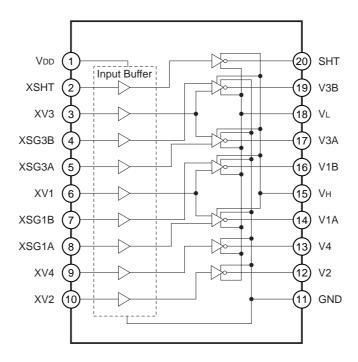
Recommended Operating Conditions

 Supply voltage 	V_{DD}	2.7 to 5.5	V
 Supply voltage 	V_L	-5.0 to -9.0	V
 Supply voltage 	Vн	11.5 to 15.5	V
 Operating temperature 	Topr	-20 to +75	°C



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Block Diagram



Pin Description

Pin No.	Symbol	I/O	Functions
1	VDD	_	Input power supply (3.3V system)
2	XSHT	I	SHT pulse input
3	XV3	I	V3A and V3B transfer pulse input
4	XSG3B	I	V3B readout pulse input
5	XSG3A	I	V3A readout pulse input
6	XV1	I	V1A and V1B readout pulse input
7	XSG1B	I	V1B readout pulse input
8	XSG1A	I	V1A readout pulse input
9	XV4	I	V4 transfer pulse input
10	XV2	I	V2 transfer pulse input
11	GND	_	GND (= VM)
12	V2	0	High voltage output (2 levels: Vм, VL)
13	V4	0	High voltage output (2 levels: Vм, VL)
14	V1A	0	High voltage output (3 levels: Vн, Vм, VL)
15	Vн	_	Positive power supply for high voltage output (15V system)
16	V1B	0	High voltage output (3 levels: Vн, Vм, VL)
17	V3A	0	High voltage output (3 levels: Vн, Vм, VL)
18	VL	_	Negative power supply for high voltage output (-7.5V system)
19	V3B	0	High voltage output (3 levels: Vн, Vм, VL)
20	SHT	0	High voltage output (2 levels: Vн, VL)

Truth Table

Input				Output		
XV1, 3	XSG1A, 1B, 3A, 3B	XV2, 4	XSHT	V1A, 1B, 3A, 3B	V2, 4	SHT
L	L	Х	Х	Vн	Х	X
L	Н	Х	Х	Vм	Х	X
Н	L	Х	Х	Z	Х	X
Н	Н	Х	Х	VL	Х	X
Х	X	L	Х	Х	Vм	X
Х	X	Н	Х	Х	VL	X
Х	Х	Х	L	Х	Х	Vн
Х	Х	Х	Н	Х	Х	VL

Z: High impedance X: Don't care

Electrical Characteristics

DC Characteristics

 $(V_{DD} = 3.3V, V_{H} = 15V, V_{M} = GND, V_{L} = -8.5V)$

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
"H" level input voltage	VIH		0.7VDD	_	_	V
"L" level input voltage	VIL		_	_	0.3VDD	V
Input current	lin	Vin = GND to 5V	-10	0.0	10	μA
Operating supply current	Ін	*1	_	0.10	0.20	mA
Operating supply current	IDD	*1	_	0.25	0.50	mA
Operating supply current	IL	*1	-8.5	-5.5	_	mA
Output current	loL	V1A, 1B, 3A, 3B, V2, 4 = -8.25V	10	_	_	mA
Output current	Іом1	V1A, 1B, 3A, 3B, V2, 4 = -0.25V	_	_	-5.0	mA
Output current	Іом2	V1A, 1B, 3A, 3B = 0.25V	5.0	_	_	mA
Output current	Іон	V1A, 1B, 3A, 3B = 14.75V	_	_	-7.2	mA
Output current	losL	SHT = -8.25V	5.4	_	_	mA
Output current	Іоѕн	SHT = 14.75V	_	_	-4.0	mA

^{*1} See Measurement Circuit. Shutter speed 1/10000

Note) Current direction +: inflow to IC; -: outflow from IC

Switching Characteristics

(VDD = 3.3V, VH = 15V, VM = GND, VL = -7.5V)

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Propagation delay time	TPLM	*1	50	70	100	ns
Propagation delay time	Трмн	*1	50	70	100	ns
Propagation delay time	TPLH	*1	50	70	100	ns
Propagation delay time	ТРМЬ	*1	10	30	50	ns
Propagation delay time	Трнм	*1	10	30	50	ns
Propagation delay time	TPHL	*1	10	30	50	ns
Rise time	Ттьм	$VL \rightarrow VM^{*1}$	200	350	500	ns
Rise time	Ттмн	$VM \rightarrow VH^{*1}$	200	350	500	ns
Rise time	TTLH	$VL \rightarrow VH^{*1}$	30	60	90	ns
Fall time	Ттмь	$V_M \rightarrow V_L^{*1}$	200	350	500	ns
Fall time	Ттнм	$VH \rightarrow VM^{*1}$	200	350	500	ns
Fall time	TTHL	$VH \rightarrow VL^{*1}$	30	60	90	ns
Output noise voltage	Vclh	*2	_	_	1.0	V
Output noise voltage	VCLL	*2	_	_	1.0	V
Output noise voltage	Vсмн	*2	_	_	1.0	V
Output noise voltage	VCML	*2	_	_	1.0	V

^{*1} See Switching Waveform.

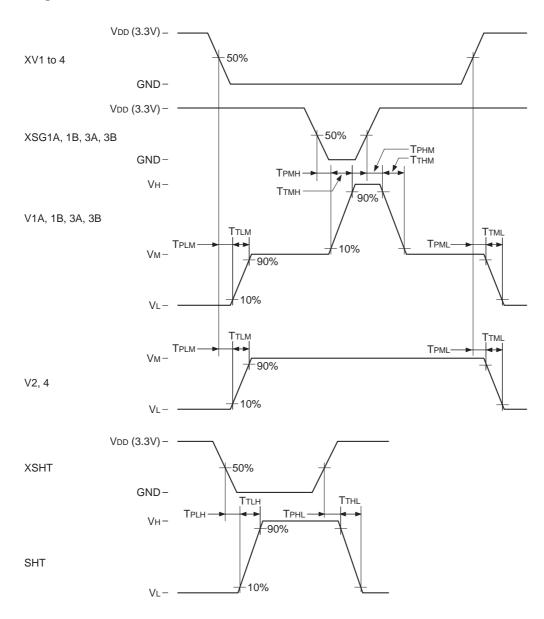
Note) Each item is evaluated by Measurement Circuit.

Notes on Operation (See Application Circuit.)

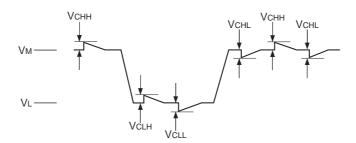
- 1. Be sure to protect against static electricity because this IC is MOS structure.
- 2. A bypass capacitor (0.1µF or more) is connected between GND and near each power supply (VH, VDD, VL).
- 3. In order to protect CCD image sensor, input SHT pin output to SUB pin of CCD image sensor after that has been clamped at VH.

^{*2} See Noise on a Waveform.

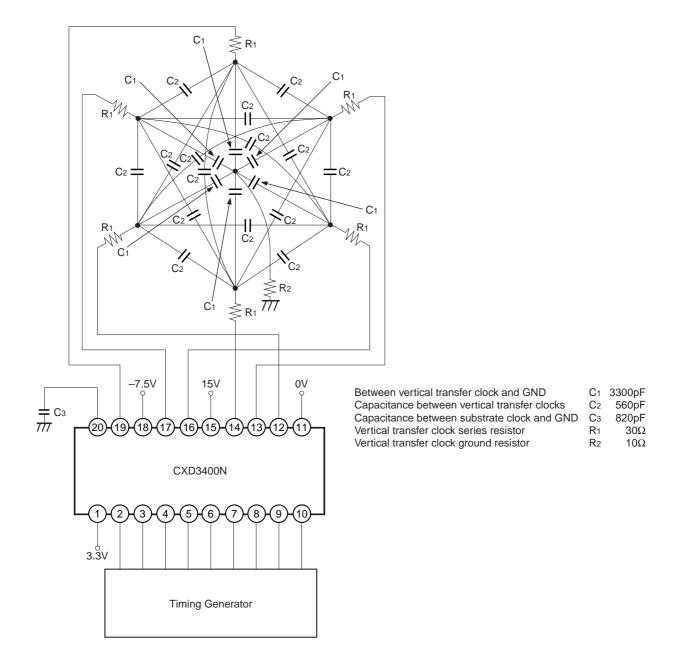
Switching Waveform



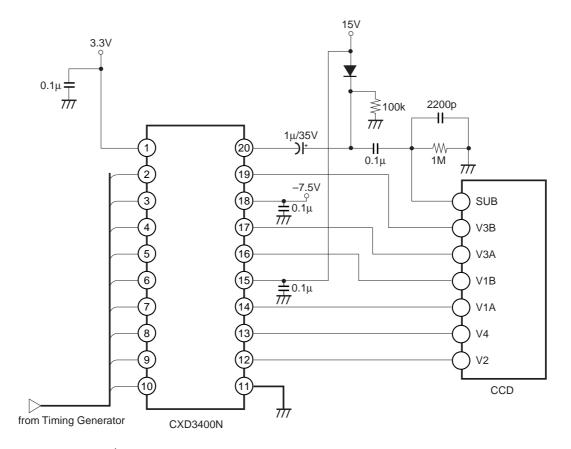
Noise on a Waveform



Measurement Circuit



Application Circuit

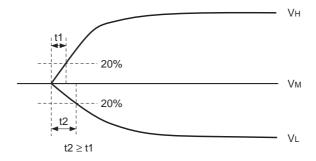


 * See with drive circuit of CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

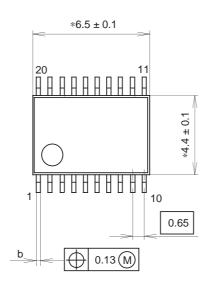
Note with Power-on Sequence

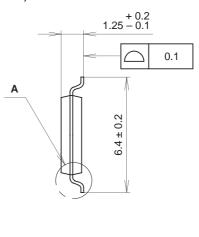
To protect CCD image sensor, rise two power supplies, V_L and V_H as follows. Note that rise V_{DD} first.



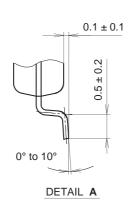
Package Outline Unit: mm

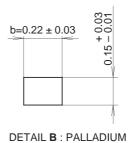
20PIN SSOP (PLASTIC)











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NOTE: Dimension "*" does not include mold protrusion.

SONY CODE SSOP-20P-L01 EIAJ CODE SSOP020-P-0044 JEDEC CODE

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g