# Andrew Cheung

503-560-9519 | acheung8@cs.washington.edu | linkedin.com/in/acheung88 | ninehusky.github.io

## Education

**University of Washington** — Seattle, WA
*B.S. in Computer Science (GPA: 3.84)* — *Aug. 2018 – Dec. 2022*
*M.S. in Computer Science (GPA: 4.00)* — *Jan. 2023 – Expected Dec. 2024*

## Experience

**UW Programming Languages & Software Engineering Lab (PLSE)** — Dec. 2021 – Present
*Research Assistant* — *Seattle, WA*

- Develop and extend programming languages to address challenges in the hardware and architecture domain
- Collaborate with researchers, graduate students, and faculty to author/submit papers to conferences and journals
- Played a vital role in projects such as Lakeroad and 3LA; see "Projects" section for detailed contributions
- Advised by Zach Tatlock (link) and Gus Smith (link)

**Intel Labs** — Jul. 2023 – Present
*Formal Verification Research Intern* — *Seattle, WA*

- Develop hardware abstractions for integration with symbolic evaluators to rigorously verify implementations
- Encode correctness proof for data movement between Number Theoretic Transform (NTT) components
- Enhance efficiency and modularity by refactoring existing proofs to include abstract modules
- Collaborate closely with engineering teams to identify and rectify discrepancies between RTL/proof codebase

**Paul G. Allen School of Computer Science & Engineering** — Sep. 2019 – Present
*CSE 12X Intro TA Coordinator* — *Seattle, WA*

- Oversee team of 100+ TAs across 4 introductory CS courses, ensuring smooth operations of the TA program
- Hire and interview 50 TAs each quarter, ensuring the selection of highly qualified and passionate individuals
- Lead weekly training of new TAs each quarter, providing necessary skills, resources, and guidance
- Maintain strong feedback loop with course faculty to align instructional strategies with TA support
- Promoted from position of Lead Teaching Assistant (Sep. 2019 – Jun. 2023)

**Amazon** — Jun. 2022 – Sep. 2022
*Software Development Engineer Intern* — *Bellevue, WA + Remote*

- Spearheaded development of a skill tree training service tailored for Amazon associates in fulfillment centers
- Designed project infrastructure capable of accommodating over 300,000 users with minimal operational costs
- Implemented full-stack web application using TypeScript, AWS, DynamoDB, and React
- Presented and conducted live demonstrations of project to audience of 20 team members

## Projects

**Lakeroad** | Team Member — Jan. 2022 – Present

- Apply program synthesis to allow FPGA HLS tools to fully leverage complex programmable units
- Extend Lakeroad-specific DSL to include solver constraints, significantly improving the synthesis runtime
- Develop robust evaluation framework to rigorously evaluate inference subroutines across mainstream HLS tools; see ICFP SRC for details
- Create internal representation of DSPs (digital signal processors) and conduct testing to verify synthesized output

**3LA** | Team Member — Jan. 2021 – Sep. 2022

- Create simplified flow for easier development and end-to-end application-level testing of accelerators
- Use Z3 to verify that intermediate transformations offloading operations to accelerators preserve correctness
- Extend capability of Glenside, an IR used in 3LA, to support additional operations and machine learning kernels

## Publications and Posters

- (PLARCH 2023, link) *Generate Compilers from Hardware Models!*
  Gus Henry Smith, Ben Kushigian, Vishal Canumalla, **Andrew Cheung**, René Just, Zachary Tatlock
- (**1st place** at ICFP Student Research Competition, link) *Surveying FPGA Technology Mapping Completeness*
- (arXiv, link) *Application-Level Validation of Accelerator Designs Using a Formal Software/Hardware Interface*
  Bo-Yuan Huang, Steven Lyubomirsky, Yi Li, Mike He, Gus Henry Smith, Thierry Tambe, Akash Gaonkar, Vishal Canumalla, **Andrew Cheung**, Gu-Yeon Wei, Aarti Gupta, Zachary Tatlock, Sharad Malik