

The diagram illustrates a logic circuit for a 74HC00 NAND gate, divided into three main functional blocks: Safe clock enable, Pulse Generation, and Data Bus Control.

Safe clock enable: This block uses two 74HC00 NAND gates (U1A and U1B) to generate a safe clock signal. The inputs are ADDRESS_WTM (pin 11) and DATA_CLK (pin 3). The outputs of U1A (pin 3) and U1B (pin 4) are connected to the inputs of a third 74HC00 NAND gate (U2A, pin 2 and 3), which produces the SAFE_CLK signal (pin 1).

Pulse Generation: This block uses two 74HC123 monostable multivibrators (U2A and U2B) to generate long and short pulses from the SAFE_CLK signal. U2A (Long pulse) is configured with R1 (4.7K), C1 (20pF), and U2B (Short pulse) is configured with R2 (4.7K), C2 (9pF). The outputs are LONG_PULSE (pin 13) and SHORT_PULSE (pin 8).

Data Bus Control: This block uses two 74HC00 NAND gates (U2C and U2D) to generate data bus control signals. U2C (Data Buf Dir) takes LONG_PULSE (pin 12) and SHORT_PULSE (pin 13) as inputs. U2D (Data Buf OE) takes LONG_PULSE (pin 11) and SHORT_PULSE (pin 10) as inputs. The outputs are DATA_BUF_DIR (pin 9) and DATA_BUF_OE (pin 10).

Power and Timing: The circuit is powered by VCC and GND. Timing components R1 (4.7K), R2 (4.7K), C1 (20pF), and C2 (9pF) are used to configure the monostable multivibrators.

Notes: The diagram includes a note stating: "Note that this direction has been inverted compared to the practical implementation and fitting because the signal of the RAM and buffers on the PCB will be opposite, meaning the signals invert in the opposite direction." This indicates that the logic is designed to invert the signals for compatibility with the physical implementation.

[illegible]

J2
peripheral_aux_connector

VCC	1	VCC
VCC	2	VCC
GND	3	GND
GND	4	GND
NC	5	
DCLK	6	DATA_CLK
NC	7	
CCLK	8	CTL_CLK
NC	9	
MEM_ACT	10	MEM_ACT
NC	11	
RFM_WTM	12	RFM_WTM
NC	13	
RST	14	RESET

```

13
peripheral_bank_connector
B_00 1 BANK_BUS_00
B_01 2 BANK_BUS_01
B_02 3 BANK_BUS_02
B_03 4 BANK_BUS_03
B_04 5 BANK_BUS_04
B_05 6 BANK_BUS_05
B_06 7 BANK_BUS_06
B_07 8 BANK_BUS_07
B_08 9 BANK_BUS_08
B_09 10 BANK_BUS_09
B_10 11 BANK_BUS_10
B_11 12 BANK_BUS_11
B_12 13 BANK_BUS_12
B_13 14 BANK_BUS_13
B_14 15 BANK_BUS_14
B_15 16 BANK_BUS_15

```

