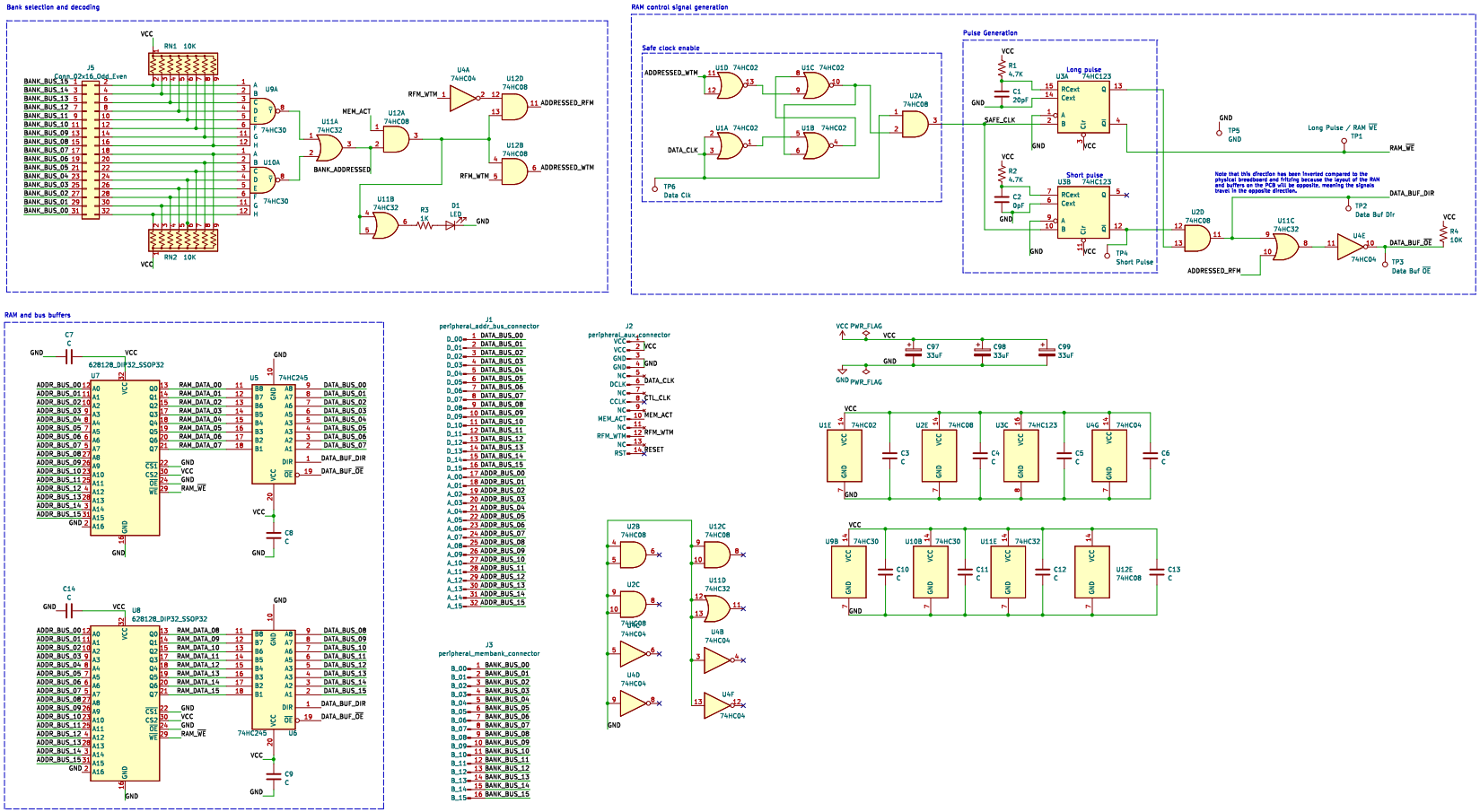
Bank selection and decoding
RAM control signal generation
RAM and bus buffers
Safe clock enable
Pulse Generation
Long pulse
Short pulse
Note that this direction has been inverted compared to the physical breadboard and fritzing because the layout of the RAM and buffers on the PCB will be opposite, meaning the signals travel in the opposite direction.
Long Pulse / RAM WE
Short Pulse
Data Buf Dir
Data Buf OE
Data Clk
J1
perlpheral_addr_bus_connector
J2
perlpheral_aux_connector
J3
perlpheral_membank_connector
62812B_DIP32_SSOP32
74HC245