

Notes: Unless Otherwise Stated

Scheme Spec:

FLASH: MLC, 3.3V
DRAM: DDR3 1.5V
Key: NEXT, PREV, Vol+, Vol-, UP, DOWN, ENTER, UB00T
Power: DCIN, 5V, 2A; BAT, 3.7V, 3600mAH
USB0: OTG
USB1: HOST
USB2: WIFI
WIFI: SDIO WIFI
Card: TFcard
Other: GPS, Headphone, MIC, G-Sensor, camera

Power Supply:

电源名称	输出电压	最大供电能力	预计谁在用
AXP209 DCDC2	1.25V	1600mA	CPU
AXP209 DCDC3	1.2V	1200mA	CORE
AXP209 LDO1	1.3V	30mA	RTC
AXP209 LDO2	3V	200mA	AVCC
AXP209 LDO3	2.8V	400mA	CSI0-IO
AXP209 LDO4	3.3V	200mA	CSI1-IO
SY8008B DCDC	1.8V	1000mA	CSI-CORE
SY8008B DCDC	1.5V/1.8V	1000mA	DRAM
SY8008B DCDC	3.3V	1000mA	VCC/LCD/NAND//WIFI
SY7208	5V	2000mA	HDMI/USB
AP1231B28ZRM	2.8V	300mA	CSI0-AF-VCC
AP1231B12ZRM	1.2V	300mA	WIFI
RT9193-33PB	3.3V	300mA	GPS

Schematics Index:

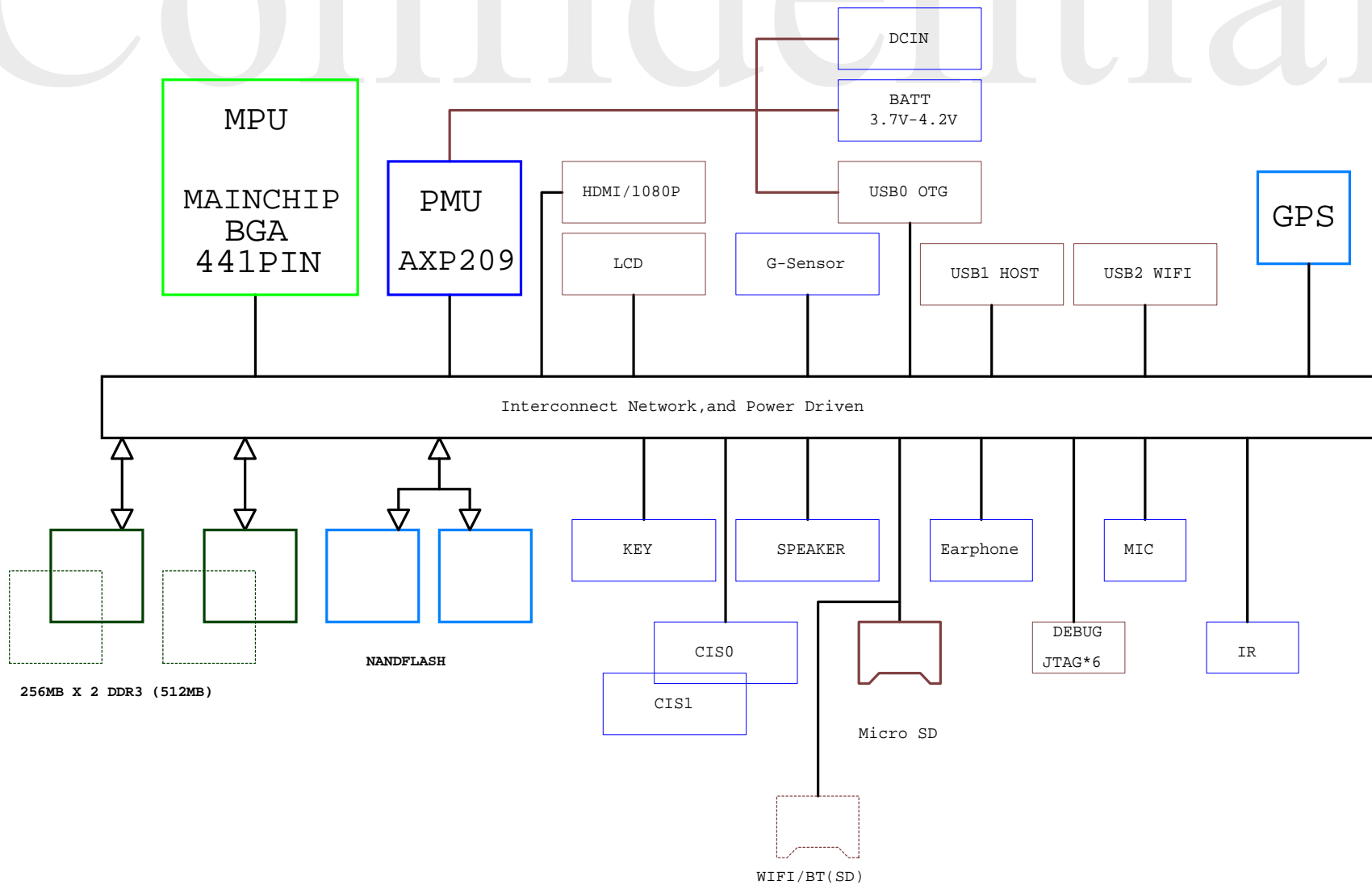
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P09: BESIDE CPU
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P15: NAND
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Rev	Description	Date	Drawn	Checked	Approved
PAD_MAINCHIP_STD_V1.15	更改了电源电路	2011-07-12	Leo		
PAD_MAINCHIP_STD_V1.15	更改了电源滤波电容 (PMU)	2011-07-18	Leo		
PAD_MAINCHIP_STD_V1.21	详见CHANGE LIST	2011-09-09	Leo		

MAINCHIP_PAD_DDR3

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BLOCK



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PIO ASSIGNMENT

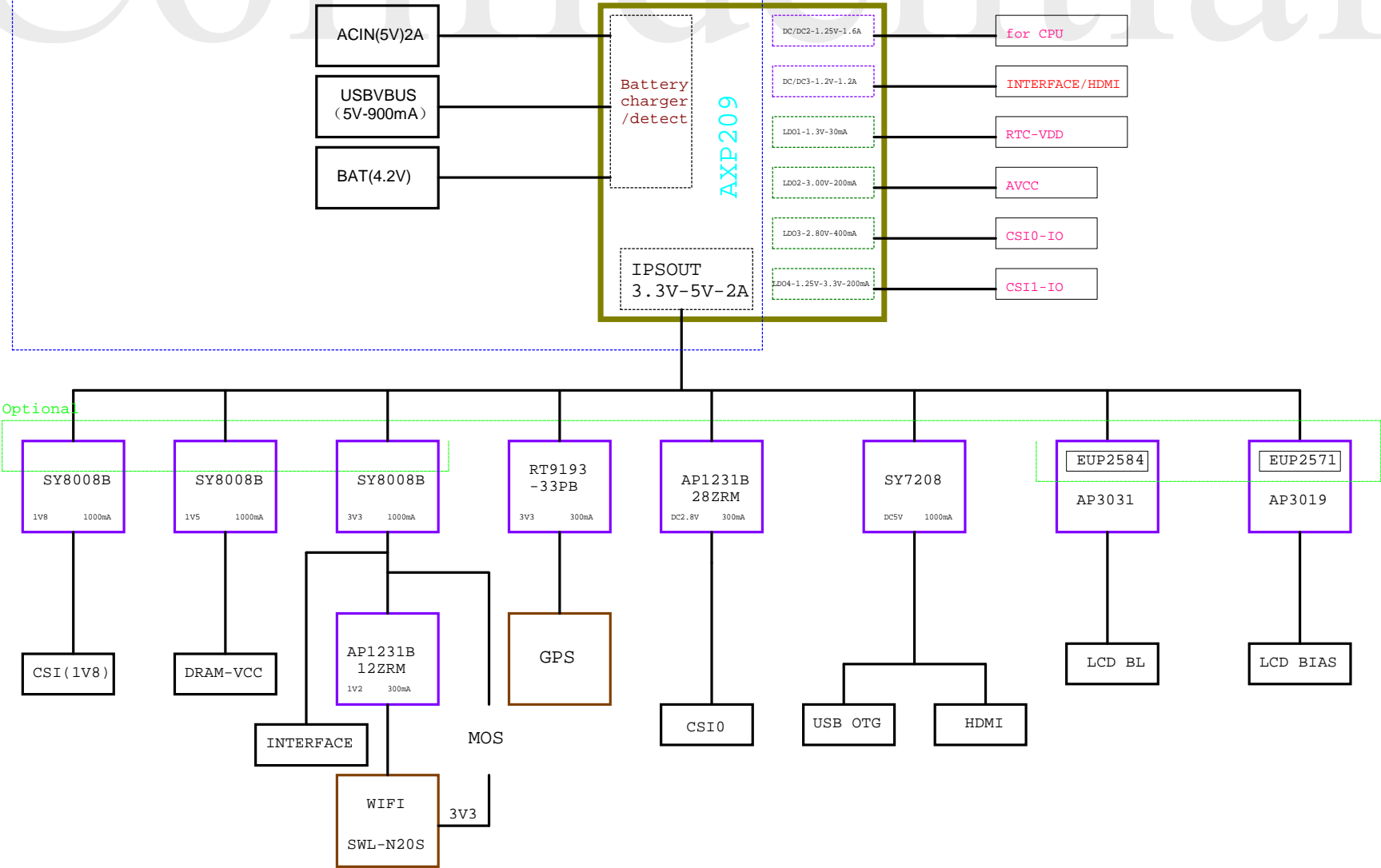
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PA(18)		PA0	ERXD3	EMAC	PC(25)		PC0	NWE#	NAND	PD(28)		PD18	LCD0_D18	LCD	PH(28)		PI(22)	PI15	GPIO_OUT	GPS-RX-EN			
		PA1	ERXD2				PC1	NALE				PD19	LCD0_D19					PH1	GPIO_IN	SD0-DET#	PI16	UART2_RTS	BT-UART-RTS
		PA2	ERXD1				PC2	NCLE				PD20	LCD0_D20					PH2	GPIO_IN	BT-HOST-WAKEUP	PI17	UART2_CTS	BT-UART-CTS
		PA3	ERXD0				PC3	NCE1				PD21	LCD0_D21					PH3	GPIO_OUT	USB2-DRV	PI18	UART2_TX	BT-UART-TX
		PA4	ETXD3				PC4	NCE0				PD22	LCD0_D22					PH4	GPIO_IN	USB0-IDDET	PI19	UART2_RX	BT-UART-RX
		PA5	ETXD2				PC5	NRE#				PD23	LCD0_D23					PH5	GPIO_IN	USB0-VBUSDET	PI20	GPIO_OUT	BT-WAKE
		PA6	ETXD1				PC6	NRB0				PD24	LCD0_CLK					PH6	GPIO_OUT	USB1-DRV	PI21	GPIO_OUT	BT-GPIO1
		PA7	ETXD0				PC7	NRB1				PD25	LCD0_DE					PH7	GPIO_OUT	LCD-BL-EN			
		PA8	ERXCK				PC8	NDQ0				PD26	LCD0_HSYNC					PH8	GPIO_OUT	LCD-PWR			
		PA9	ERXERR				PC9	NDQ1				PD27	LCD0_VSYNC					PH9	GPIO_OUT	WIFI-SHDN#			
		PA10	ERXDV				PC10	NDQ2		PE(12)		PE0	CSIO_PCLK	CSIO				PH10	GPIO_OUT	WIFI-HOST WAKEUP			
		PA11	EMDC				PC11	NDQ3				PE1	CSIO_MCLK					PH11	GPIO_OUT	WIFI-VDD-EN			
		PA12	EMDIO				PC12	NDQ4				PE2	CSIO_HSYNC					PH12	GPIO_OUT	WIFI-VCC-EN			
		PA13	ETXEN				PC13	NDQ5				PE3	CSIO_VSYNC					PH13	GPIO_OUT	CSIO-RESET#			
		PA14	ETXCK				PC14	NDQ6				PE4	CSIO_D0					PH14	GPIO_OUT	CSII-RESET#			
		PA15	ECRS				PC15	NDQ7				PE5	CSIO_D1					PH15	GPIO_OUT	PA-SHDN#			
		PA16	ECOL				PC16	NWP				PE6	CSIO_D2					PH16	GPIO_OUT	CSIO-1V8-EN			
PA17	GPIO_OUT	E-RST	PC17	NCE2		PE7	CSIO_D3	PH17	GPIO_OUT			CSII-1V8-EN											
PB(24)		PB0	TWIO_SCK	PMU		PC18	NCE3	GPS-SCS	PF(6)		PF0	SDC0_D1	SDC0	PI(22)				PI0	GPS_CLK	GPS			
		PB1	TWIO_SDA			PC19	SPI2_CS				PF1	SDC0_D0						PI1	GPS_SIGN				
		PB2	PWM0		PWM	PC20	SPI2_SCLK				PF2	SDC0_CLK						PI2	GPS_MAG				
		PB3	GPIO_OUT			MT-C	PC21				SPI2_MOSI	GPS-MOSI						PF3	SDC0_CMD	PI3	PWM1	WIFI	
		PB4	IR0_RX	IR		PC22	GPIO_OUT	PG(12)				CSII						PF4	SDC0_D3	PI4	SDC3_CMD		
		PB5	GPIO_OUT	BT-RST	GPS-VCC-EN	PC23	NC											PF5	SDC0_D2	PI5	SDC3_CLK		
		PB6	I2S_BCLK	BT-PCM-CLK		PC24	NDQS		LCD				PG0					CSII_PCLK	WIFI		PI6		SDC3_D0
		PB7	I2S_LRCK	BT-PCM-SYNC	PD0	LCD0_D0	PG1						CSII_MCLK					PI7			SDC3_D1		
		PB8	I2S_DO0	BT-PCM-OUT	PD1	LCD0_D1	PG2						CSII_HSYNC					PI8			SDC3_D2		
		PB9	GPIO_OUT	USB0-DRV	PD2	LCD0_D2	PG3						CSII_VSYNC					PI9			SDC3_D3		
		PB10	GPIO_OUT	LCD0-SCK	PD3	LCD0_D3	PG4						CSII_D0		PI10			SPI0_CS0			GS-INT2		
		PB11	GPIO_OUT	LCD0-SDA	PD4	LCD0_D4	PG5						CSII_D1		PI11			SPI0_CLK			CSIO-AF-EN		
		PB12	I2S_DI	BT-PCM-INT	PD5	LCD0_D5	PG6						CSII_D2		PI12			SPI0_MOSI			TV-EN		
		PB13	GPIO_OUT	TP-WAKEUP	PD6	LCD0_D6	PG7						CSII_D3		PI13			SPI0_MISO			GY-INT		
		PB14	JTAG_MS0	JTAG	PD7	LCD0_D7	PG8						CSII_D4		PI14			GPIO_OUT			GPS-OSC-EN		
		PB15	JTAG_CK0		PD8	LCD0_D8	PG9						CSII_D5										
		PB16	JTAG_DO0		PD9	LCD0_D9	PG10						CSII_D6										
		PB17	JTAG_DI0	TWI1	PD10	LCD0_D10	PG11						CSII_D7										
		PB18	TWI1_SCK		PD11	LCD0_D11																	
		PB19	TWI1_SDA		PD12	LCD0_D12																	
		PB20	TWI2_SCK	TWI2	PD13	LCD0_D13																	
		PB21	TWI2_SDA		PD14	LCD0_D14																	
		PB22	UART0_TX		UART (DBG)	PD15	LCD0_D15																
		PB23	UART0_RX	PD16		LCD0_D16																	
				PD17		LCD0_D17																	

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POWER TREE

LAYOUT: ACIN、BATT、IPSOUT输入或输出线，从PMU管脚处就要保证尽量粗。



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POWER TREE			
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The diagram illustrates a PCB layout for a CPU1 and a component U1-1. The CPU1 is connected to U1-1 via a signal trace labeled SDQ[31:0]. The trace is shown as a blue line with a green cross-hatch pattern. The component U1-1 has pins labeled AB4, AC7, and SDQ0. The SDQ[31:0] trace is connected to the SDQ0 pin of U1-1. The diagram also shows a differential pair trace labeled SDQ0, which is connected to the SDQ0 pin of U1-1. The differential pair is shown as a blue line with a green cross-hatch pattern. The diagram includes labels for Equilong BUS (Z0= 50 ohm) and Differential pairs (Z0= 100 ohm).



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PA剩余口全部过孔接地, 用于散热

虚线框内的电路部分，是当没有SATA功能的时的连接方式。



Title

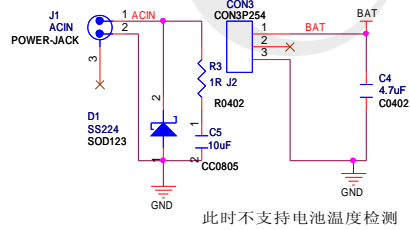
CPU2

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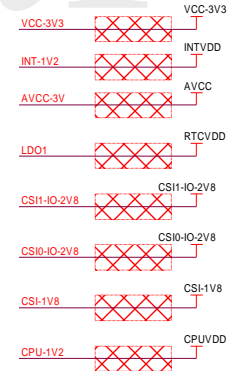
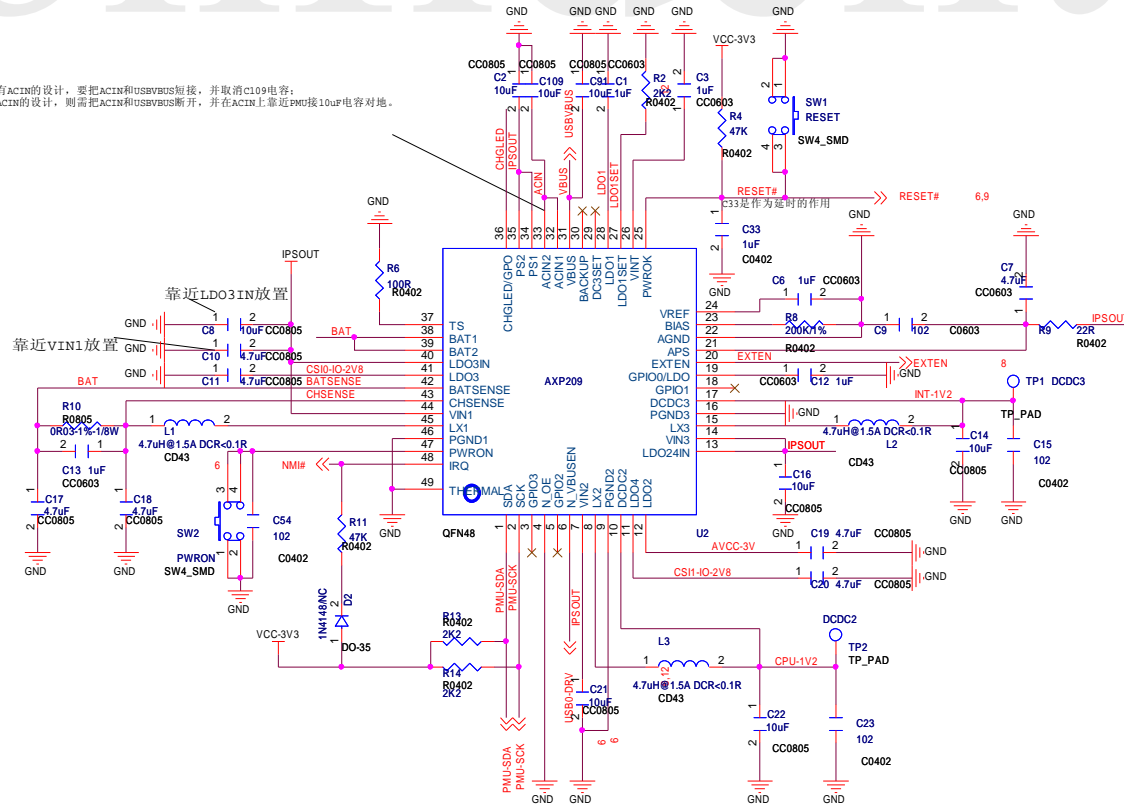
Rev

POWER-PMU

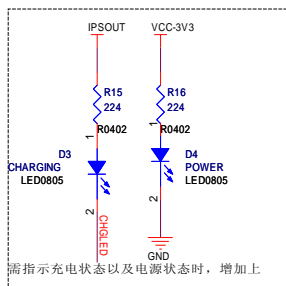


如果没有ACIN的设计, 要把ACIN和USBVDD短接, 并取消C109电容;
如果有ACIN的设计, 则需把ACIN和USBVDD断开, 并在ACIN上靠近PMU接10uF电容对地。

POWER INPUT



POWER LINE:Width>=60mil

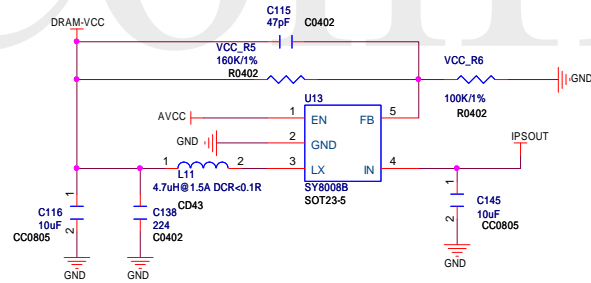


需指示充电状态以及电源状态时, 增加上

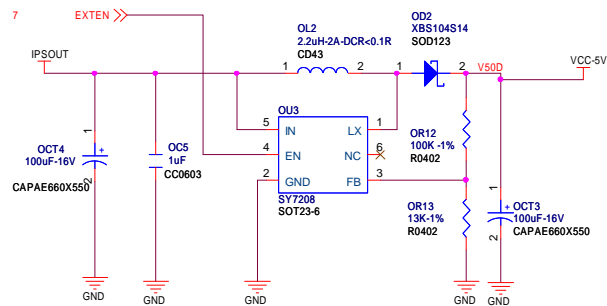
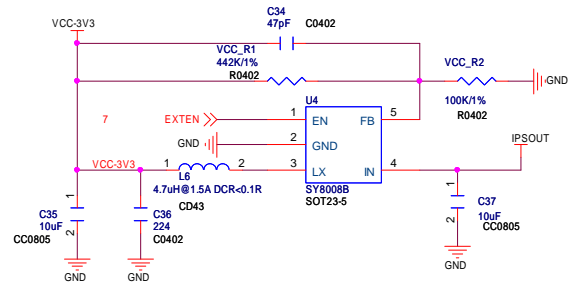
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POWER-DC/DC

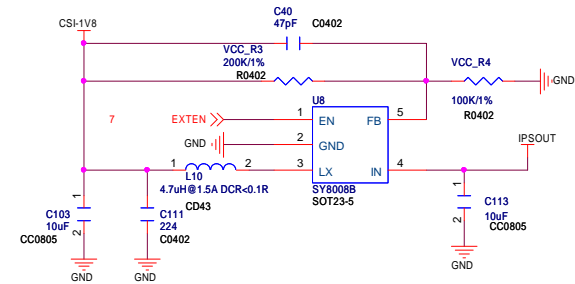
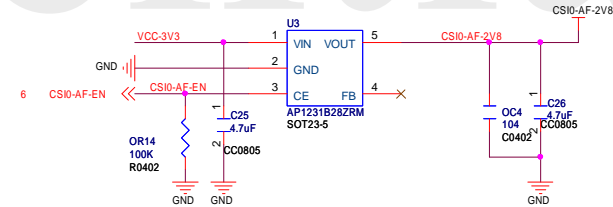


$$V_{out} = 0.6 * (1 + R1/R2)$$



$$V_{out} = 0.6 * (1 + R1/R2) \quad \text{实际输出控制在5.2V}$$

如果摄像头没有自动对焦功能，此电路省略。

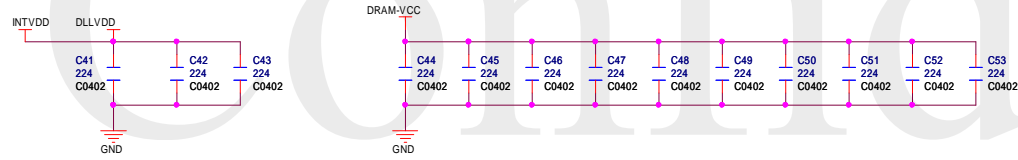


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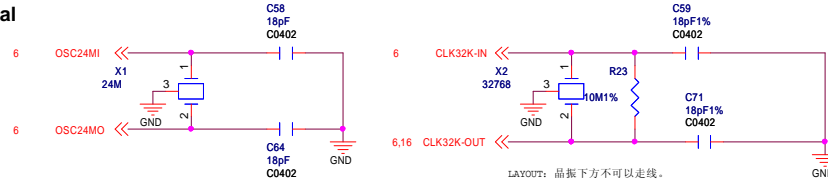
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POWER-DC/DC		
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BESIDE CPU

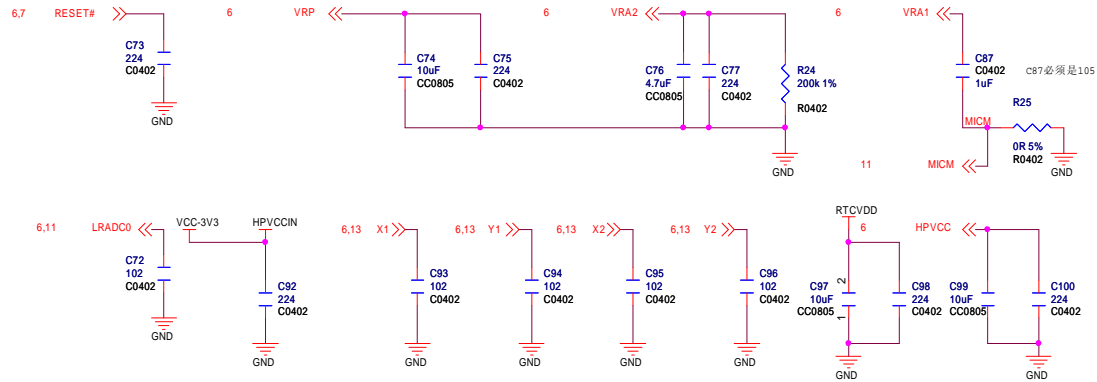
DRAM



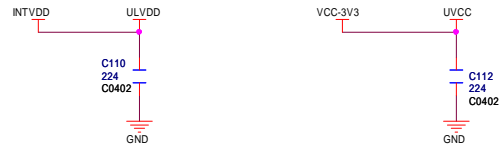
Crystal



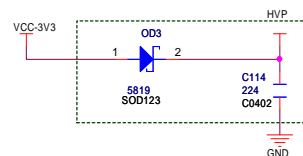
AUDIO&SYS&TP



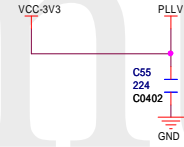
USB



HDMI

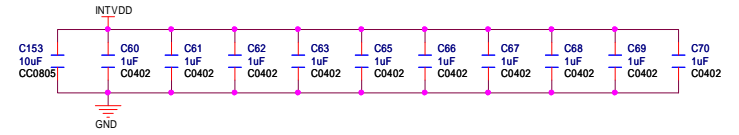


PLL

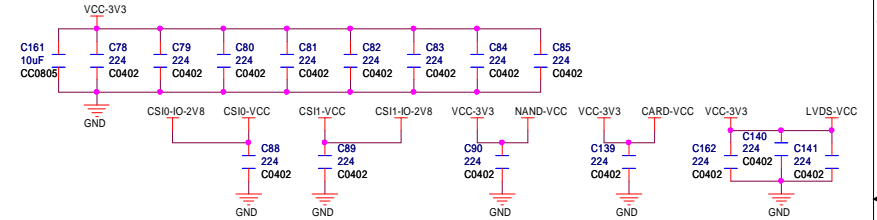


CORE

LAYOUT: 按照一个PIN, 放一个电容, 并且尽量靠近PIN摆放。

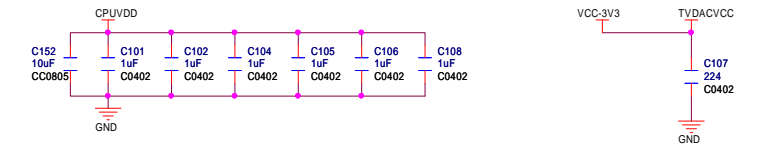


PIO-INTFACE

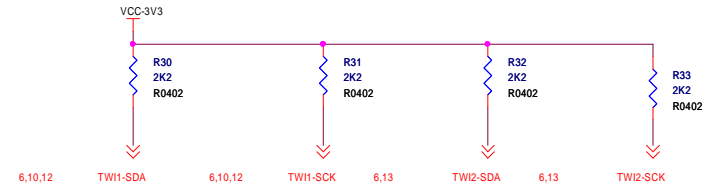


CPU&TV

LAYOUT: 按照一个PIN, 放一个电容, 并且尽量靠近PIN摆放。



TWI-PULLUP



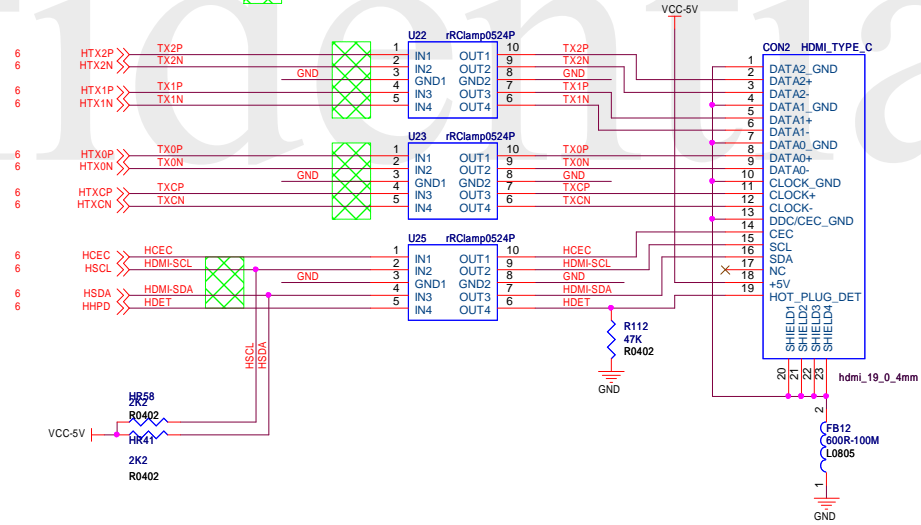
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HDMI-CSIO

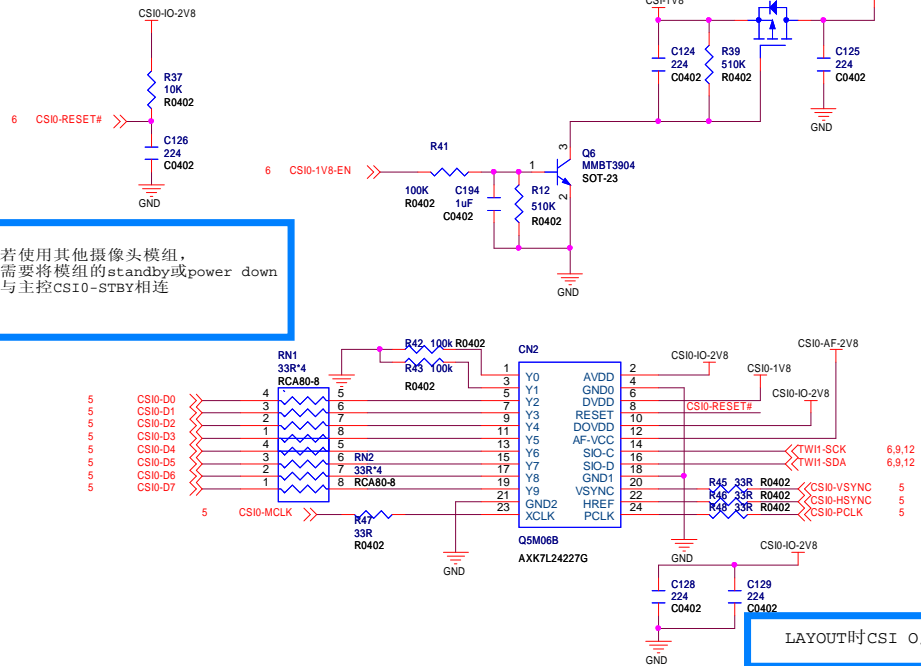
HDMI

Differential pairs
Z0= 100 ohm



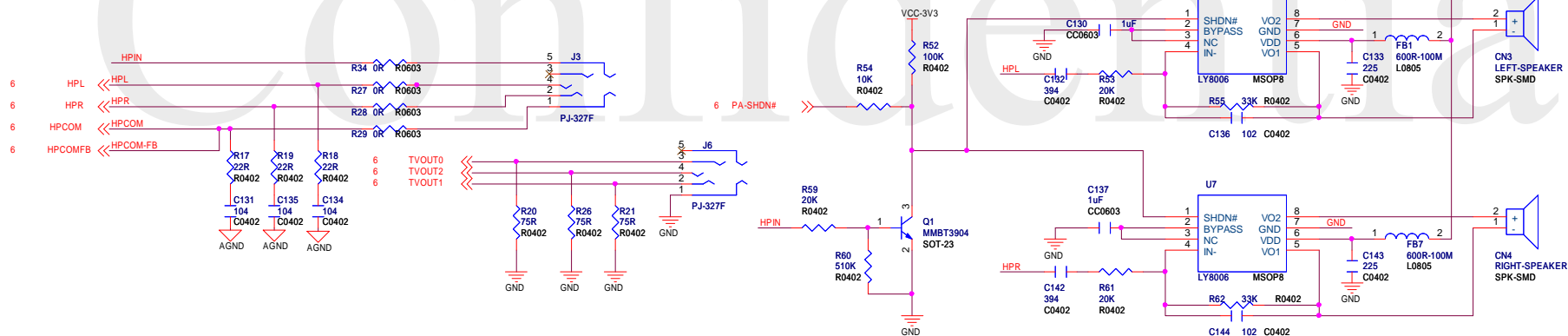
CSIO

后置高分辨率

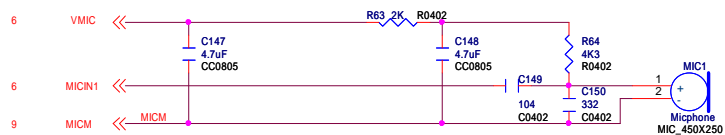


HP-KEY-MIC-IR-TVOUT-MT

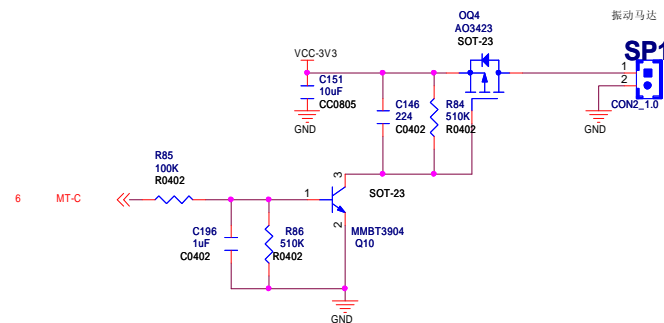
Head Phone & TVOUT



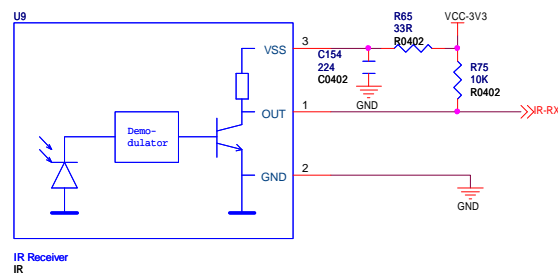
Microphone



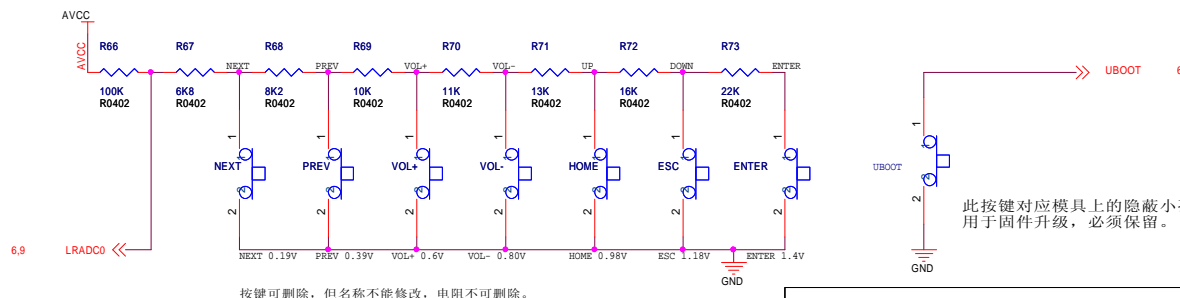
Motor



IR MODULE



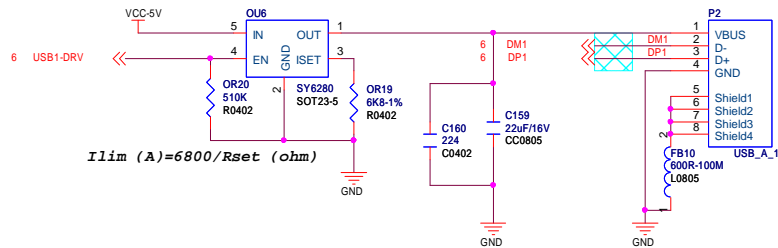
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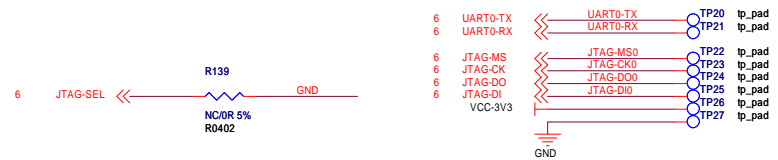
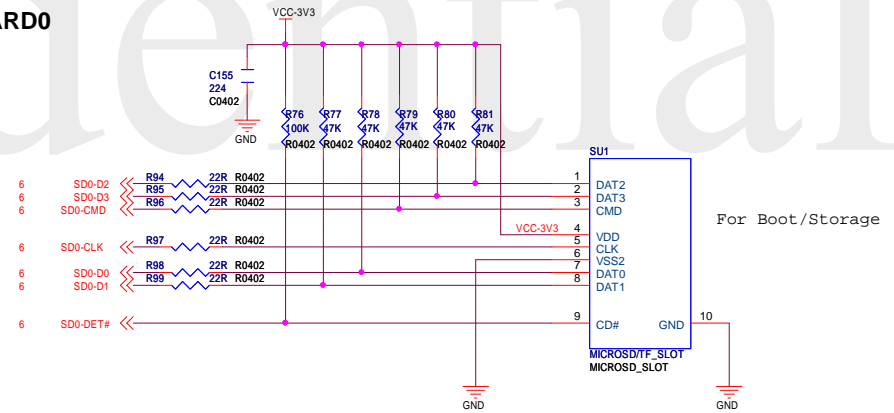
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USB

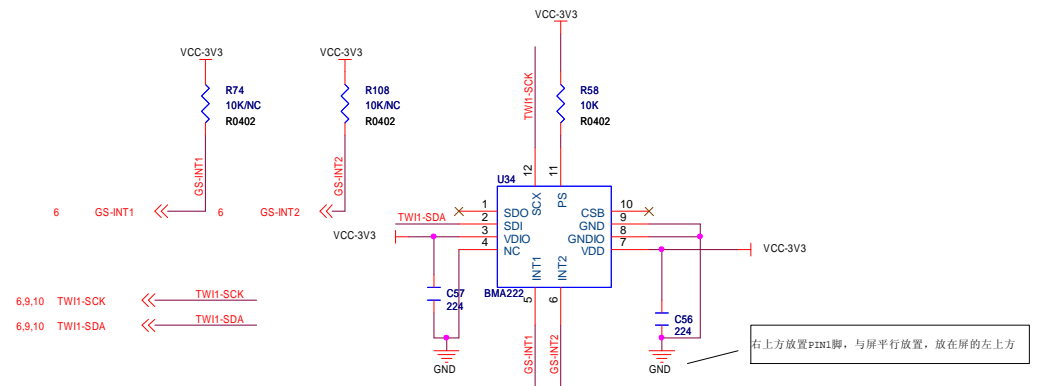


DEBUG



预留DEBUG测试点，以备调试使用

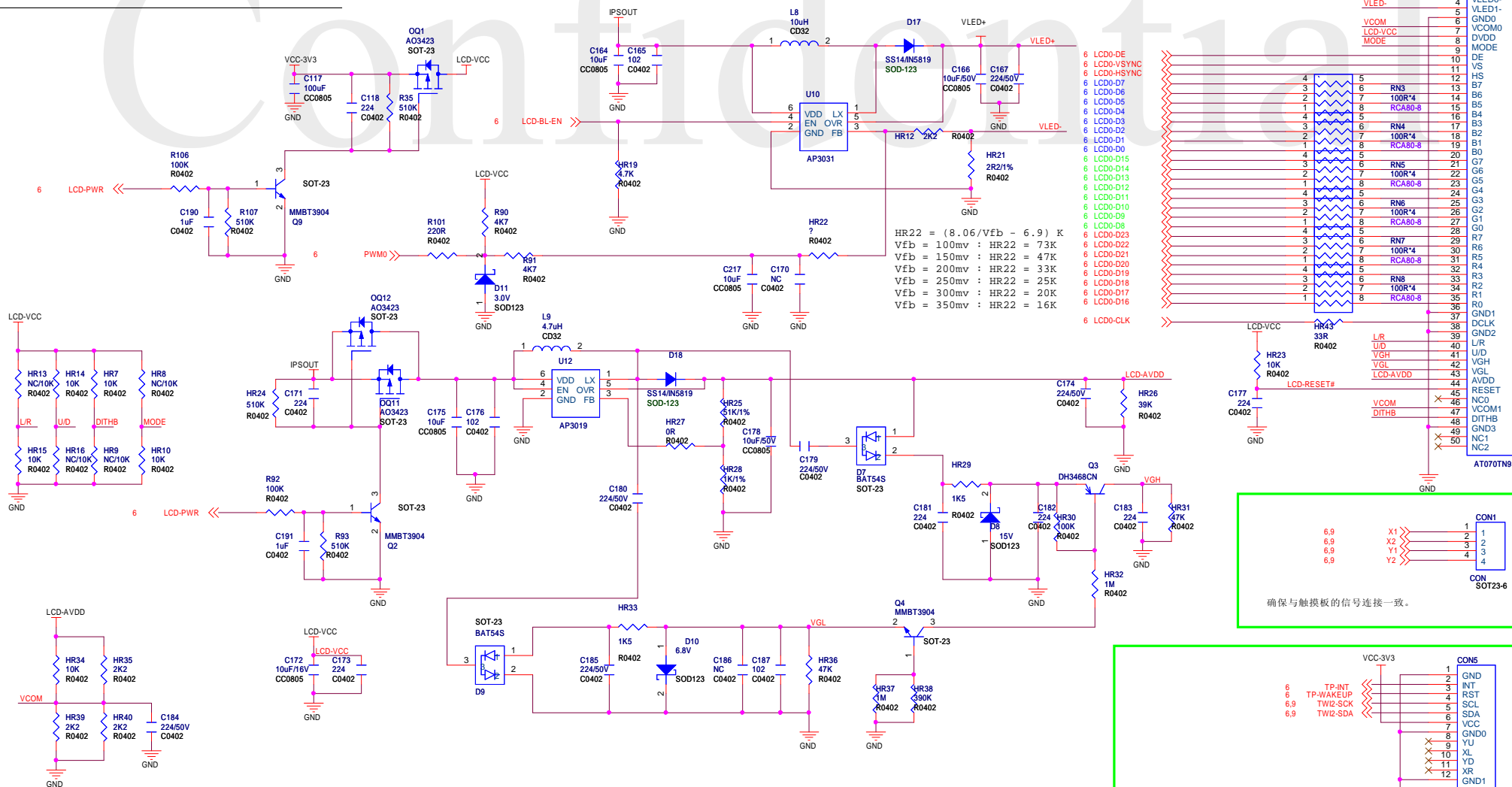
G-SENSOR



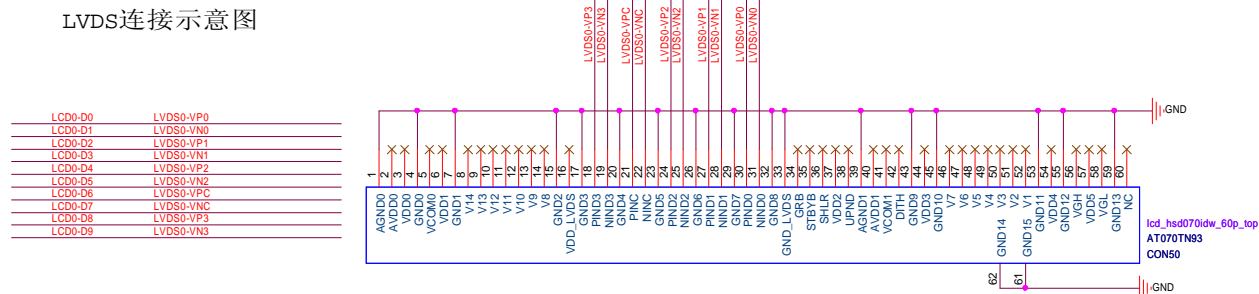
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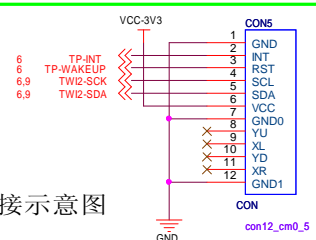
LCD



LVDS连接示意图



电容屏信号连接示意图



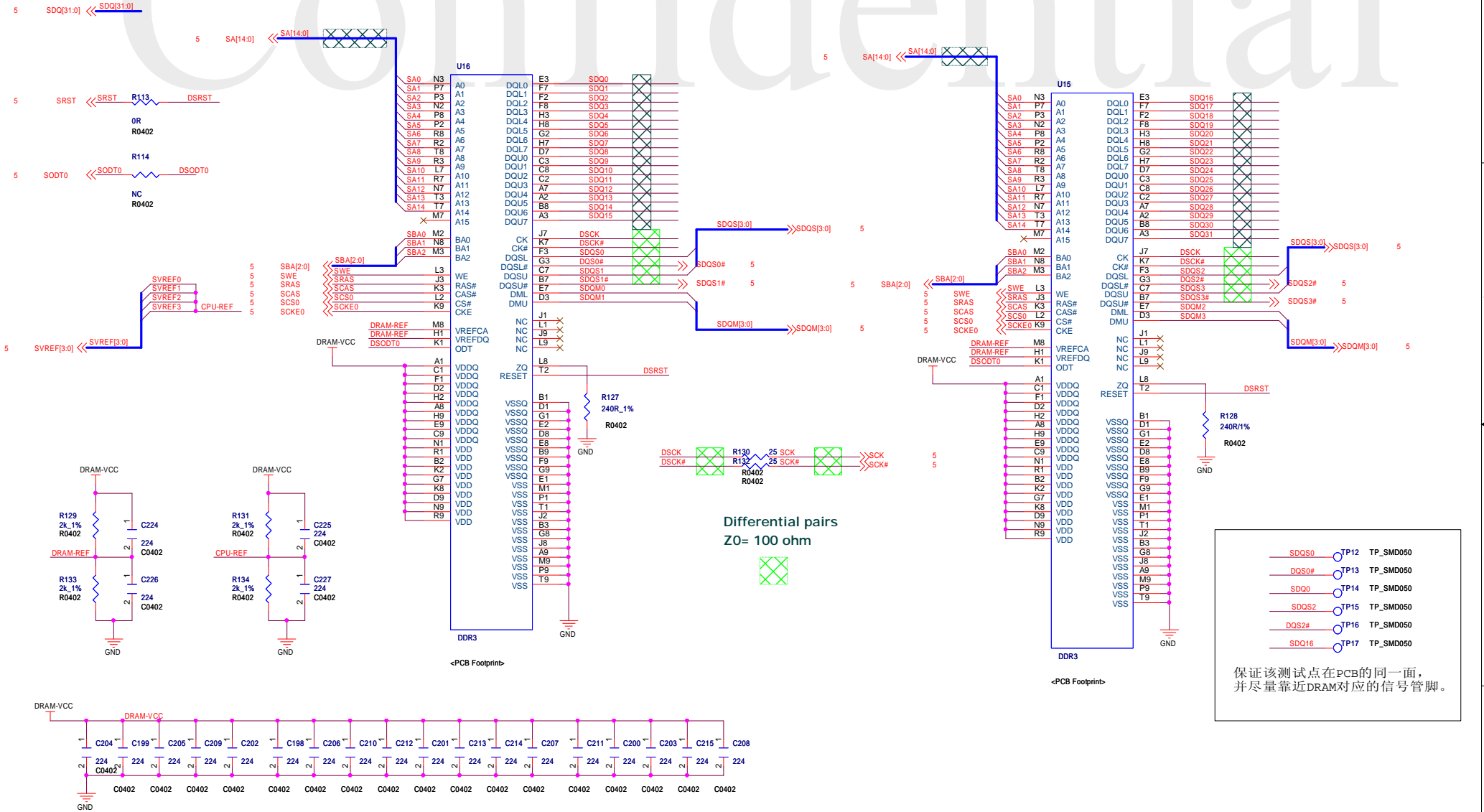
MAINCHIP PAD DDR3

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LCD			
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DDR3

Equilong BUS

Z0= 50 ohm



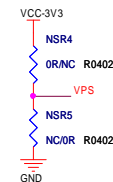
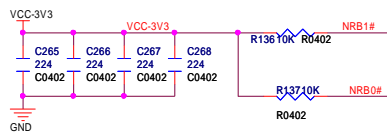
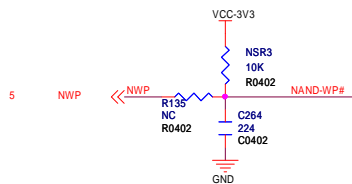
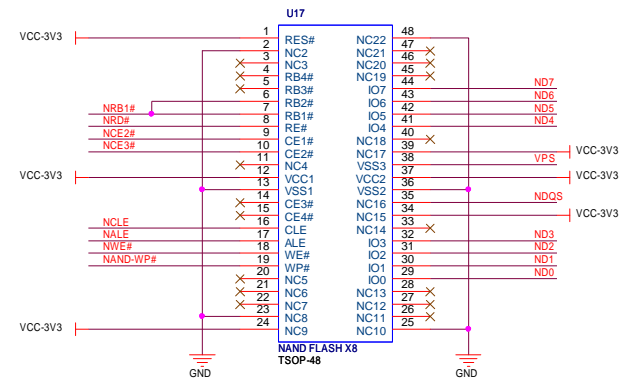
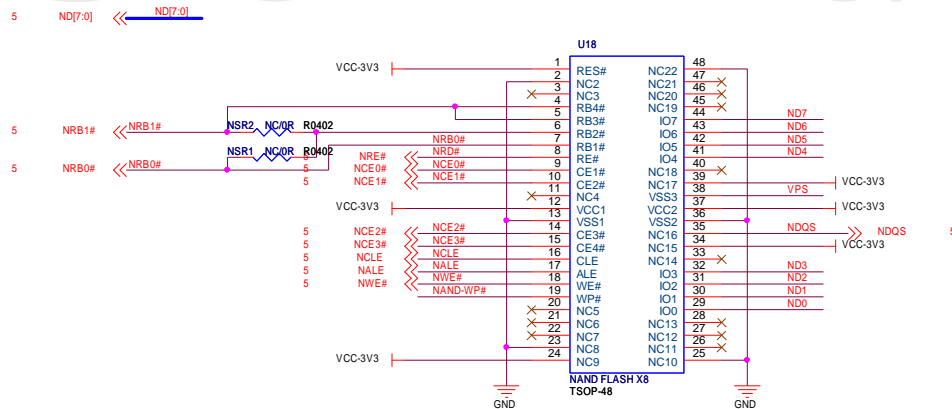
DQ0-7, DQM0, DQS0 Length matching 100mil
 DQ8-15, DQM1, DQS1 Length matching 100mil
 DQ16-23, DQM2, DQS2 Length matching 100mil
 DQ24-31, DQM3, DQS3 Length matching 100mil
 DA, CONTROL, CK Length matching 300mil
 DQSn, DQSn# Differential pairs Z0= 100 ohm, Length matching 10mil
 CK, CK# Differential pairs Z0= 100 ohm, Length matching 10mil

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DDR3		
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NAND Flash

TSOP-48 Nand



- (1) 接1片单片选Nand 时, NSR2、NSR1断开
- (2) 接1片双片选Nand 时, 连接NSR2, 断开NSR1
- (3) 接1片四片选Nand 时, 连接NSR1, 断开NSR2
- (4) 接2片单片选或接2片双片选Nand时, 连接NSR1, 断开NSR2
- (5) 接Intel、Toshiba、Samsung 2xnm TSOP Nand时, NSR4连接, NSR5断开; 其它的NSR4断开, NSR5连接

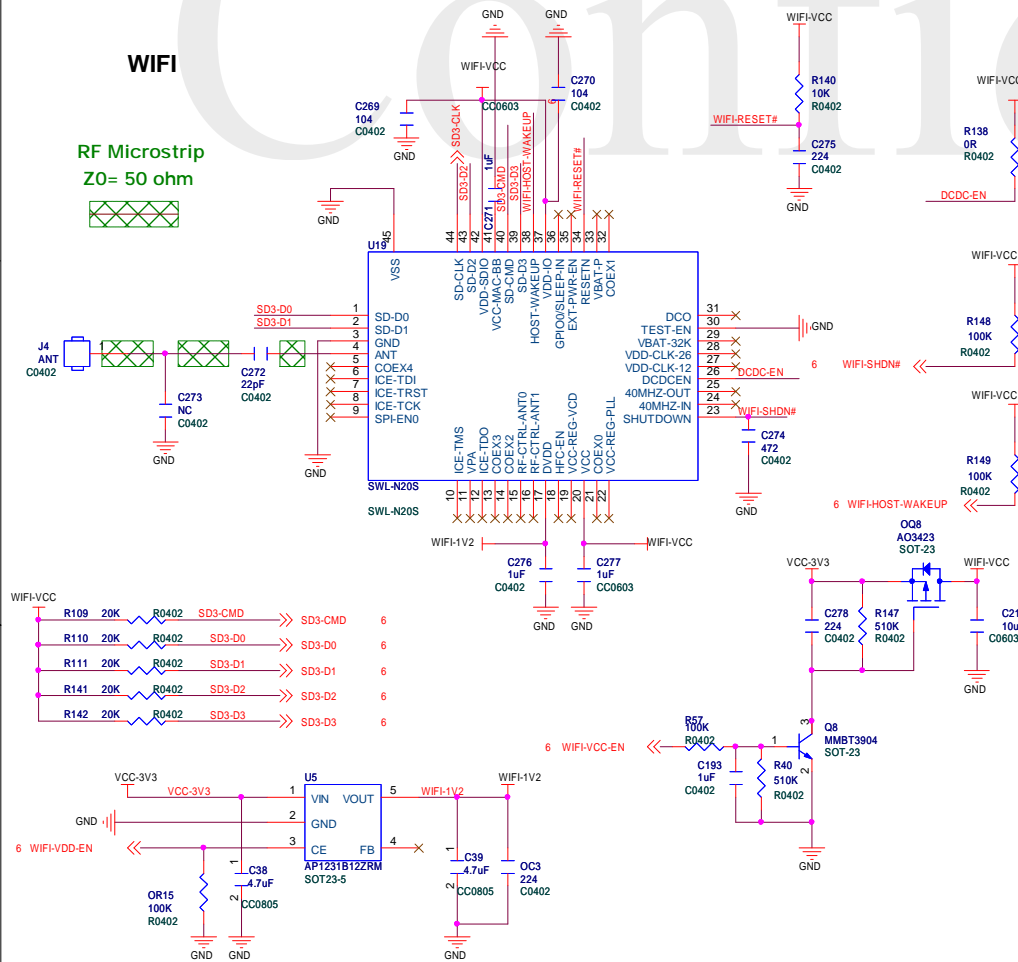
MAINCHIP_PAD_DDR3

File		
NAND Flash		
Size	Document Number	Rev
A3		<V1.0>
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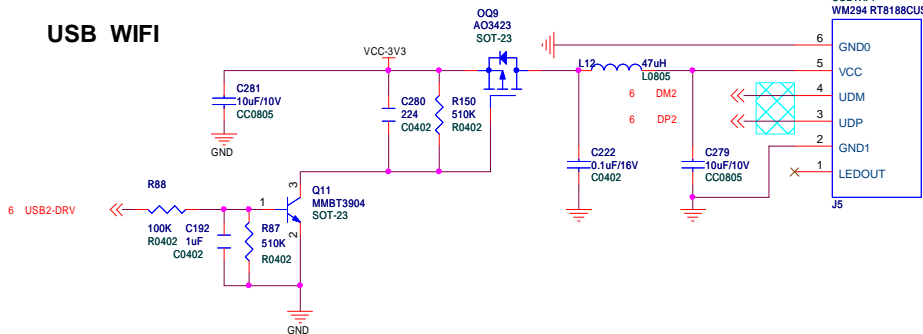
WIFI-BT

WIFI

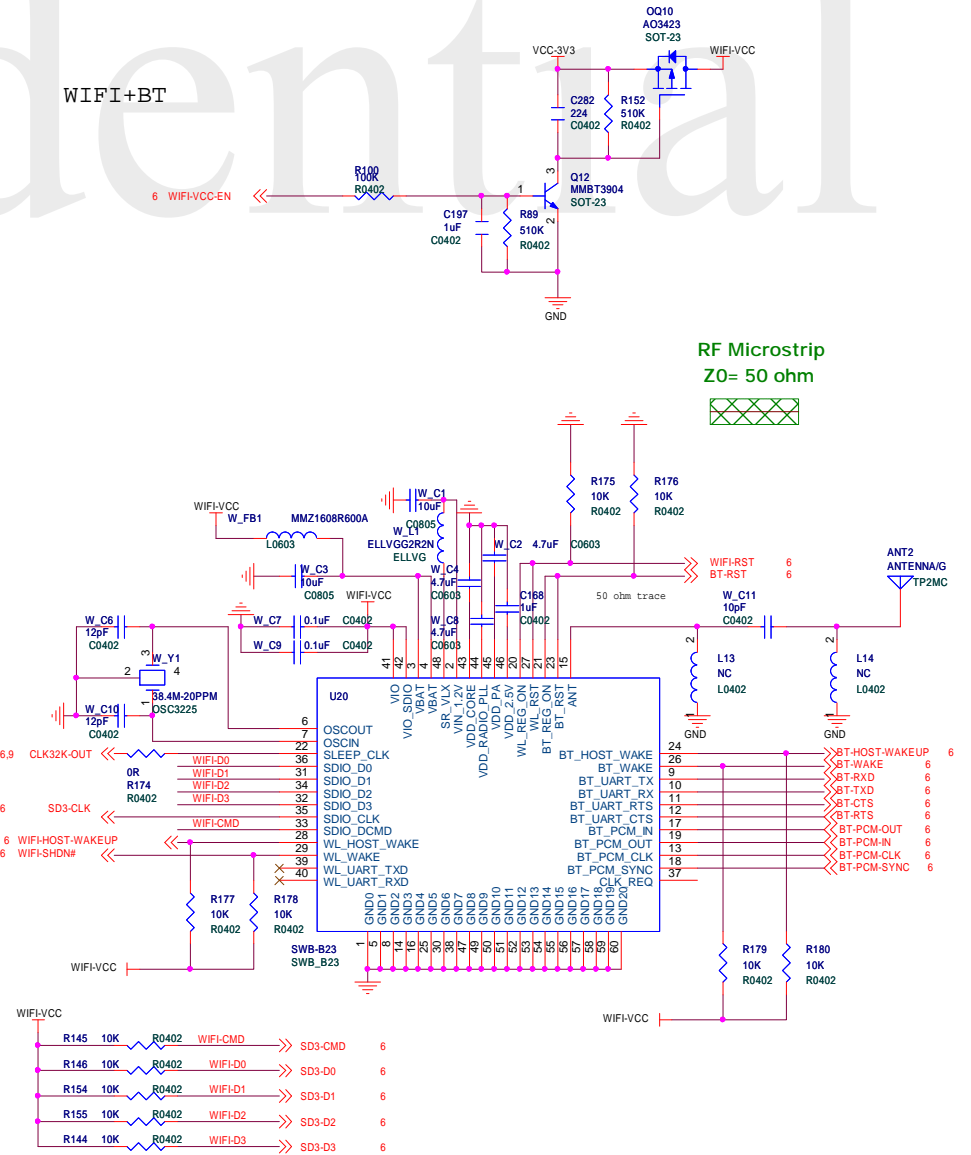
RF Microstrip
Z0= 50 ohm



USB WIFI



WIFI+BT



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Title		
WIFI-GSENSOR		
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Must be placed into
RF shielding case

RX_EN	OSC_EN	Mode
0	0	All stand by
0	1	Oscillator only
1	0	Full active (external reference)
1	1	Full active (internal oscillator)

To GPS Antenna.

[illegible]

- | | | | |
|---|------------|---|------------|
| 6 | GPS-OSC-EN | ↔ | GPS-OSC-EN |
| 6 | GPS-RX-EN | ↔ | GPS-RX-EN |
| 5 | GPS-VCC-EN | ↔ | GPS-VCC-EN |
| | | | |
| 5 | GPS-SCS | ↔ | GPS-SCS |
| 5 | GPS-SCLK | ↔ | GPS-SCLK |
| 5 | GPS-MOSI | ↔ | GPS-MOSI |
| 6 | LRADC1 | ↔ | LRADC1 |

MAINCHIP_PAD_DDR3			
Title GPS			
Size A3	Document Number <V1.0>		Rev
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