A New ZVS Bidirectional DC–DC Converter for Fuel Cell and Battery Application

Fang Z. Peng, *Senior Member, IEEE*, Hui Li, *Senior Member, IEEE*, Gui-Jia Su, *Senior Member, IEEE*, and Jack S. Lawler, *Senior Member, IEEE*

***Abstract*—This paper presents a new zero-voltage-switching (ZVS) bidirectional dc–dc converter. Compared to the traditional full and half bridge bidirectional dc–dc converters for the similar applications, the new topology has the advantages of simple circuit topology with no total device rating (TDR) penalty, soft-switching implementation without additional devices, high efficiency and simple control. These advantages make the new converter promising for medium and high power applications especially for auxiliary power supply in fuel cell vehicles and power generation where the high power density, low cost, lightweight and high reliability power converters are required. The operating principle, theoretical analysis, and design guidelines are provided in this paper. The simulation and the experimental verifications are also presented.**

***Index Terms*—Auxiliary power supply, dc–dc converter, fuel cell vehicle, power generation, TDR, ZVS.**

I. Introduction

In RECENT years, the development of high power isolated bidirectional dc–dc converters has become an urgent topic because of the requirements of fuel cell vehicle applications and battery based energy storage systems. Fig. 1 shows a typical system configuration of a fuel cell system where a bidirectional dc–dc converter is needed for cold start and battery recharge. For cold start, the dc–dc converter boosts the 12-V battery voltage to a desired high voltage (normally 150–300 V) for the fuel cell to start. Once the fuel cell is started, the dc-dc converter recharges the battery from the fuel cell or regenerative braking. In order to increase efficiency, soft-switching technology has been widely used in dc–dc converters. However, most of the existing soft-switched dc–dc converters are low power [6]–[8] or unidirectional [9]–[13], and often are difficult to meet the requirements of the above applications. Full-bridge bidirectional dc–dc converters with soft switching are considered as one of the best choices for these applications. Several full-bridge based topologies [1]–[4] have been published in the literature to reduce switching loss, improve EMI and increase efficiency. Normally, a voltage-source converter has high current ripples, while a current-source converter requires voltage clamp circuits [5].

Manuscript received October 22, 2002; revised April 28, 2003. Recommended by Associate Editor F. Blaabjerg.

F. Z. Peng is with Michigan State University, East Lansing, MI 48824-1226 USA (e-mail: fzpeng@egr.msu.edu).

H. Li is with the Department of Electrical and Computer Engineering, Florida State University, Tallahassee, FL 32308.

G.-J. Su is with the Oak Ridge National Laboratory, Knoxville, TN 37932 USA.

J. S. Lawler is with the Department of Electrical and Computer Engineering, University of Tennessee, Knoxville, TN 37996 USA.

Digital Object Identifier 10.1109/TPEL.2003.820550

This paper presents a new bidirectional, isolated dc–dc converter. The new converter is based on a dual half-bridge topology. Compared to the dual full-bridge topologies, it has half the component count for the same power rating with no total device rating (TDR) penalty. In addition, unified ZVS is achieved in either direction of power flow without any additional component. Therefore, a minimum number of devices is used in the proposed circuit. Also the design has less control and accessory power needs than its full-bridge competitors. All these new features allow efficient power conversion, easy control, lightweight and compacted packaging. A 1.6 kW prototype of the converter has been built and successfully tested under full power. The experimental results of the converter's steady-state operation confirm the theoretical analysis and simulation results. The proposed converter is a good alternative to the full-bridge isolated bidirectional dc–dc converter in high power applications and has distinct advantages for high power density and low cost applications.

II. Power Stage Description and Operating Principle

The proposed bidirectional dc–dc converter for fuel cell applications is shown in Fig. 2. The circuit consists of an inductor $(L_{\rm dc})$ on the battery side and two half-bridges each placed on each side of the main transformer T_r. Each switching device has a small parallel capacitor for soft switching. When power flows from the low voltage side (LVS) to the high voltage side (HVS), the circuit works in boost mode to keep the HVS voltage at a desired high value. In the other direction of power flow, the circuit works in buck mode to recharge the battery from the fuel cell or from absorbing regenerated energy. The HVS switches are implemented with IGBTs, while the low voltage side switches are MOSFETs. The arrangement of the inductor and the LVS half bridge is unique. The LVS half bridge has double functions serving as

1) a boost converter to step up voltage;
2) an inverter to produce high frequency ac voltage.

The boost function is achieved by the inductor $(L_{\rm dc})$ and the LVS half bridge. The LVS boost converter draws much smoother current from the load voltage source than full bridge voltage-source inverter. This integrated double function provided by the LVS half bridge is advantageous over other topologies, because the primary current rating of the transformer and current stress of the LVS devices are minimized. This feature will be explained in more detail in the following comparison of TDR and the analysis in Section IV. The capacitor across each switch is a lossless

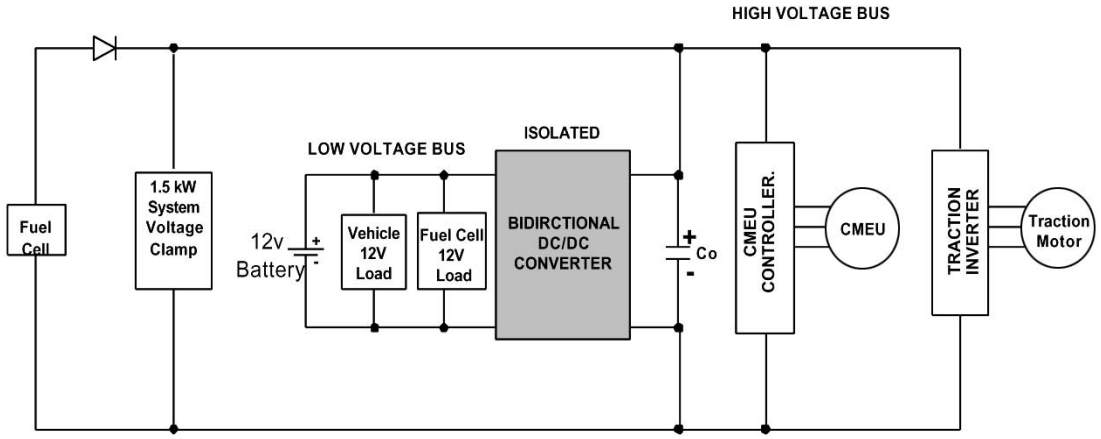

Fig. 1. Block diagram of fuel cell power bus and energy management system. The low voltage bus is 12-V battery and the high voltage bus is the fuel cell voltage 150–300 V.

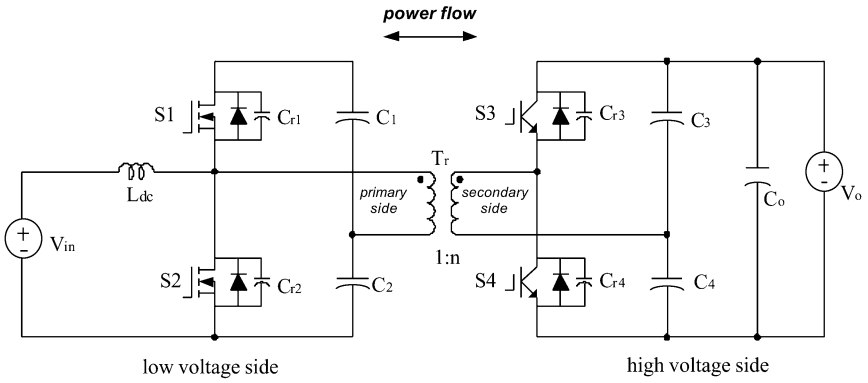

Fig. 2. Proposed soft-switched bidirectional half-bridge dc–dc converter.

snubber (or resonant capacitor) for soft switching. The transformer is used to provide isolation and voltage matching. The leakage inductance of the transformer is utilized as an interface and energy transfer element between the two voltage-source half bridge inverters: LVS and HVS half bridges. Fig. 3 shows the energy transfer principle [4]. The two voltage-source half bridge inverters: LVS and HVS half bridges, each generates a square-wave voltage applied to the primary and secondary of the transformer, respectively. The amount of power transferred is determined by the phase shift of the two square-wave voltages. The current waveform is determined by the phase shift and voltage relationships of (V_1 and V_3) and (V_2 and V_4). The optimum case would be $(V_1 = V_3)$ and $(V_2 = V_4)$ to minimize the peak current. Detailed analysis will be given in Section IV. However, it should be noted here that the two half bridges could have a synchronized duty cycle control rather than 50%. When the duty cycle is 50%, we obtain the easiest and most traditional case of $\phi_2 = \pi, V_1 = V_2$, and $V_3 = V_4$. This paper focuses on the 50% duty cycle case.

The use of the dual half-bridge topology instead of a dual full-bridge configuration can be justified as follows. A comparison of total device rating (TDR) in full bridge and half bridge can be made as shown in Fig. 4. The full bridge is used to produce a high-frequency square-wave ($+V_{\rm dc}$ and $-V_{\rm dc}$) voltage. Each switching device in the full bridge is subject to a voltage stress equal to the dc-input voltage $(V_{\rm dc})$, and the current stress is equal to the load current $(I_{\rm ac})$. The TDR of the full bridge is calculated as $\mathrm{TDR}_F = V_{\rm dc} \cdot I_{\rm ac} \cdot (4\,\text{devices}) = 4 \cdot P_o$, where P_o is the output power. The LVS half bridge in the proposed converter Fig. 2 boosts the dc-rail voltage to twice the dc-input voltage $(2V_{\rm dc})$ and generates a same high-frequency square-wave ($+V_{\rm dc}$ and $-V_{\rm dc}$) voltage with when operated at 50% duty cycle. Therefore, for the half bridge in Fig. 4, each switching device's voltage stress is twice the dc input voltage $(2V_{\rm dc})$, and the current stress is still the load current $(I_{\rm ac})$. Similarly, the TDR of the half-bridge can be calculated as $\mathrm{TDR}_F = (2V_{\rm dc}) \cdot I_{\rm ac} \cdot (2\,\text{devices}) = 4 \cdot P_o$, where P_o is again the output power. The conclusions can be made as follows.

1) The total device rating is the same for the dual half bridge topology and the dual full bridge for the same output power.
2) Although the devices of the half-bridge are subject to twice the dc input voltage, this is an advantage in EV/HEV and fuel cell applications because the dc input voltage is very low (12 V battery).
3) The dual half bridge topology uses only half the number of devices as the full-bridge topology.

The major drawback of the half bridge is the split dc capacitors that have to handle the full load current. For the intended application, high current electrolytic capacitors in conjunction with high frequency polypropylene capacitors are used. The other advantages of the proposed circuit are

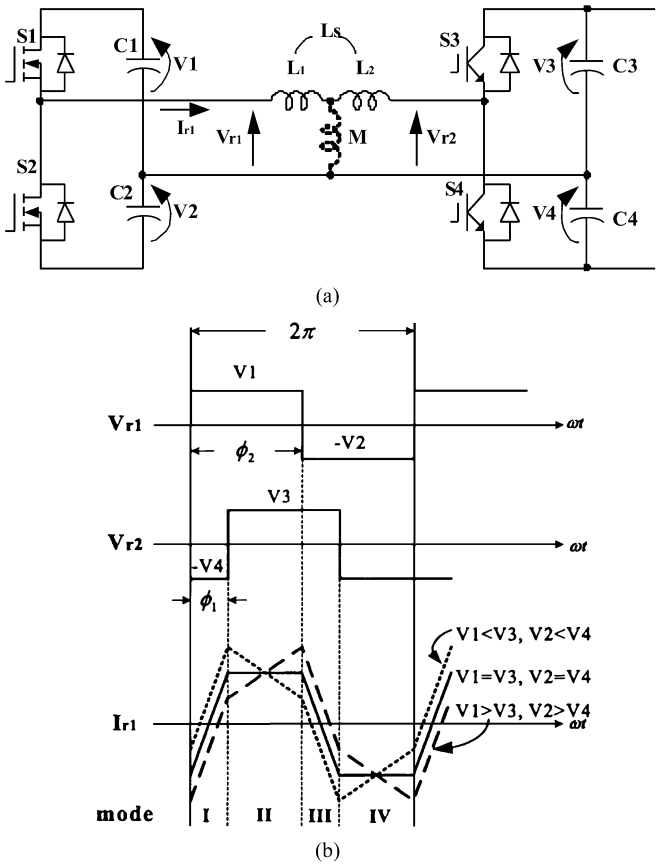

Fig. 3. (a) Simplified equivalent circuit referred to the primary and (b) idealized voltage and current waveforms of transformer. Note that V_3 and V_4 are the values after referred (a factor of $1/n$) to the primary.

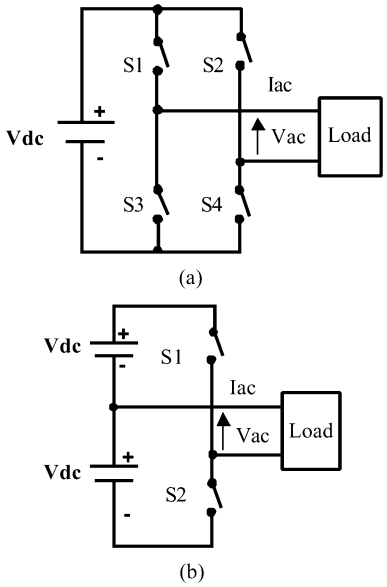

Fig. 4. Comparison of (a) full-bridge topology and (b) half-bridge topology.

1) the LVS half bridge produces a relatively ripple-free dc current that is desirable and friendly to the low-voltage source (fuel cell or battery);
2) current ratings (stresses) are minimized for the LVS switching devices and transformer thanks to the boost function of the LVS half bridge;
3) the unified soft-switching capabilities in either direction of power flow without additional switching devices are achieved.

This will be described in the following section. The low input ripple current is achieved due to the current source functionality in this converter. Other topologies (e.g., the full bridge) can also operate as current source. However, a relatively large active clamping circuit is needed for such current source full bridge as indicated in [1], [2].

III. Soft-Switching Principle

The soft switching of each device in either direction of power flow is demonstrated by exploring the commutation process in boost mode and buck mode, respectively. In order to simplify the circuit analysis, the primary referred equivalent circuit is drawn in Fig. 5 where the transformer is replaced with a leakage inductance L_S.

A. Boost Mode

The interval t_0 to t_{12} of Fig. 6 describes the various stages of operation during one switching period in boost mode. The converter operation is repetitive in the switching cycle. One complete switching cycle is divided into thirteen steps. To aid in understanding each step, a set of corresponding annotated circuit diagrams is given in Fig. 7 with a brief description of each step.

Step 1) (*before* t_1): Circuit steady state. S1 and D3 are conducting.

Step 2) $(t_1 - t_2)$: At t_1, S1 is turned off. C_{r1}, C_{r2} and T_r begin to resonate, making V_{cr2} across C_{r2} fall from $V_1 + V_2$. V_{r1} also drops from V_1. The rate of change depends on the magnitude of I_{off}, which is the difference between I_{r1} and I_{d1} at t_1.

Step 3) $(t_2 - t_3)$: At t_2, V_{cr2} attempts to overshoot the negative rail. D2 is therefore forward biased. During this period, S2 can be gated on at zero voltage.

Step 4) $(t_3 - t_4)$: From t_3, I_{r1} is less than I_{d1}, so S2 begins to transfer current from D2. I_{r1} keeps on decreasing until it is equal to 0 at t_4. D3 is thereby still conducting until t_4.

Step 5) $(t_4 - t_5)$: From t_4 to t_5, I_{r1} begins to change polarity; therefore, current is commutated from D3 to S3.

Step 6) $(t_5 - t_6)$: At t_5, S3 is gated to turn off. C_{r3} and C_{r4} begin to be charged and discharged, respectively. The rate of change of the voltage depends on I_{r1} at t_5.

Step 7) $(t_6 - t_7)$: At t_6, when V_{cr4} attempts to overshoot the negative rail, D4 is forward biased. During this period, S4 can be gated on at any time at zero voltage.

Step 8) $(t_7 - t_8)$: At t_7, S2 is gated off. C_{r1}, C_{r2} and T_r begin to resonant again, making V_{cr1} across C_{r1} discharge from $V_1 + V_2$. V_{r1} therefore increases from $-V_2$. The rate of change now is decided primarily by the sum of the magnitude of I_{d1} and I_{r1}.

Step 9) $(t_8 - t_9)$: At t_8, when V_{cr1} attempts to overshoot the positive rail, D1 is forward biased. I_{r1} increases until it equals 0 at t_9. During this period, S1 can be gated on at zero voltage.

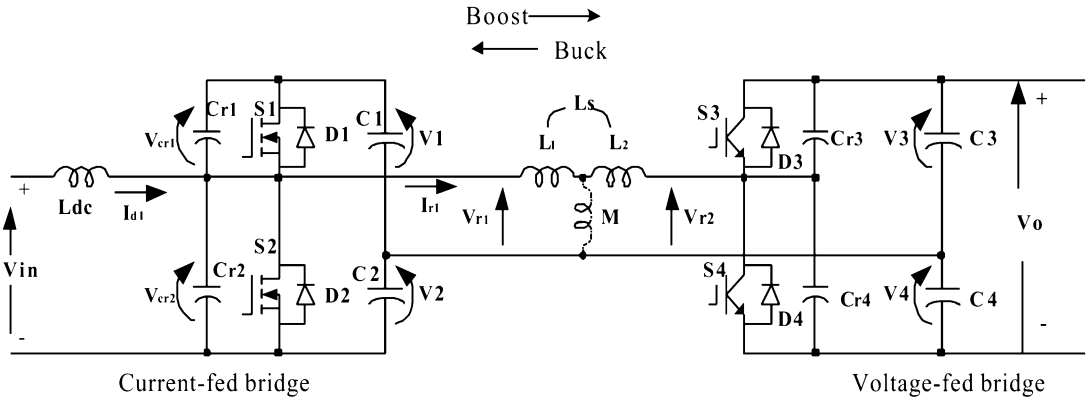

Fig. 5. Primary referred equivalent circuit.

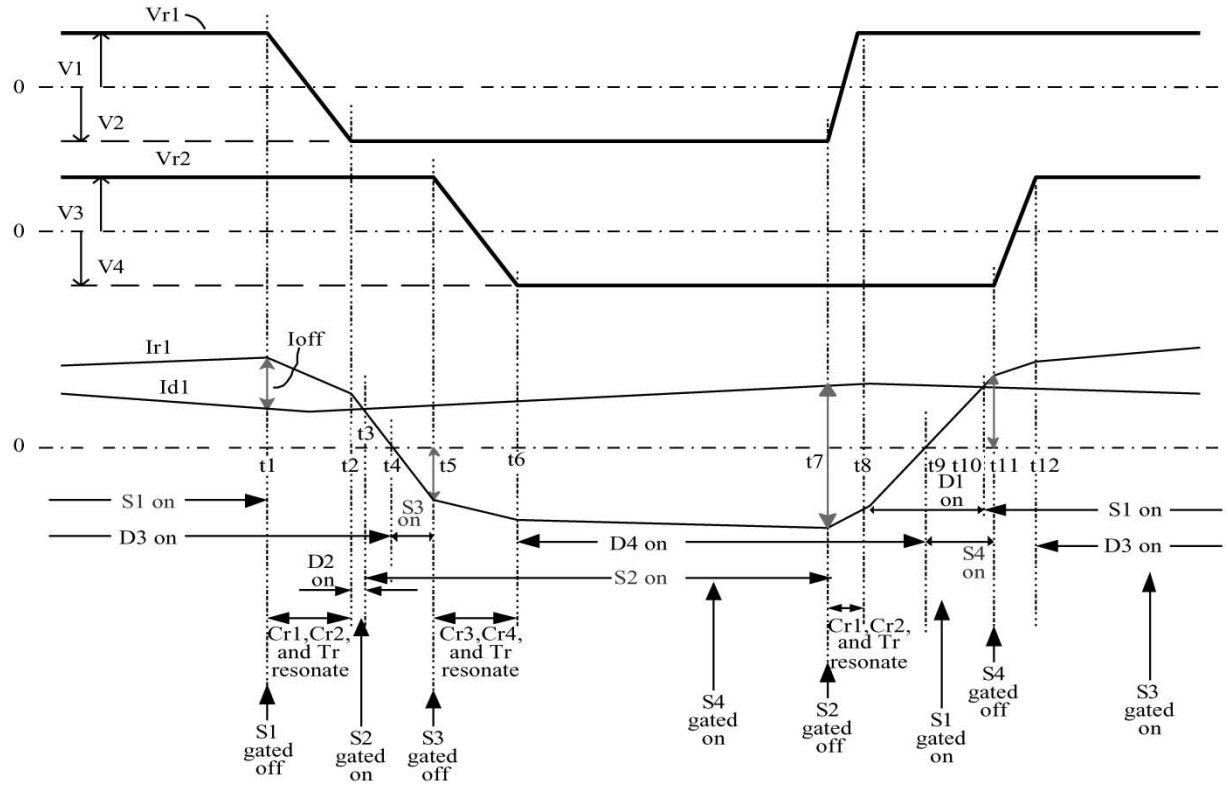

Fig. 6. Waveforms and switching timing of boost mode.

Step 10) $(t_9 - t_{10})$: From t_9 to t_{10}, I_{r1} begins to change its polarity and continue to increase until it equals I_{d1}. The current is commutated from D4 to S4.

Step 11) $(t_{10} - t_{11})$: From t_{10} to t_{11}, I_{r1} begins to exceed I_{d1}. The current is transferred from D1 to S1.

Step 12) $(t_{11} - t_{12})$: At t_{11}, S4 is gated to turn off. C_{r3} and C_{r4} begin to be charged and discharged again. The charge/discharge rate depends mainly on the magnitude of I_{r1} at t_{11}.

Step 13) $(t_{12} - t_{13})$: At t_{12}, when V_{cr3} attempts to overshoot the positive rail, D3 is forward biased. The circuit returns to the original steady state. During this period, S3 can be gated on any time at zero voltage.

Commutation in the proposed circuit is similar to the diode-to-switch commutation mode of the ARCP inverter [14], i.e., turn-off of the main conducting device diverts the current to the corresponding resonant capacitors to charge one and discharge the other, resulting in a zero voltage turn-off. The zero voltage turn-on is achieved by gating on the in-coming device while the anti-parallel diode is conducting. However, unlike ARCP inverter, the proposed circuit does not require an auxiliary circuit to achieve soft switching. From Fig. 6, it is clear that the conditions of soft switching in boost mode depend on the magnitude of I_{r1} and I_{d1} at t_1, t_5, t_7 and t_{11}, respectively. This is summarized as

$$\begin{cases} I_{r1}(t_1) > I_{d1}(t_1) \\ I_{r1}(t_5) < 0 \\ I_{r1}(t_7) > I_{d1}(t_7) \\ I_{r1}(t_{11}) > 0. \end{cases} \tag{1}$$

For boost mode, it is observed that rate of change of the voltage of S1 and S2 at t_1 is different from that at t_7. This

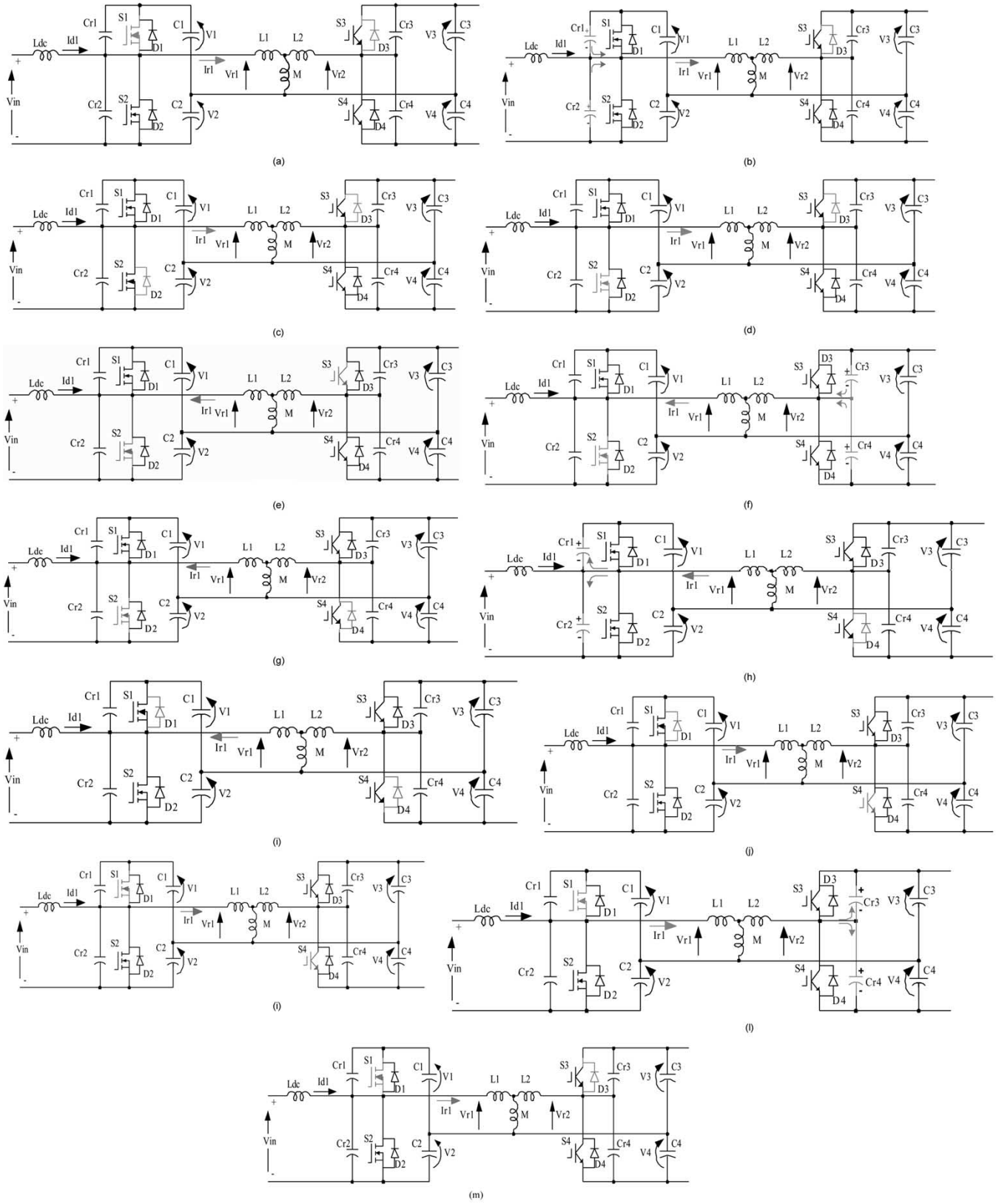

Fig. 7. Commutation step diagrams during a switching cycle in boost mode: (a) Step 1: Current path before t_1, (b) Step 2: Current path between $t_1 - t_2$, (c) Step 3: Current path between $t_2 - t_3$, (d) Step 4: Current path between $t_3 - t_4$, (e) Step 5: Current path between $t_4 - t_5$, (f) Step 6: Current path between $t_5 - t_6$, (g) Step 7: Current path between $t_6 - t_7$, (h) Step 8: Current path between $t_7 - t_8$, (i) Step 9: Current path between $t_8 - t_9$, (j) Step 10: Current path between $t_9 - t_{10}$, (k) Step 11: Current path between $t_{10} - t_{11}$, (l) Step 12: Current path between $t_{11} - t_{12}$, and (m) Step 13: Current path after t_{12} (one cycle completes).

is because the turn-off currents are different at their switching instants. Similarly, devices S3 and S4 have different voltage change rates at t_5 and t_{11}. Comparing these four voltage slopes, dv/dt at t_1 and dv/dt at t_7 represent the minimum and max-

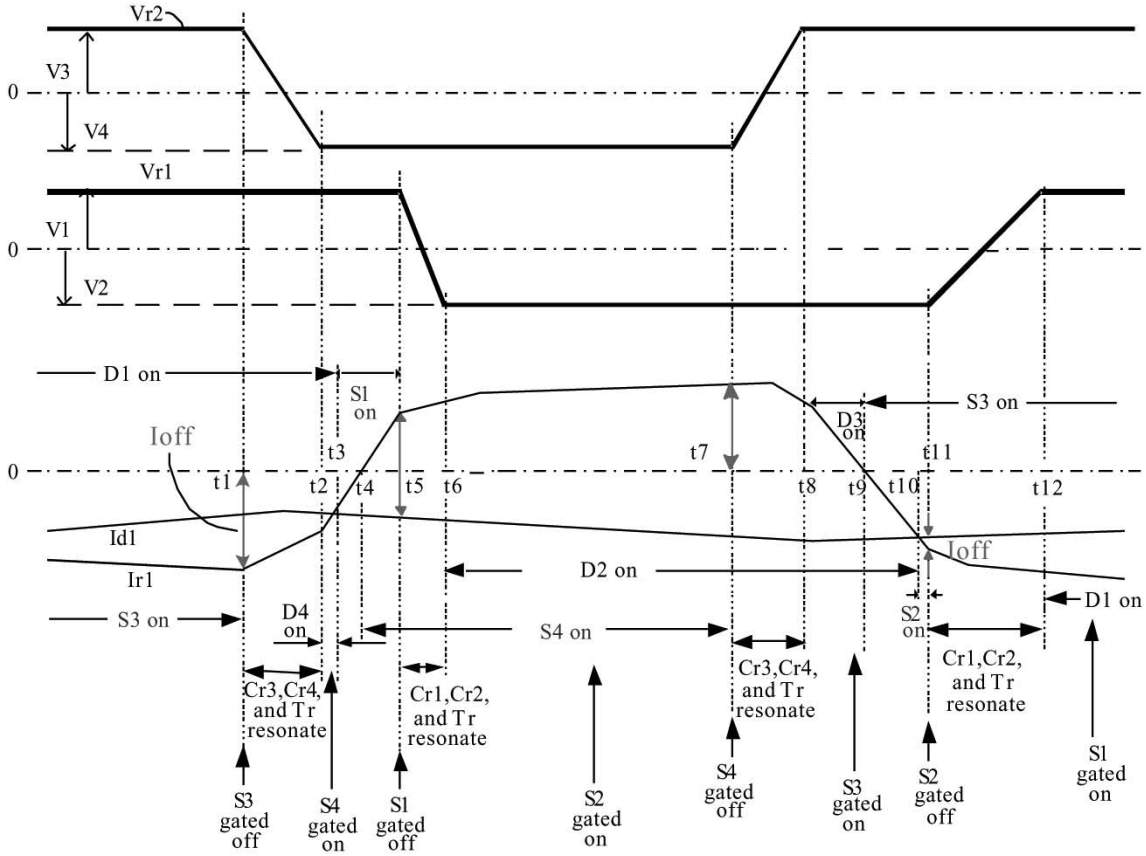

Fig. 8. Waveforms and switching timing of buck mode.

imum, respectively, because the turn-off current is minimum at t_1 and maximum at t_7. As a result, the allowable minimum and maximum dv/dt should be designed according to application requirements.

B. Buck Mode

Because the half-bridge topology of the two sides is symmetrical, the operation principles in buck mode are similar to those in boost mode. Fig. 8 describes one switching cycle in buck mode. Due to the reversed power-flow direction, the phase of V_{r2} is leading V_{r1}. In addition, the inductor current I_{d1} is reversed. The buck mode operation can also be divided into thirteen steps. The description of each step can be analogously inferred and will not be discussed here.

Like boost mode, the soft-switching conditions in buck mode can be derived similarly as

$$\begin{cases} I_{r1}(t_1) < 0 \\ I_{r1}(t_5) > I_{d1}(t_5) \\ I_{r1}(t_7) > 0 \\ I_{r1}(t_{11}) < I_{d1}(t_{11}). \end{cases} \tag{2}$$

IV. Design Guidelines

A. Transformer

The transformer has three functions in the proposed converter.

1) It isolates the LVS and HVS.
2) It boosts the voltage of HVS.
3) The leakage inductance of the transformer is used as an energy storage and transfer element.

The turns-ratio selection of transformer is easy and based on the voltage ratio of the HVS over the LVS. The selection of leakage inductance will be presented in the following.

In order to find the right leakage inductance value, the transfer power must be derived first. If no loss is considered in the converter, the transfer power equals to output power. The derivation of output power is based on the primary-referred equivalent circuit and the idealized waveforms in Fig. 3.

The phase shift between the two voltage waveforms of Fig. 3 is ϕ_1. The transformer current I_{r1} is a function of $\theta = \omega t$, where ω is the switching frequency. There are four operation modes in one switching period. In mode I

$$I_{r1}(\theta) = \frac{V_1 + V_4}{\omega L_s}\theta + I_{r1}(0) \tag{3}$$

where V_1 and V_4 are voltages across C_1 and $C_4, I_{r1}(0)$ is the initial current of I_{r1} at $\theta = 0$. Mode I ends at $\theta = \phi_1$. In mode II

$$I_{r1}(\theta) = \frac{V_1 - V_3}{\omega L_S}(\theta - \phi_1) + I_{r1}(\phi_1). \tag{4}$$

Similarly, the current in mode III can be found to be

$$I_{r1}(\theta) = \frac{-V_2 - V_3}{\omega L_S}(\theta - \phi_2) + I_{r1}(\phi_2) \tag{5}$$

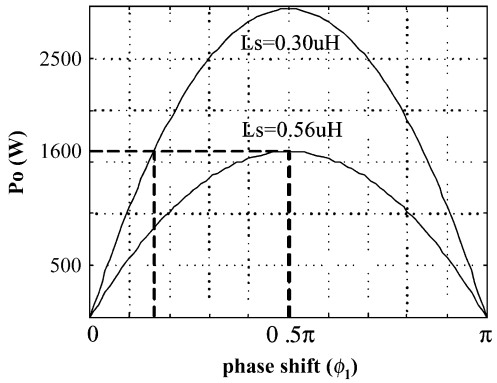

Fig. 9. Output power, ϕ_1 and leakage inductance L_S.

and the current in mode IV is

$$I_{r1}(\theta) = \frac{-V_2 + V_4}{\omega L_S}(\theta - \phi_1 - \phi_2) + I_{r1}(\phi_1 + \phi_2). \quad (6)$$

From the representation of $I_{r1}(\theta)$, the output power can be found to be

$$P_O = \frac{\int_0^{T_S} I_{r1} V_{r1} dt}{T_S} = \frac{\phi_1 \frac{1}{D}\left[4\pi(1-D) - \frac{1}{D}\phi_1\right]}{4\pi\omega L_S} \cdot V_{\text{in}}^2 \quad (7)$$

where T_s is the period of the switching frequency and $D = \phi_2/2\pi$. The output power (output voltage) can be regulated by phase shift angle ϕ_1 duty cycle D and switching frequency ω.

If $D = 50\%$ is assumed and the switching frequency is set at 20 kHz, then the output power equation can be simplified further to

$$P_O = \frac{V_{\text{in}}^2}{\omega L_s} \frac{\phi_1(\pi - \phi_1)}{\pi}. \quad (8)$$

According to (8), when duty cycle and switching frequency are fixed, the output power is related to phase shift angle and leakage inductance of transformer.

If the output power is chosen to be 1.6 kW for example, Fig. 9 illustrates the output power curves of $L_S = 0.56$ μH and $L_S = 0.30$ μH. It is interesting to notice that if the leakage inductance is selected differently, the phase shift angle of the same output power is changed. The smaller leakage inductance results in the smaller the phase shift angle. It will find out later that different phase shift angle will have different current stresses over the devices. Therefore, the leakage inductance of the transformer can be designed according to the expected phase shift angle at the required power rating to reduce current stresses.

Suppose the maximum output power is P_O, the input dc voltage is V_{in}, the switching frequency is ω, the expected phase shift angle at P_O is ϕ_1, L_S can be calculated as

$$L_S = \frac{V_{\text{in}}^2 \cdot \phi_1 \cdot (\pi - \phi_1)}{P_O \cdot \omega\pi}. \quad (9)$$

Fig. 9 shows that the leakage inductance L_S shall not be greater than 0.56 μH in order to deliver a maximum power of 1.6 kW.

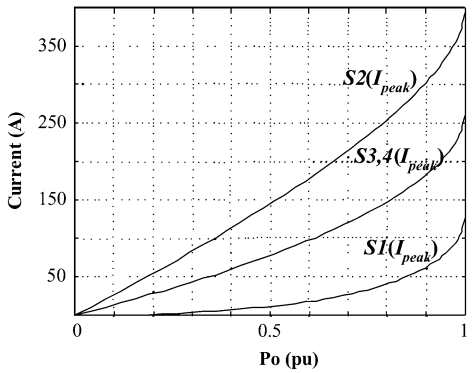

Fig. 10. Current stresses of devices versus output power.

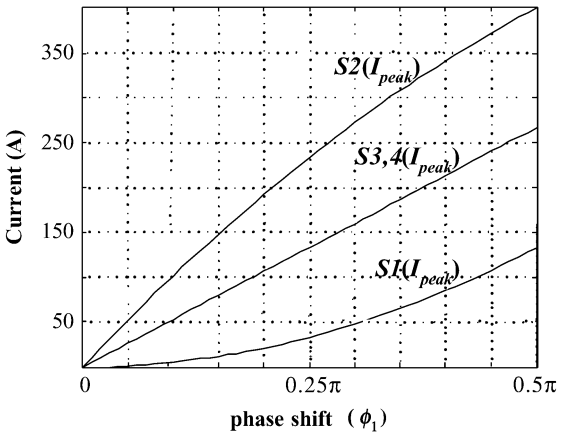

Fig. 11. Current stresses of devices versus phase shift ϕ_1.

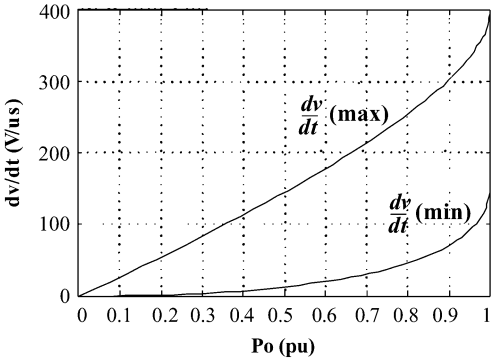

Fig. 12. The dv/dt range versus output power.

B. Input Inductor L_{dc}

The average current I_{d1} provided by the power supply can be found to be

$$I_{d1} = \frac{P_O}{V_{\text{in}}}. \quad (10)$$

If ΔI of I_{d1} is selected according to the system requirements, then L_{dc} is designed to be

$$L_{\text{dc}} = \frac{V_{\text{in}} \cdot \Delta t}{\Delta I} \quad (11)$$

where ΔI is the ripple current and Δt is the turn on time interval of S2 during each switching cycle.

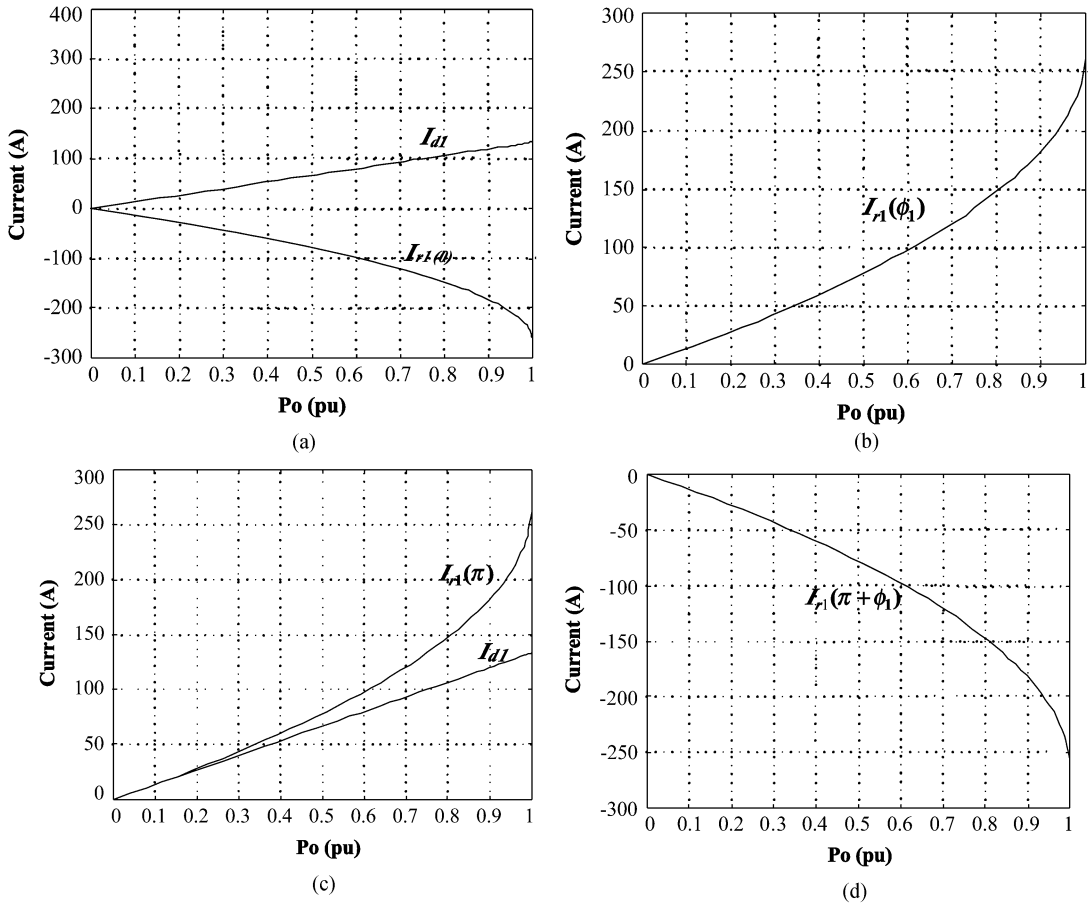

Fig. 13. Soft-switching conditions versus output power of $L_S = 0.56\ \mu$H: (a) I_{d1} and $I_{r1}(0)$ versus output power, (b) $I_{r1}(\phi_1)$ versus output power, (c) $I_{d1}, I_{r1}(\pi)$ versus output power, and (d) $I_{r1}(\pi + \phi_1)$ versus output power.

C. Power Device

The voltage and current peak values and the dv/dt range are the interesting design topics for devices.

Referred to Fig. 3, the initial states $I_{r1}(0), I_{r1}(\phi_1), I_{r1}(\phi_2), I_{r1}(\phi_2 + \phi_1)$ of current I_{r1} during one complete switching cycle can be derived based on the boundary conditions

$$\begin{aligned} I_{r1}(0) &= -I_{r1}(\phi_2) \\ I_{r1}(\phi_1) &= -I_{r1}(\phi_2 + \phi_1). \end{aligned} \tag{12}$$

When $D = 50\%, \phi_2 = \pi$, the initial conditions of I_{r1} are calculated in

$$\begin{cases} I_{r1}(0) = \frac{V_3 - V_1}{2\omega L_S}(\pi - \phi_1) - \frac{V_1 + V_4}{2\omega L_S}\phi_1 \\ I_{r1}(\phi_1) = \frac{V_1 + V_4}{2\omega L_S}\phi_1 + \frac{V_3 - V_1}{2\omega L_S}(\pi - \phi_1) \\ I_{r1}(\pi) = -I_{r1}(0) \\ I_{r1}(\pi + \phi_1) = -I_{r1}(\phi_1). \end{cases} \tag{13}$$

The device rating of LVS can be calculated as

$$\begin{aligned} I_{\text{peak}} &= I_{d1} - I_{r1}(0) \\ V_{\text{peak}} &= 2V_{\text{in}}. \end{aligned} \tag{14}$$

The HVS devices design can be derived similarly.

Fig. 10 shows the current stress of the main switches of the low voltage side and the high voltage side against output power in per unit (pu) with the base value of 1.6 kW as an example. The current stress of high voltage side is calculated based on the primary-preferred circuit. Fig. 11 plots the current stress as a function of phase shift ϕ_1 instead of output power.

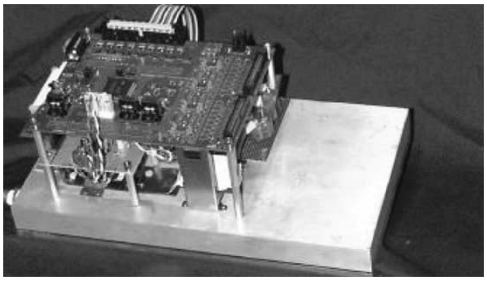

Fig. 14. Photo of the prototype.

An interesting feature can be brought to light by examining Fig. 11, which shows that the current stresses of the devices are proportional to the phase shift angle. As a result, if the phase shift is decreased for the same output power, the current stress becomes less. This is important to improve the system efficiency because the power losses are closely related to the current stress.

One important feature of soft switching over hard switching is the soft dv/dt. However, the dv/dt cannot be too soft or too hard otherwise it will cause other problems. Unlike ARCP inverter, in which the dv/dt can be controlled as a fixed desired value with the price of using an auxiliary switch and complicated control,

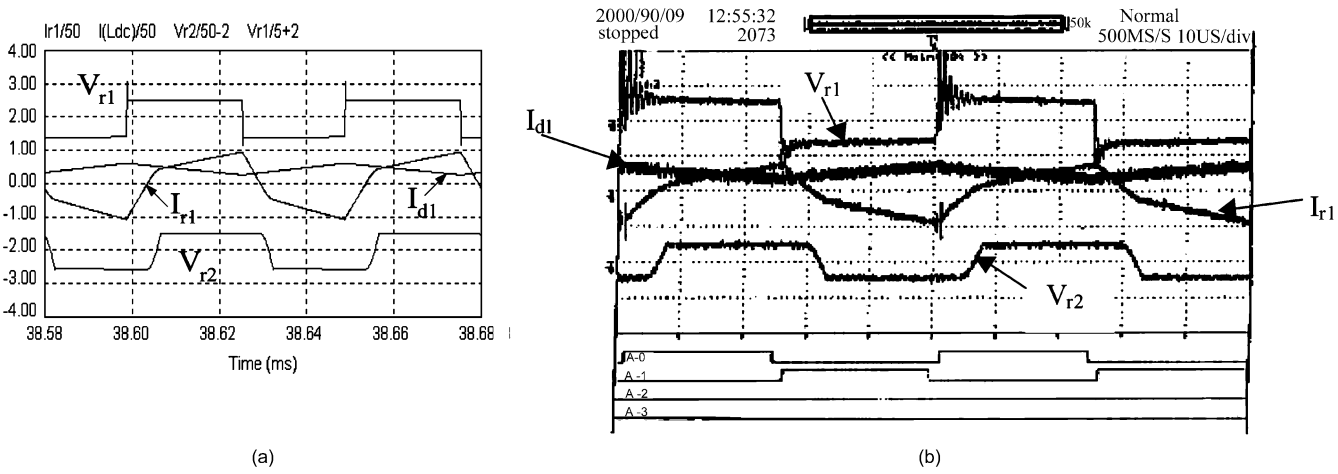

Fig. 15. Steady state operation of boost mode ($v_b = 3$ V): (a) simulation results of V_{r1} (5 V/div), I_{d1} (50 A/div), I_{r1} (50 A/div), V_{r2} (50 V/div) and (b) experimental results of V_{r1} (5 V/div), I_{d1} (50 A/div), I_{r1} (50 A/div), V_{r2} (50 V/div).

the dv/dt of the proposed converter is not a fixed value. However, by selecting right circuit components, the dv/dt range can be carefully designed to meet the requirements. Based on the analysis in the previous section, the maximum and minimum voltage change rates happened at $\theta = 0$ and $\theta = \pi$, respectively. The corresponding turn-off currents are calculated as

$$I_{\text{off}}|_{\max,\theta=0} = |I_{r1}(0)| + |I_{d1}|, I_{\text{off}}|_{\min,\theta=\pi} = |I_{r1}(\pi)| - |I_{d1}|.$$

Assuming resonant capacitors are selected as 1 μF, $I_{\text{off}} = C_{r1} \cdot dv/dt$, the range of dv/dt in V/μs is derived as

$$\frac{I_{\text{off}}|_{\min}}{1\mu F} \le \frac{dv}{dt} \le \frac{I_{\text{off}}|_{\max}}{1\mu F}. \tag{15}$$

Again, if 1.6 kW output power is selected as the base value, Fig. 12 plots the $dv/dt(\max)$ and $dv/dt(\min)$ over the whole power range.

D. ZVS Range

For some uni-directional ZVS phase shift full bridge topology, ZVS conditions cannot be met in low output power range. The devices will go through hard switching at light load and this will cause some serious problems [15]. For the proposed converter, the problem does not exist at least for the steady state operation. The soft switching conditions in boost mode and buck mode will be re-shown here

$$\text{boost} \begin{cases} I_{r1}(0) - I_{d1} < 0 \\ I_{r1}(\phi_1) > 0 \\ I_{r1}(\pi) - I_{d1} > 0 \\ I_{r1}(\pi + \phi_1) < 0 \end{cases} \quad \text{and} \quad \text{buck} \begin{cases} I_{r1}(0) > 0 \\ I_{d1} > I_{r1}(\phi_1) \\ I_{r1}(\pi) < 0 \\ I_{r1}(\pi + \phi_1) > I_{d1}. \end{cases} \tag{16}$$

Fig. 13(a)–(d) plots the input current, transformer current over the full output power range when transformer leakage inductance is selected as 0.56 μH. The purpose of Fig. 13 is to show that the soft-switching condition is satisfied during the whole operating range. According to (16), soft switching is maintained at any output power in the boost mode. Soft switching of the buck mode can be similarly inferred.

V. Experimental and Simulation Verifications

A 1.6 kW soft-switched bidirectional dc-dc converter has been built and experimentally tested to validate the soft switching analysis. The prototype is pictured in Fig. 14. The overall size is about 7.25″ width and 8.5″ in length. Compared to a full bridge counterpart converter that was developed previously at the lab, the size of the converter is saved more than 1/3, which shows the high power density feature. The size saving was mainly from less current stress, less gate drive circuit, and higher efficiency (94% versus 92%). As described previously, the new converter has the same primary current rating of the transformer as the full bridge converter. The primary current of the transformer flows through only one MOSFET at any time instead of two in the full bridge converter. This resulted in a great efficiency improvement, because the conduction loss is a major power loss. The switching loss is minimized due to soft switching.

A. Boost Mode Verification

The experimental results and circuit simulation results of steady-state performance in boost mode are obtained in Fig.15. There is a good agreement between simulation results and experimental results. The converter is operating at 20 kHz. The limitation of 20 kHz switching is limited by the high voltage side IGBTs and efficiency considerations. For inductor current I_{d1} and transformer current I_{r1}, the wave shapes of simulation and those of experiment agree with each other. In addition, the peak values of I_{r1} in simulation are $+45$ A and -55 A and those of experimental values are $+40$ A and -50 A. The average value of I_{d1} in (a) is about 22 A and that of (b) is 25 A. The magnitude of V_{r2} in simulation is 26 V, the experimental magnitude is also about 26 V. In addition, there are also similarities in shape and frequency of V_{r2}. The phase shift angle between V_{r1} and V_{r2} in the two figures are consistent. Although the magnitude and the shape of V_{r1} are almost the same in the two figures, the experimental result of V_{r1} waveform has a ringing effect. This is because it is hard to measure directly the two terminals of the primary side of the transformer, consequently the measurement loop

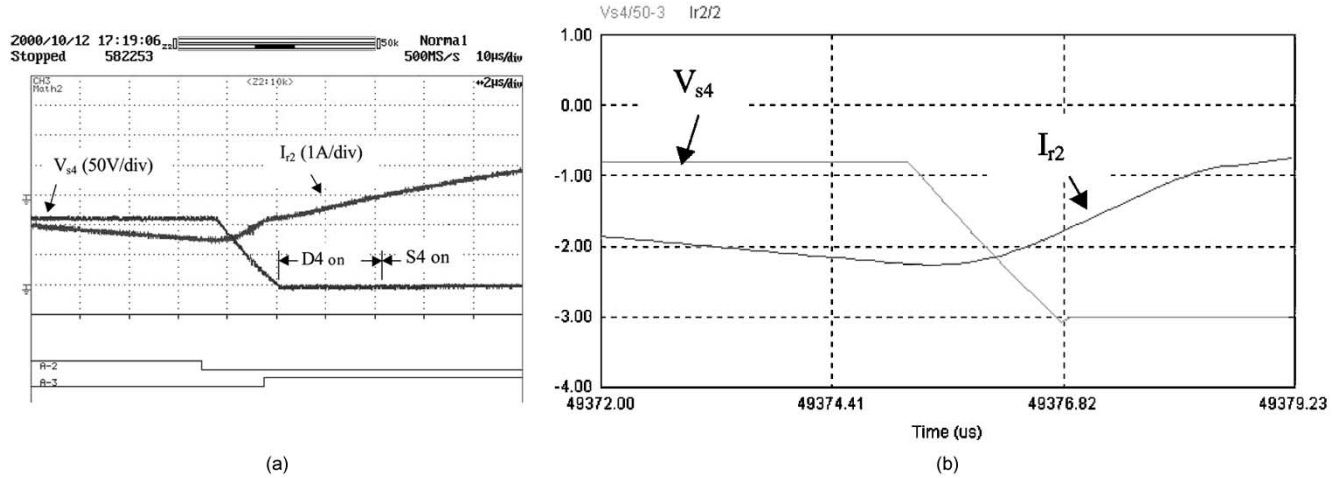

Fig. 16. Zero voltage turn on of S4 in buck mode. (a) Experimental zero-voltage turn on of S4 in buck mode and (b) simulation zero-voltage turn on of S4 in buck mode.

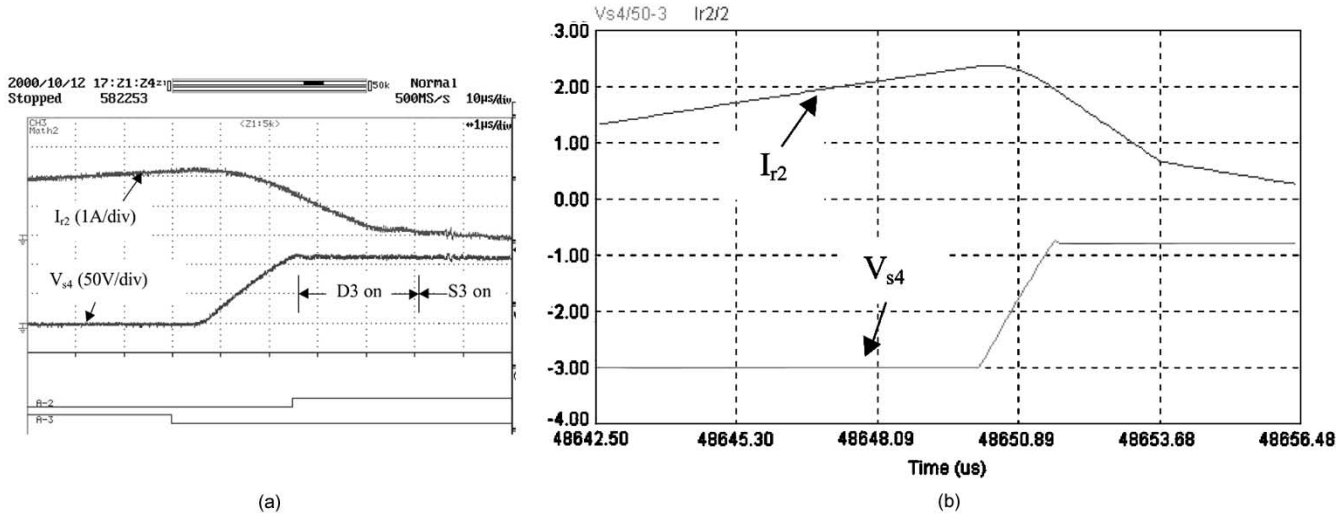

Fig. 17. Zero voltage turn off of S4 in buck mode. (a) Experimental zero-voltage turn off of S4 in buck mode and (b) simulation zero-voltage turn off of S4 in buck mode.

for current may be the main reason for this ringing effect. This extra current measurement loop (about 2 in long) is significant compared with the transformer that has only two turns in the primary. In this and next sections to verify the boost and buck mode operation, only low input voltage was applied.

The soft switching operation, which was depicted in Fig. 6 and Fig. 7, is also confirmed from the experimental results. When S2 is gated off, the sum of I_{r1} and I_{d1} charges and discharges resonant capacitors C_{r1} and C_{r2}, respectively. As a result, V_{r1} changes from -2.5 V to $+2.5$ V with a limited dv/dt of 160 V/μs. The transient peak voltage is mainly due to the parasitic inductance of the measured loop. Although S1 is given an "on" signal after 1.5 μs when S2 is gated off, D1 is conducting the current at this moment until I_{r1} increases to I_{d1}. When I_{r1} is bigger than I_{d1}, the current is diverted from D1 to S1 and S1 is turned on at zero voltage. The soft-switching process can be derived similarly when S1 is gated off. Because the turn off current is 20 A at this moment, the dv/dt of V_{r1} is 40 V/μs. S3 and S4 are operating in the diode rectification mode.

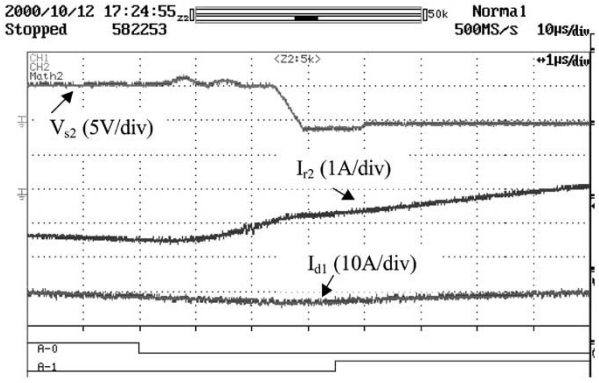

Fig. 18. Zero voltage turn on of S2 in buck mode.

B. Buck Mode Verification

The details of switching process of S1 to S4 in buck mode are demonstrated from Figs. 16–18 at the following conditions. The voltage source of the high voltage side is 116 V. The load resistance of the low voltage side is a 0.1 Ω. The phase shift

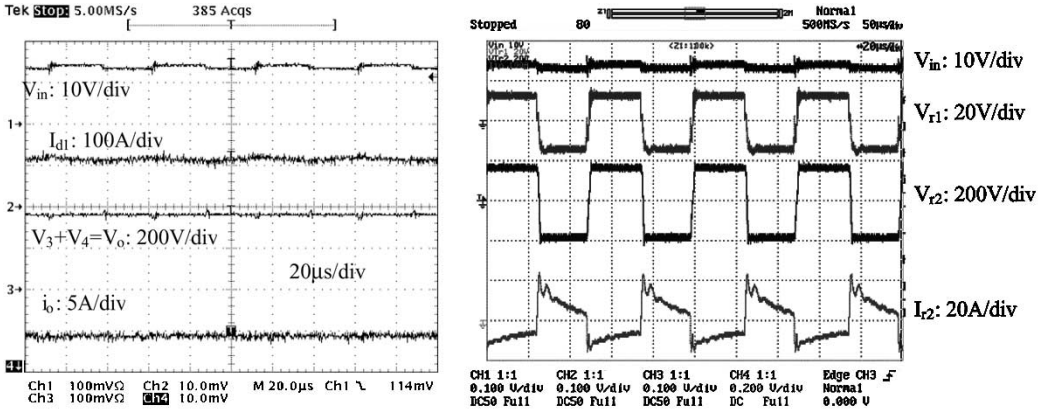

Fig. 19. Steady state waveforms in low-to-high conversion mode; load power: 1.42 kW, efficiency: 92.5%: (a) input, output current and voltage waveforms and (b) transformer current and voltage waveforms.

angle of S3 leading to S1 is 0.04 π, namely 1 μs under 20 kHz switching frequency. The leakage inductance of the transformer is 0.4 μH.

In Fig. 16, the experimental zero-voltage turn on of S4 is shown in (a), and the simulation waveforms are shown in (b) for comparison. There is a good agreement between (a) and (b). When S3 is gated off, I_{r2} is negative. The resonant capacitors C_{r3} and C_{r4} are charged and discharged, respectively. The calculated dv/dt is 46 V/μs, the experimental value is 45 V/μs. After V_{S4} is discharged to the negative value, D4 is on. During this period, S4 receives an "on" signal. When I_{r2} changes the polarity, the current is diverted from D4 to S4, S4 is turning on at zero voltage.

In Fig. 17, the details of zero-voltage turn off of S4 are shown. When S4 is gated off, I_{r2} is positive. The resonant capacitors C_{r3} and C_{r4} are discharged and charged, respectively. The calculated dv/dt is 60 V/μs, the experimental value is 58 V/μs. After V_{S3} is discharged to the negative value, D3 is on and V_{s4} increases to 116 V without an obvious overshoot. With this limited dv/dt of turn off voltage across S4, the switching loss at turn off can be regarded as negligible or zero. The soft switching of S3 can be derived symmetrically. In addition, zero voltage turn on of S2 is inferred from Fig. 18. Comparing Fig. 8 with Figs. 16–18, there is a good agreement between experimental results, simulation waveforms and the operation principles analysis.

C. Full Load Operation

Typical oscillograms in boost mode, i.e., charging the high voltage side from the low voltage at full rated input voltage, are given in Fig. 19. Fig. 19(a) shows, from the top toward the bottom, the low side input voltage, $V_{\rm in}$, input current, I_{d1}, high side output voltage, V_o, output current, I_o, and (b) shows $V_{\rm in}$, the transformer primary side voltage, V_{r1}, secondary voltage, V_{r2} and current, I_{r2}. Fig. 20 plots an efficiency chart in the boost mode. Efficiency is above 92% over a wide range of output power form 0.45 kW to 1.4 kW [16]–[22].

VI. Conclusion

A new soft-switched isolated bidirectional dc–dc converter has been presented in this paper. The operation, analysis, features and design consideration were illustrated. Simulation and experimental results for the 1.6 kW, 20 kHz prototype were shown to verify the operation principle.

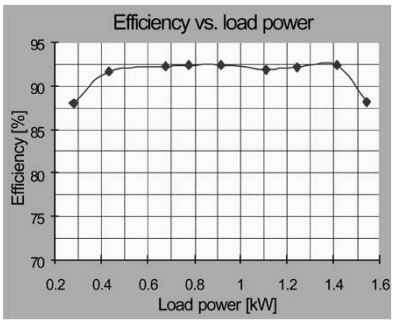

Fig. 20. Efficiency chart.

It is shown that ZVS in either direction of power flow is achieved with no lossy components involved, no additional active switch, no additional TDR exhibited. Thanks to the dual functions (simultaneous boost conversion and inversion) provided by the low voltage side half bridge, current stresses on the switching devices and transformer are kept minimum. As results, advantages of the new circuit including ZVS with full load range, decreased device count, high efficiency (measured more than 94% at rated power), and low cost as well as less control and accessory power needs, make the proposed converter very promising for medium power applications with high power density.

References

[1] K. Wang *et al.*, "Bidirectional dc to dc converters for fuel cell systems," in *Proc. IEEE Workshop Power Electron. Transport*, 1998, pp. 47–51.

[2] ——, "Design, implementation, and experimental results of bidirectional full-bridge dc-dc converter with unified soft-switching scheme and soft-starting capability," in *Proc. IEEE Power Electron. Spec. Conf.*, 2000, pp. 1058–1063.

[3] T. Reimann, S. Szeponik, G. Berger, and J. Petzoldt, "A novel control principle of bidirectional dc-dc power conversion," *Proc. IEEE Power Electron. Spec. Conf.*, pp. 978–984, 1997.

[4] R. W. DeDonker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft- switched high power density dc-dc converter for high power applications," *IEEE Trans. Ind. Applicat.*, vol. 27, pp. 63–73, Jan./Feb. 1991.

[5] E. Deschamps and I. Barbi, "A flying-capacitor ZVS 1.5 kW dc-to-dc converter with half of the input voltage across the switches," *IEEE Trans. Power Electron.*, vol. 15, pp. 855–860, Sept. 2000.

[6] H. L. Chan, K. Cheng, and D. Sutanto, "An extended load range ZCS-ZVS bidirectional phase-shift dc–dc converter," in *Proc. 8th Int. Conf. Power Electron. Variable Speed Drives*, 2000, pp. 74–79.

[7] H. Chung *et al.*, "A ZCS bidirectional flyback dc–dc converter using the leakage inductance of the coupled inductor," in *Proc. IEEE APEC Conf.*, 2000, pp. 979–985.
[8] M. Jain, P. K. Jain, and M. Daniel, "A bidirectional dc–dc converter topology for low power application," in *Proc. IEEE Power Electron. Spec. Conf.*, 1997, pp. 804–810.
[9] C. Ianello *et al.*, "Full bridge ZCS PWM converter for high-voltage high-power applications," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, pp. 515–526, Apr. 2002.
[10] S. Hamada *et al.*, "A novel zero-voltage and zero-current switching PWM dc–dc converter with reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 17, pp. 413–419, May 2002.
[11] J. Zhang *et al.*, "A novel ZVS dc–dc converter for high power applications," in *Proc. IEEE APEC Conf.*, 2002, pp. 635–640.
[12] R. Ayyanar *et al.*, "Novel soft-switching dc–dc converter with full ZVS-range and reduced filter requirement. I. Regulated-output applications," *IEEE Trans. Power Electron.*, vol. 16, pp. 184–192, Mar. 2001.
[13] R. Torrico-Bascop *et al.*, "A double ZVS-PWM active-clamping forward converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 16, pp. 745–751, Nov. 2001.
[14] R. W. DeDonker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE IAS Annu. Meeting Conf.*, 1990, pp. 1228–1235.
[15] A. Fiel *et al.*, "MOSFET failure modes in the zero-voltage-switched full-bridge switching mode power supply applications," in *Proc. IEEE APEC Conf.*, 2001, pp. 1247–1252.
[16] H. Watanabe and H. Matsuo, "Analysis of a novel soft-switching dc–dc converter with low output voltage," in *Proc. IEEE PESC*, Galway, Ireland, June 18–23, 2000.
[17] H. Watanabe, H. Hatakeyama, and T. Ishikawa, "Boost half-bridge power supply," Tech. Rep. IEICE, EE98-17, July 1998.
[18] E. Romanello and I. Barbi, "A new isolated phase-shift controlled non-pulsating input-output current converter," in *Proc. IEEE PESC*, 2001, pp. 237–242.
[19] ——, "An isolated ZVS-PWM active clamping nonpulsating input and output dc–dc converter," in *Proc. IEEE PESC*, 2000, pp. 205–210.
[20] J. Zeng, J. Ying, and Q. Zhang, "A novel DC/DC ZVS converter for battery input applications," in *Proc. IEEE APEC*, vol. 2, 2002, pp. 892–896.
[21] C. Choi, C. Kim, F. S. Kang, and S. J. Park, "Zero voltage and zero current switching single-stage power factor correction ac–dc half-bridge converter with low cost," in *Proc. IEEE IECON*, vol. I, 2000, pp. 313–319.
[22] J. Y. Lee, G. W. Moon, and M. J. Youn, "Design of high-quality AC/DC converter with high-efficiency based on half-bridge topology," in *Proc. IEEE PESC*, June 1998, pp. 1054–1060.

Fang Zheng Peng (M'92–SM'96) received the B.S. degree in electrical engineering from Wuhan University, China, in 1983 and the M.S. and Ph.D. degrees in electrical engineering from Nagaoka University of Technology, Japan, in 1987 and 1990, respectively.

He joined Toyo Electric Manufacturing Company, Ltd., from 1990 to 1992 as a Research Scientist, was engaged in research and development of active power filters, flexible ac transmission systems (FACTS) applications and motor drives. From 1992 to 1994, he worked with the Tokyo Institute of Technology, Tokyo, Japan, as a Research Assistant Professor, initiated a multilevel inverter program for FACTS applications, and a speed-sensorless vector control project. From 1994 to 2000, he worked for Oak Ridge National Laboratory (ORNL), as a Research Assistant Professor at University of Tennessee, Knoxville, from 1994 to 1997 and was a Staff Member, Lead (principal) Scientist of the Power Electronics and Electric Machinery Research Center, ORNL, from 1997 to 2000. In 2000, he joined Michigan State University, East Lansing, as an Associate Professor of the Department of Electrical and Computer Engineering. He holds 10 patents.

Dr. Peng received the 1996 First Prize Paper Award and the 1995 Second Prize Paper Award of Industrial Power Converter Committee from the IEEE/IAS Annual Meeting; the 1996 Advanced Technology Award from the Inventors Clubs of America, Inc., the International Hall of Fame; the 1991 First Prize Paper Award in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, the 1990 Best Paper Award in the Transactions of the Institute of Electrical Engineers of Japan, and the Promotion Award of Electrical Academy. He has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1997 and Chair of Technical Committee for Rectifiers and Inverters of IEEE Power Electronics Society.

Hui Li (S'97–M'00–SM'01) received the B.S. and M.S. degree in electrical engineering from Huazhong University of Science and Technology, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Tennessee, Knoxville, in 2000.

From 1999 to 2000, she worked for the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory, on developing soft-switching power converter for hybrid electric vehicle, uninterrupted power supply and motor drive application. In 2001, she joined Tyco Electronics working on high efficiency high power density rectifier and dc–dc converter. Currently, she is an Assistant Professor with the Electrical and Computer Engineering Department, Florida State University, Tallahassee. Her research interests include soft-switching converters, motor drive control, modeling and simulation of power electronics system, and application of new power semiconductor devices.

Gui-Jia Su (M'93–SM'01) received the B.S. degree in electrical power system engineering from Wuhan University of Hydraulic and Electrical Engineering, Wuhan, China, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1989 and 1992, respectively.

He was an Assistant Professor from 1992 to 1995 at Nagaoka University of Technology. From 1995 to 1998, he was with Sanken Electrical Co., Ltd., Kawagoe, Japan, where he has engaged in research and development of uninterruptible power supply, sensorless PM motor drive, and power factor correction for single- and three-phase rectifiers. Since 1998, he has been with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory (ORNL), as a Research Scientist with the Oak Ridge Associated Universities and then joined ORNL as a Staff Engineer in 2000. He is currently a Senior R&D Staff Member and holds the position of Lead Engineer in power electronics at ORNL. His current research interests include high power dc/dc converter, inverter, motor drive, and power electronics system packaging and thermal management for electric/hybrid electric vehicle applications.

Jack S. Lawler (S'78–M'79–SM'85) received the B.S.E.E., M.S., and Ph.D. degrees in systems science from Michigan State University, East Lansing, in 1971, 1972, and 1979, respectively.

Since 1979, he has been with the Department of Electrical and Computer Engineering, University of Tennessee, Knoxville, and holds the rank of Professor. He teaches courses in electric power systems engineering and power electronics. His research interests include power system operations and electric and hybrid/electric vehicles. He is especially interested in traction applications that require very large constant power speed range.