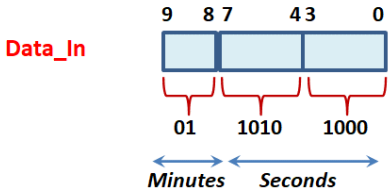
Instructions for Lab – 3

Thu. 1 April and Tue 20 April and Thu. 23 April (2-3:45 pm)

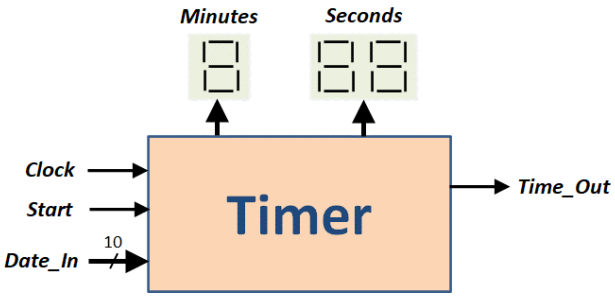
[5 Marks]

(This lab can be done by 2 or 3 students in one group).

The aim of this lab is to design a simple programmable timer, which can display minutes and seconds (up to 3 minutes and 59 seconds) and implement it on DE0 FPGA board.
The output of this timer is connected to 7-segment displays as shown below. Output signal ***Time_Out*** will change from '0' to '1' when the specified time elapsed (or in other words when the timer times out) and it is displayed on one LED on DE0 board. The timer is initialized through ***Data_In*** input, which is connected to ***10 switches*** on DE0 board and the 10 switches positions determines the required time. For example, if the switches are set as **"01 0010 1000"** that means the required time is ***1 minute and 28 seconds***. Note that bits **3 to 0** and bits **7 to 4** each represent a BCD number as shown below. If the related switches (for group bits 3 to 0 or 7 to 4 are set mistakenly to indicate a 4-bit binary value bigger than 1001, then it should be either considered as an invalid input number by the digital or if it is easier just consider it as 1001).



The timer starts working from the specified time value (which is through ***Data_In*** input and displayed on seven segments) towards 0, when input ***Start*** (a push button switch on DE0) is pressed. The count values from the beginning to 0 are displayed on the three seven-segment displays on DE0 board.



Hint: *Note that the input clock frequency in DE0 FPGA board is 50 MHz. So, you need to have clock frequency of 1 Hz for your timer. This can be done by designing a component (which will be placed between the input clock pin from DE0 and your timer clock needed to provide the required frequency).*

(a) Design a one-digit BCD counter (or use your designed component from Lab-2) as a component and make proper connections to design the timer. Note that the code for one-digit BCD counter should be **synthesizable**. You may make

the connections in this system through using "schematic diagram design entry" in Quartus II (or write the required VHDL code for structural description of the system).
The BCD to Seven Segment display converter code may be used from lecture notes if needed. (Note that each segment on DE0 board 7-segment displays should be **'0'** in order to make that segment on).

(b) Write a testbench to test your code for the timer system and test it using ModelSim. (**You may use a clock generator with frequency of 1 Hz in your testbench for the main component or use 50 MHz for the whole system**).

(c) Do the required pin assignments (with TA helps in the lab) to make proper connections to switches, push button LED and seven-segment displays on DE0 board in Quartus II tool. Then synthesize your code for the target device **Cyclone III EP3C16F484** and determine how many logic elements (LE) are used for your design.

(d) Download the generated FPGA bit-stream to program DE0 board.

Refer to Chapter 4 of DE0 board manual (especially pages 22 to 26) for more details about the board and FPGA pin assignments used in this lab.