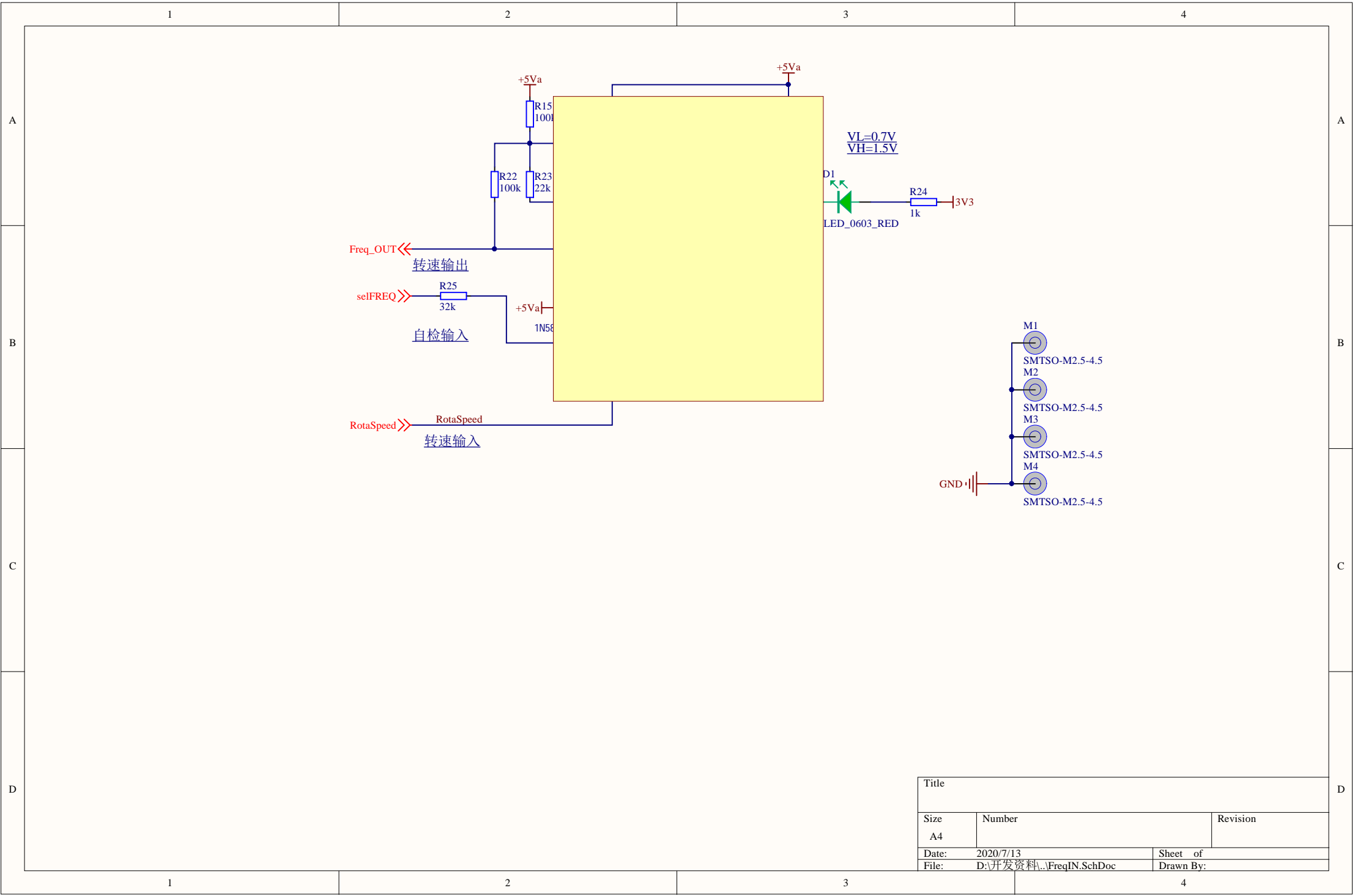


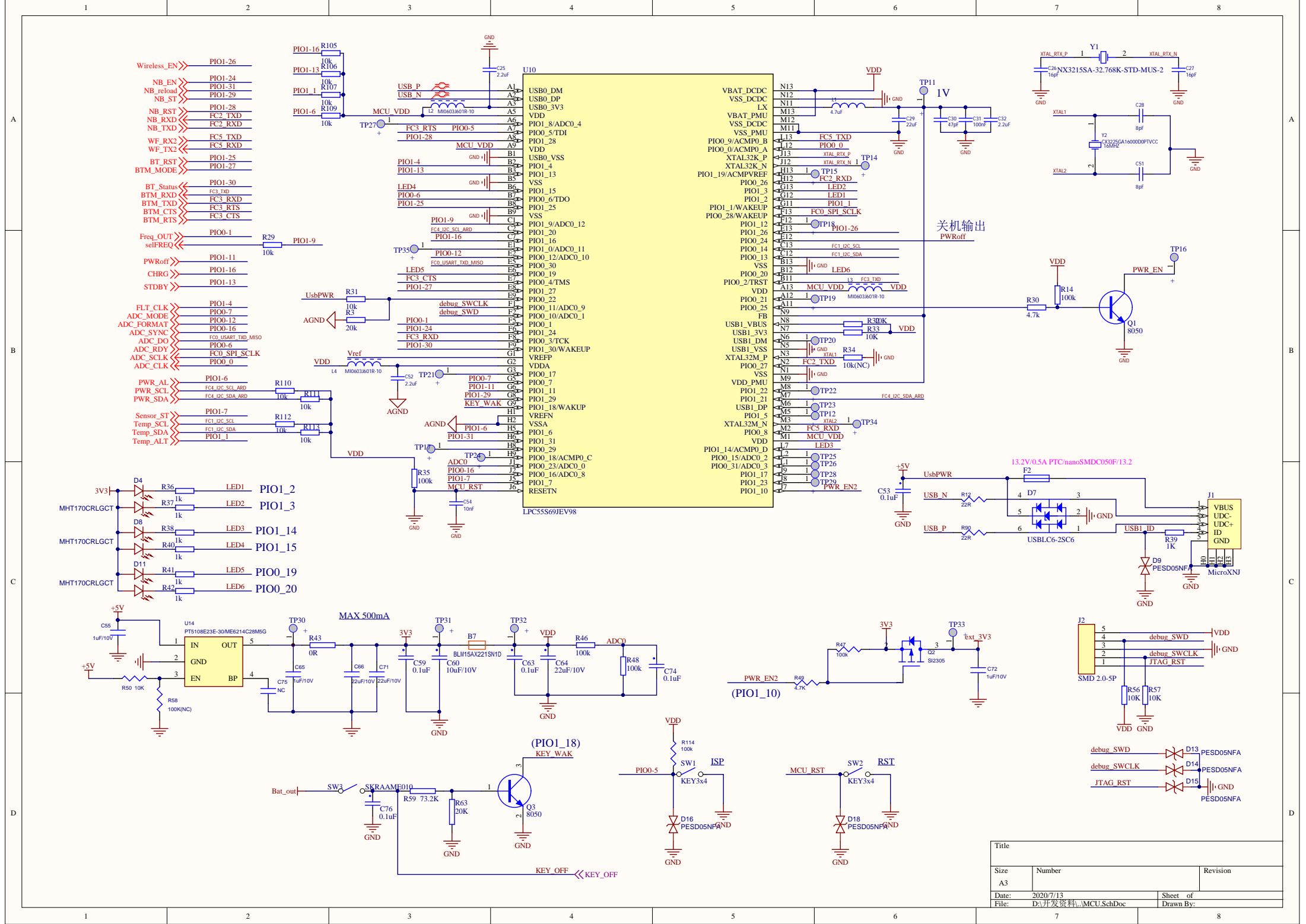
PARAMETER	MIN	TYP	MAX	UNIT
CLK period (1/f <sub>CLK</sub> )	37		10,000	ns
CLK positive or negative pulse width	15			ns
Conversion period (1/f <sub>DATA</sub> )		256		CLK periods
High-Speed mode				CLK periods
High-Resolution mode		512		CLK periods
Low-Power mode		512		CLK periods
Falling edge of CLK to falling edge of DRDY		8		ns

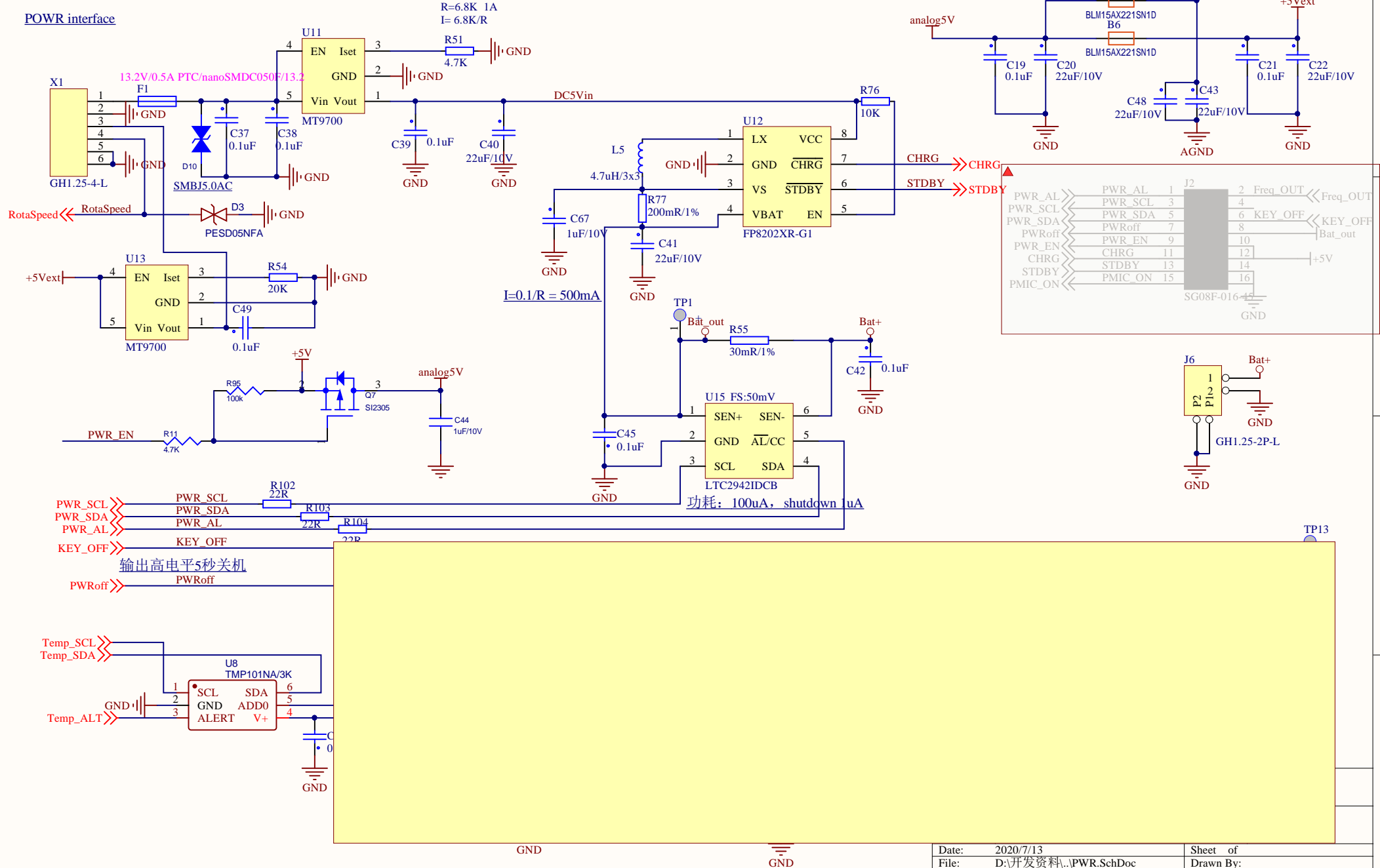
Table 6. Format Selection	
FORMAT PIN STATUS	SERIAL INTERFACE FORMAT
Logic Low (DGND)	SPI
Float <sup>(1)</sup>	Modulator Output <sup>(2)</sup>
Logic High (DVDD)	Frame-Sync

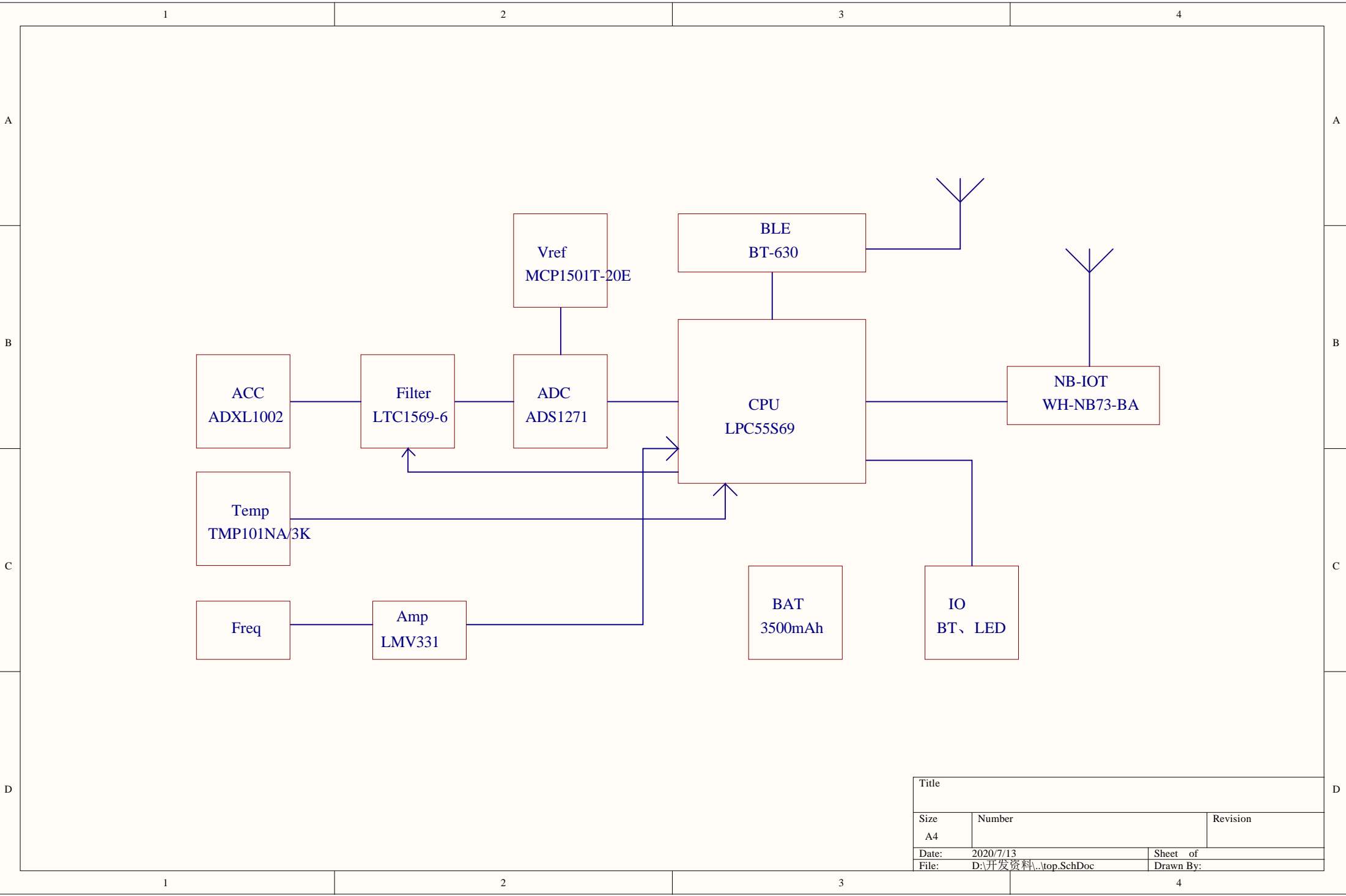
Table 5. Mode Selection	
MODE PIN STATUS	MODE SELECTION
Logic Low (DGND)	High-Speed
Float <sup>(1)</sup>	High-Resolution
Logic High (DVDD)	Low-Power

Title		
Size	Number	Revision
A4		
Date:	2020/7/13	Sheet of
File:	D:\开发资料\ADC.SchDoc	Drawn By:

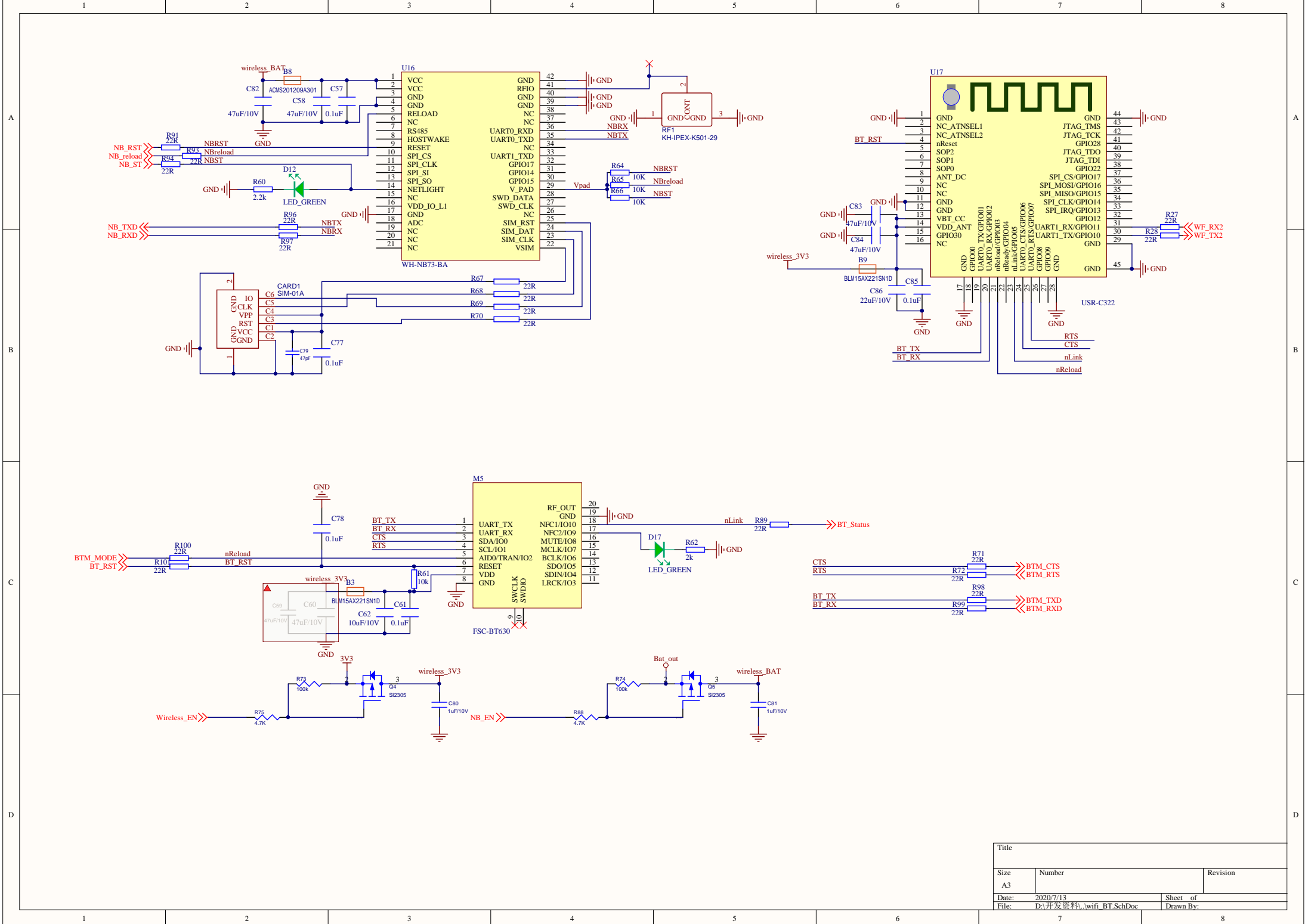








Title			
Size	Number		Revision
A4			
Date:	2020/7/13		Sheet of
File:	D:\开发资料\...\top.SchDoc		Drawn By:



Title		
Size	Number	Revision
A3		
Date:	2020/7/13	Sheet of
File:	D:\开发资料\wifi_BT.SchDoc	Drawn By: