

PARAMETER	MIN	TYP	MAX	UNIT
CLK period (1/f _{CLK})		37	10,000	ns
CLK positive or negative pulse width	15			ns
Conversion period (1/f _{DATA})		256		CLK periods
High-Speed mode				CLK periods
High-Resolution mode		512		CLK periods
Low-Power mode		512		CLK periods
Falling edge of CLK to falling edge of DRDY		8		ns

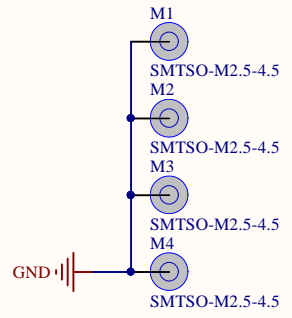
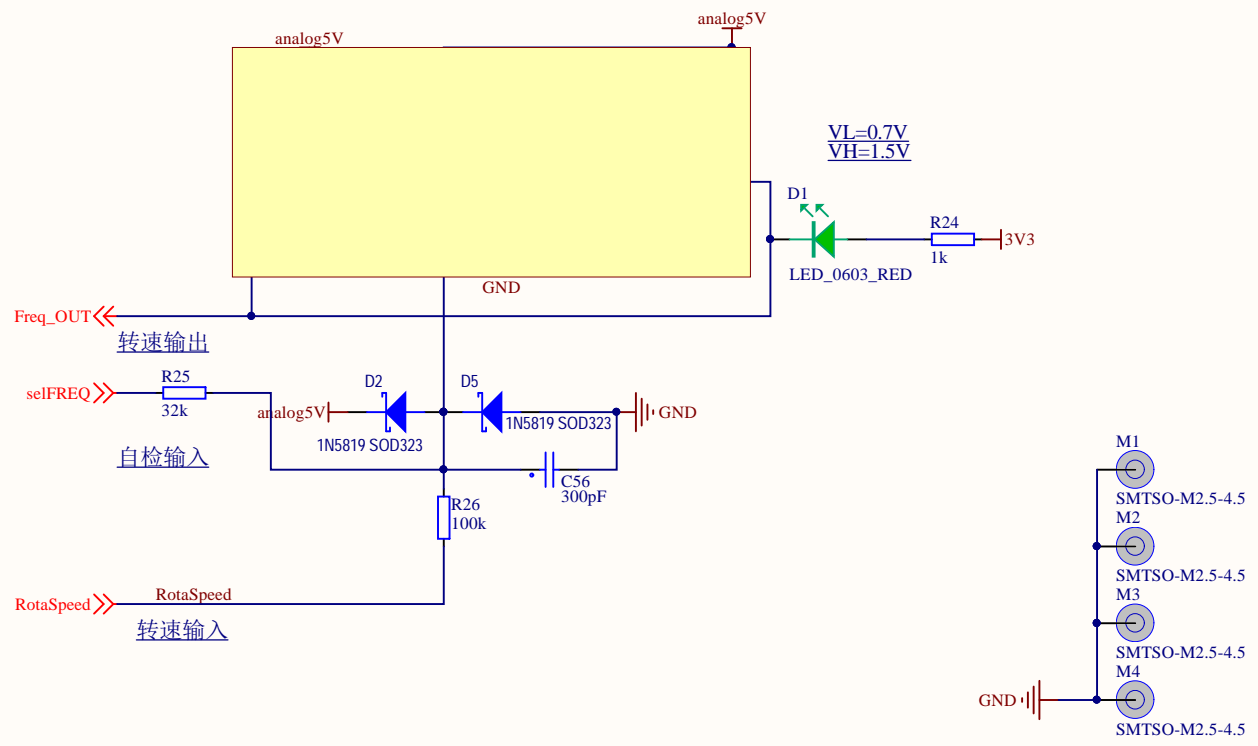
Table 5. Mode Selection

MODE PIN STATUS	MODE SELECTION
Logic Low (DGND)	High-Speed
Float(1)	High-Resolution
Logic High (DVDD)	Low-Power

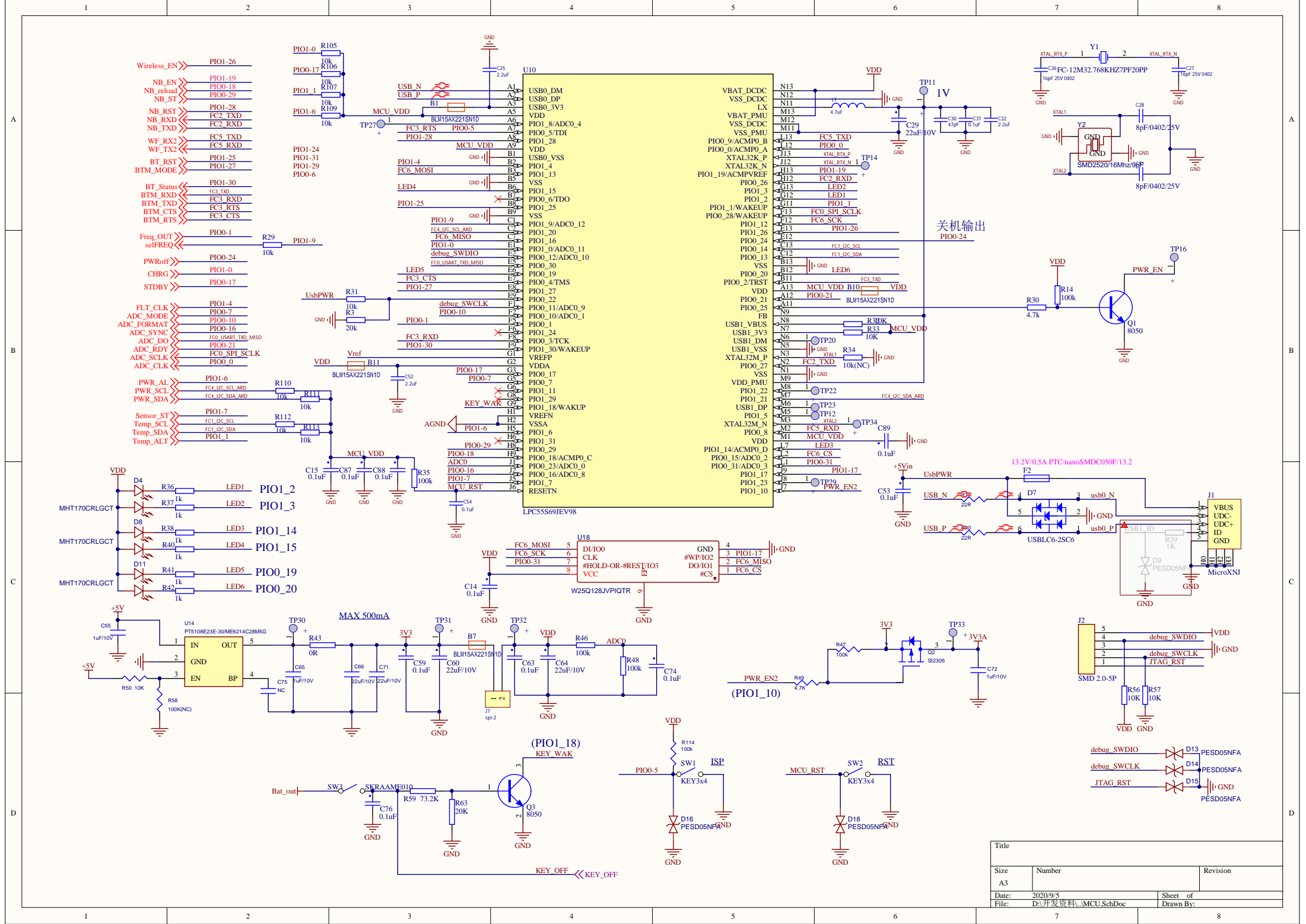
Table 6. Format Selection

FORMAT PIN STATUS	SERIAL INTERFACE FORMAT
Logic Low (DGND)	SPI
Float(1)	Modulator Output(2)
Logic High (DVDD)	Frame-Sync

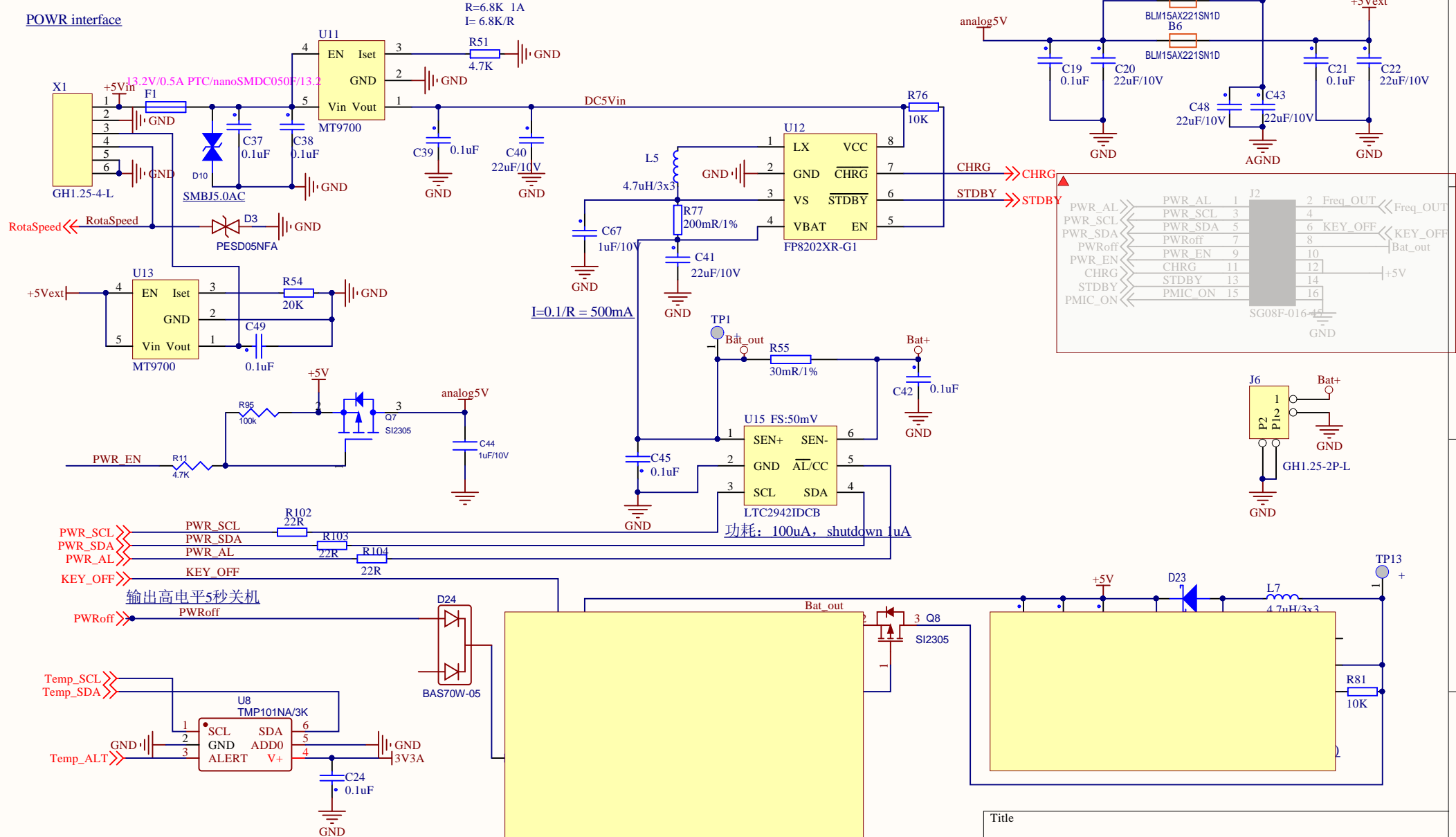
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Date:	2020/9/5	Sheet of
File:	D:\开发资料\ADC.SchDoc	Drawn By:



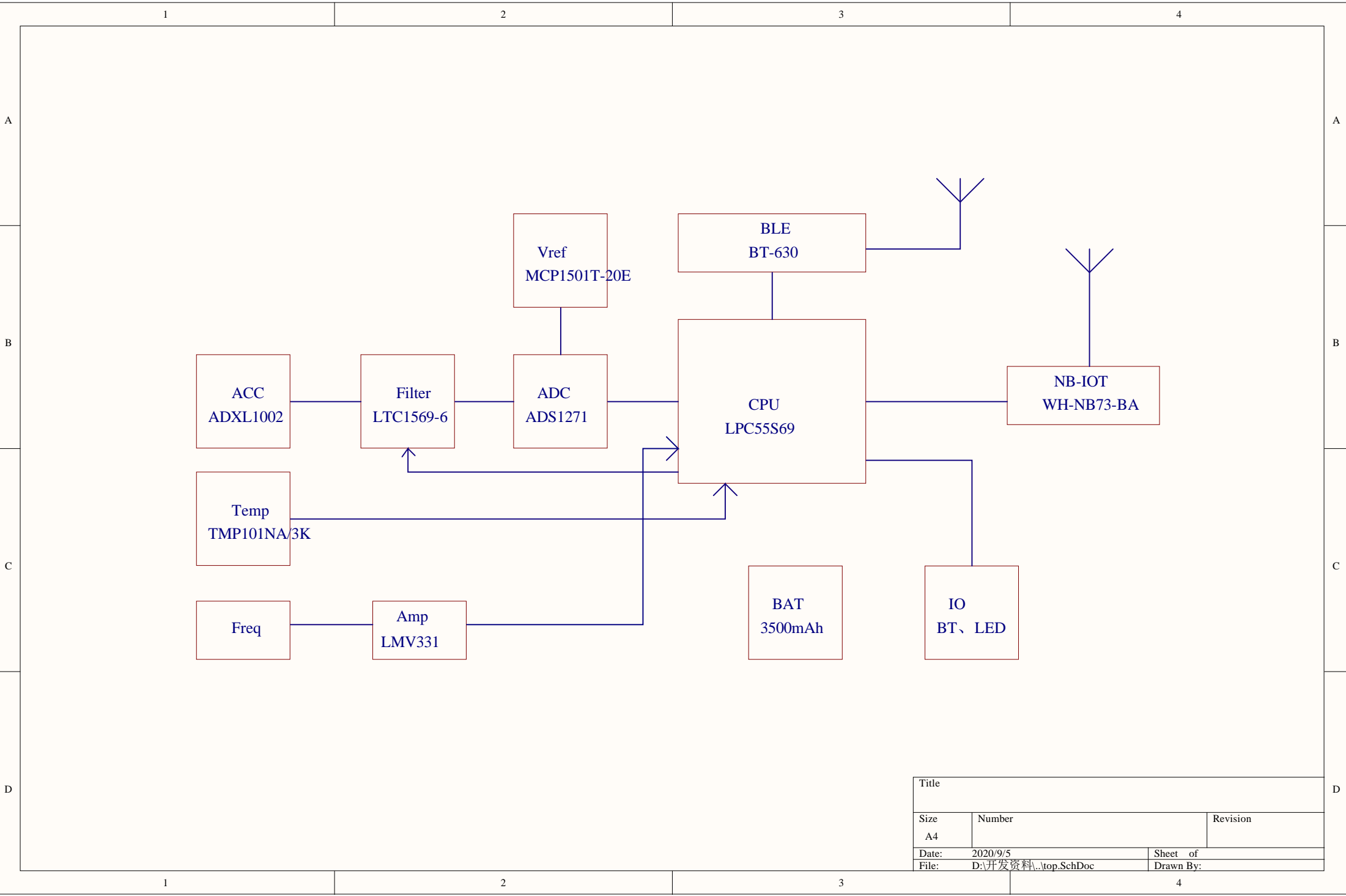
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Date:	2020/9/5	Sheet of
File:	D:\开发资料\FreqIN.SchDoc	Drawn By:



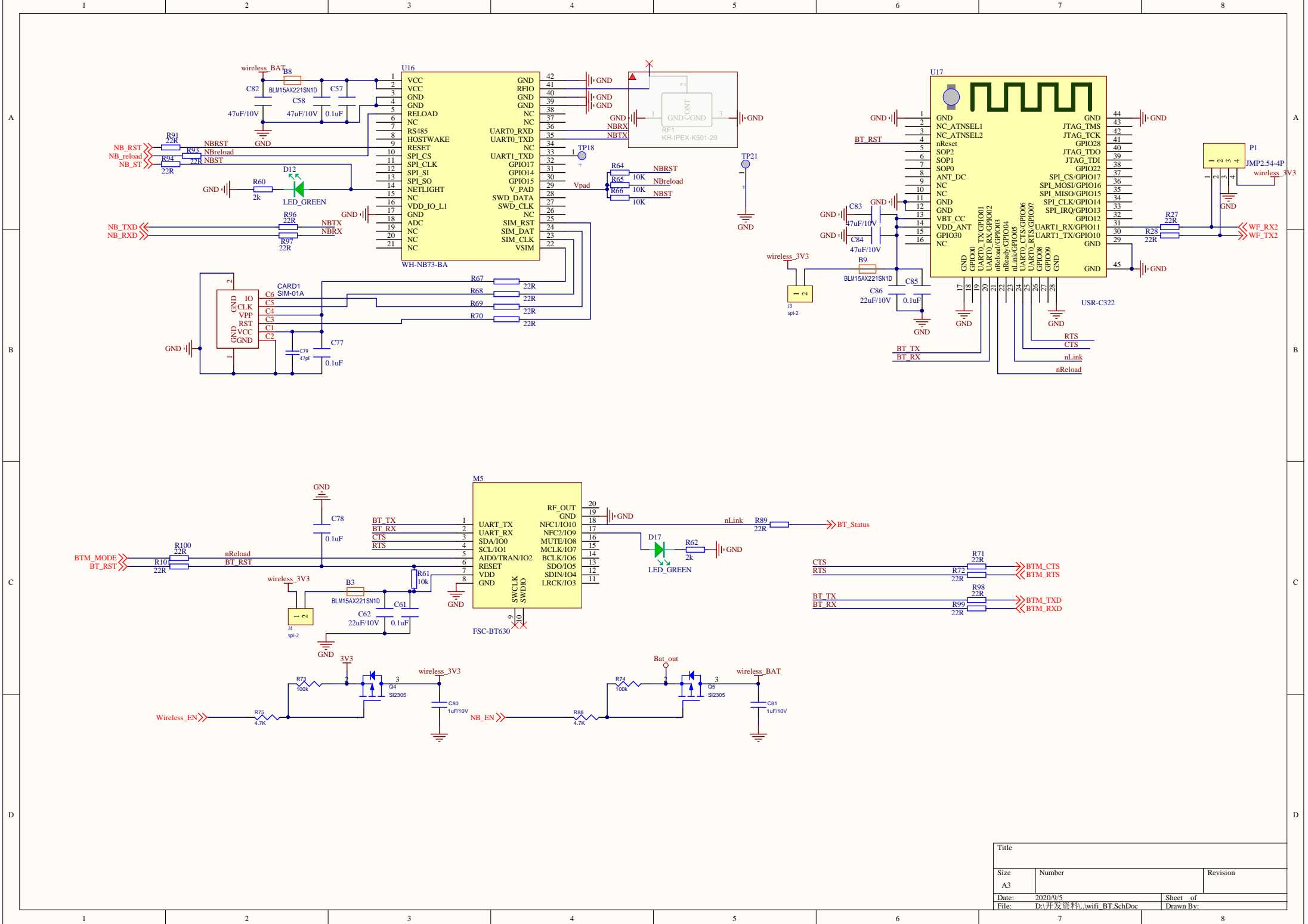
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Date:	2020/9/5	Sheet of
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Title		
Size A4	Number	Revision
Date:	2020/9/5	Sheet of
File:	D:\开发资料\...PWR.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2020/9/5	Sheet of
File:	D:\开发资料\...\top.SchDoc	Drawn By:



Title		
Size	Number	Revision
A3		
Date:	2020/9/5	Sheet of
File:	D:\开发资料\wifi_BT.SchDoc	Drawn By: