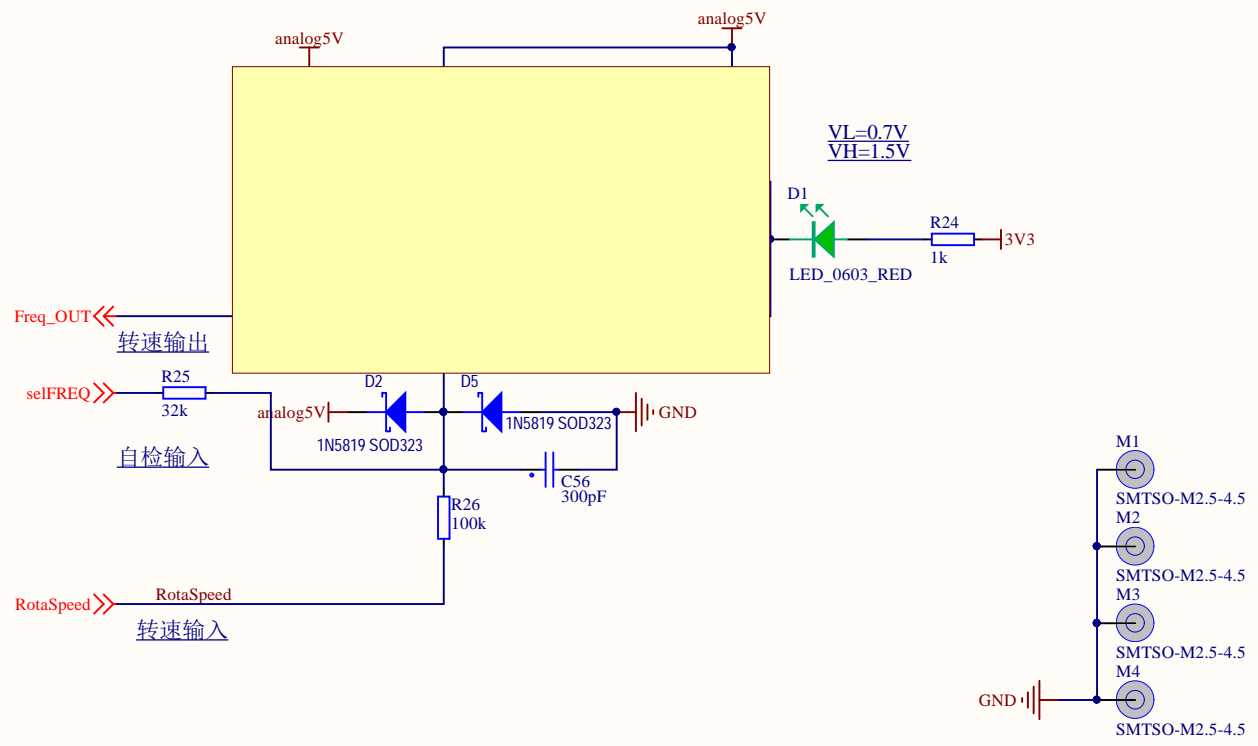


PARAMETER	MIN	TYP	MAX	UNIT
CLK period (1/f _{CLK})	37		10,000	ns
CLK positive or negative pulse width	15			ns
Conversion period (1/f _{DATA})		256		CLK periods
		512		CLK periods
		512		CLK periods
Falling edge of CLK to falling edge of DRDY		8		ns

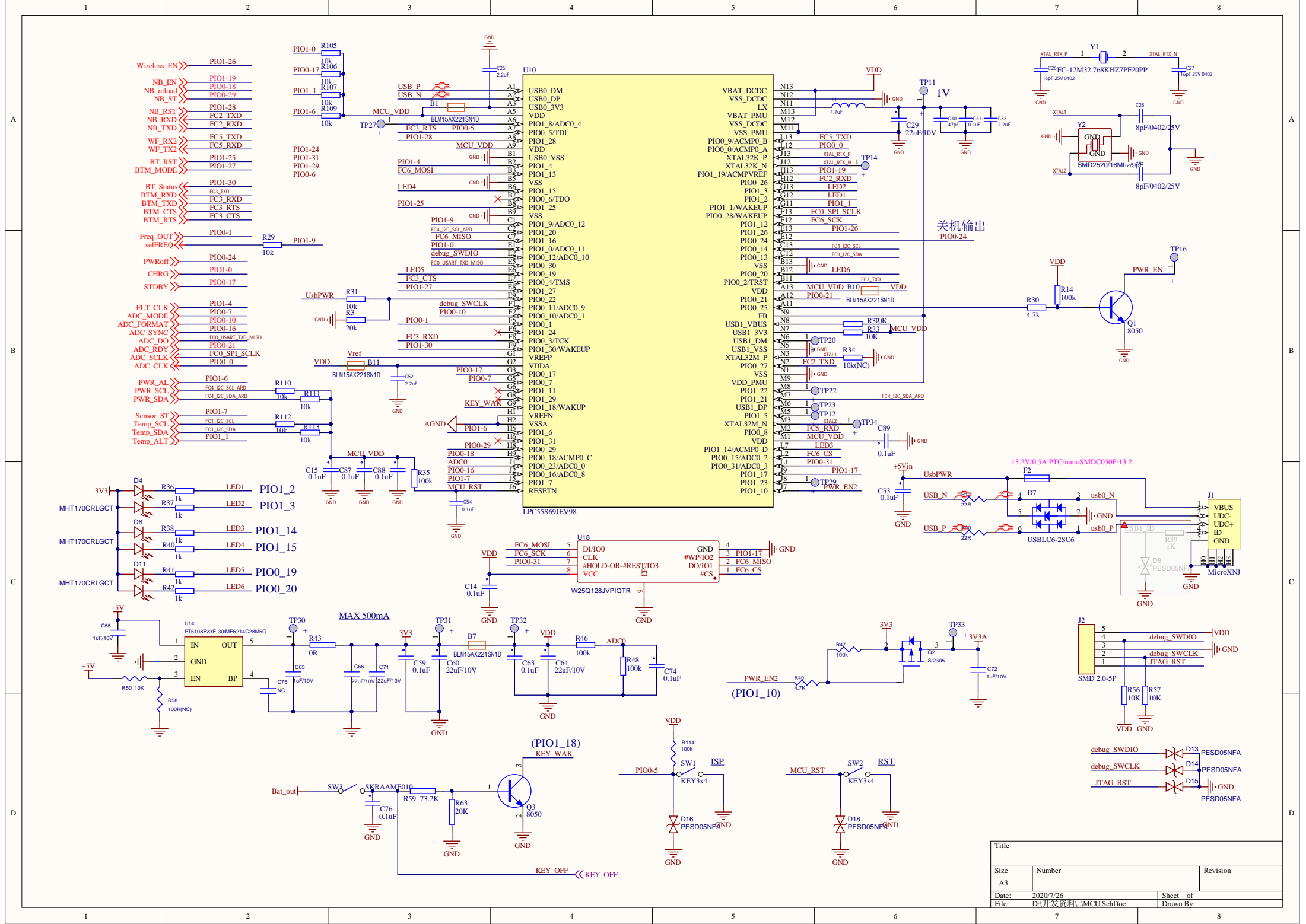
Table 6. Format Selection	
FORMAT PIN STATUS	SERIAL INTERFACE FORMAT
Logic Low (DGND)	SPI
Float ⁽¹⁾	Modulator Output ⁽²⁾
Logic High (DVDD)	Frame-Sync

Table 5. Mode Selection	
MODE PIN STATUS	MODE SELECTION
Logic Low (DGND)	High-Speed
Float ⁽¹⁾	High-Resolution
Logic High (DVDD)	Low-Power

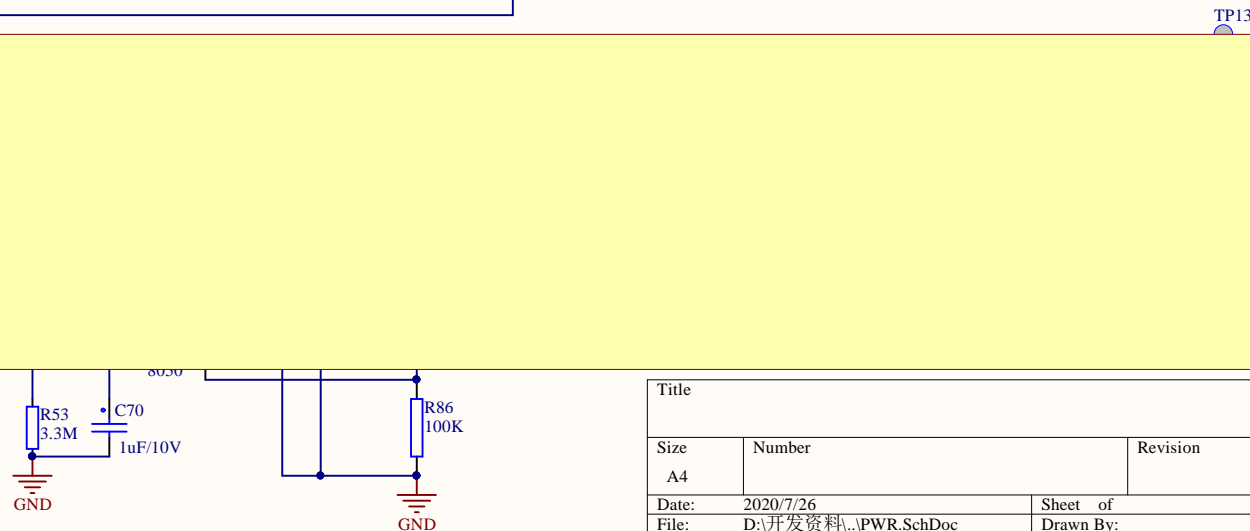
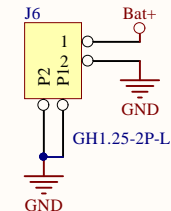
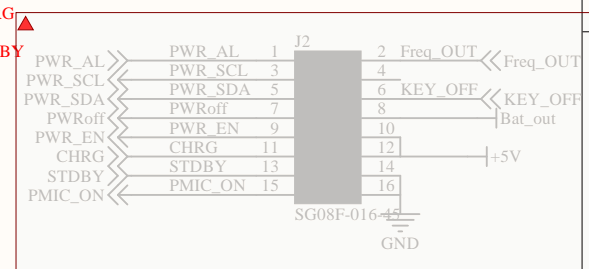
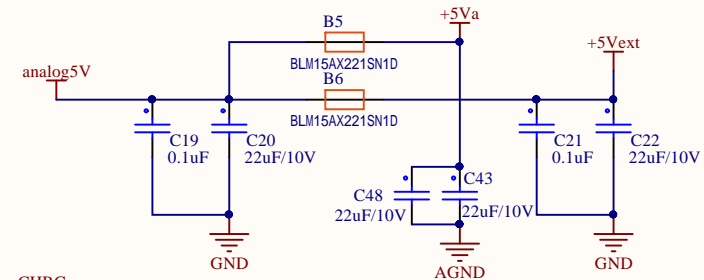
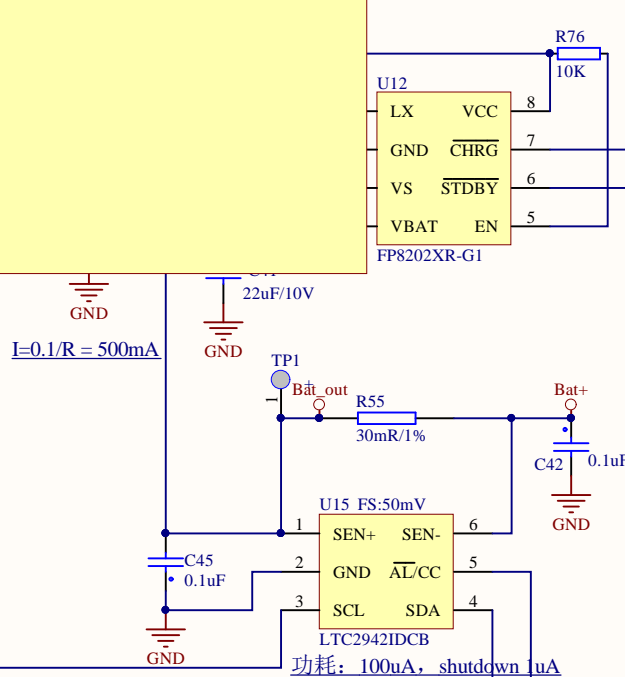
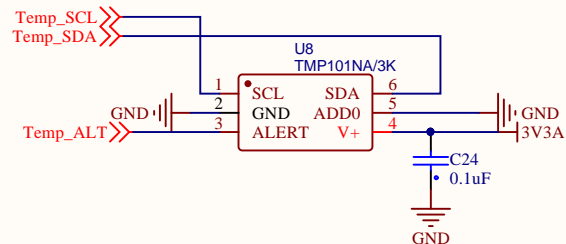
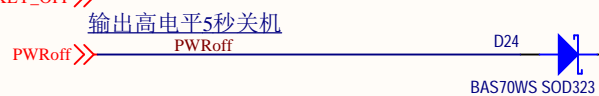
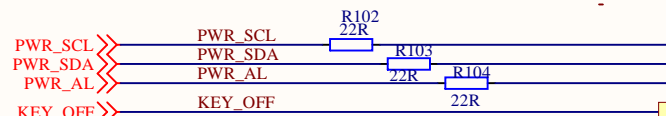
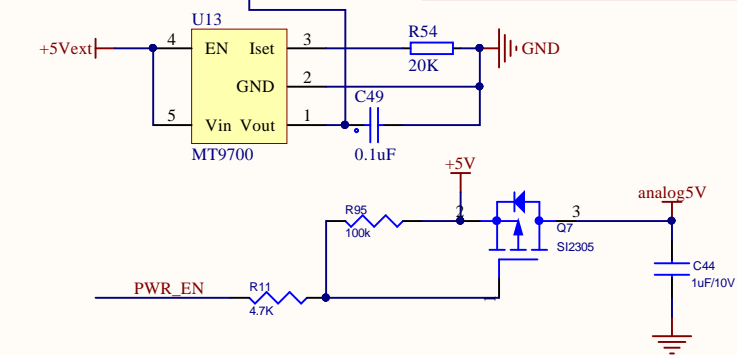
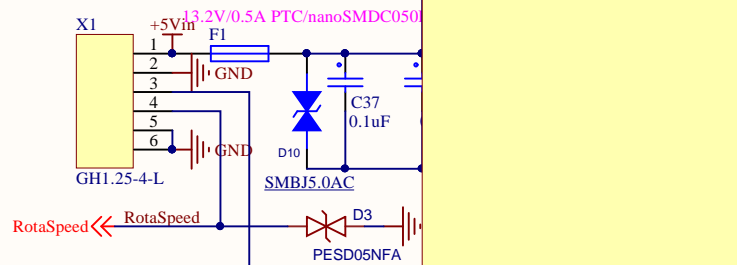
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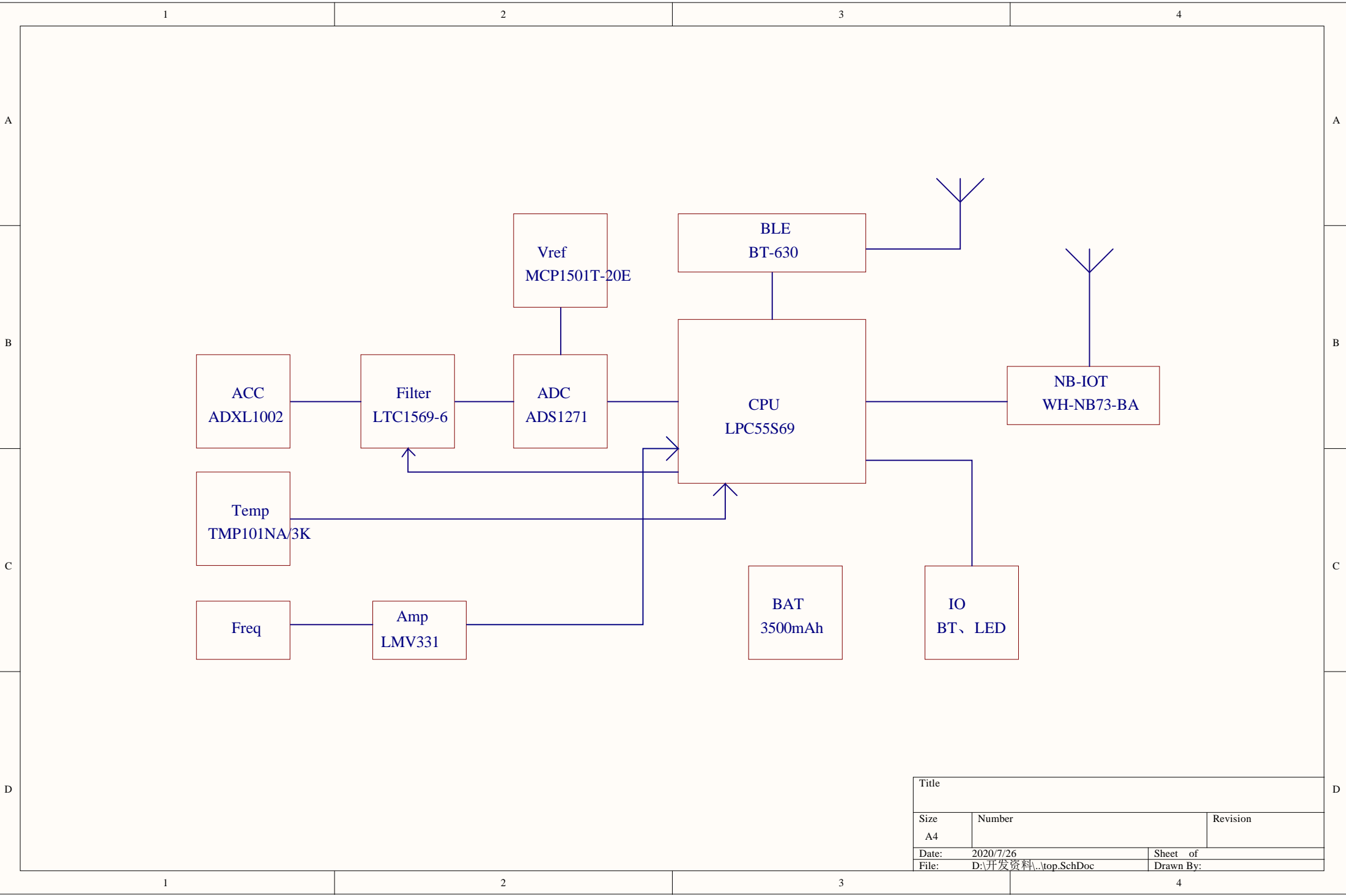


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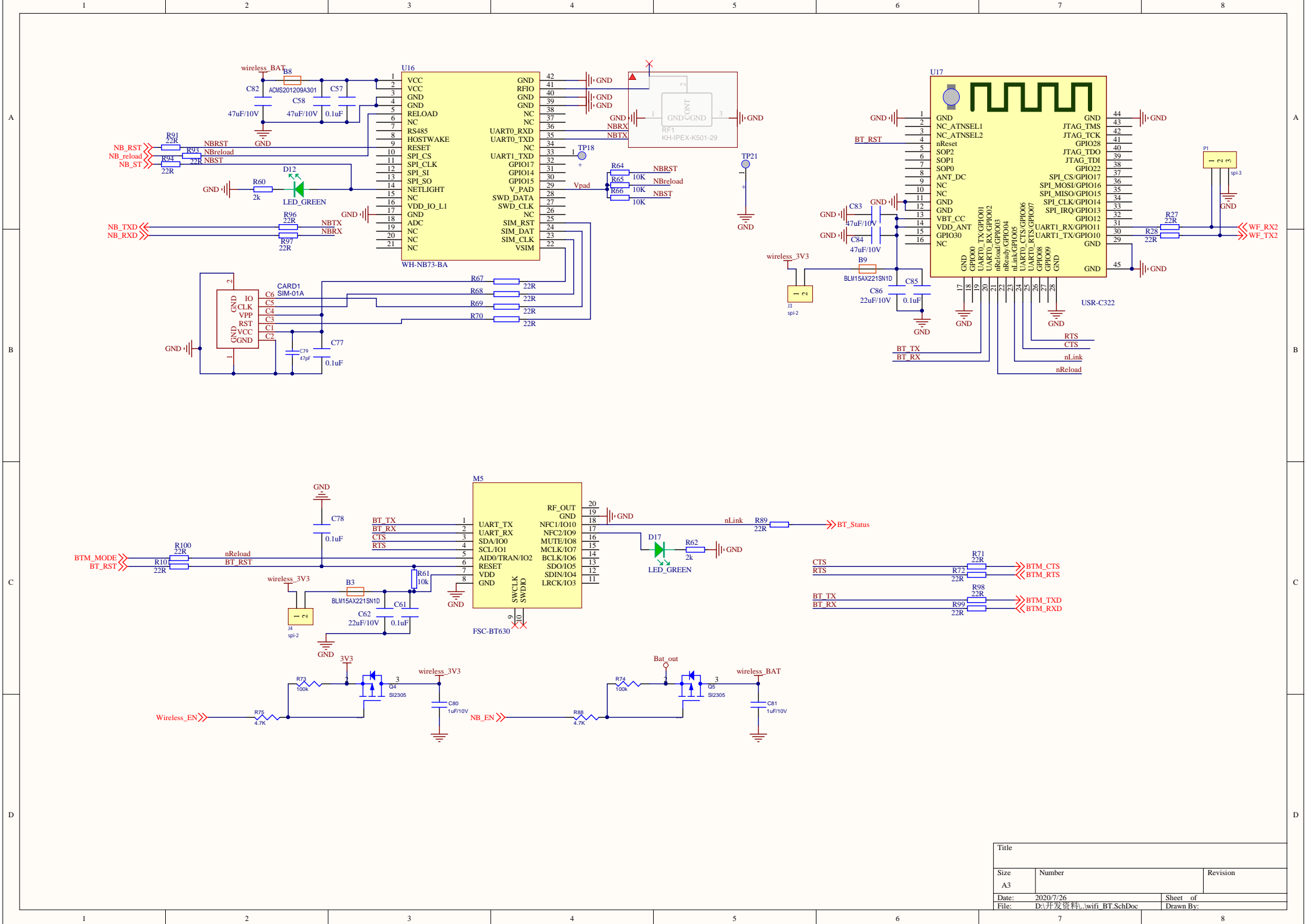


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