# LPC55S6x

## Errata sheet LPC55S6x

Rev. 1.1 — 25 February 2019 Errata sheet

### Document information

| Info | Content |
|---|---|
| **Keywords** | LPC55S69JBD100, LPC55S69JEV98, LPC55S66JBD100, LPC55S66JEV98 |
| **Abstract** | LPC55S6x errata |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 1.1 | 20190221 | Updated device markings |
| 1.0 | 20181204 | Initial version |

## Contact information

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# 1. Product identification

The LPC55S6x VFBGA98 package has the following top-side marking:

- First line: LPC55S6x
- Second line: JEV98
- Third line: xxxxxxxx
- Fourth line: xxxyywwx1
  - yyww: Date code with yy = year and ww = week.

The LPC55S6x HLQFP100 package has the following top-side marking:

- First line: LPC55S6xJBD100
- Second line: xxxxxxx
- Third line: xxxxxyywwx1
  - yyww: Date code with yy = year and ww = week.

## 2. Errata overview

**Table 1. Functional problems table**

| Functional problems | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| ROM.1 | For PRINCE encrypted region, partial erase cannot be performed | 0A | Section 3.1 |
| ROM.2 | For PUF based key provisioning, a reset must be performed | 0A | Section 3.2 |
| ROM.3 | Unprotected sub regions in PRINCE defined regions cannot be used | 0A | Section 3.3 |
| ROM.4 | Last page of image is erased when simultaneously programming the signed image and CFPA region. | 0A | Section 3.4 |
| VDD.1 | The minimum operating voltage is 1.85 V | 0A | Section 3.5 |
| CMP.1 | The hysteresis on the comparator cannot be enabled | 0A | Section 3.6 |

**Table 2. AC/DC deviations table**

| AC/DC deviations | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| n/a | n/a | n/a | n/a |

**Table 3. Errata notes**

| Note | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| n/a | n/a | n/a | n/a |

# 3. Functional problems detail

## 3.1 ROM.1: For PRINCE encrypted region, partial erase cannot be performed

### Introduction

The LPC55S6x devices supports real-time encryption and decryption for on-chip flash using the PRINCE encryption algorithm. The PRINCE module supports three flash memory regions for real-time encryption and decryption, referred to as crypto regions. Each crypto region resides at a 256 kB address boundary within the flash. Each crypto region is divided into 8 kB sub-regions which can be individually enabled.

### Problem

For the LPC55S6x, when an erase operation is performed with size less then 8 kB for PRINCE encrypted region, a return error is returned and subsequent ISP commands does not respond.

### Work-around

When region is marked as PRINCE encrypted region, user must perform full erase of the PRINCE encrypted region. This will be fixed on the next silicon revision 1A.

## 3.2 ROM.2: For PUF based key provisioning, a reset must be performed

### Introduction

On the LPC55S6x, the Key Management module supports storing three 128-bit PRINCE Keys (KEY1, KEY2, KEY3) used for decryption process.

### Problem

After PUF based key provisioning, the PRINCE module cannot perform decryption process without performing a reset.

### Work-around

The user must perform reset via the external reset pin or power cycle the device for successful decryption process when using PUF key. This will be fixed on the next silicon revision 1A.

## 3.3 ROM.3: Unprotected sub regions in PRINCE defined regions cannot be used

### Introduction

The LPC55S6x devices supports real-time encryption and decryption for on-chip flash using the PRINCE encryption algorithm. The PRINCE module supports three flash memory regions for real-time encryption and decryption, referred to as crypto regions. Each crypto region resides at a 256 kB address boundary within the flash. Each crypto region is divided into 8 kB sub-regions which can be individually enabled.

### Problem

Unprotected (non PRINCE encrypted) sub flash in PRINCE defined regions cannot be written after erase operation. Any non PRINCE encrypted sub regions in the PRINCE defined regions can not be used.

### Work-around

There is no work-around. This will be fixed on the next silicon revision 1A

## 3.4 ROM.4: Last page of image is erased when simultaneously programming the signed image and CFPA region

### Introduction

On the LPC55S6x, the protected flash region (PFR) supports a Customer Field Programmable Area (CFPA) which can be used for Monotonic counters, Key revocation, and PRINCE IV codes. Also, the ROM supports secure boot using signed image.

### Problem

The last page of the image will be erased when simultaneously programming the signed image and the CFPA via the Secure Binary (SB2 file) image format.

### Work-around

The signed image and the CFPA needs to be programmed one a time to prevent erase of the last page of the image. This will be fixed on the next silicon revision 1A.

## 3.5 VDD.1: The minimum operating voltage is 1.85 V

### Introduction

The LPC55S6x operating voltage range specification is from 1.80 V to 3.6 V.

### Problem

On the LPC55S6x rev 0A, the minimum operating range is 1.85 V.

### Work-around

There is no work-around. This will be fixed on the next silicon revision 1A.

## 3.6 CMP.1: The hysteresis on the comparator cannot be enabled

### Introduction

On the LPC55S6x, Analog comparator control register (COMP) provides an option to enable and disable the hysteresis.

### Problem

On the LPC55S6x, the hysteresis on the comparator cannot be enabled.

### Work-around

There is no work-around. This will be fixed on the next silicon revision 1A.

## 4. AC/DC deviations detail

No known errata.

## 5. Errata notes

No known errata.

# 6. Legal information

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