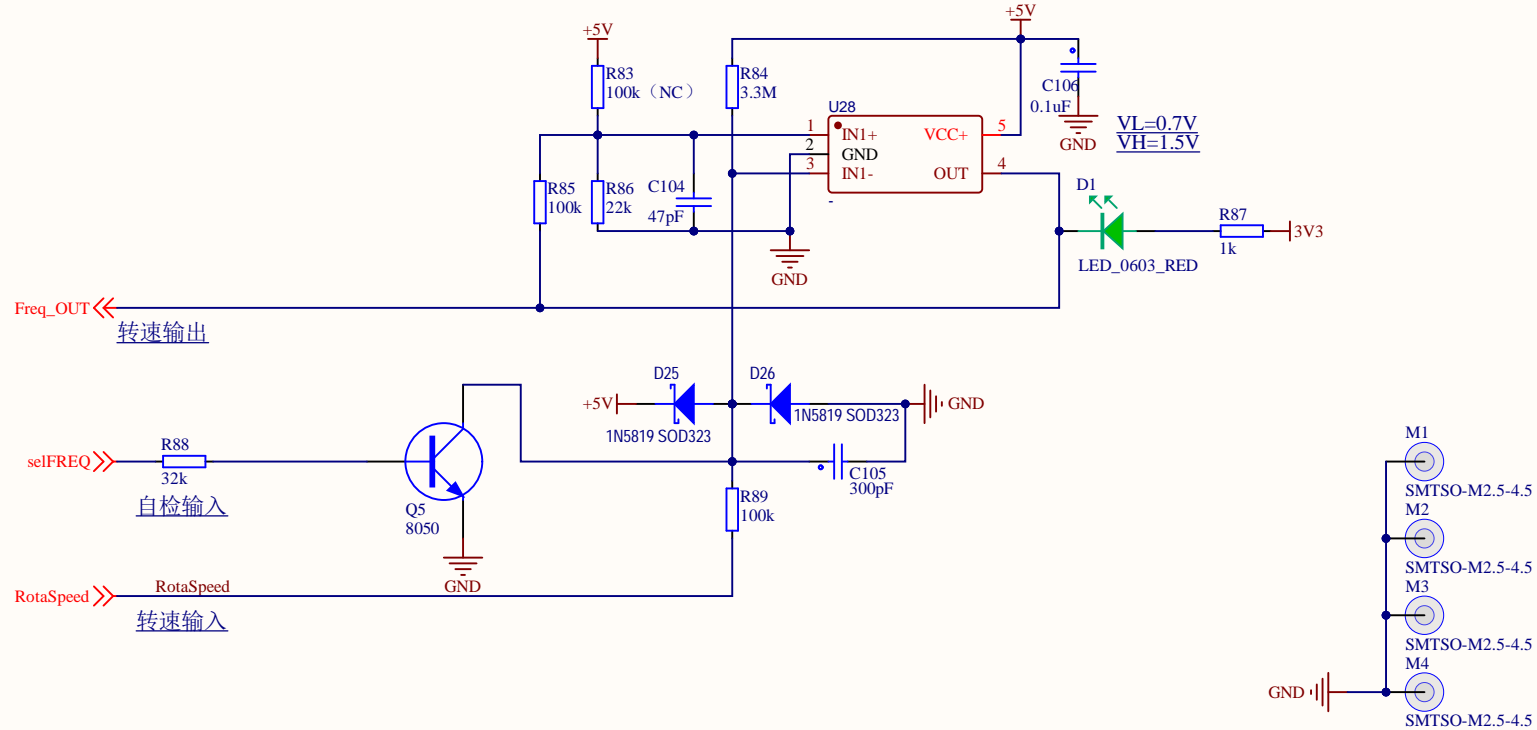


Table 6. Format Selection				
PARAMETER	MIN	TYP	MAX	UNIT
CLK period (1/f _{CLK})	37		10,000	ns
CLK positive or negative pulse width	15			ns
Conversion period (1/f _{DATA})	High-Speed mode	256		CLK periods
	High-Resolution mode	512		CLK periods
	Low-Power mode	512		CLK periods
Falling edge of CLK to falling edge of DRDY		8		ns

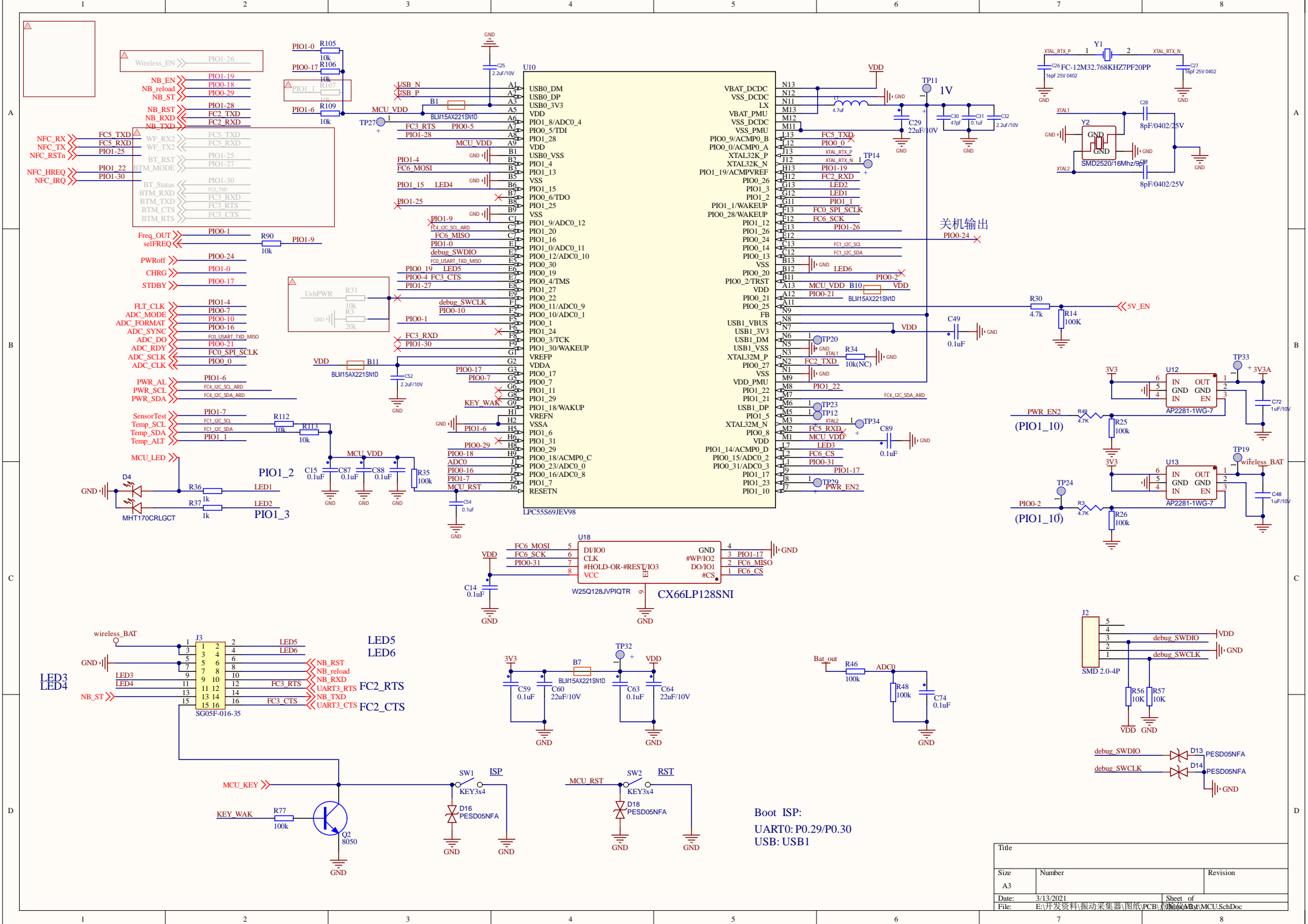
FORMAT PIN STATUS	SERIAL INTERFACE FORMAT
Logic Low (DGND)	SPI
Float ⁽¹⁾	Modulator Output ⁽²⁾
Logic High (DVDD)	Frame-Sync

Table 5. Mode Selection	
MODE PIN STATUS	MODE SELECTION
Logic Low (DGND)	High-Speed
Float ⁽¹⁾	High-Resolution
Logic High (DVDD)	Low-Power

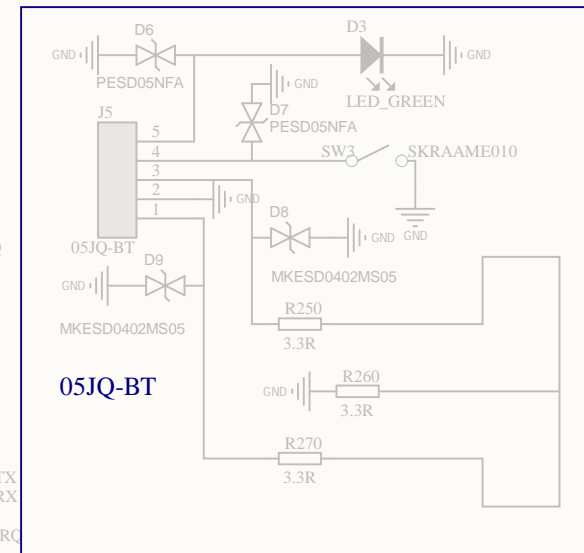
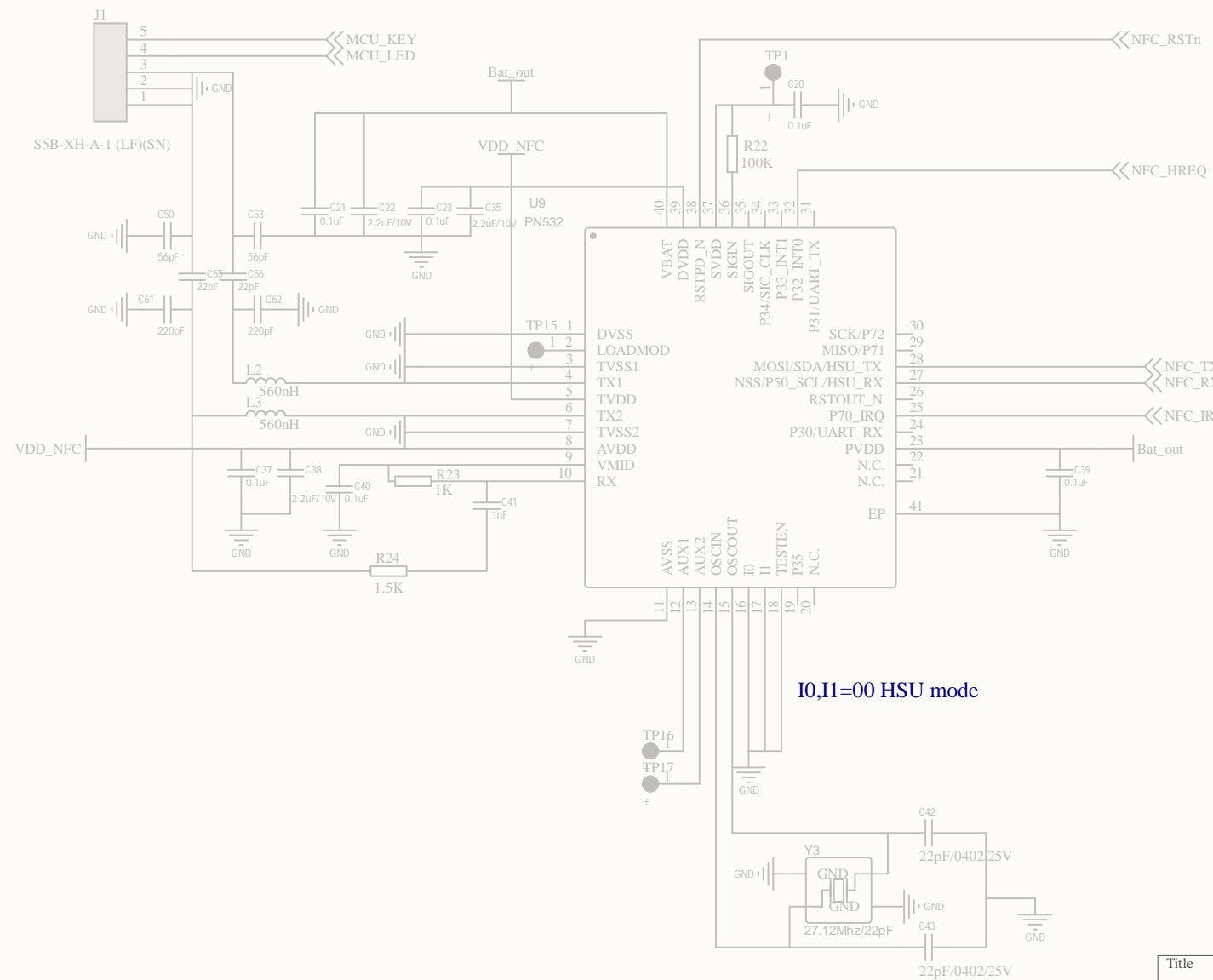
Title		
Size	Number	Revision
A4		
Date:	3/13/2021	Sheet of
File:	E:\开发资料\振动采集器\图纸\PCB\点焊\ADC.SchDoc	



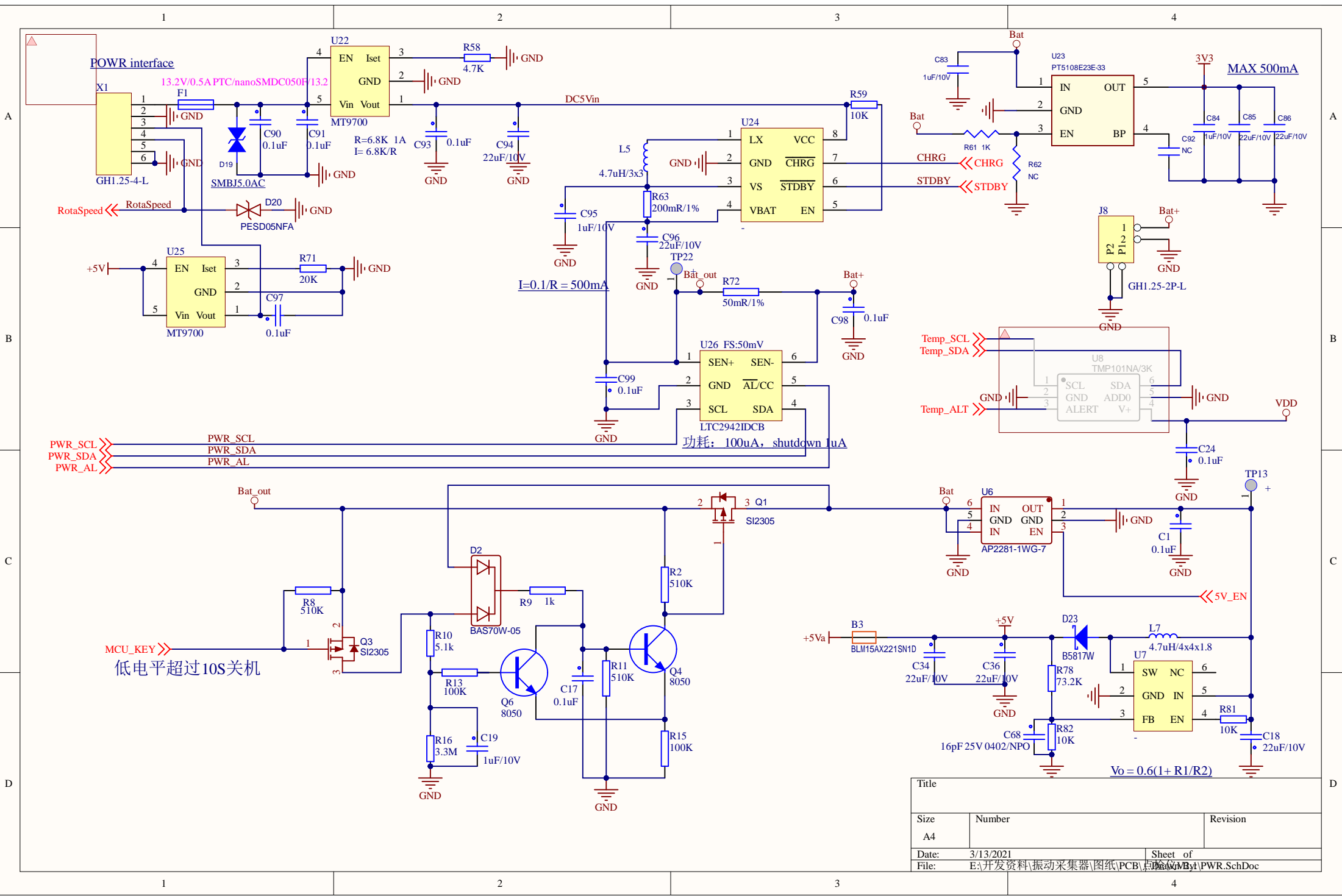
Title		
Size	Number	Revision
A4		
Date:	3/13/2021	Sheet of
File:	E:\开发资料\...\FreqIN.SchDoc	Drawn By:



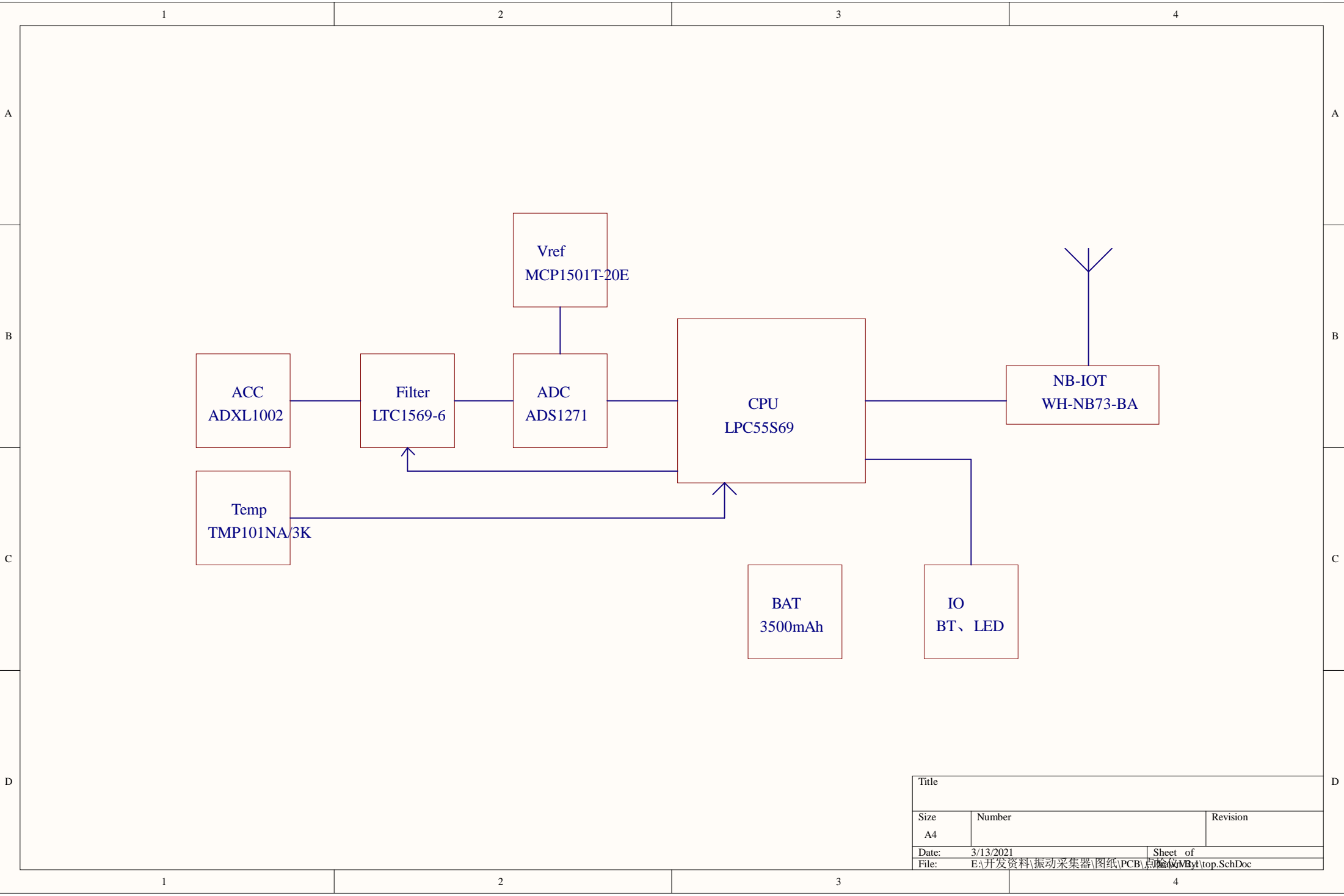
Title		
Size	Number	Revision
A3		
Date:	3/13/2021	Sheet of
File:	E:\开发资料\振动采集器\图纸\PCB\控制板\MCU.SchDoc	



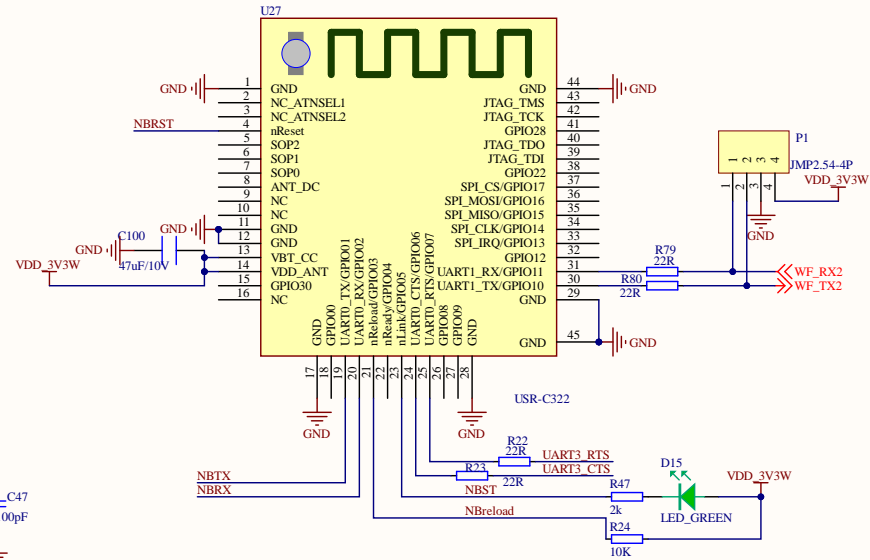
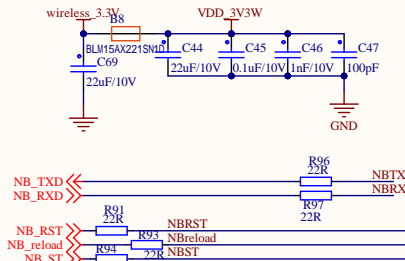
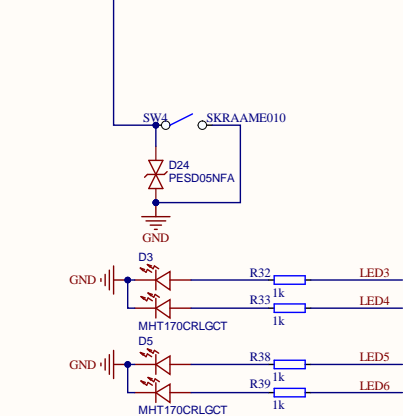
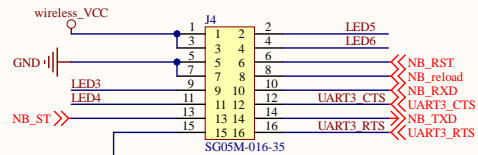
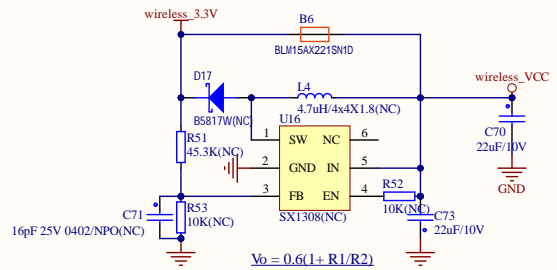
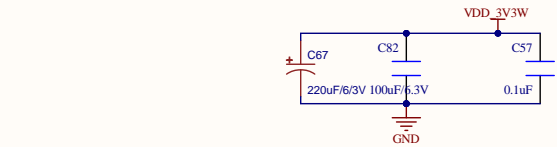
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A4		
Date:	3/13/2021	Sheet of
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Title		
Size	Number	Revision
A4		
Date:	3/13/2021	Sheet of
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Title		
Size	Number	Revision
A4		
Date:	3/13/2021	Sheet of
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Title		
Size	Number	Revision
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Date:	3/13/2021	Sheet of
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