2022

ELECTRONIC SCIENCE

Paper : ELCGE-31

(Electronics)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***any five*** questions.

1. (a) What is Fermi level?

   (b) We have two intrinsic semiconductors, SI and S2. The E-k diagram for each of them is shown in Fig. 1 below.

   (i) Which one of them should have higher electron mobility and why?

   (ii) Which one of them is likely to have higher intrinsic carrier concentration at a given temperature? Justify your answer.

   (iii) Where should the Fermi level lie for SI with reference to the middle of the band gap? Justify your answer.

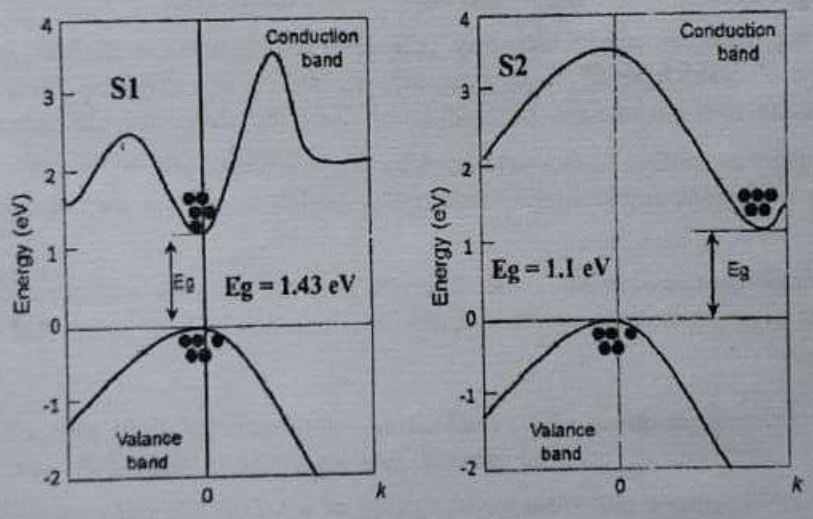

Figure 1

   (c) Calculate the resistivity of an n-type silicon doped with 10^{16} phosphorus atoms/cm^3. Assume, $q = 1.6\times10^{-19}$ C and $\mu_n = 1300$ cm^2/V.s. 1+(2+2+3)+2

2. (a) What is diffusion capacitance in connection with a p-n junction diode?

(b) Calculate the contact potential for a p-n junction with $N_A = 10^{17}$ cm^{-3} and $N_D = 10^{16}$ cm^{-3} at room temperature. Given: kT/q = 25.9 mV and $n_i = 9.65 \times 10^9$ at room temperature, where the terms have their usual meanings. Derive the expression used.

(c) Two different p-n junction diodes Dl and D2 are formed using semiconductors SI and S2, respectively. The acceptor doping concentration is 10^{16} cm^{-3} for both Dl and D2. Similarly, the donor doping concentration is 10^{17} cm^{-3} for both Dl and D2. Consider the E-k diagram as shown in Fig. 1 for S1 and S2.

(i) Which one of them is likely to have higher reverse saturation current at a given temperature? Justify your answer.

(ii) Which one of them can be used as an LED and why? 2+4+(2+2)

3. (a) Sketch the input and output characteristics of a transistor operating in the CB configuration. What is base width modulation or early effect? What are the biasing conditions at the junctions of the transistor operating in the active, saturation and cutoff regions? Why does the collector current remain practically constant in the active region of the output characteristics of a transistor?

(b) What are the conditions that must be satisfied in a transistor circuit for faithful amplification? Explain the importance of proper choice of the Q-point.

(c) Draw the fixed bias circuit of a transistor. In a fixed bias circuit of transistor, $V_{CC} = 9$V, $R_B = 100$ kΩ and $R_C = 1.2$ kΩ. If $\beta = 50$, $I_{CO} = 20$ nA and $V_{BE} = 0.7$ V, determine the Q-point and find the thermal stability factor of the bias circuit. 4+3+3

4. (a) Draw the r_e-model of a transistor operating in CB mode. Explain how this model can be established. Draw the r_e-model of a transistor operating in CE mode also.

(b) Draw the h-parameter model for any transistor configuration at low frequency. Why these parameters are called hybrid? Show that only h_{ie} and h_{fe} are important in the h-parameter model. How can these two parameters be calculated from the transistor characteristics?

(c) A CE transistor amplifier is characterized by $h_{ie} = 1200\ \Omega$ and $h_{fe} = 100$. If the load resistance is 1 kΩ, then using the approximate h-parameter model, determine the voltage gain of the amplifier. 4+4+2

5. Schematically draw the equilibrium band diagram of a metal-oxide-semiconductor (MOS) structure. With appropriate diagram explain how accumulation, depletion and inversion capacitance forms in such a MOS structure. 2+8

6. (a) Draw the schematic diagram of a metal-oxide-semiconductor field effect transistor (MOSFET). Explain how pinch-off occurs and current gets saturated in such a device.

(b) Define threshold voltage and trans-conductance of a MOSFET and explain how such parameters can be extracted from the measured current-voltage characteristics. (1+3)+(3+3)

7. (a) What are CMRR and PSRR of an op-amp?

(b) Explain how op-amp is used as a voltage comparator. How can it be used as a zero-crossing detector?

(c) Draw the circuit diagrams for the four feedback topologies. 2+(3+1)+4

8. (a) From the truth table below, determine the standard SOP expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(b) Draw the circuit diagrams of a 4-bit multiplexer and de-multiplexer.

(c) Draw the circuit diagram of a J-K flip-flop using NAND gates. Write its truth table. How to convert a J-K flip-flop to a D flip-flop? 2+(2+2)+(2+1+1)