Evolution of CMOS device and technology for low power applications

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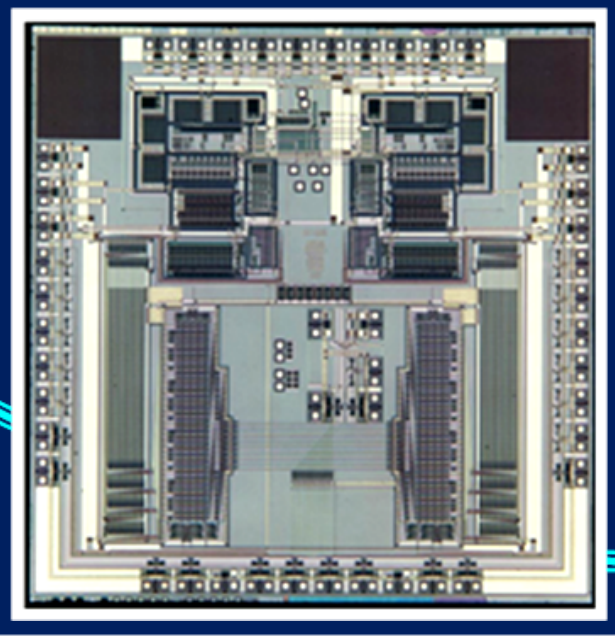
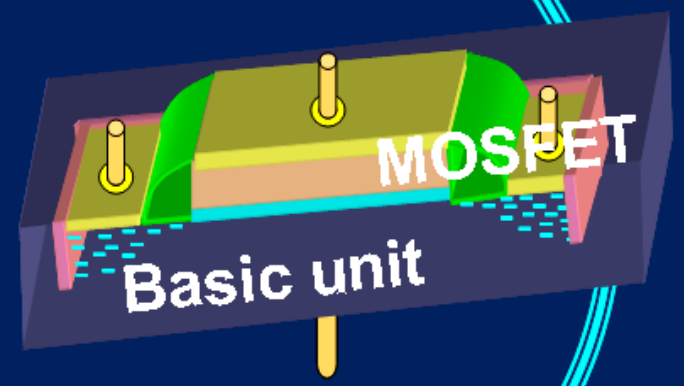
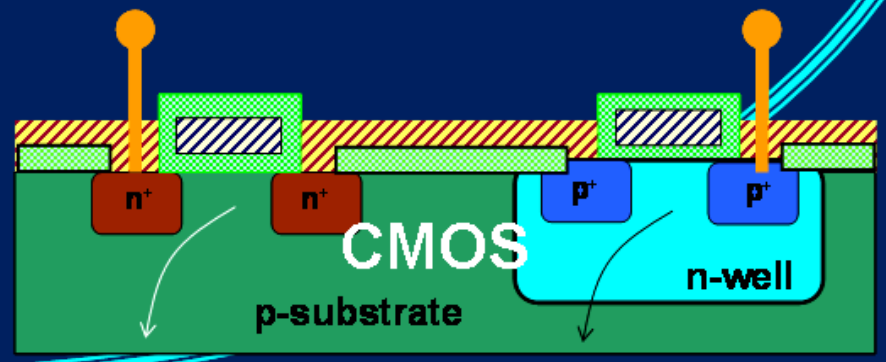
Systems, circuits and devices



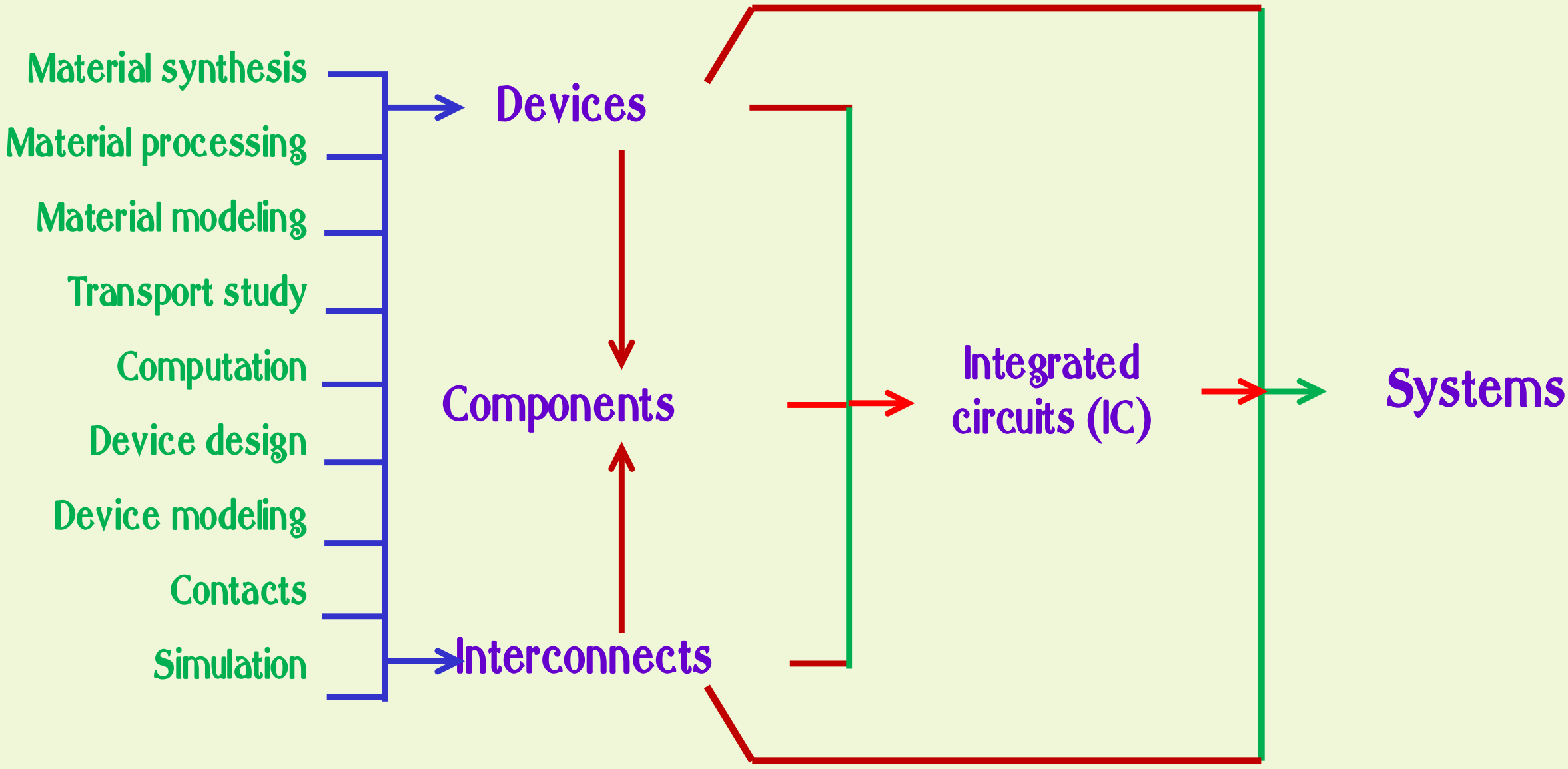
Si, Ge, SiGe,
GaAs, AlGaAs,
InP, ...



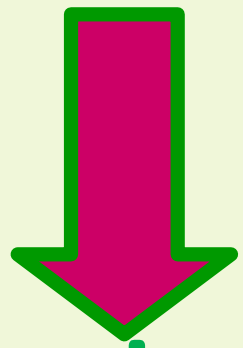


Developing an electronic system

Material	Device/Circuit	Circuit/System



Metal-oxide-semiconductor field effect transistors (MOSFETs)



The workhorse of modern electronic gadgets

Si based CMOS is the key

As a material

Si is abundant in nature

↓

High quality native oxide (SiO_2)

↓

Appropriate mechanical strength

Market

Microelectronic market

↓

80% is dominated by CMOS**

↓

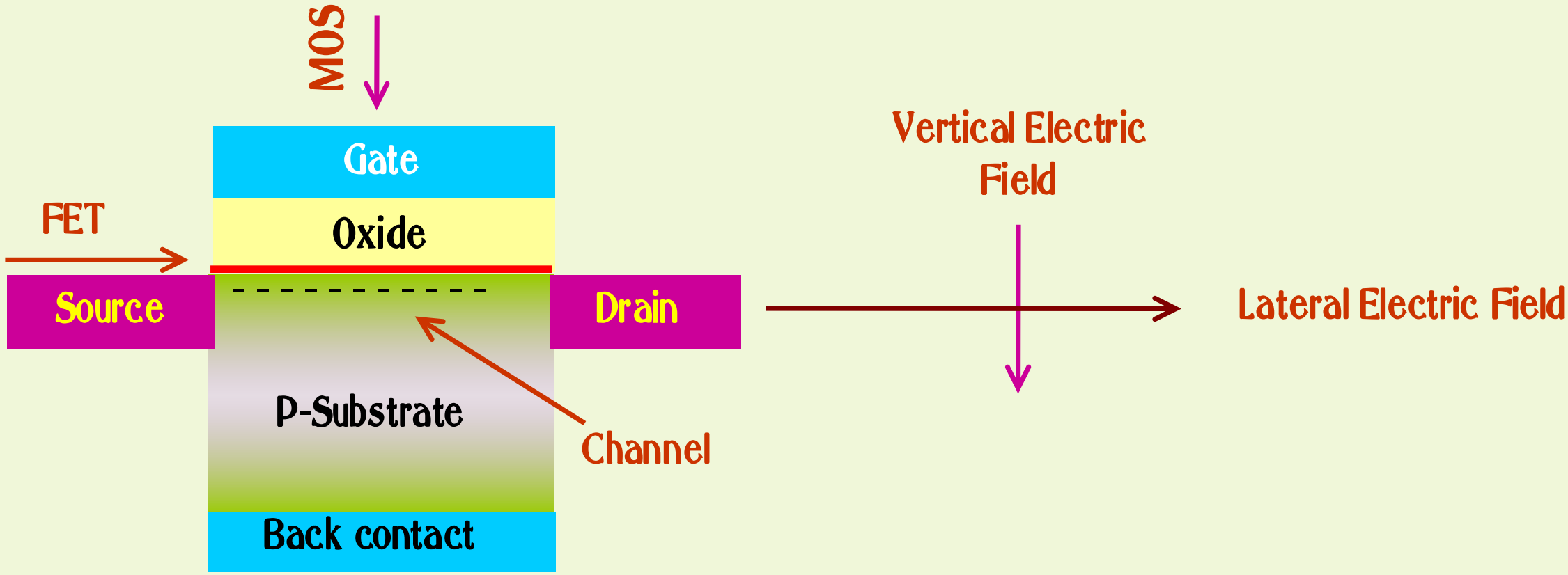
97% is covered by Si

- Complementary-Metal-oxide-Semiconductor (CMOS).
- P - Metal-Oxide-Semiconductor Field Effect Transistor (p-MOSFET).
- N - Metal-Oxide-Semiconductor Field Effect Transistor (n-MOSFET).

$$CMOS = p-MOS + n-MOS$$

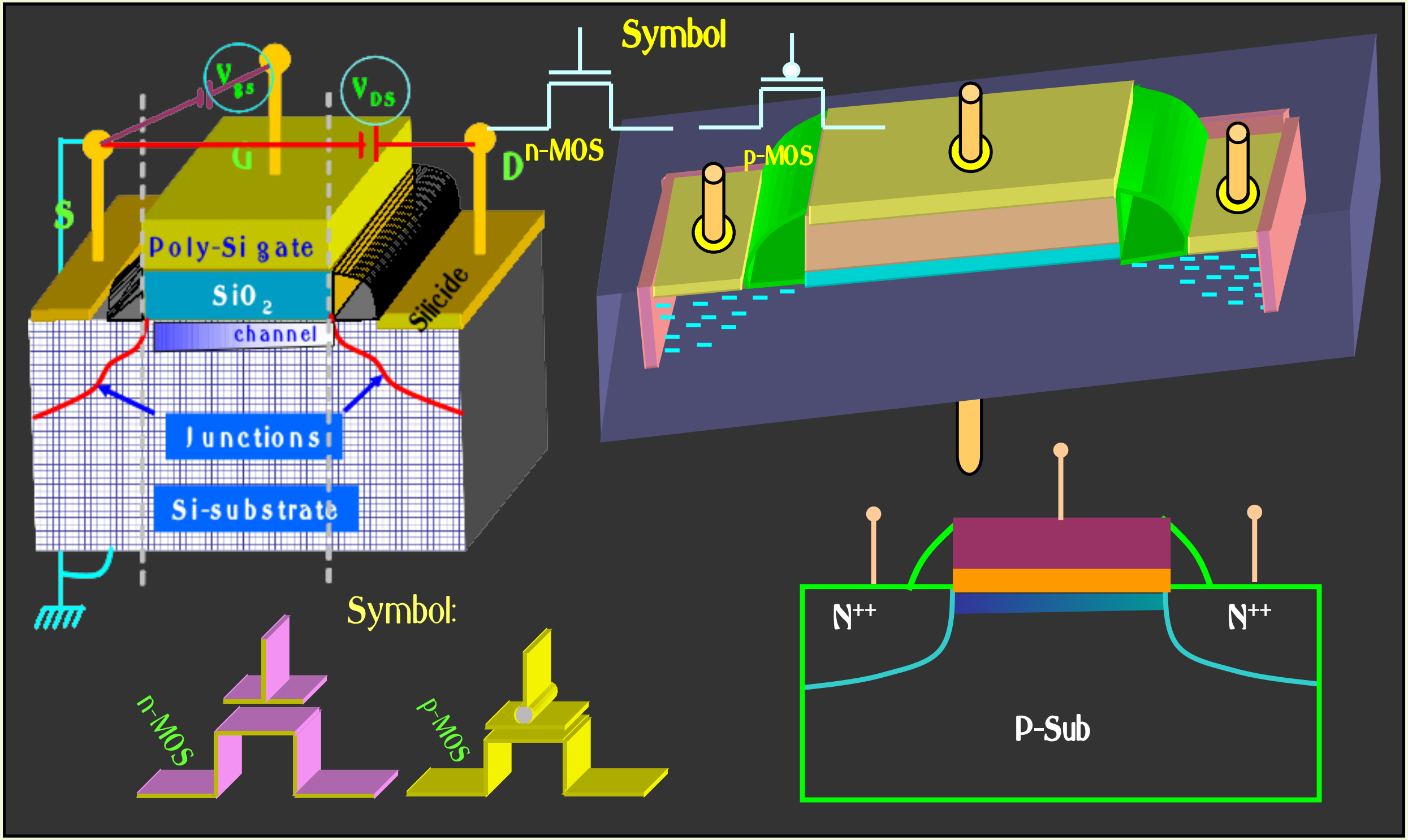
- CMOS is a combination of an n-MOSFET and p-MOSFET.

MOSFET

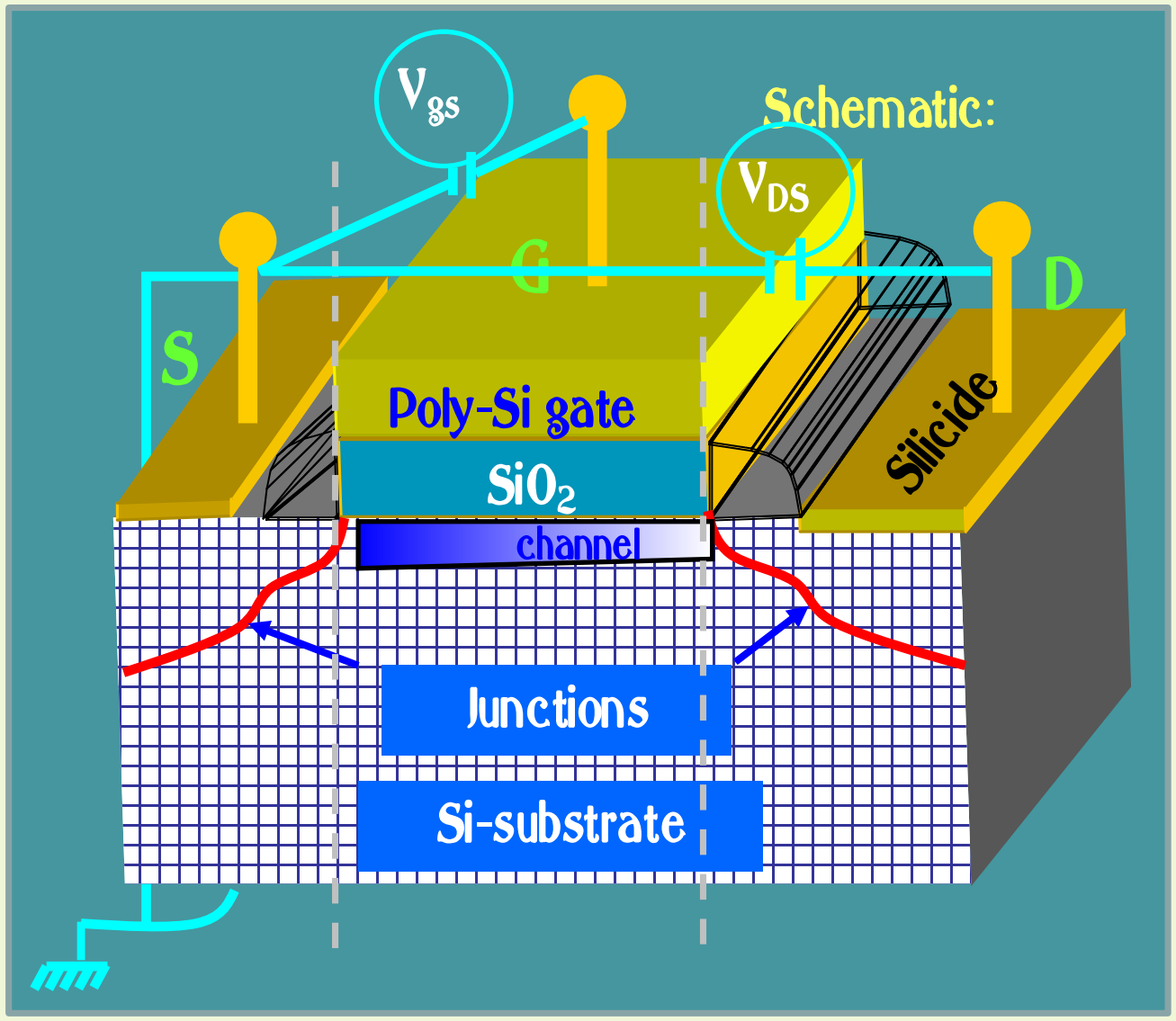


Two orthogonal electric fields work together to initiate the operation of a MOSFET. Vertical field applied from the gate creates a channel for the carriers and lateral electric field drags the carriers from source to the drain, leading to generate a current along the channel.

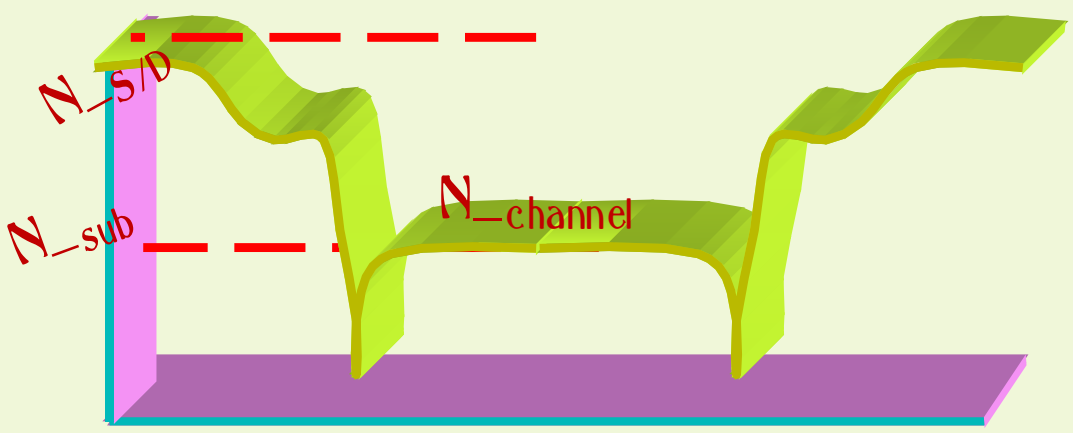
MOSFET schematics



MOSFET schematics

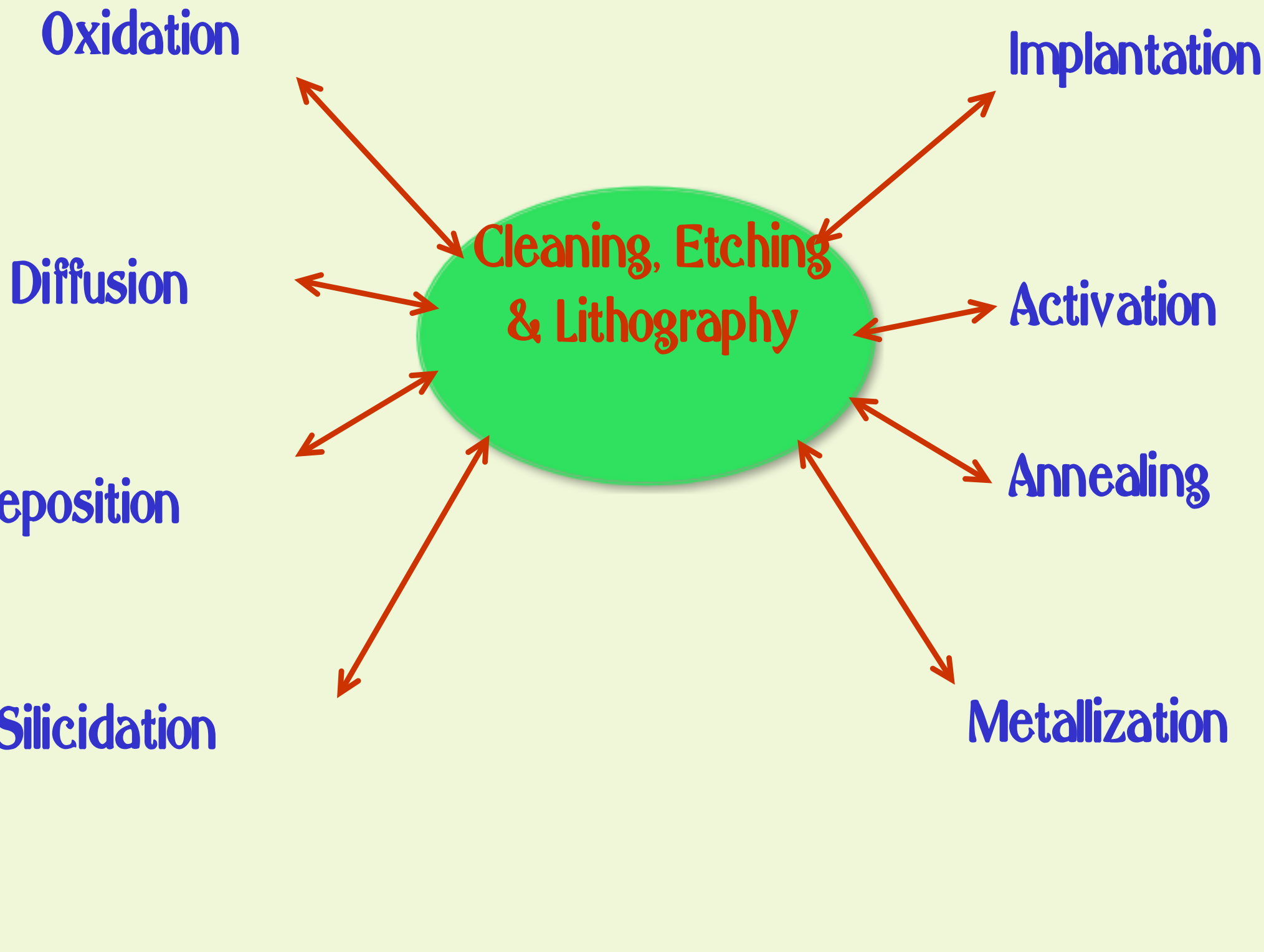


- 3 or 4-terminal devices: Gate (G), Source (S) and Drain (D).
- Import regions: channel, junctions, gate insulator.
- Device parameters: Gate length (L), device width (W), oxide thickness, channel doping.



- On application of voltages at the gate (V_G), and S/D regions (V_{DS}), current flows through the channel (from S to D).

Basic processing modules



Typical MOSFET process flow

Thermal gate oxidation

Poly-Si deposition and gate definition

LDD implant and activation

Si_3Ni_4 deposition & RIE

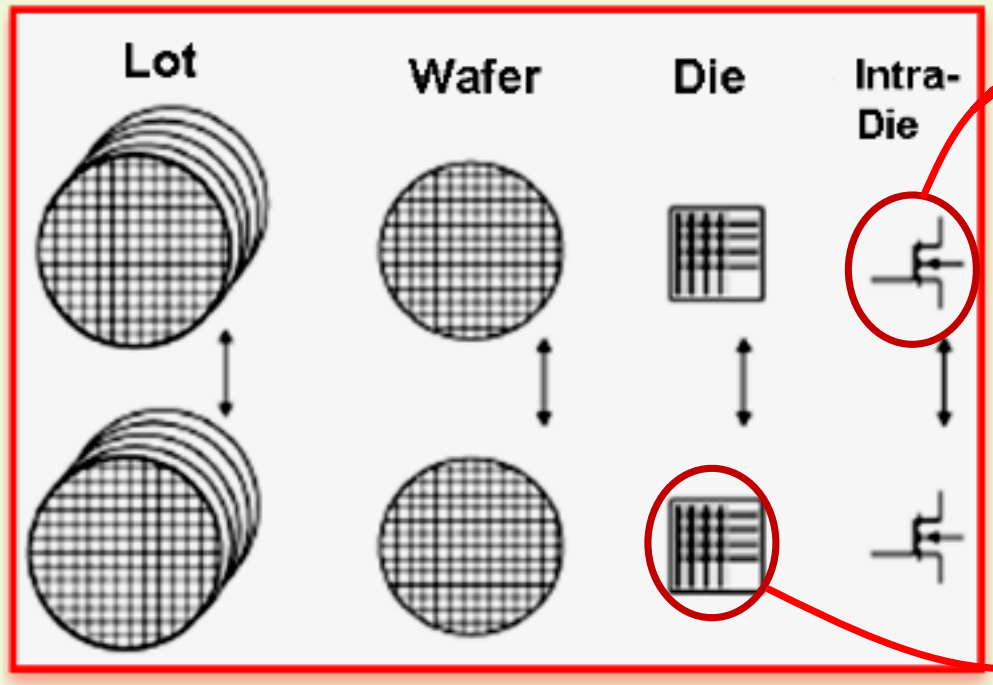
HDD implant and activation

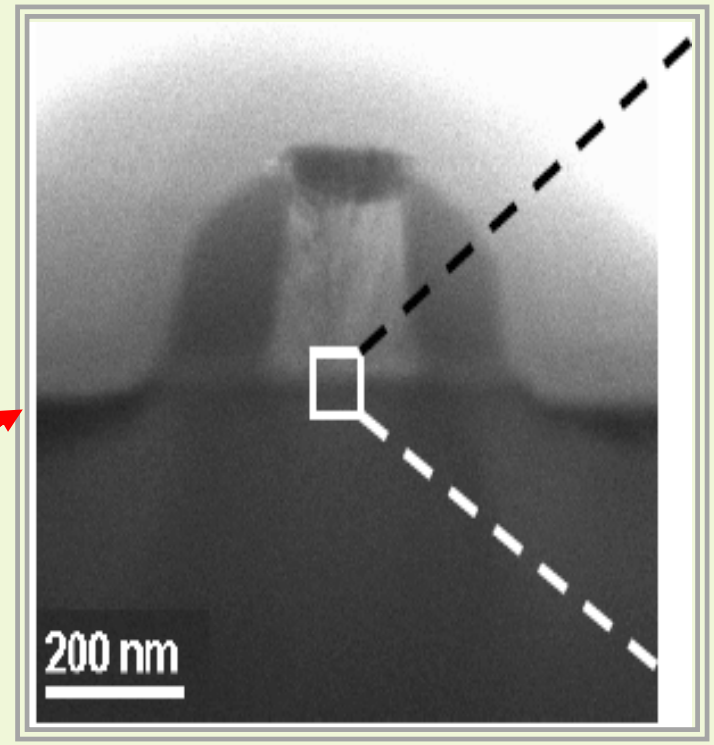
Ti deposition and SALICIDATION

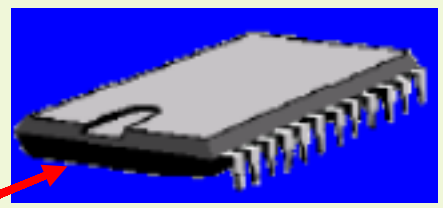
Back end process & contact creation

Main features:

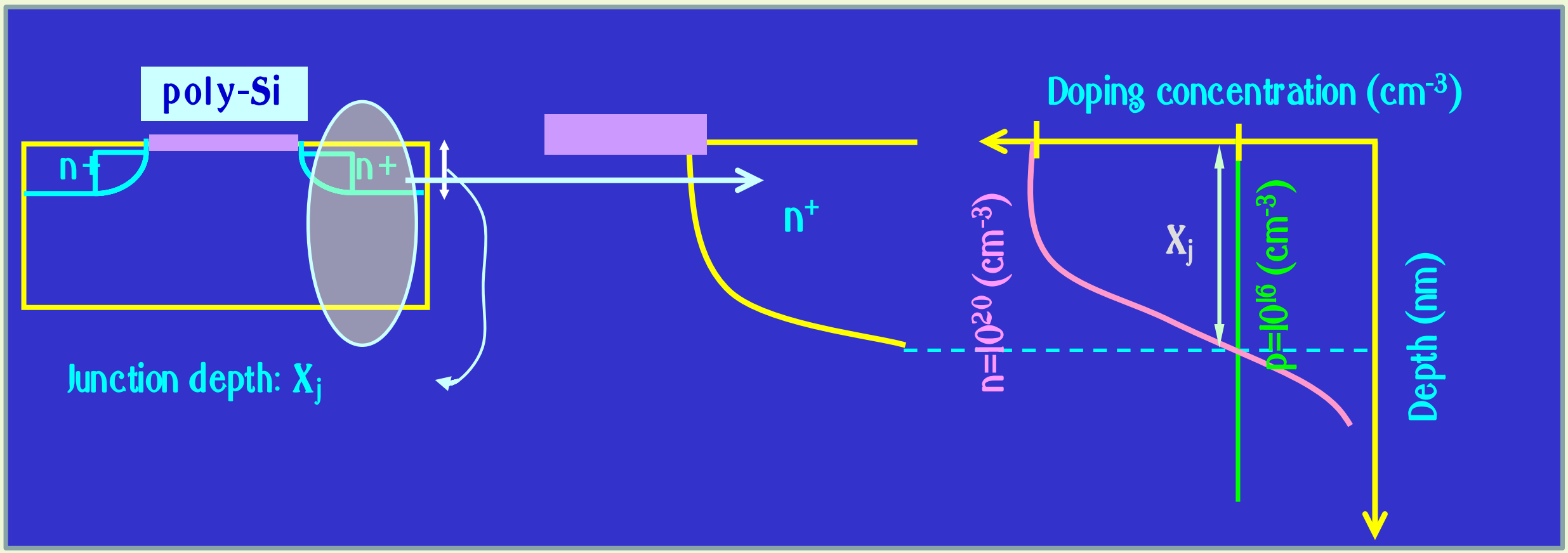
- Gate oxidation: ~ 800 C;
- Dopant activation: 1000 C;
- Side nitride spacer wall:
- Anisotropic dry etching;
- Silicide module: 800 C.







Junction depth (X_j) and doping profile

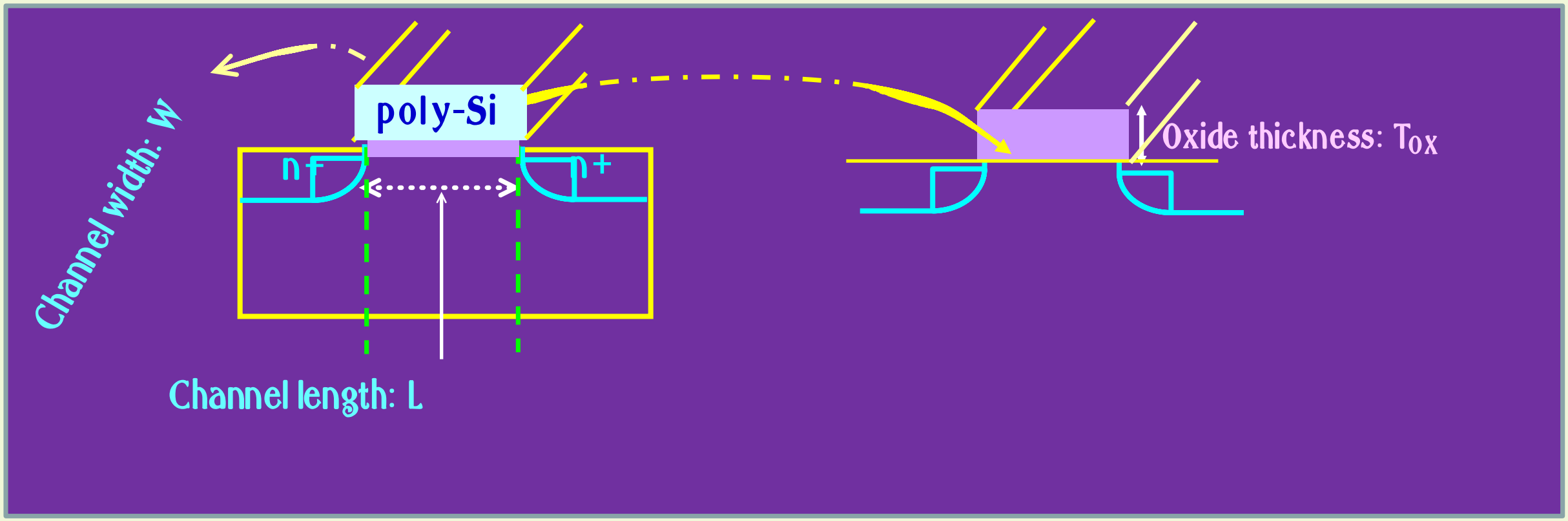


Process parameters:

- Implantation
- Implantation dose
- Implantation energy
- Implantation profile

- At the depth of X_j, the n-type (S/D) and p-type (substrate) doping concentrations will be same.
- Low implant energy reduces junction depth, high energy increases it.

Dimension: L_g, T_{ox} and W



Process parameters:

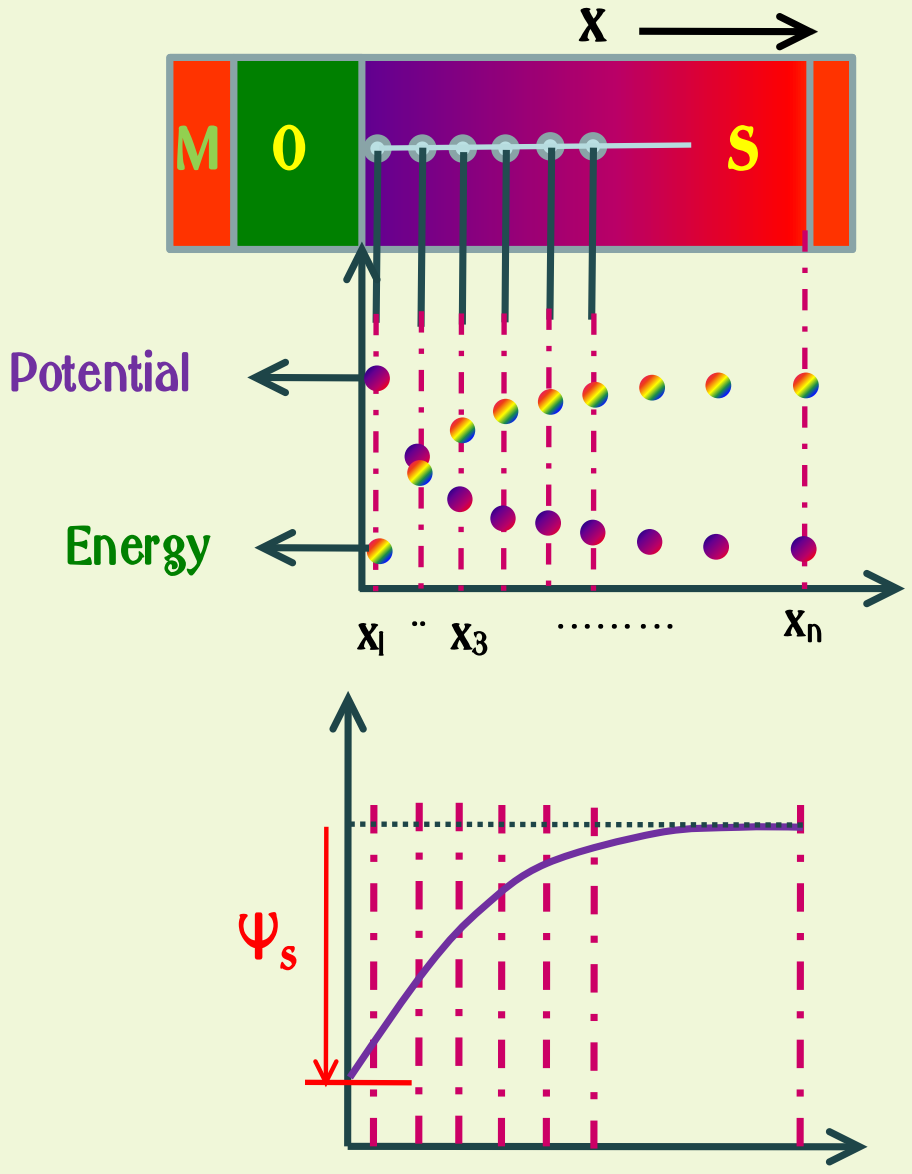
- Lithography
- Wavelength used
- Different techniques
- Exposure time
- Lateral diffusion of dopants
- Physical and electrical length

Process parameters:

- Oxidation time
- Oxidation temperature
- Oxidation environment
- Oxidation techniques
- Oxidation kinetics

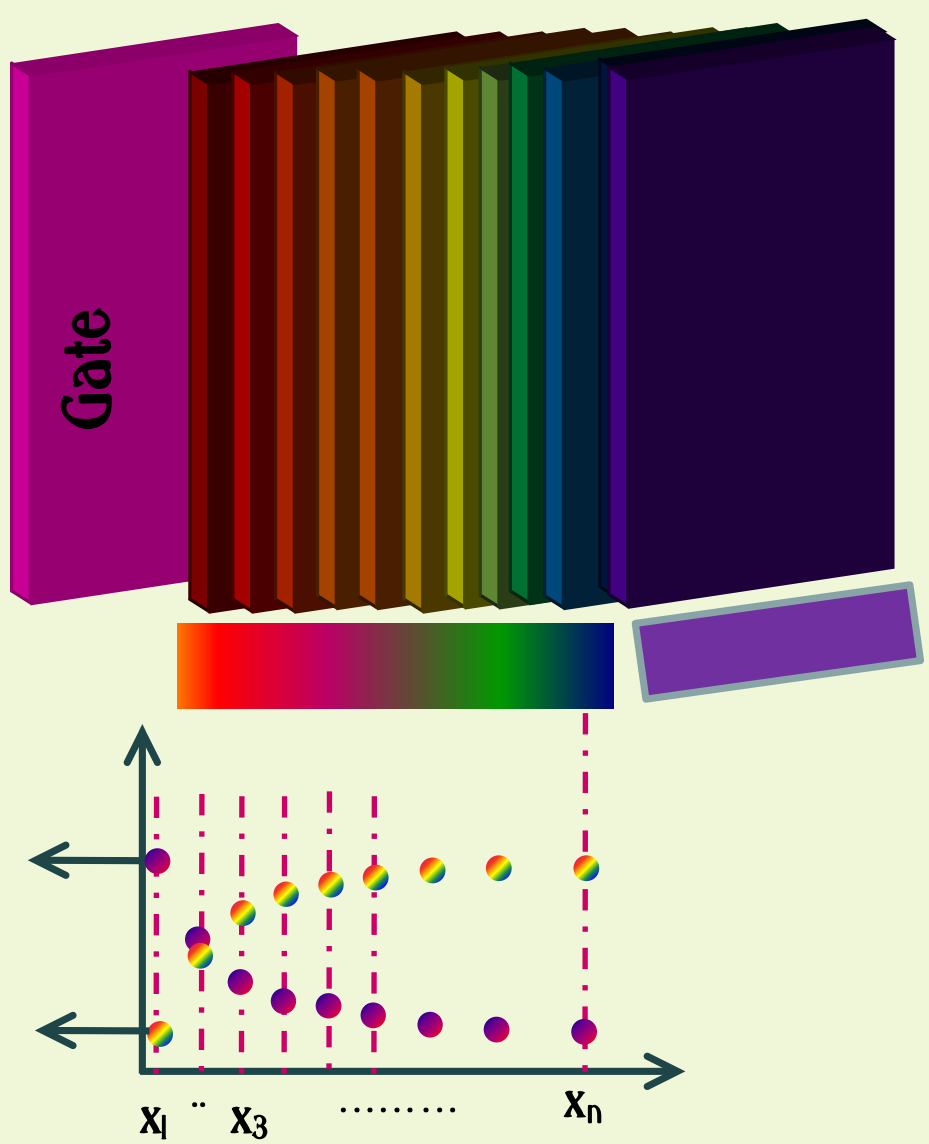
Physics of the metal-oxide-semiconductor (MOS) systems

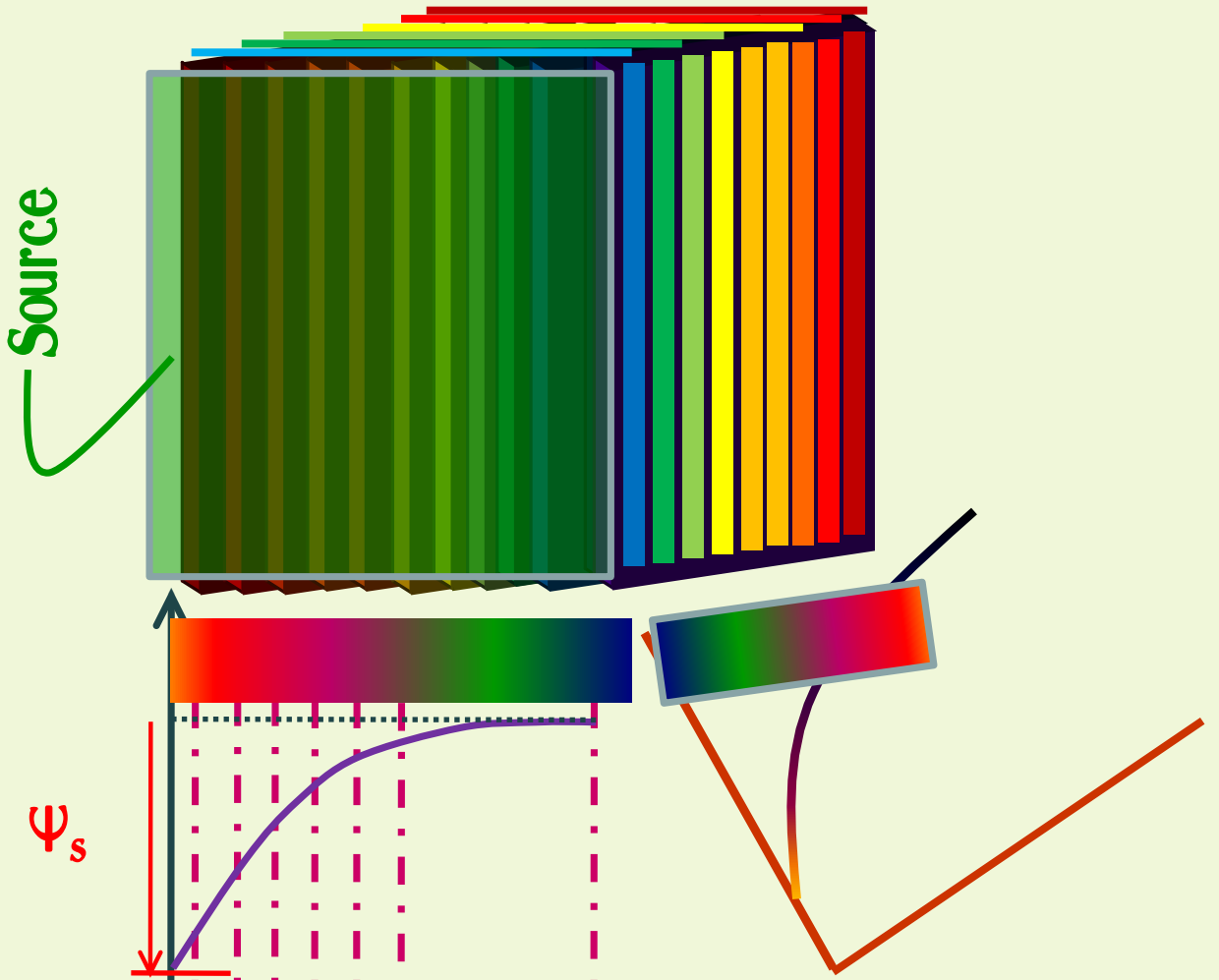
Band diagram of MOS system

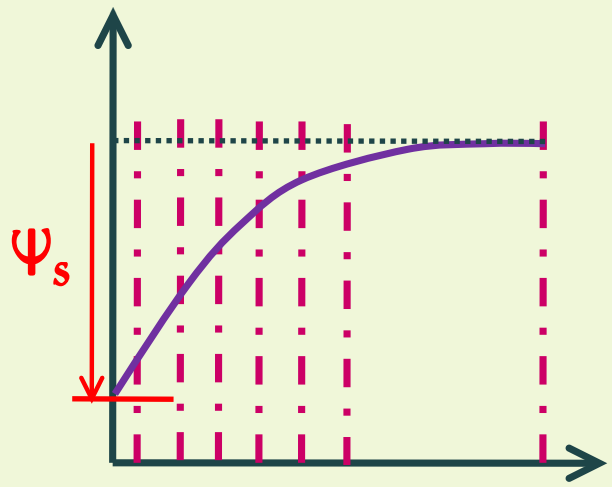


- Band bends on application of a gate voltage, leading to redistribution of carrier underneath the oxide layer.
- Either the majority carrier or minority carriers will be attracted, depending upon the polarity of the applied voltage and substrate doping nature.
- The measurement parameter is the surface potential (Ψ_s).
- Surface potential is positive when band bend downward and it is negative when it bend upward.

3-D band alignment in a MOSEFT

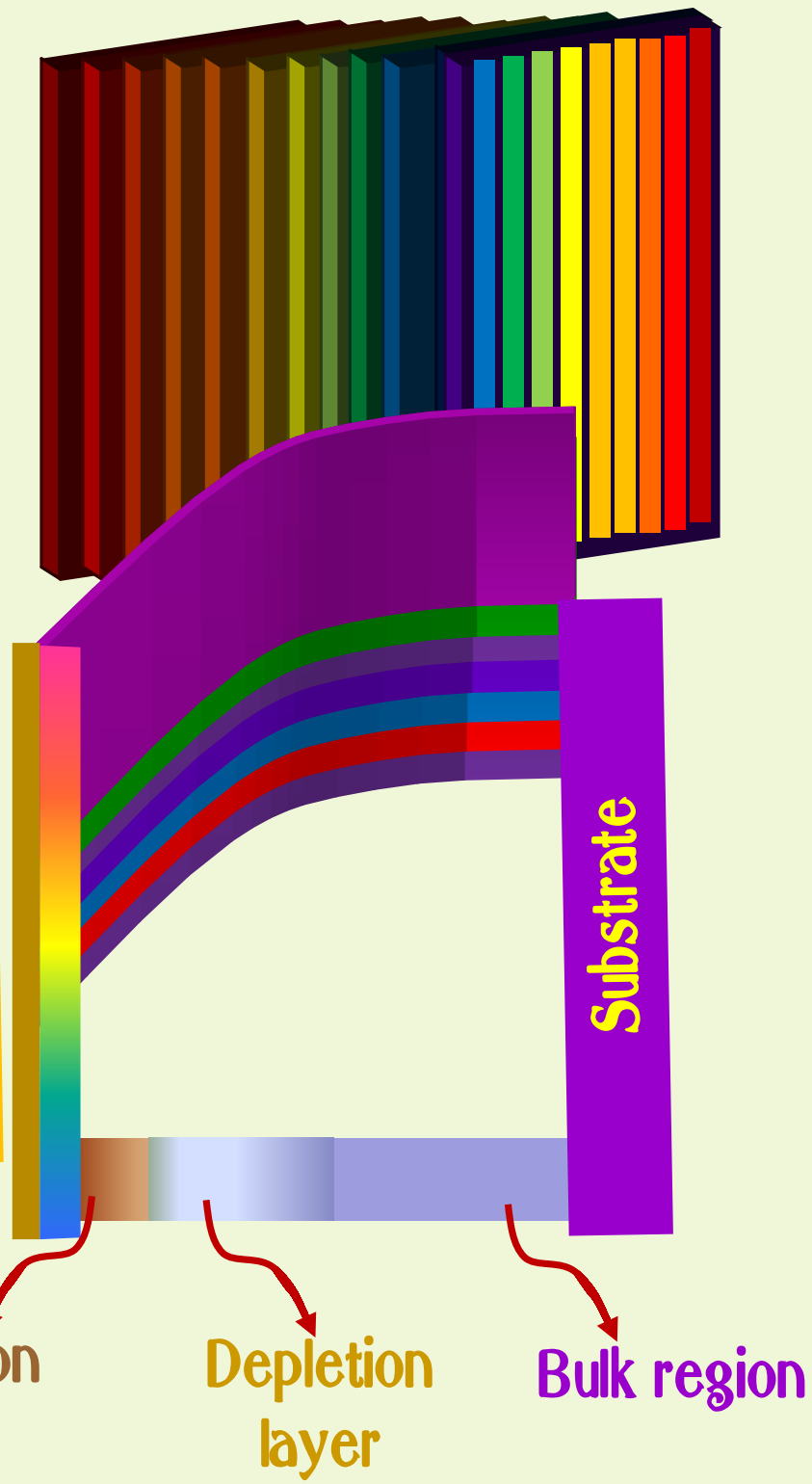


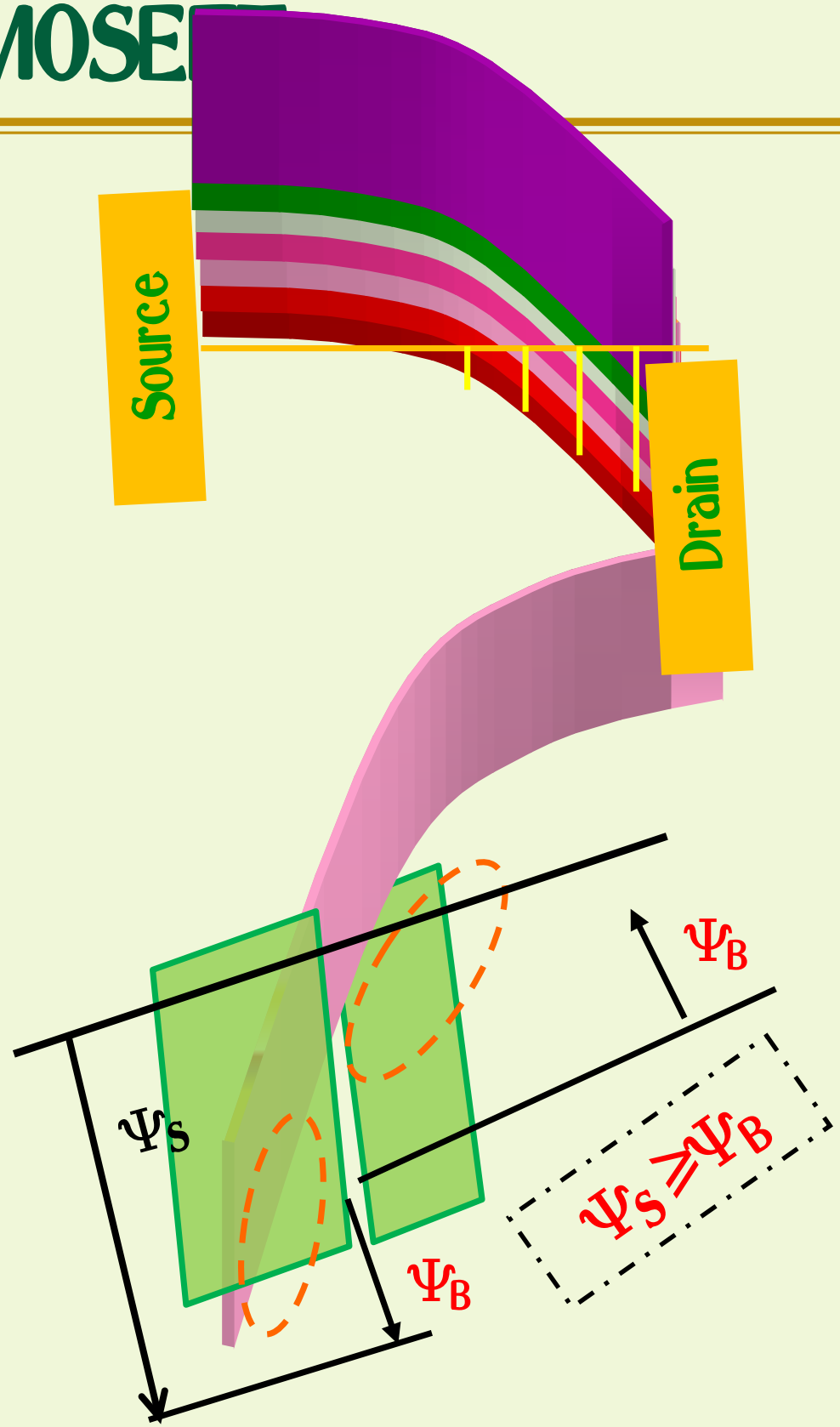




- Final surface potential is controlled by the simultaneous action of both the gate-to-channel and source-to-drain voltages.

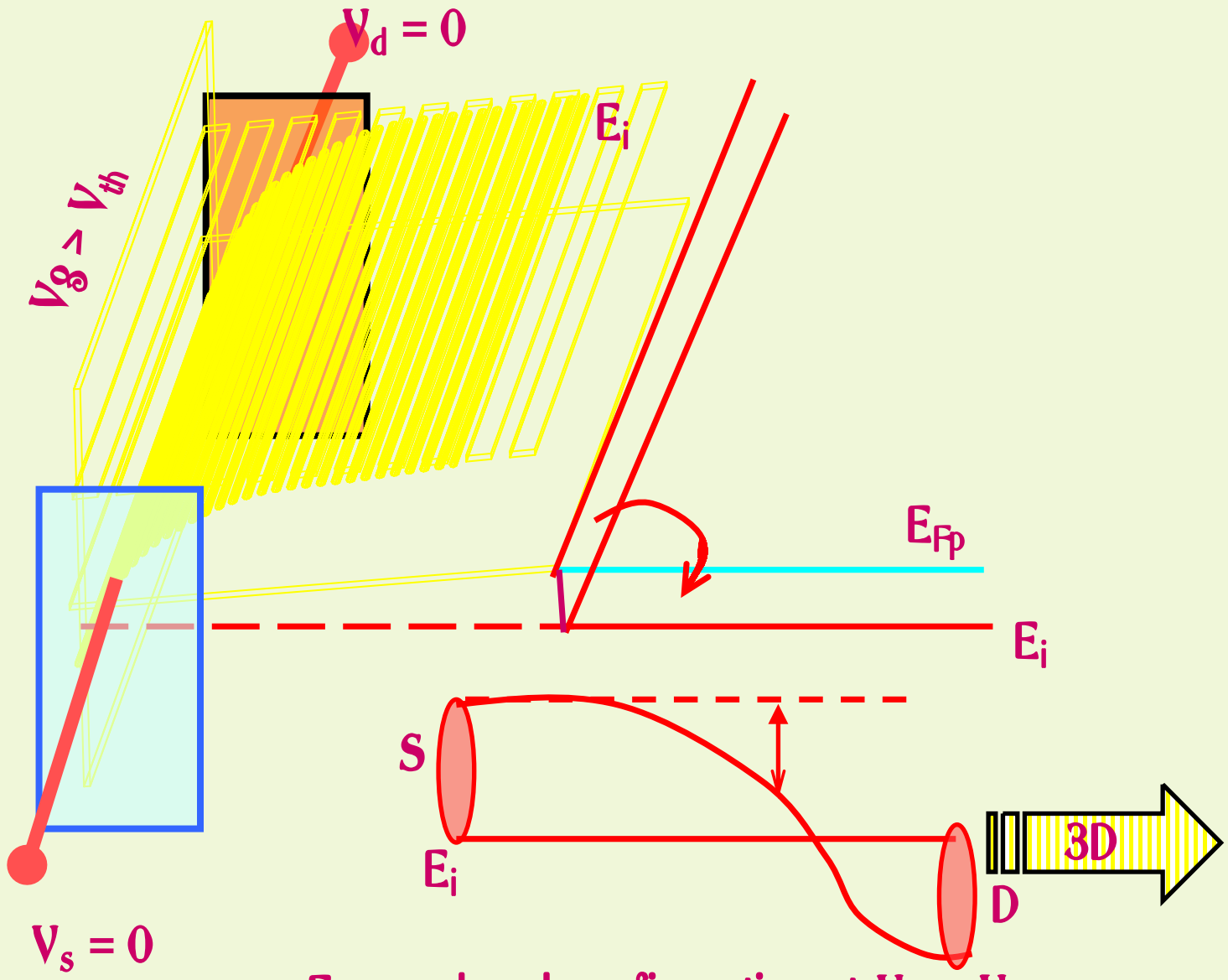
3-D band alignment in a MOSFET

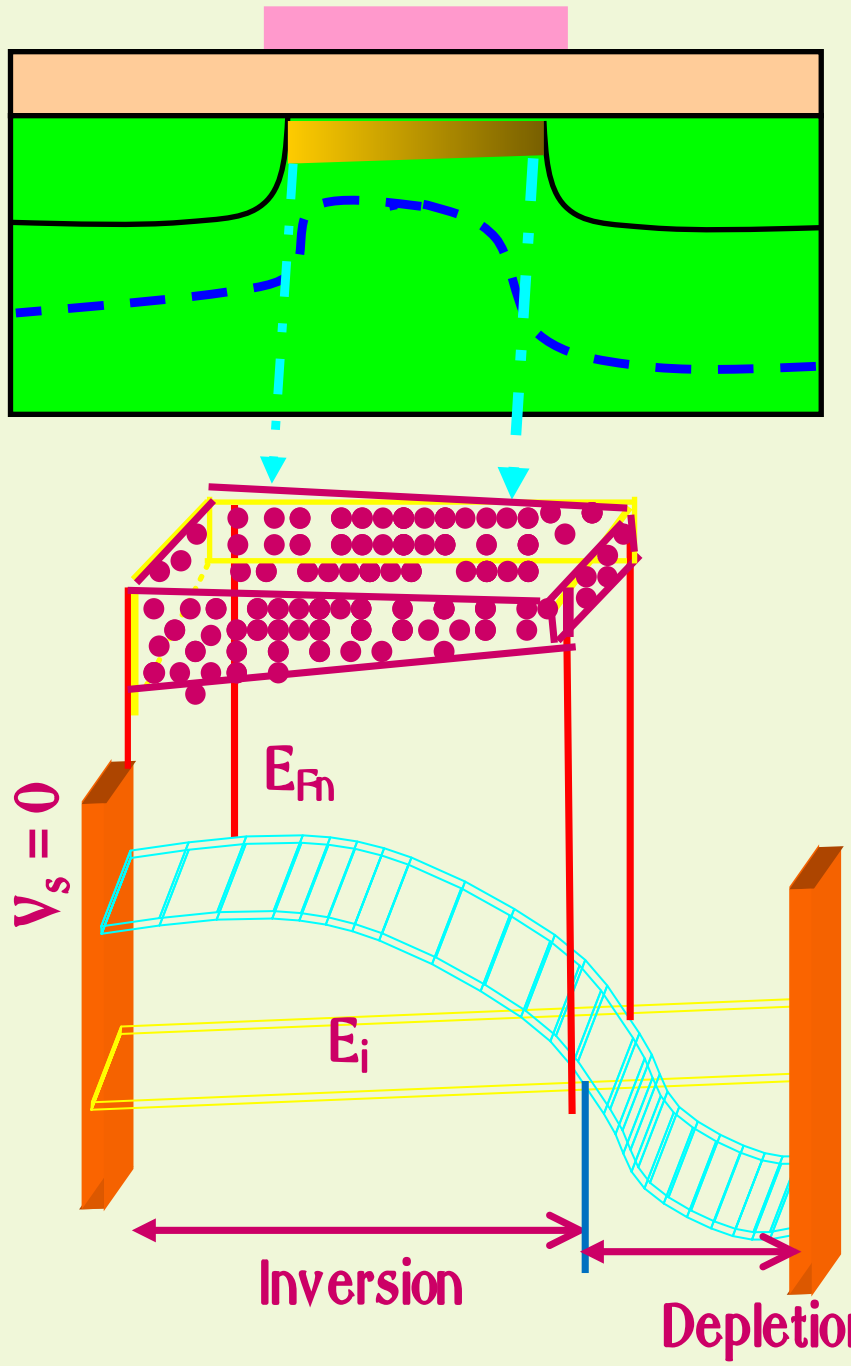




3-D band alignment in a MOSEFT

- Inversion layer is tapered @ drain end. E_{Fn} crosses down to E_i near the drain.





3D

Energy band configuration at $V_g > V_{th}$ and $V_d > 0$.

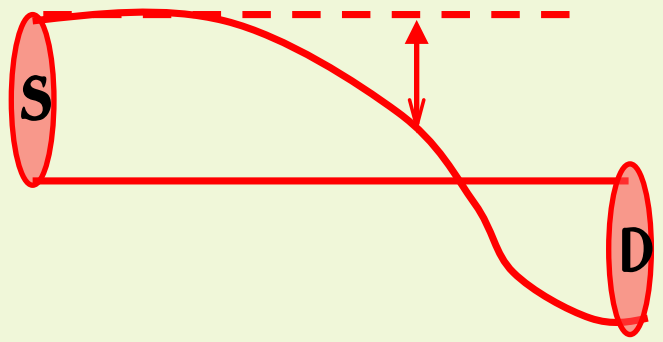
MOSFET: transport modeling

Charge sheet model:

- channel is very thin, no voltage drops across it.
- vertical electric field is very high compared to lateral electric field.
- total charge at the metal side = to the net charge in the semiconductor side.

Net charge:

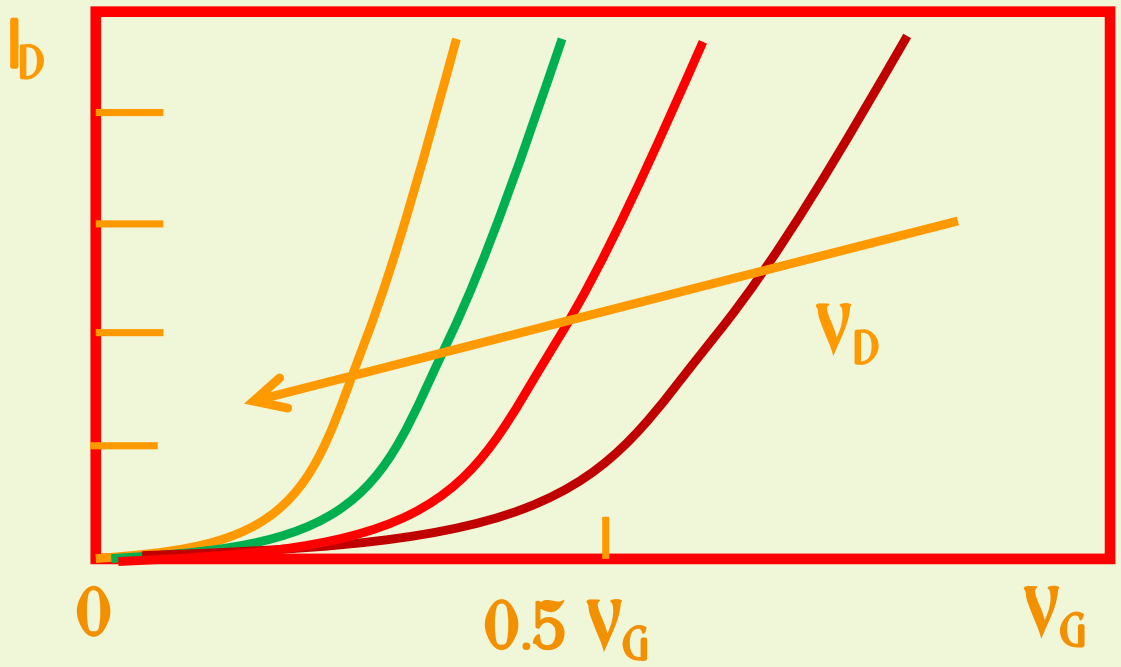
$$|Q_n(y)| = [V_G - y - 2\Psi_B]C_{ox} - \sqrt{2\varepsilon_s q N_A (2\Psi_B + y)}$$

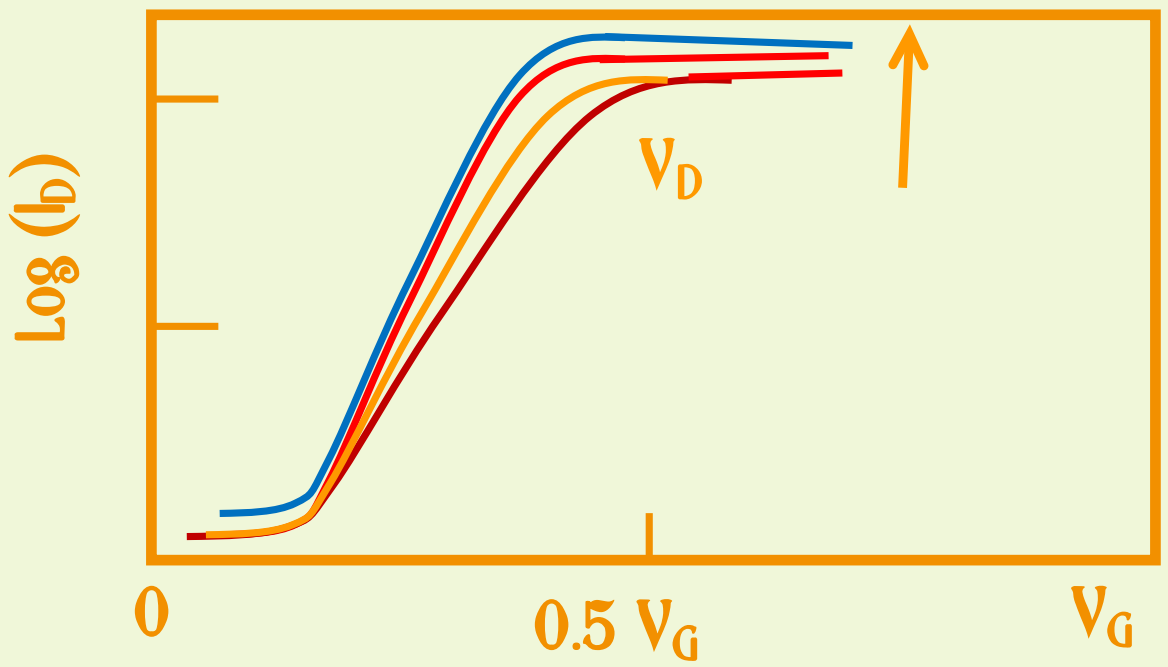


Current-voltage characteristic:

$$I_D = \frac{W}{L}\cdot\mu_n\cdot C_{ox}\left\{\left(V_G - V_{FB} - 2\Psi_B - \frac{V_D}{2}\right)V_D - \frac{2\sqrt{2\varepsilon_s q N_A}}{3 C_{ox}}\left[3\cdot\sqrt{\frac{\Psi_B}{2}\cdot V_D}\right]\right\}$$

Electrical characteristics





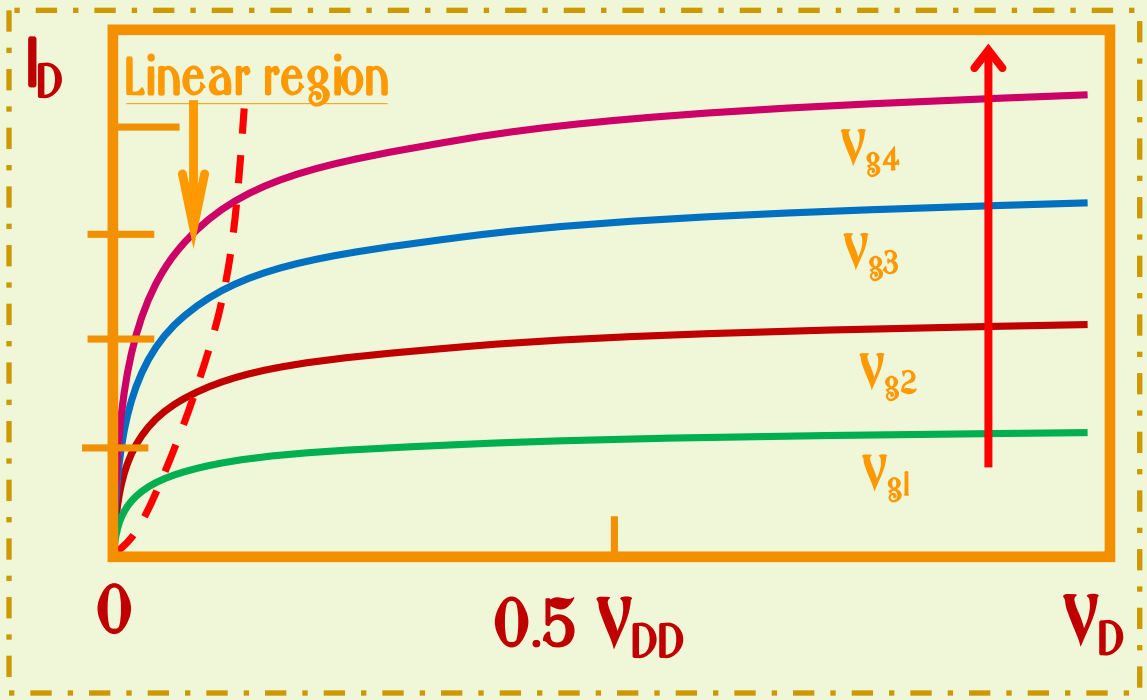
Transfer characteristics

Linear region:

$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}\frac{W}{L}.(V_G - V_{th})V_D$$

Saturation region:

$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}.\frac{W}{L}.\frac{(V_G - V_{th})^2}{2}$$



Output characteristics

Characteristic parameters

- Threshold voltage: V_{th}
- Off-state leakage current: I_{off}
- On-state current: I_{on}
- On-state/off-state current: I_{on}/I_{off}
- Trans-conductance: g_m
- Channel conductance: g_d
- Sub-threshold slope: S
- Drain voltage: V_{dd}
- Channel mobility: μ
- S/D resistance: R_s and R_d
- DIBL