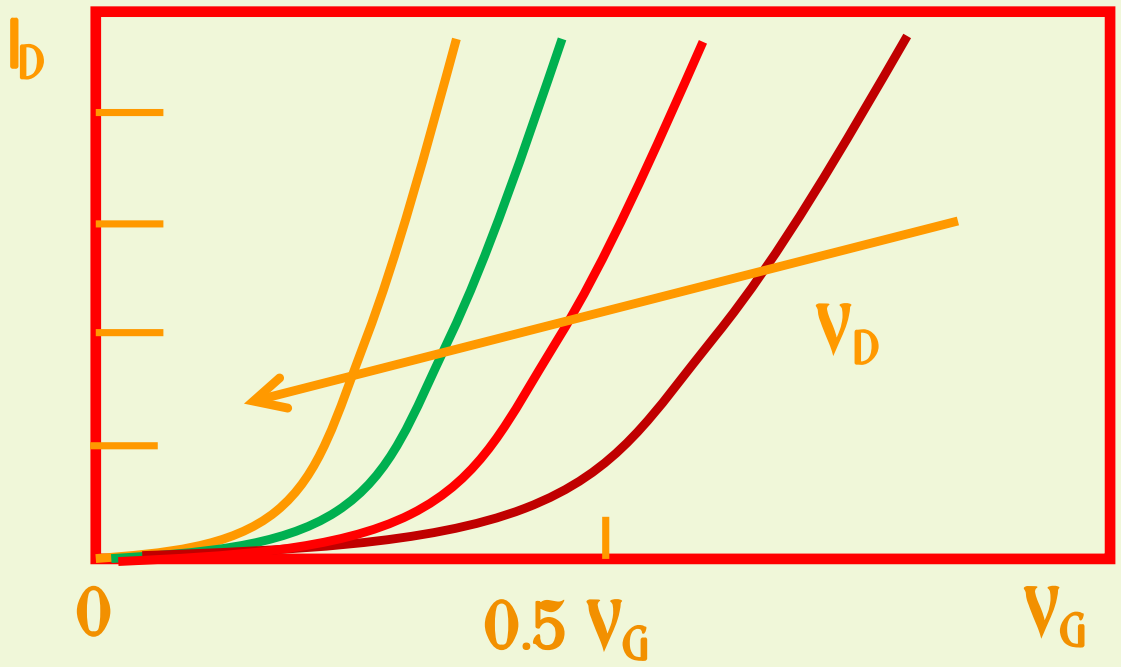
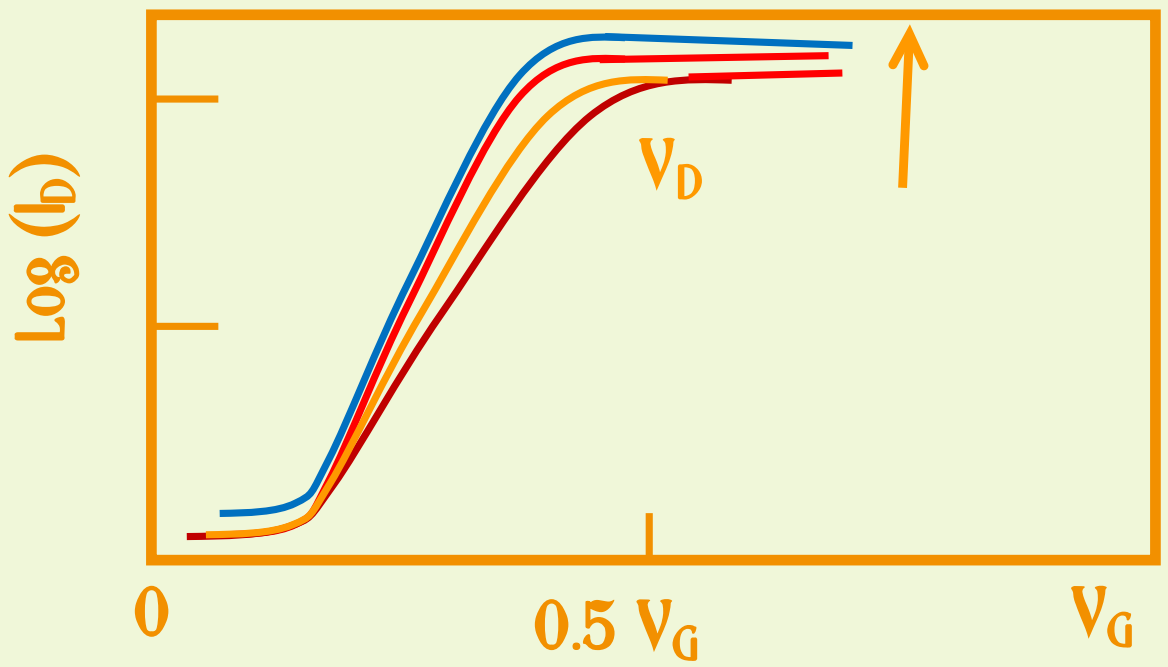
The performance parameters of MOSFETs

Dr. Sanatan Chattopadhyay

University of Calcutta

Electrical characteristics





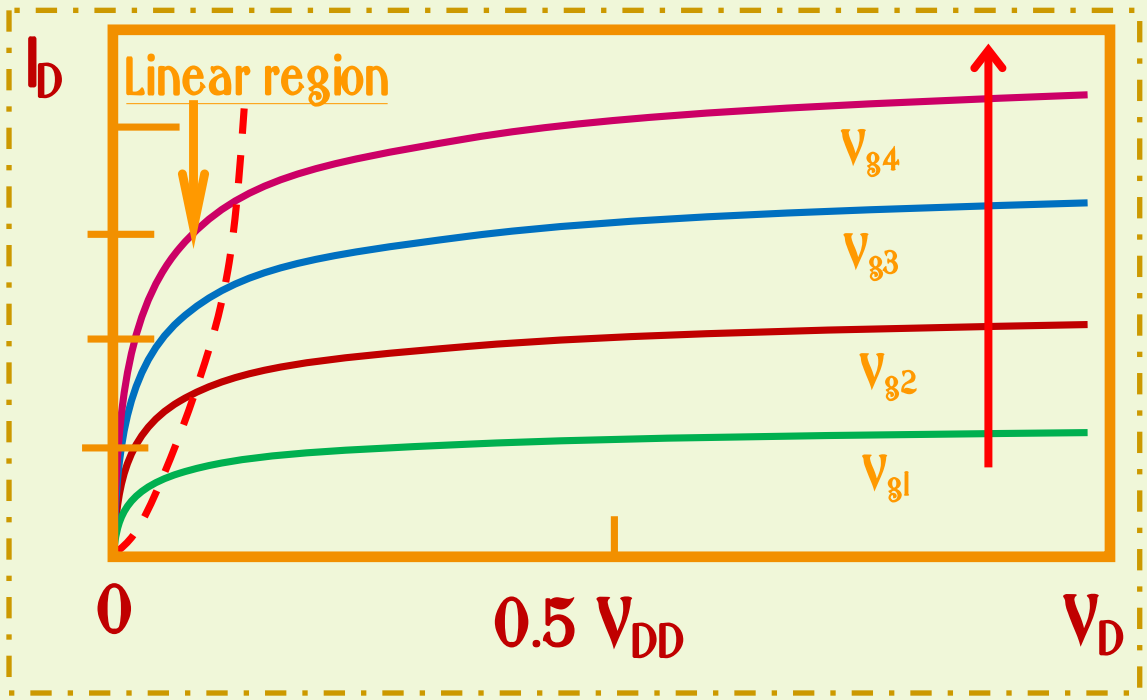
Transfer characteristics

Linear region:

$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}\frac{W}{L}.(V_G - V_{th})V_D$$

Saturation region:

$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}.\frac{W}{L}.\frac{(V_G - V_{th})^2}{2}$$



Output characteristics

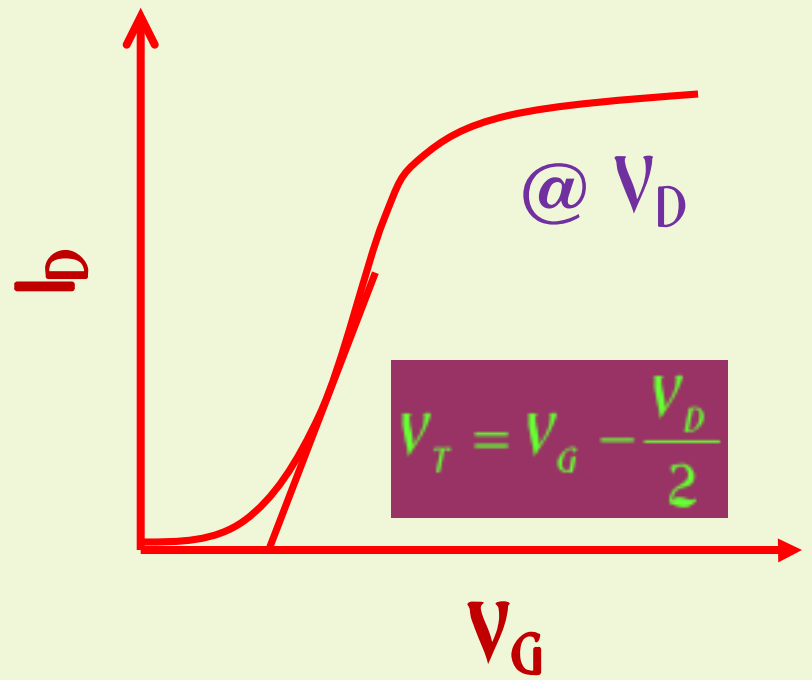
Characteristic parameters

- Threshold voltage: V_{th}
- Off-state leakage current: I_{off}
- On-state current: I_{on}
- On-state/off-state current: I_{on}/I_{off}
- Trans-conductance: g_m
- Channel conductance: g_d
- Sub-threshold slope: S
- Drain voltage: V_{dd}
- Channel mobility: μ
- S/D resistance: R_s and R_d
- DIBL

Threshold voltage of a MOSFET

- Minimum gate voltage required to create an inversion layer in a MOSFET.

$$V_{th} = V_{FB} + 2\Psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\Psi_B)}}{C_{ox}}$$



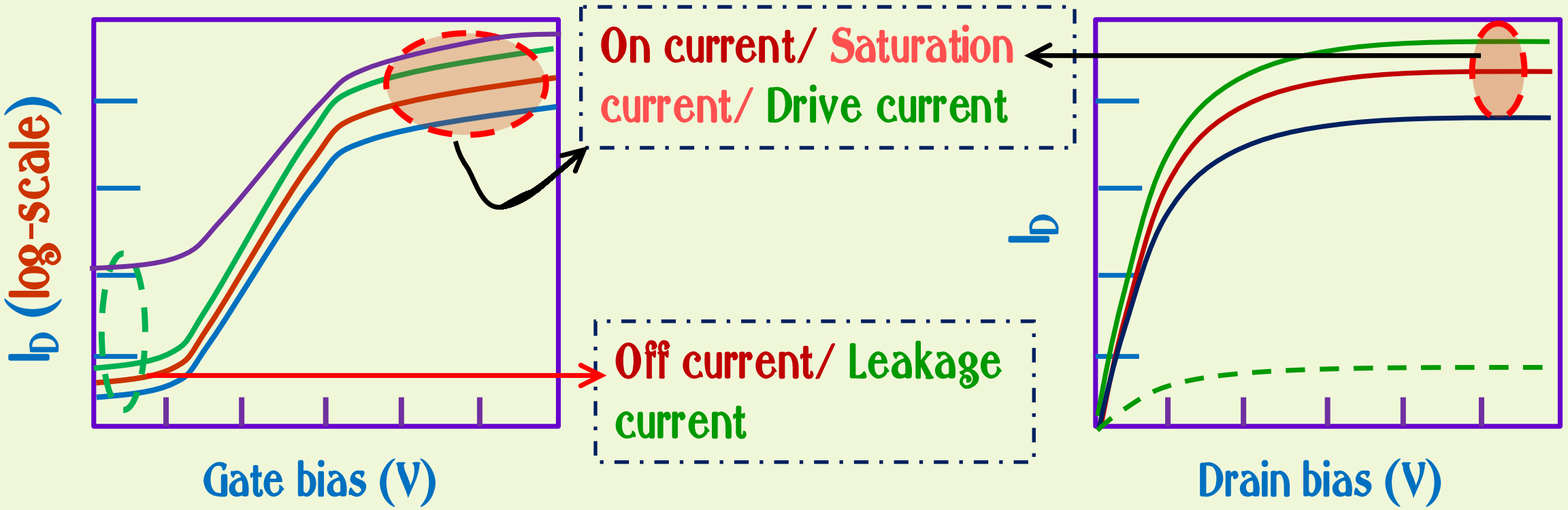
Threshold voltage increases with:

- the increase of substrate doping concentration,

- the oxide thickness, and

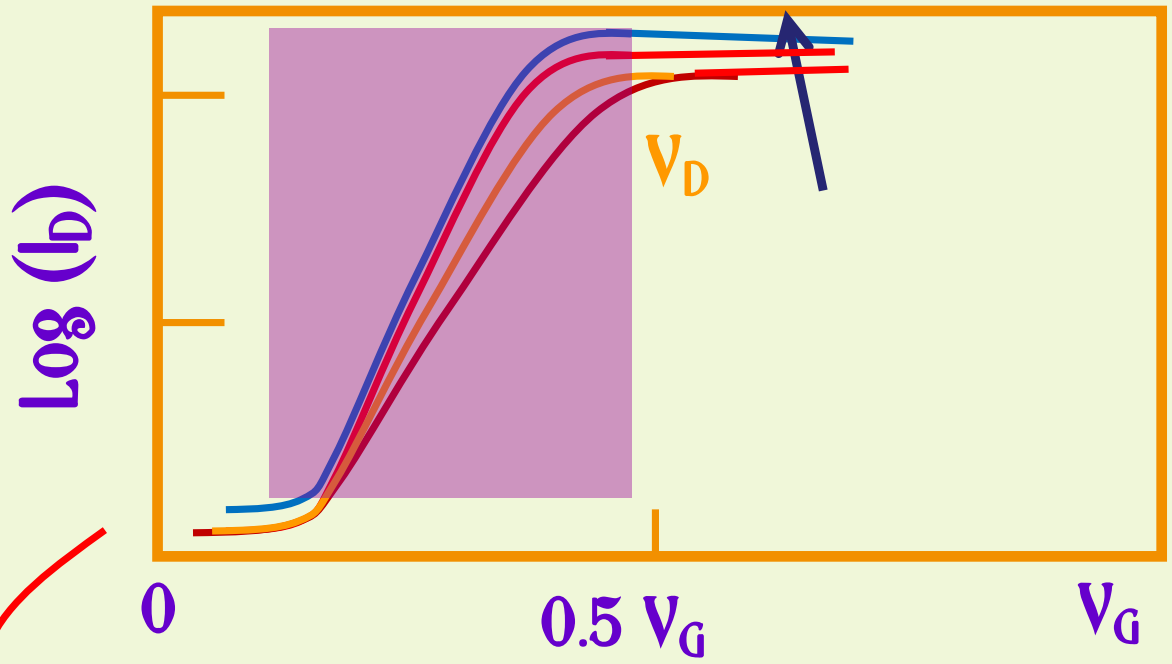
- the difference between the metal and semiconductor work functions.

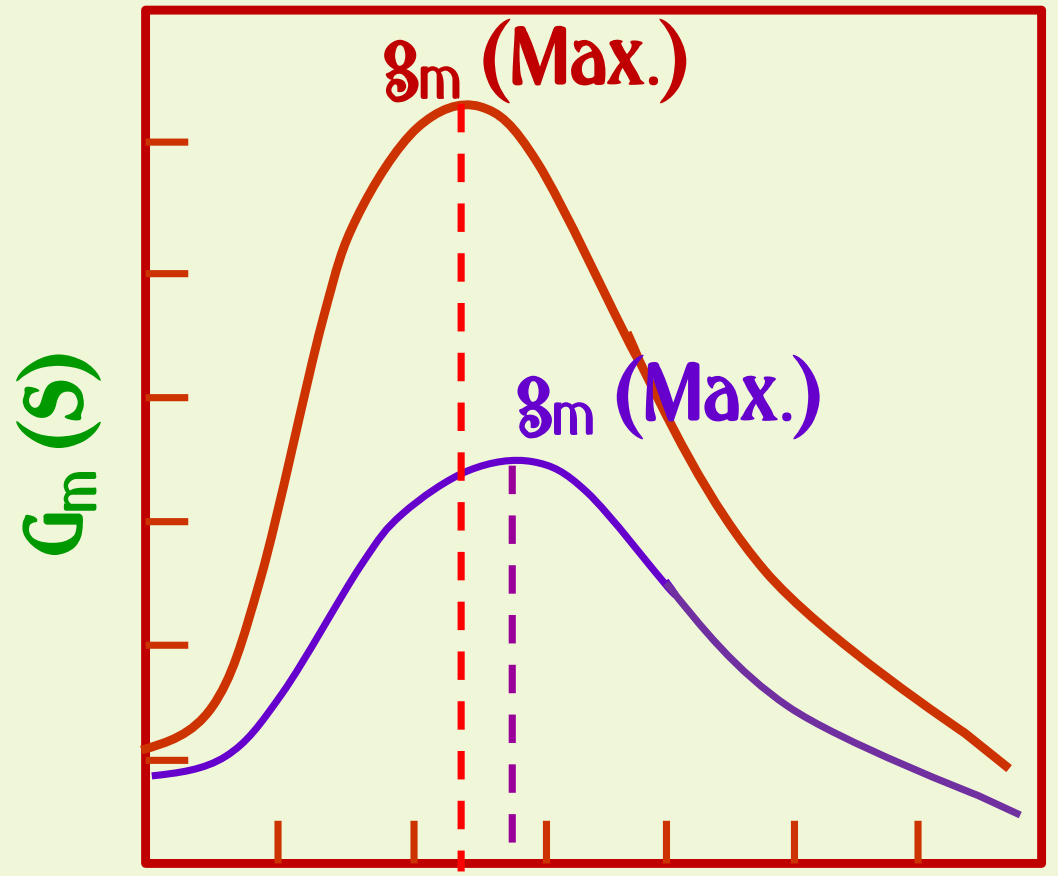
I_{on} and I_{off}



- I_{off} is the root cause of static power dissipation.
- I_{on} sets up the driving capability of a device if it is at the output of a circuit. It also indicates the level of dynamic power dissipation.

Trans-conductance (g_m)



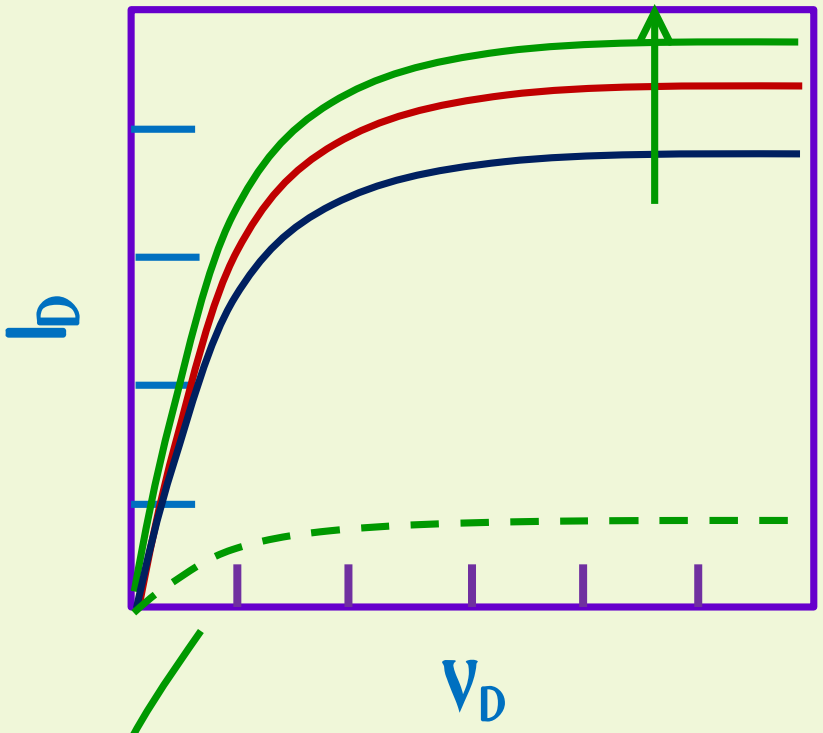


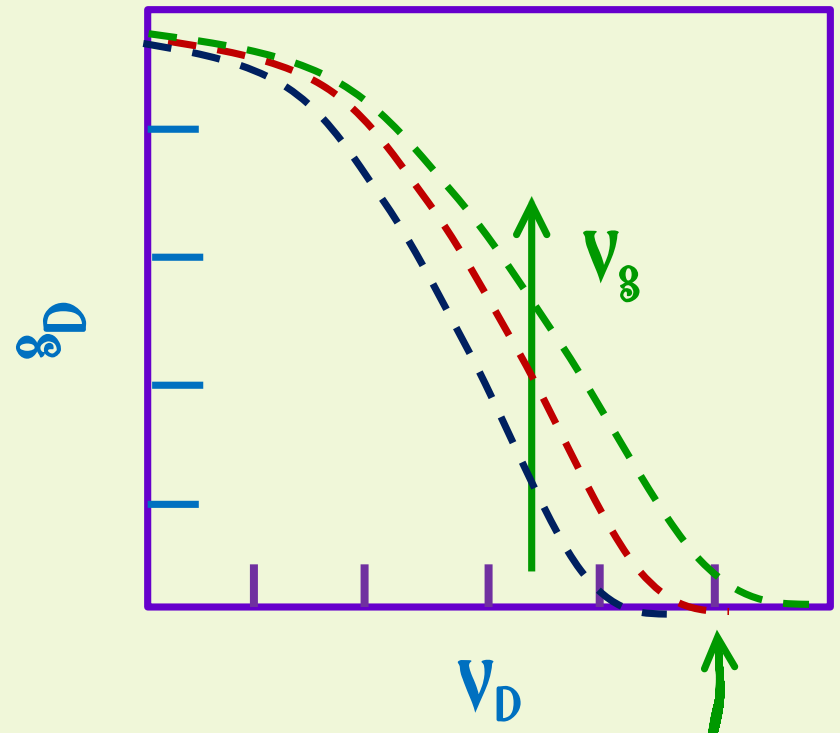
$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}\frac{W}{L}.(V_G - V_{th})V_D$$

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = Const.}$$

$$g_m = \frac{\mu\varepsilon_{ins}\varepsilon_0}{t_{ox}}.\frac{W}{L}V_{DS}$$

Output conductance (g_D)





$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}\frac{W}{L}.(V_G - V_{th})V_D$$

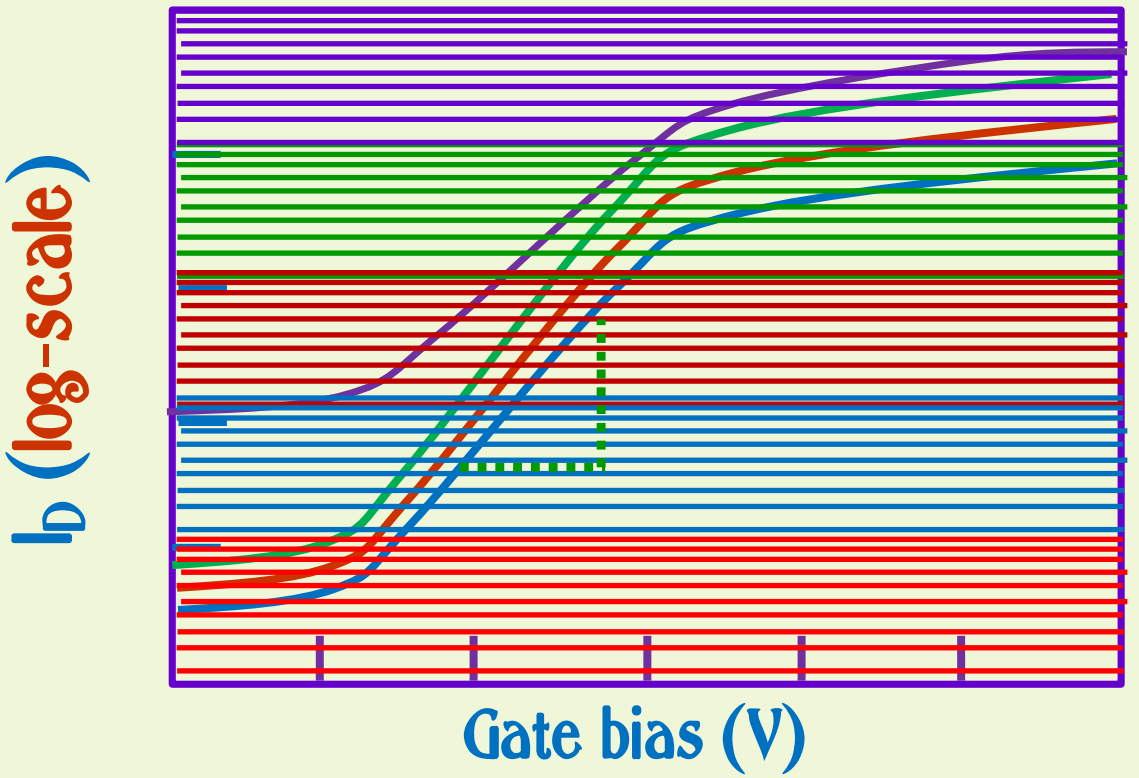
$$g_d = \frac{\partial I_D}{\partial V_D}\bigg|_{V_g = Const.}$$

$$g_d = \frac{\mu\varepsilon_{ins}\varepsilon_0}{t_{ox}}.\frac{W}{L}\left(V_{gs} - V_{th}\right)$$

Sub-threshold swing (SS)

Sub-threshold swing (SS):

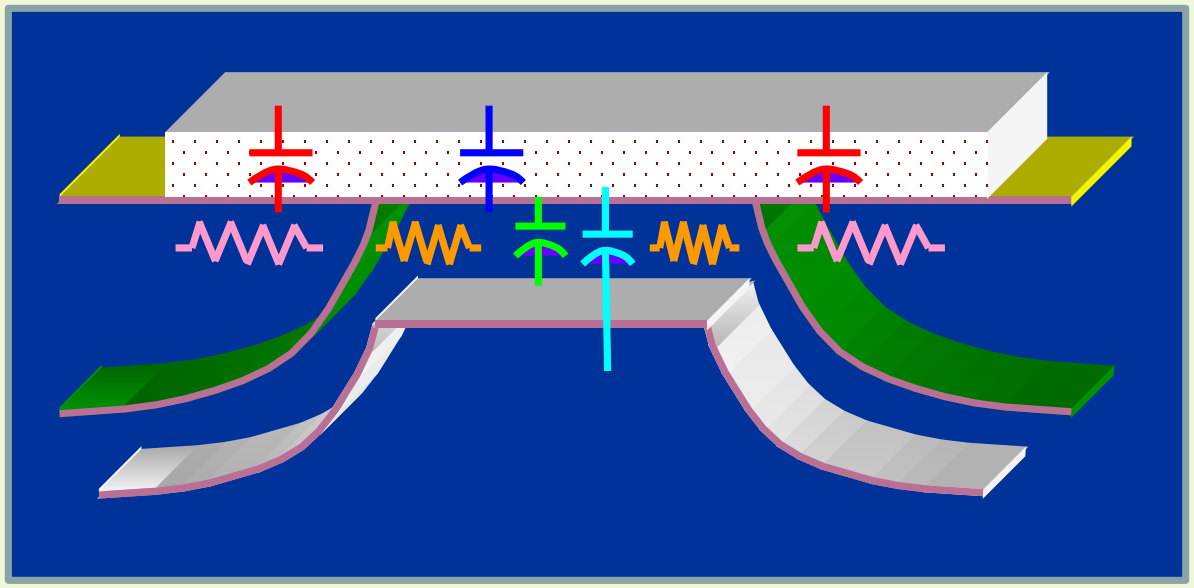
- It is the voltage required to change the drain current by one decade.
- It is the inverse of sub-threshold slope.



$$SS = \left(\frac{d(\log_{10} I_D)}{dV_{GS}} \right)^{-1} = \ln(10) \frac{k_B T}{q} \left(1 + \frac{C_D}{C_{ox}} \right)$$

- k_B is Boltzmann's constant, q is the charge of one electron, C_{ox} is the areal gate oxide capacitance and C_D is the areal depletion layer capacitance.
- It approaches to a lower limit of approximately 60 mV/dec at T = 300K when $C_D = C_{ox}$ is close to zero.

Mobility measurement



- Channel capacitance
- Oxide capacitance
- Substrate capacitance
- Channel resistance
- S/D resistance
- Overlap capacitance

$$\mu_{eff} = \frac{g_d L_{eff}}{Q_n W}$$

g_d: output conductance;

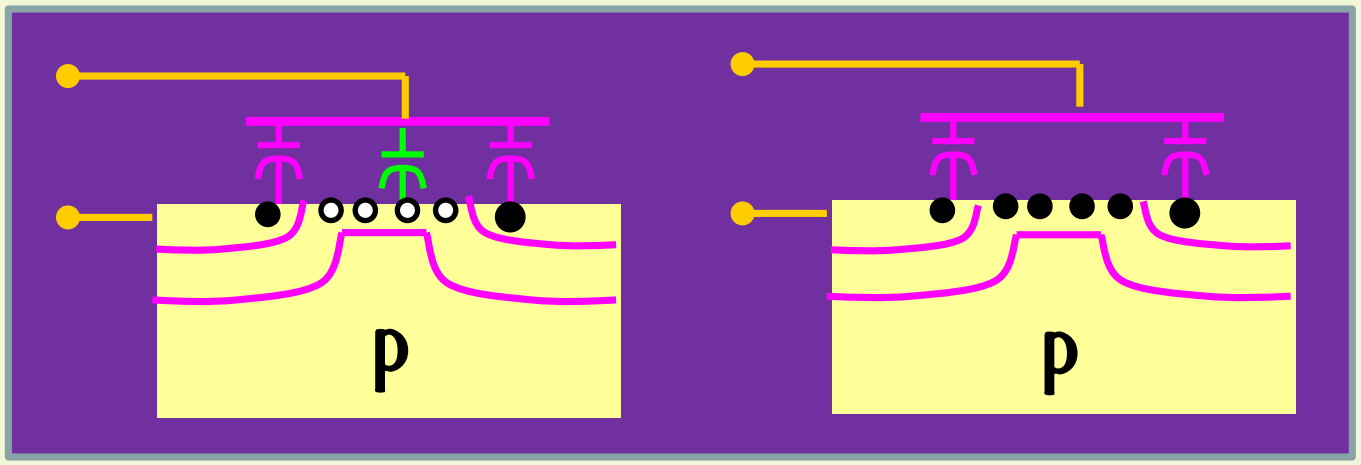
L_{eff}: effective channel length;

W: channel width.

Q_n: channel charge (inversion charge).

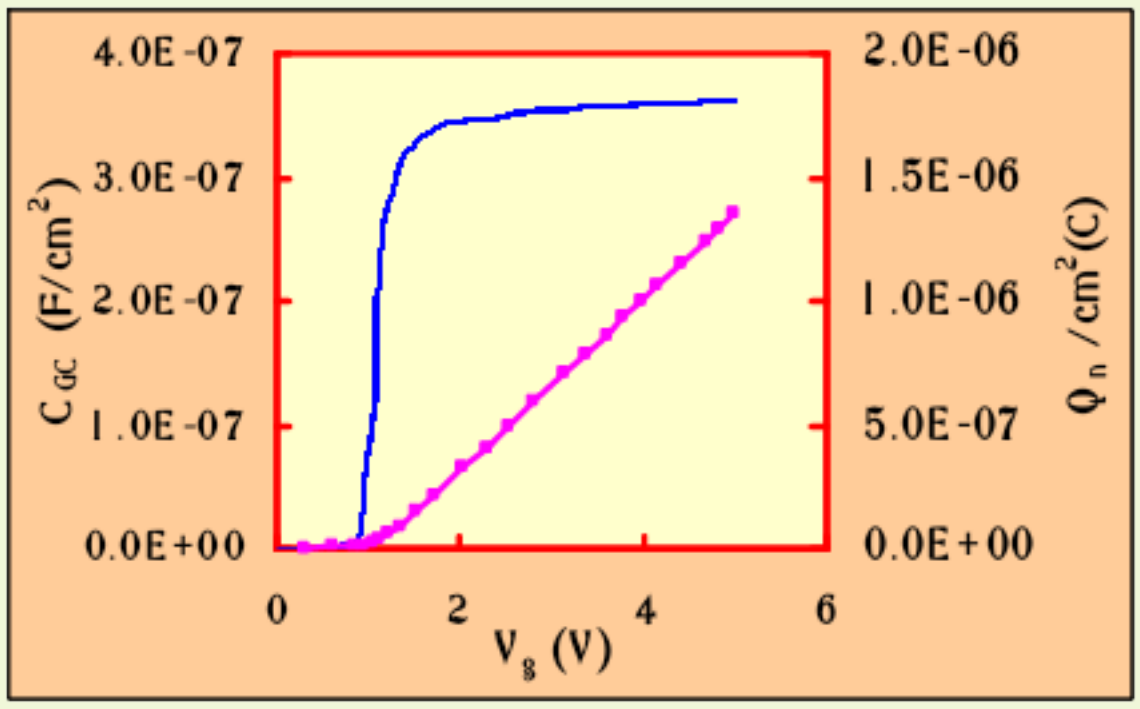
Device parameter: capacitance

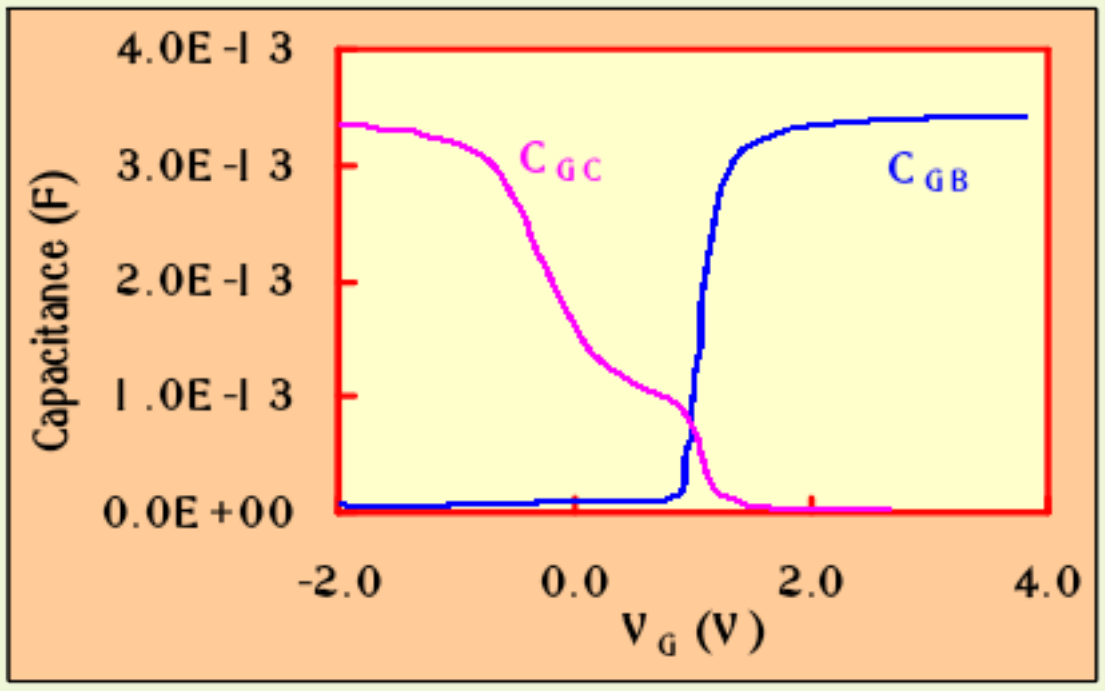
- Channel charge is measured from channel capacitance.
- The channel capacitance is measured by split C-V technique.
- The split C-V method: gate-to-body (C_{GB}) and gate-to-channel (C_{GC}) are measured.



C_{ov}= overlap capacitance

C_{ch}= channel capacitance





How to improve its performance?

- Performance improves by increasing the device width, reducing the oxide thickness and scaling down the channel length.

- Device width cannot be increased since it adversely affects the packing density.

- Scaling down of device dimensions has been the preferred route for sustained performance improvement.

$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}\frac{W}{L}.(V_G - V_{th})V_D$$

Linear region

$$I_D = \frac{\varepsilon_{ox}\varepsilon_0\mu}{t_{ox}}.\frac{W}{L}.\frac{(V_G - V_{th})^2}{2}$$

Saturation region

Down scaling: the primary solution

$$I = \frac{W}{L}.\mu_n.C_{ox}.\left(V_G - V_T - \frac{V_D}{2}\right)V_D$$

$$V_{th} = V_{FB} + 2\Psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\Psi_B)}}{C_{ox}}$$

$$g_m = \frac{\mu\varepsilon_{ins}\varepsilon_0}{t_{ox}}.\frac{W}{L}V_{DS}$$

$$g_d = \frac{\mu\varepsilon_{ins}\varepsilon_0}{t_{ox}}.\frac{W}{L}\left(V_{gs} - V_{th}\right)$$

- Geometrical parameters:
  - width (W),
  - gate length (L_g), and
  - Oxide thickness (t_{ox}).
- Material parameters:
  - Mobility (μ) and
  - dielectric constant (ε).
- *From 1970 onwards, drastic scaling down of geometric dimensions has been the preferred route.*

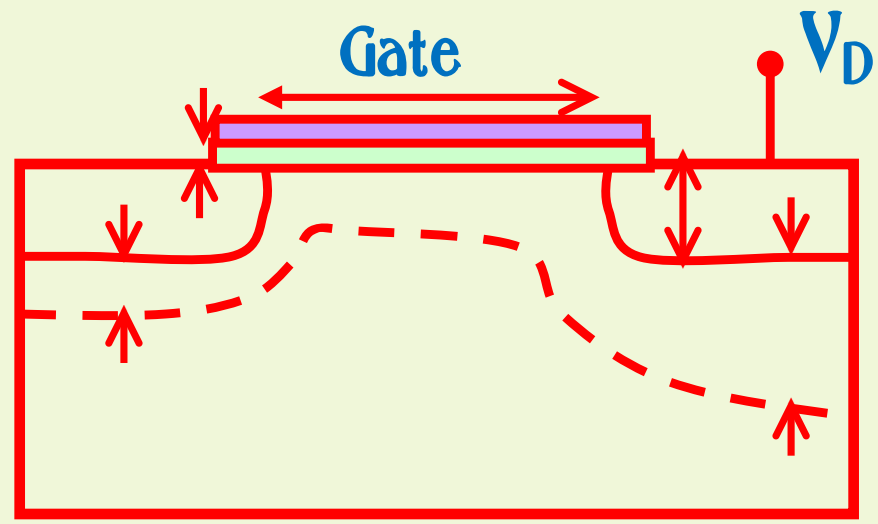
MOSFET performance improvement

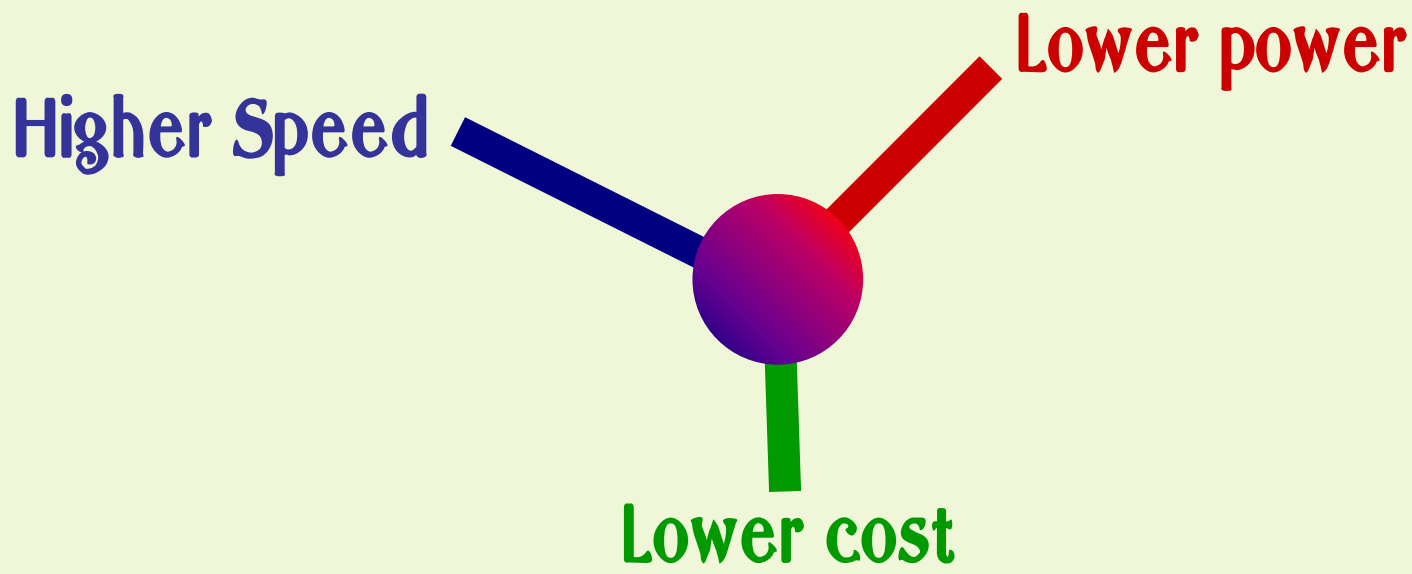
Preferred route:

- The gradual down scaling of device dimensions.

Target:

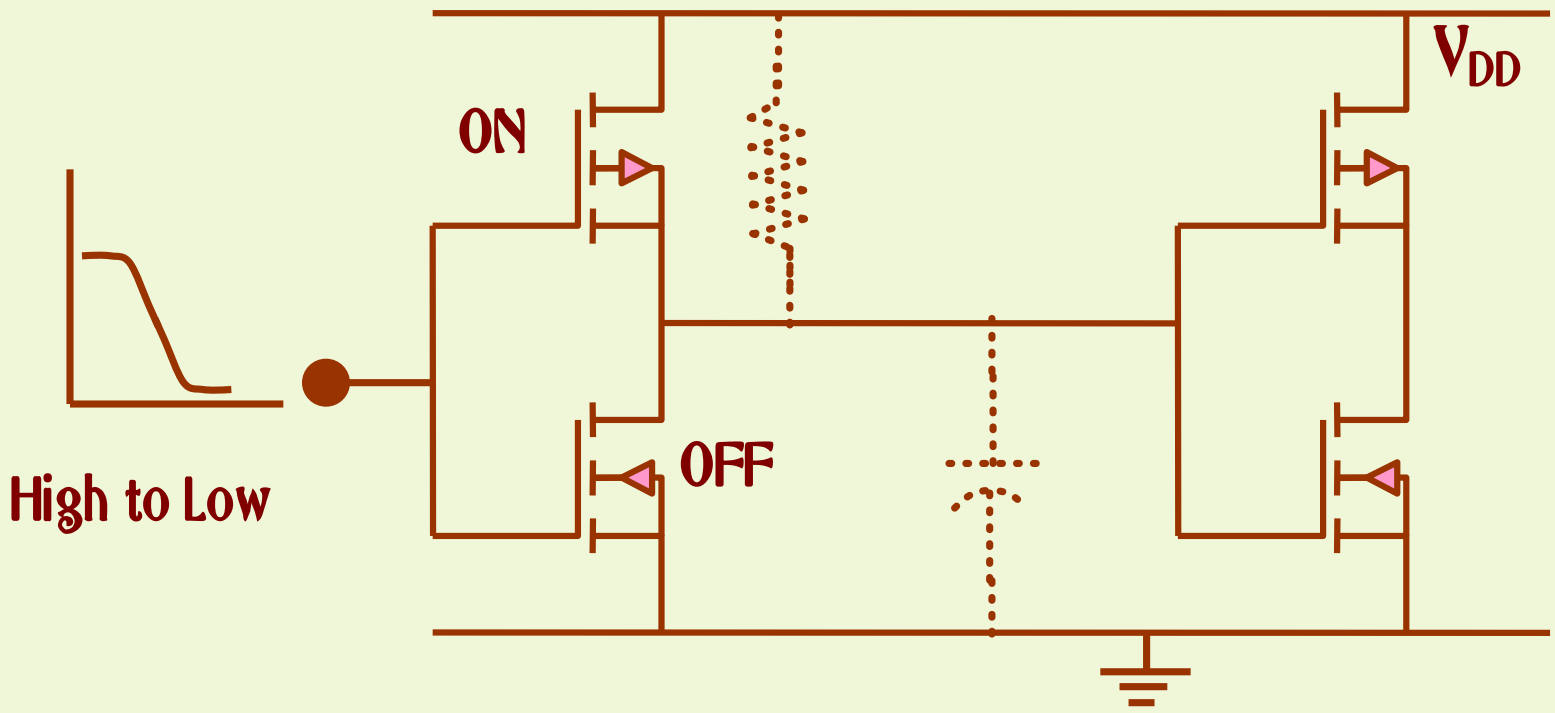
- more functionality,
- higher packing density,
- higher speed,
- less power consumption.





Benefit of scaling

- I_{DS} ↑ as L ↓ (decreased effective "R")
- Gate area ↓ as L ↓ (decreased load "C")
- Therefore, RC ↓ (implies faster switch)



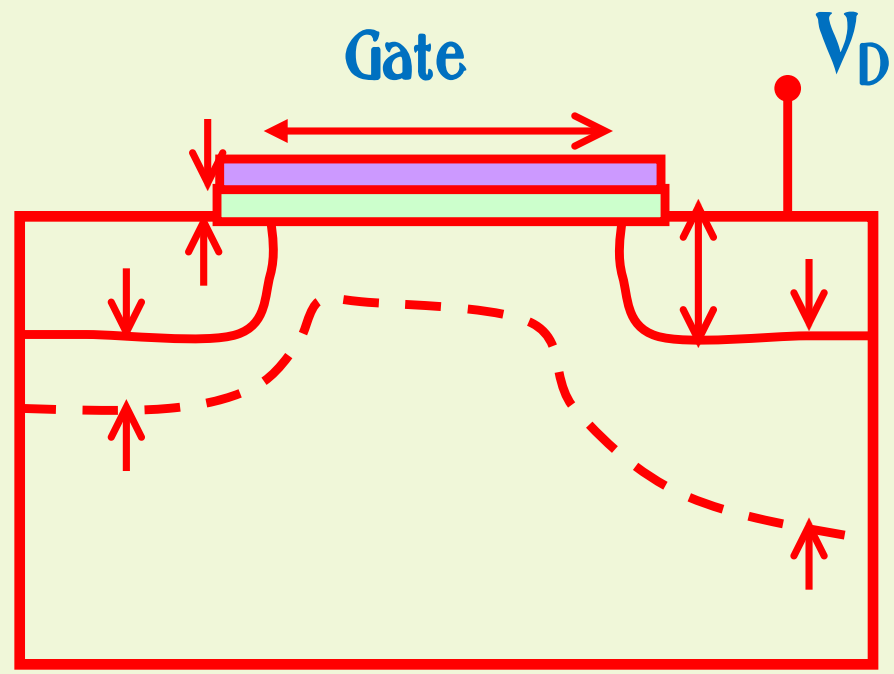
$$I = C\frac{dV}{dt}$$

$$\therefore \Delta t = \frac{C.(\Delta V)}{I}$$

Maximize I to minimize Δt

Device scaling: constant field

Parameter	Scaling Factor: Constant field	Limitation
L	1/K	.....
E	1	.....
d	1/K	Tunneling, defects
r_j	1/K	Resistance
V_T	1/K	off current
V_D	1/K	System, V_T
N_d	k	Junction Breakdown



Scaling and device dimension