

NINAD JANGLE

RISC-V and Circuit Design Enthusiast

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EDUCATION

Veermata Jijabai Technological Institute

B.Tech in Electronics Engineering CGPA: 9.52/10

Mumbai

July 2019 - Present

Monash University

Coursework completed 36 Credits towards B.E Honors

Melbourne

July 2017 - Dec 2018

EXPERIENCE

Open Source Developer

The Linux Foundation Mentorship, RISC-V

Wei Wu

September 2021 - Present

- Cross compiling Spidermonkey for RISC-V
- Made a riscv64 image on qemu to run native builds.
- Built Spidermonkey on x86 and ran Octane, Sunspider and Kraken benchmarks
- Ran regression tests on Spidermonkey post changes and logged results.
- Studying and documenting the baseline compilers for Spidermonkey
- Documenting the mach builds for Firefox

Open Source Developer

Google Summer of Code 2021, FOSSi Foundation

Dr Gayatri Mehta, Mr. Steve Hoover

June 2021 - September 2021

- Designing and Developed a TL-Verilog solution for developers and new entrants to the sphere.
- Powered by Blockly from Google, it will deliver a simple, concise, and intuitive gateway to Circuit Design.
- Developed a TL-Verilog Generator from scratch in JavaScript and developed a dashboard for visualising it with Blockly.
- Tested and Presented the solution at a seminar showcasing its power of designing complex circuits of validity tutorials and memory based calculators using simple drag and drop feature of blocks.
- Researched and Calibrated non-documented instructions from the JS based Blockly library and realised the intended designs and blocks.

Research Intern, Industrial Automation

7th Delta Advanced Automation Contest, Delta Electronics

Dr. Faruk Kazi

May 2021 - July 2021

- Team Leader for one the two Indian Division Representative teams. Received the **Second Prize** in the Finals i.e. Ranked in **Top 40**.
- Designed a solution for a problem faced by the packaging Industry when dealing with varied sized items such is the case with subscription boxes.
- Developed the project through the whole life-cycle from design to modelling to manufacturing and programming of the system.
- Calibrated mechanical and software offsets and achieved an efficient working model.
- Networked and implemented a system using a PLC, Servo Drivers, Machine Vision System, IIOT devices.

PROJECTS

RISC-V CPU Core

TL-Verilog, riscv-gnu-toolchain, MakerchipIDE

github.com/riscv-cpu-core

May 2021 - June 2021

- Tested simple .c programs on the riscv-gnu-toolchain
- Developed a simple calculator with memory to learn the instructions in TL-Verilog
- Reverse Engineered and coded a pipelined RV64I core in TL-Verilog
- There are 6 types of instructions I have implemented: R,I,S,B,U,J
- Successfully ran the ASM of the same .c programs on the core for testing

8-Bit Computer

github.com/8bitcomputer

logisim , C

May 2020 – July 2020

- o Successfully developed an 8 bit computer system using basic gates and logic knowledge to recreate chips using ad-hoc models.
- o Implemented Look ahead adders and efficient instruction routing to deal with timing hazards that prop up due to signal delays
- o Integrated the said chips in a Harvard architecture to make an operational computer system with an assembly to code in.
- o Tested and Verified functioning of sequences such as Fibonacci and natural number sequences.

Vitarana Drone

github.com/EYRC-VD1632

ROS, Gazebo, Python, cv2, cascade classifiers

Sept 2020 – March 2021

- o Implementing a drone solution that can pick and drop off loads autonomously using way point navigation for disaster management.
- o Embedded software to read QR codes and used cascade classifiers to orient the drones with the parcels and the platforms.
- o Devised and developed a Scheduling Algorithm to maximise profit of the drone on a round trip.

SKILLS

- o **Languages:** JavaScript, TL-Verilog, Python, Verilog, C++, ASM Languages(RISC-V,8085,8086)
- o **Frameworks:** Icarus Verilog, GTKWave, Logisim, Linux, MakerchipIDE, Blockly, risc-v gnu toolchain
- o **Microcontrollers:** ESP-32, ESP-8266, Atmega328p
- o **Domains:** Circuit Design, Assemblers, Automation

EXTRA CURRICULAR

- o **Courses:** Successfully Built a **16 Bit HACK Microprocessor** by following the Nand2Tetris Course on Coursera. Along with [various other](#) up-skilling courses.
- o **Conducted Trainings:** Conducted Trainings for Juniors and peers on projects based on ROS and TL-Verilog.
- o Ranked **third** in an intra-club SLAM Competition in which we built a DDR that performs grid solving, line following using cv2, QR decoder and more.

POSITIONS OF RESPONSIBILITY

- o **Electronics Head, SRA (June 2021-Present)** : Educated juniors on Electronics topics through seminars and workshops. Designed and implemented the annual mentorship program in which I will be a mentor on a RISC-V based project.
- o **Branch Representative, VJTI (August 2019-Present)**: Communication and decision making channel to bridge information between the college administration and the students.

ACHIEVEMENTS

- o Selected as 1 of 2 teams **Representing India Division** and received **Second Prize** in the International 7 Th Delta Advanced Automation Contest organised Delta Electronics
- o Ranked **Top 20, Pan-India** in the e-Drone competition, **e-yantra**.
- o My proposal Block Based Circuit Design got accepted into **Google Summer Of Code, 2021**
- o **Rank 1** in academics in B.Tech Electronics
- o **Governor's Gold** in academics in 10th Boards.