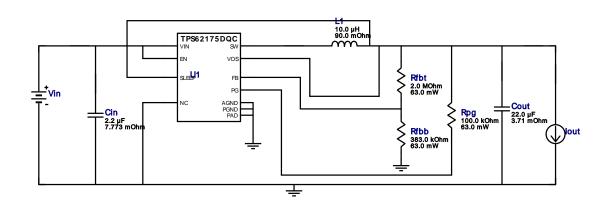


WEBENCH® Design Report

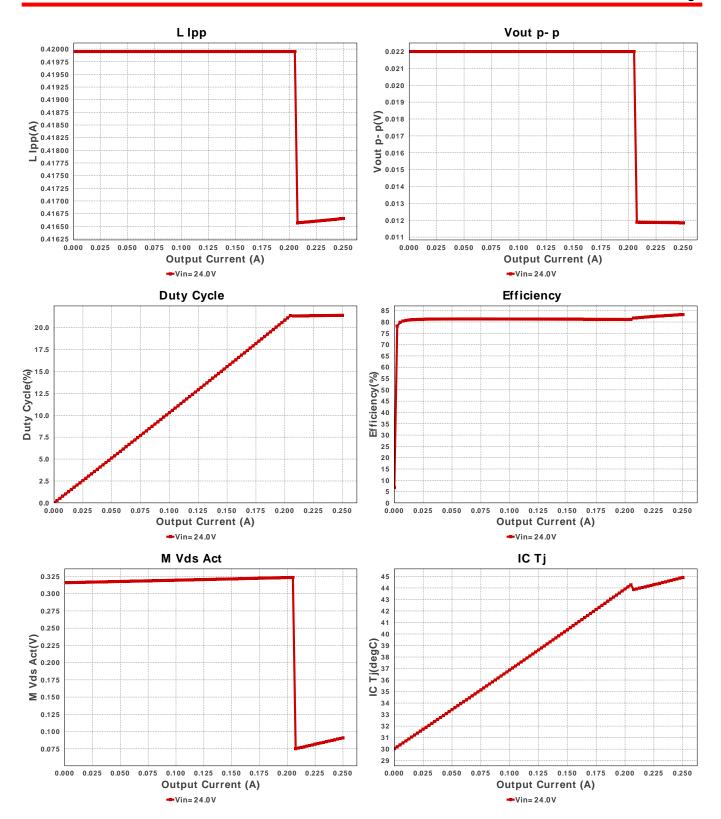
VinMin = 24.0V VinMax = 24.0V Vout = 5.0V lout = 0.25A Device = TPS62175DQCR Topology = Buck Created = 2021-02-22 16:03:55.702 BOM Cost = \$0.94 BOM Count = 7 Total Pd = 0.25W

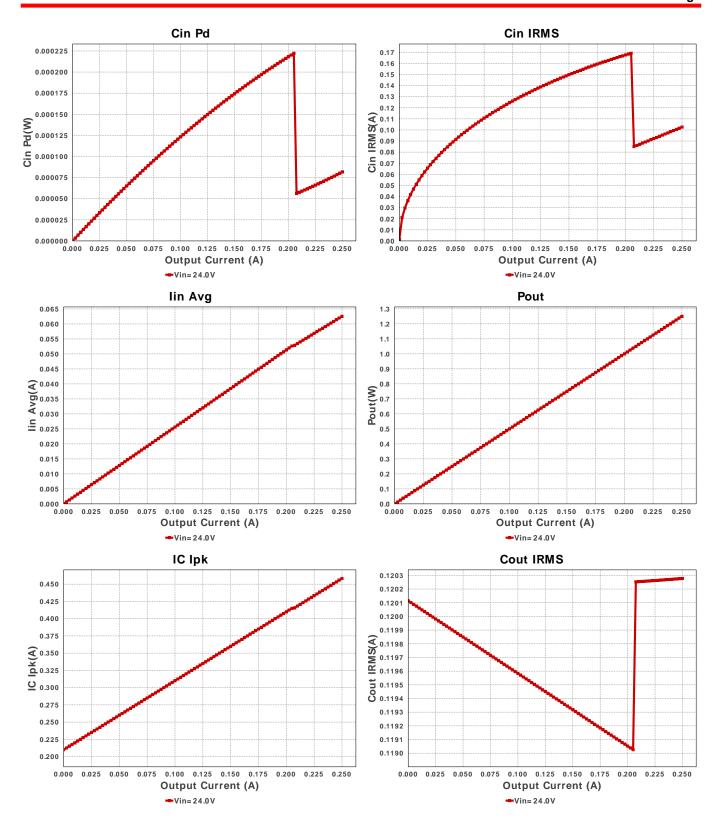
Design: 2 TPS62175DQCR TPS62175DQCR 24V-24V to 5.00V @ 0.25A

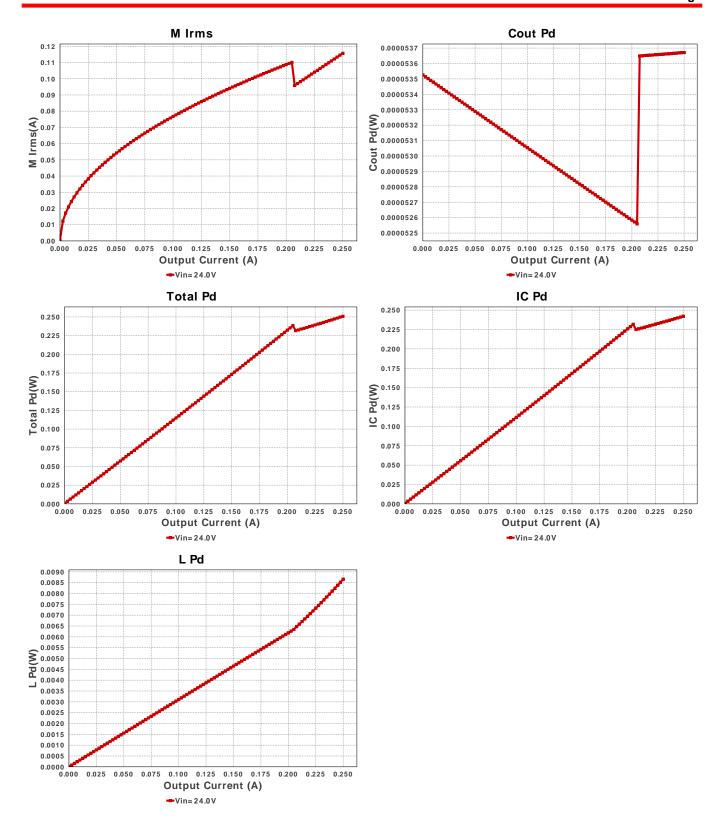


Electrical BOM

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	MuRata	GRM21BR71E225KA73L Series= X7R	Cap= 2.2 uF ESR= 7.773 mOhm VDC= 25.0 V IRMS= 1.35654 A	1	\$0.13	0805 7 mm ²
Cout	TDK	C1608X5R1A226M080AC Series= X5R	Cap= 22.0 uF ESR= 3.71 mOhm VDC= 10.0 V IRMS= 2.69936 A	1	\$0.12	0603 5 mm ²
L1	NIC Components	NPI54C100MTRF	L= 10.0 μH 90.0 mOhm	1	\$0.18	IND_NPI54C 61 mm ²
Rfbb	Vishay-Dale	CRCW0402383KFKED Series= CRCWe3	Res= 383.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rfbt	Vishay-Dale	CRCW04022M00FKED Series= CRCWe3	Res= 2.0 MOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rpg	Vishay-Dale	CRCW0402100KFKED Series= CRCWe3	Res= 100.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
U1	Texas Instruments	TPS62175DQCR	Switcher	1	\$0.48	DQC0010A 12 mm ²







Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	102.549 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	81.744 μW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	120.278 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	53.671 μW	Capacitor	Output capacitor power dissipation
5.	IC lpk	458.327 mA	IC	Peak switch current in IC
6.	IC Pd	242.05 mW	IC	IC power dissipation
7.	IC Tj	44.91 degC	IC	IC junction temperature
8.	IC Tolerance	14.4 mV	IC	IC Feedback Tolerance
9.	ICThetaJA	61.6 degC/W	IC	IC junction-to-ambient thermal resistance
10.	lin Avg	62.535 mA	IC	Average input current
11.	L Ipp	416.65 mA	Inductor	Peak-to-peak inductor ripple current

#	Name	Value	Category	Description
12.	L Pd	8.659 mW	Inductor	Inductor power dissipation
13.	M1 Irms	115.678 mA	Mosfet	Q lavg
14.	M Vds Act	90.899 mV	Mosfet	Voltage drop across the MosFET
15.	Cin Pd	81.744 μW	Power	Input capacitor power dissipation
16.	Cout Pd	53.671 μW	Power	Output capacitor power dissipation
17.	IC Pd	242.05 mW	Power	IC power dissipation
18.	L Pd	8.659 mW	Power	Inductor power dissipation
19.	Total Pd	250.835 mW	Power	Total Power Dissipation
20.	BOM Count	7	System	Total Design BOM count
			Information	
21.	Duty Cycle	21.41 %	System	Duty cycle
			Information	
22.	Efficiency	83.287 %	System	Steady state efficiency
			Information	
23.	FootPrint	93.0 mm ²	System	Total Foot Print Area of BOM components
			Information	
24.	Frequency	976.335 kHz	System	Switching frequency
			Information	
25.	lout	250.0 mA	System	lout operating point
			Information	
26.	Mode	CCM	System	Conduction Mode
	_		Information	
27.	Pout	1.25 W	System	Total output power
		.	Information	
28.	Total BOM	\$0.94	System	Total BOM Cost
		0.4.0.14	Information	
29.	Vin	24.0 V	System	Vin operating point
00		E 0.1/	Information	0 10 10 11 11
30.	Vout	5.0 V	System	Operational Output Voltage
0.4	Manut Antonal	4.070.1/	Information	Most Astrological solution beautifus and as a selected college of Steen as Steen
31.	Vout Actual	4.978 V	System	Vout Actual calculated based on selected voltage divider resistors
00	Marit Talamana	0.500.0/	Information	Vest Television has a design to Television (full lead) and college distance
32.	Vout Tolerance	3.526 %	System	Vout Tolerance based on IC Tolerance (full load) and voltage divider
20	\/at m m	44.040\/	Information	resistors if applicable
33.	Vout p-p	11.848 mV	System	Peak-to-peak output ripple voltage
			Information	

Design Inputs

Name	Value	Description	
lout	250.0 m	Maximum Output Current	
VinMax	24.0	Maximum input voltage	
VinMin	24.0	Minimum input voltage	
Vout	5.0	Output Voltage	
base_pn	TPS62175	Base Product Number	
source	DC	Input Source Type	
Та	30.0	Ambient temperature	

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 24.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum lout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

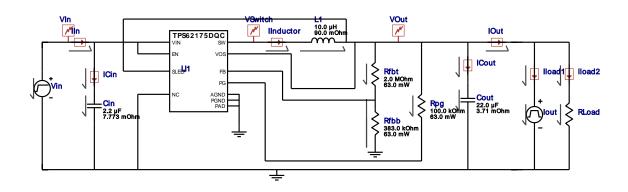


WEBENCH® Electrical Simulation Report

Design Id = 2

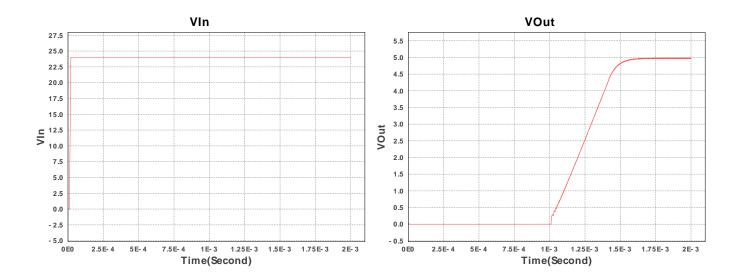
 $sim_id = 5$

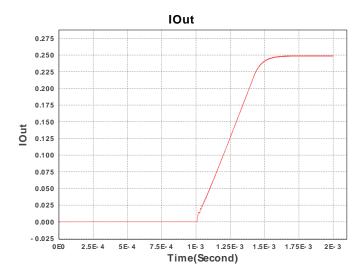
Simulation Type = 2-Step Startup



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Cout	IC	no description	0
2.	lout	signal_type I1 I2 Td Tr	Signal Type Initial Load Current Minimum Load Current Initial Time Delay Rise Time	PULSE 0 A 0.0 A 0.0017 s 1u s
3.	RLoad	R	Load Resistance	20.0 ohm





Design Assistance

1. Master key: 9810EF8B6453D2AE[v1]

2. TPS62175 Product Folder: http://www.ti.com/product/TPS62175: contains the data sheet and other resources.

Important Notice and Disclaimer

TI provides technical and reliability data (including datasheets), design resources (including reference designs), application or other design advice, web tools, safety information, and other resources AS IS and with all faults, and disclaims all warranties. These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Providing these resources does not expand or otherwise alter TI's applicable Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with TI products.