A Working Phase-Locked Loop

Introduction

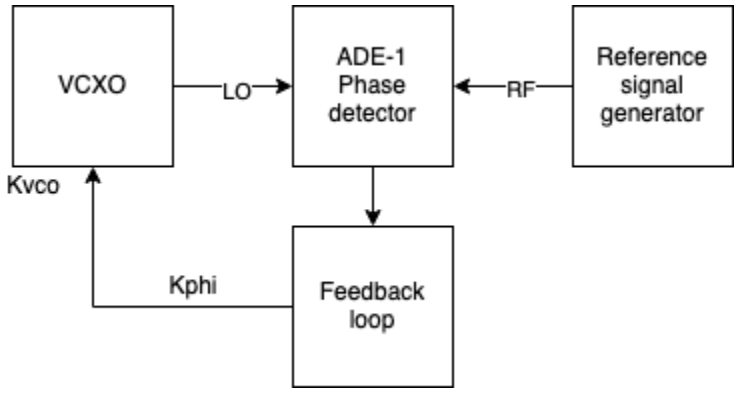


Figure 1: A block diagram of a PLL

Despite spending many hours in the lab, I did not have an incredibly hard time with this project, not least of all due to good luck, but also because of my prior experience with oscillating feedback systems, music, and finding methods to minimize frustration when working with analog circuitry. I spent a lot of time going back and forth between the Tektronix lab and the Capstone lab, testing the circuit and then taking it to resolder something, just to make sure that my connections were solid and that I was using paired wires as much as possible. On more than one occasion I had to sleep on an issue and come back to it later just to find a simple fix. Despite my lack of major problems to surpass, I found it just as rewarding and interesting as Dr. Campbell described at the beginning of the term.

Below is a schematic of my final working PLL, simplifying the VCXO and ADE-1 which were detailed in previous reports.

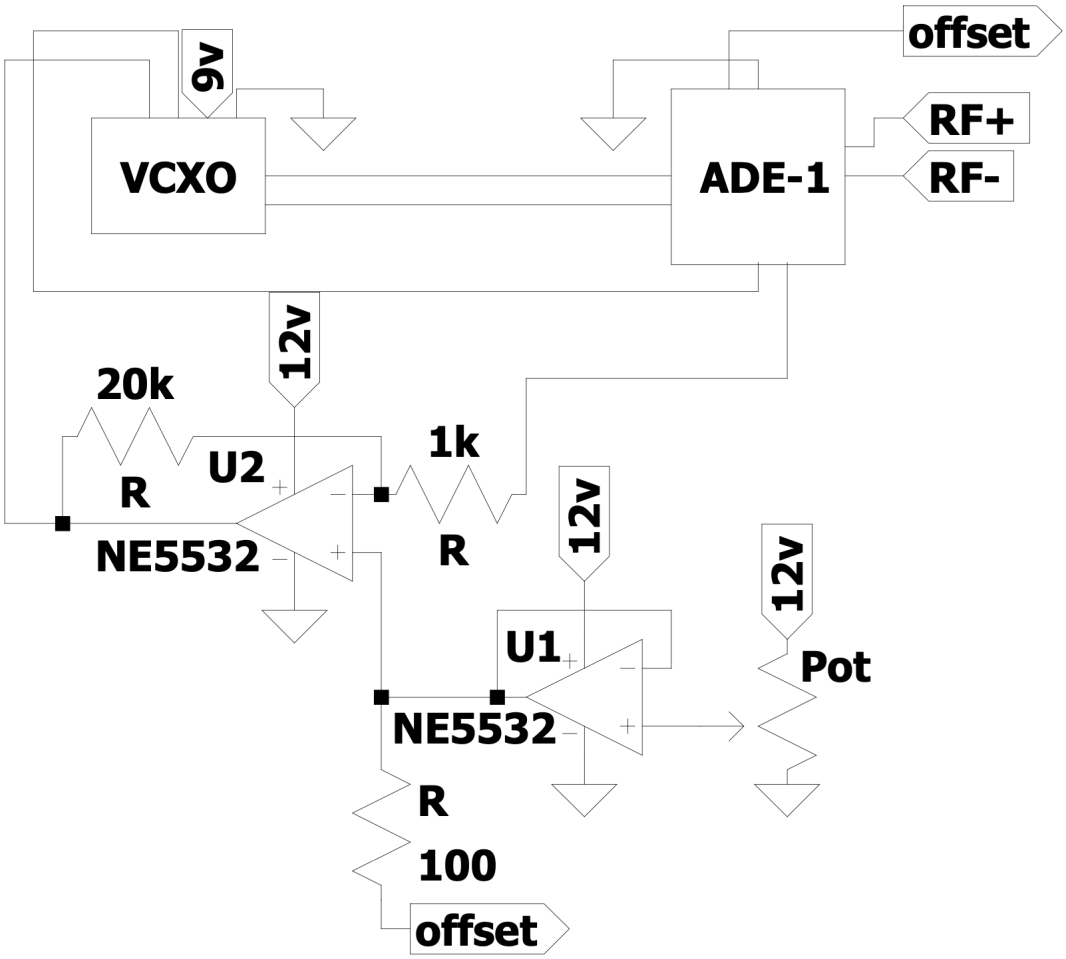


Figure 2: Schematic of final PLL with loop gain = 20

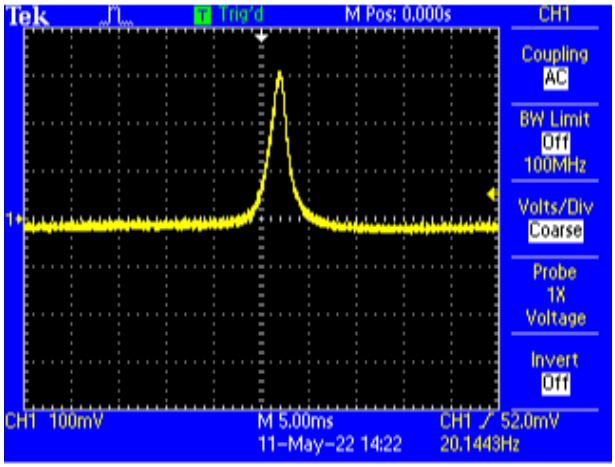
For all RF inputs from the signal generator to the ADE-1, a peak-to-peak amplitude of 200mV was used. This was based on that being a pretty good value to keep the output in a sinusoidal shape during Lab 2.

No gain loop

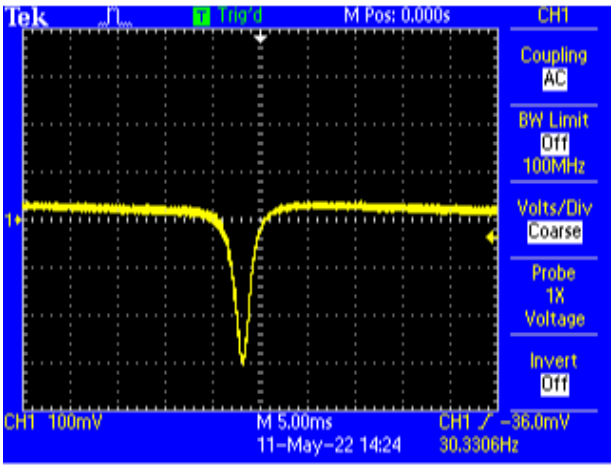
In my Lab 2 report, I found a lock range of 80 Hz. When I tested this PLL with no gain, I found a lock range about the same, maybe less. That was a somewhat inaccurate measure, though, since I had found that value by adjusting the VCXO offset voltage on the ADE-1, instead of setting that voltage and adjusting the RF frequency. This section details the results of setting a VCXO offset (labeled the bias voltage) and adjusting the RF frequency on the signal generator to find the lock range.

In my excitement of getting this thing to lock, I did not get any pictures of the actual circuit before adding loop gain. Pictures of the circuit with loop gain are in the following section.

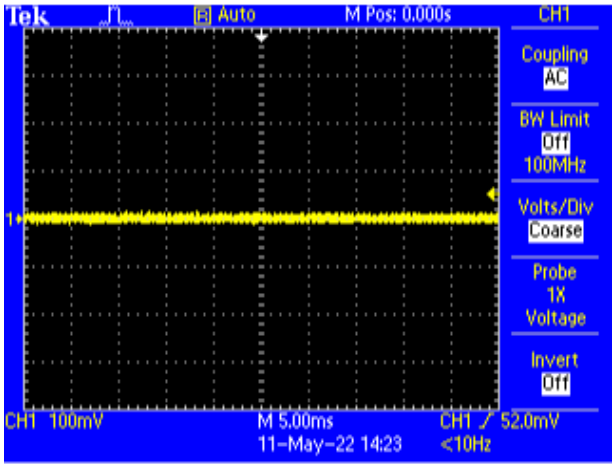
Oscilloscope images of lock range measured at the output of the ADE-1:



Low frequency edge of lock



High frequency edge of lock



Lock

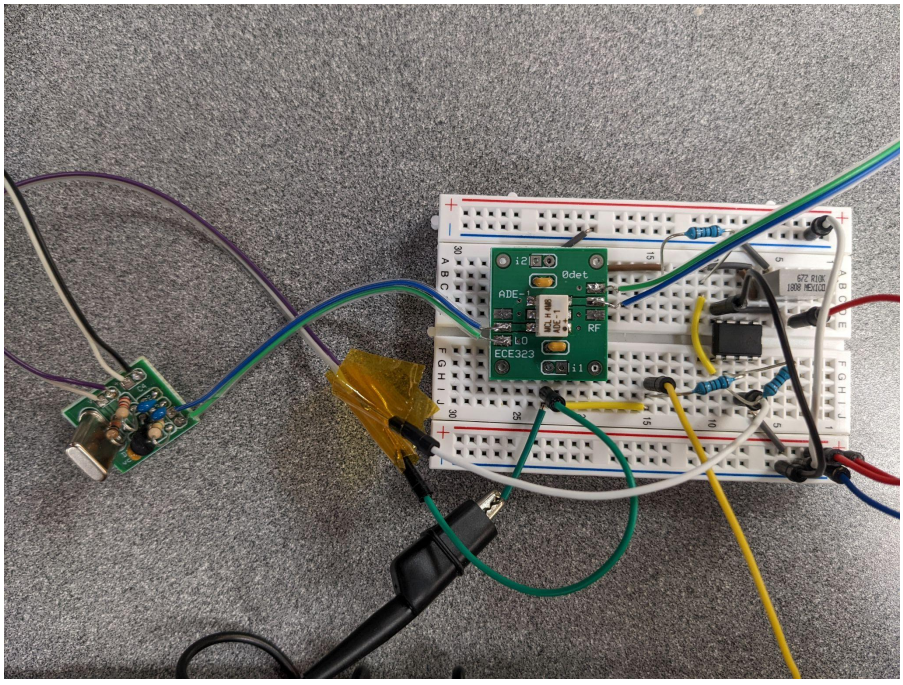
Table 1 below is a collection of data gathered when testing this circuit with no loop gain. At first, I had used VCXO power at 6V, and realized I'd been advised to use 9V, so I switched halfway through. Throughout this process, a VCXO bias voltage of about 5V seemed to work well for each setup. This was the same bias voltage used to test the VCXO for finding $k_\phi = 120mV/rad$ in Lab 2. With a $k_{VCO} = 650\ Hz/V$ over a bias range of 0-18V, that gives a lock range of about 80 Hz. What is found below is far above that range, and agrees with the no gain lock ranges many others were getting for our PLL design in the class. For the calculated k_ϕ in all tables, $k_{VCO} = 650\ Hz/V$ was assumed, since it was derived from a range of bias voltages between 0 and 18 V.

Table 1: Lock ranges for 0 loop gain

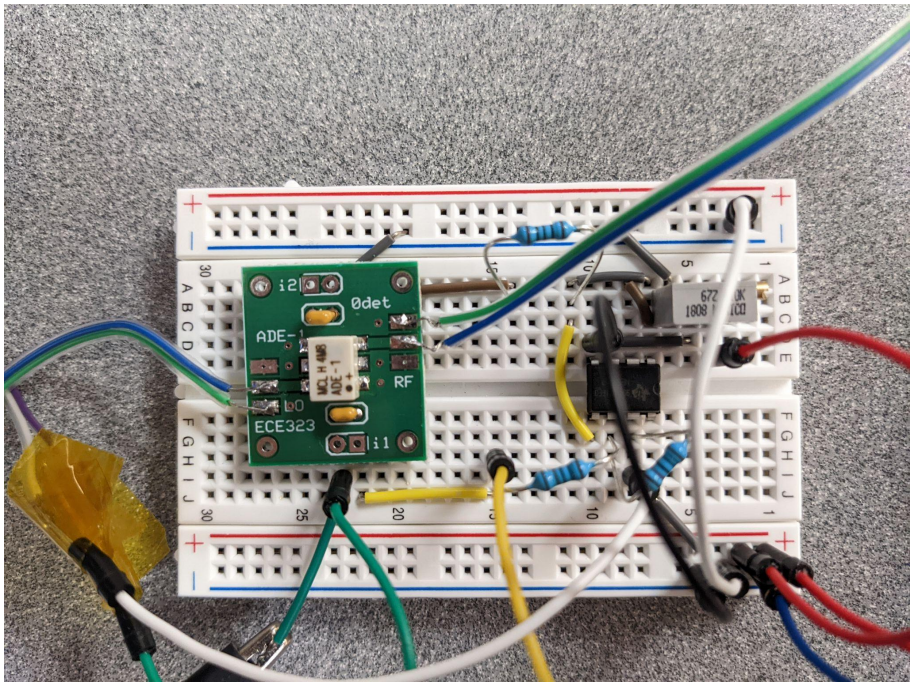
VCXO power at 6V				From Lab2	Calculated
Bias voltage [V]	Low edge [MHz]	Hi edge [MHz]	BW [Hz]	k_vco [Hz/V]	k_phi [V/rad]
1.24	0.039600	0.039920	320.00	650	0.492
1.3	0.039650	0.039970	320.00	650	0.492
1.5	0.039850	0.040170	320.00	650	0.492
2.5	0.040760	0.041020	260.00	650	0.400
5	0.042670	0.042920	250.00	650	0.385
VCXO power at 9V					
2	0.040300	0.040490	190.00	650	0.292
3	0.041050	0.041310	260.00	650	0.400
5	0.042570	0.042800	230.00	650	0.354
8	0.044710	0.044940	230.00	650	0.354

Gain = 10 loop

Adding gain to the feedback loop increases the amplitude of the waveform on the ADE-1 output, which increases k_{VCO}, which increases the lock range of the PLL.



Picture of the full circuit



Picture of just the ADE-1 board with the loop gain circuit

With some help from Dr. Campbell, I noticed that with the op-amp in the feedback loop, as the bias voltage nears the supply rails of the op-amp, the lock-range decreases and the ADE-1 output looks more like a sine wave. The solution was to increase the supply rails of the op-amp. In my circuit, the op-amp supply and the input to the potentiometer have the same voltage source.

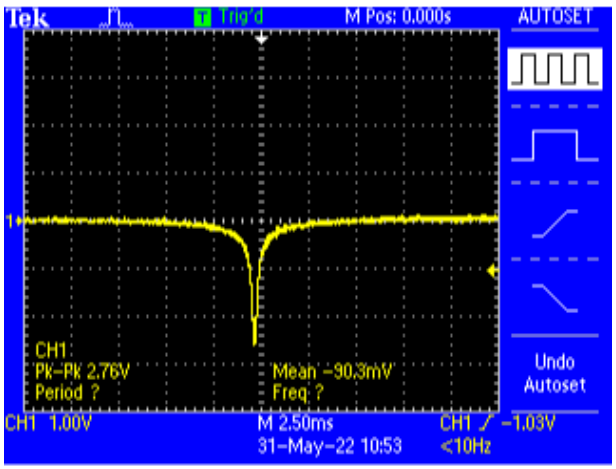
Table 2: Lock ranges for loop gain = 10

	with 10x gain	Rf = 10k	Rin = 1k		
VCXO power at 9V, pot input at 6V				From Lab 2	Calculated
Bias voltage [V]	Low edge [MHz]	Hi edge [MHz]	BW [Hz]	k_vco [Hz/V]	k_phi [V/rad]
2.5	0.040180	0.041890	1710.00	650	2.63
4	0.040980	0.042960	1980.00	650	3.05
4.58	0.042570	0.042970	400.00	650	0.62
VCXO at 9V, pot input at 12V					
2.5	0.040180	0.041870	1690.00	650	2.60
5	0.041780	0.043700	1920.00	650	2.95
6	0.042540	0.044420	1880.00	650	2.89

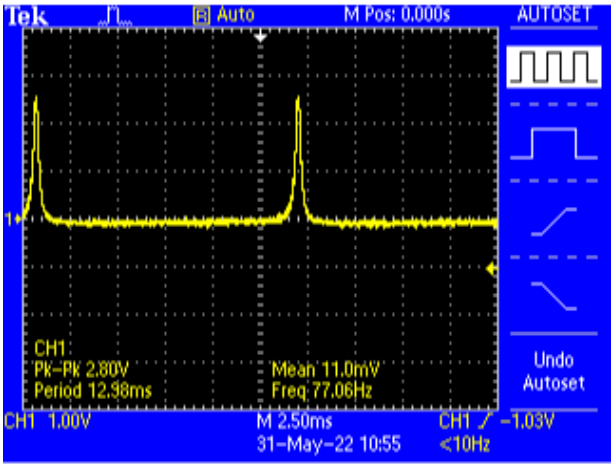
Gain = 20 loop

Table 3: Lock ranges for loop gain = 20

	gain of 20	Rf = 20k	Rin = 1k		
VCXO at 9V, pot input at 12V				From Lab2	Calculated
Bias voltage [V]	Low edge [MHz]	Hi edge [MHz]	BW [Hz]	k_vco [Hz/V]	k_phi [V/rad]
2.5	0.040170	0.042850	2680.00	650	4.12
5	0.040710	0.044640	3930.00	650	6.05
6	0.041530	0.045340	3810.00	650	5.86



LF lock edge at 24.040130 MHz



HF lock edge at 24.041820 MHz

What is interesting in the above outputs is that the spikes are reversed from what was seen in the 0 gain PLL before. Below the lock range we should see the signal spike upwards, yet it spikes downwards here. This could be because the feedback loop has gain through an inverting op-amp.

Conclusion

To compare these different gain settings, I chose a specific bias voltage used in each test and set the results side by side with the calculated values from Lab 2.

Table 3: Comparison with bias = 5V, V+ = 9V, and RF signal at 200mV

Gain	BW [Hz]	Calc. k_phi [V/rad]
0	78	0.120
0	230	0.354
10	1920	2.950
20	3930	6.050

Based on the original derived numbers, these values make sense, in that they're in the ballpark of what's to be expected. The difference in bandwidth between a gain of 10 and 20 is almost exactly 2, which is much closer than I thought it would be. I think I could increase the bandwidth with more loop gain, and it would interesting to see the limit of diminishing returns. I have a toolbox full of little RF project materials I might get into over the summer, so this is a nice starting point.