VCXO testing and finding k_{VCO}

I figured out many less-than-nominal methods of testing this circuit before getting clear values. Some of those included: improperly soldered pin-headers; using poorly fit jumper wires; and not understanding how to get accurate readings from the oscilloscope. It's nice to be back in the lab, but I've forgotten a few things while working remotely.

I ended up wiring the two boards in the EPL. I got some ribbon wire to separate into pairs for each port on the VCXO and ADE-1 then tack-soldered them to the boards. My measurements were much cleaner using paired wires and soldered connections, as well as using the Tektronix lab oscilloscopes.

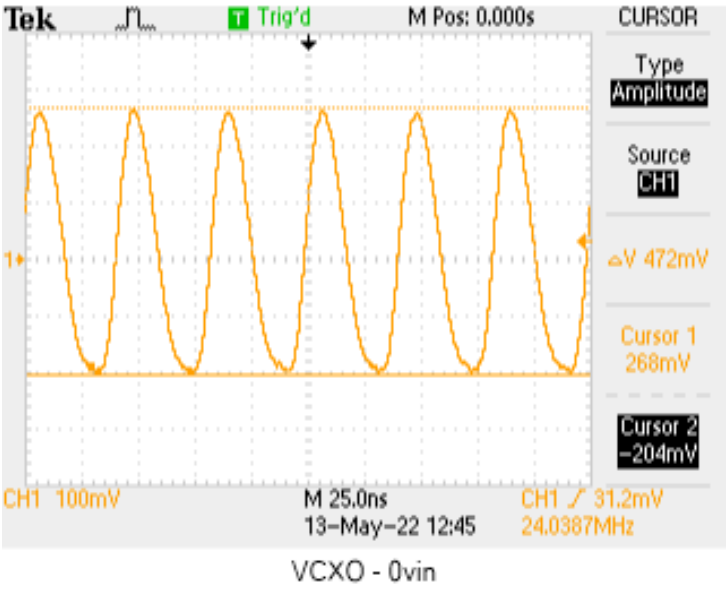

Figure 1. Output of the VCXO without any ΔV input

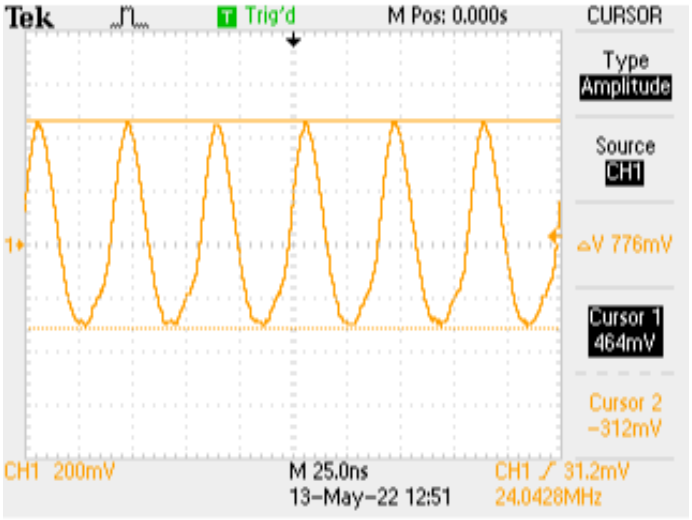

Figure 2. VCXO Output with $\Delta V = 5V$

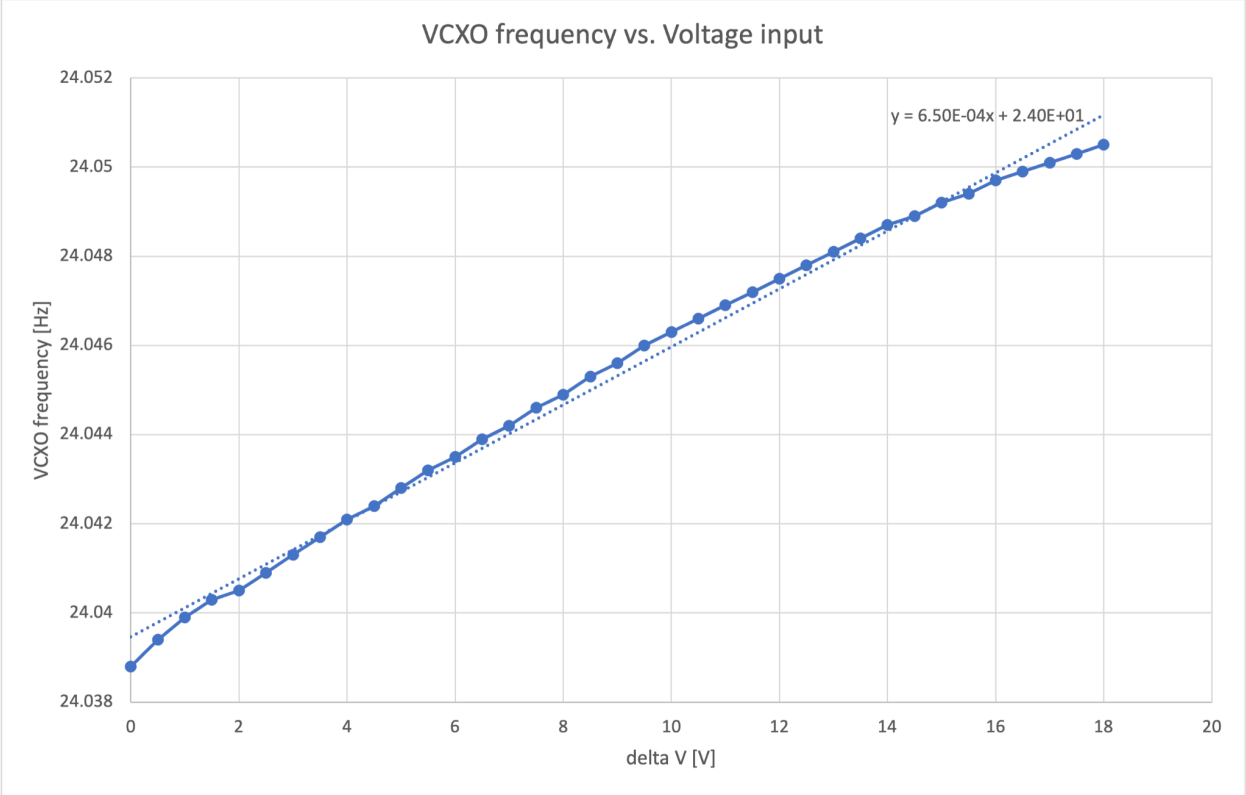

Figure 3. Output frequency versus input voltage to find k_{VCO}

The trendline of this plot yields $k_{VCO} = 650\ Hz/V$.

ADE-1 testing and finding k_ϕ

To test the ADE-1 I soldered the paired wires from the output of the VCXO to the LO port of the ADE-1 and placed the board with the capacitor legs in a breadboard so that I could connect them to jumper wires. I set the VCXO variable voltage to 5V and used the corresponding frequency from the previous section to set the function generator at 24.042800 Hz. I chose a peak voltage of 200mV for the function generator such that the output of the ADE-1 was a nice sine wave. I noticed that by setting the function generator amplitude much higher would result in a clear distortion of the waveform.

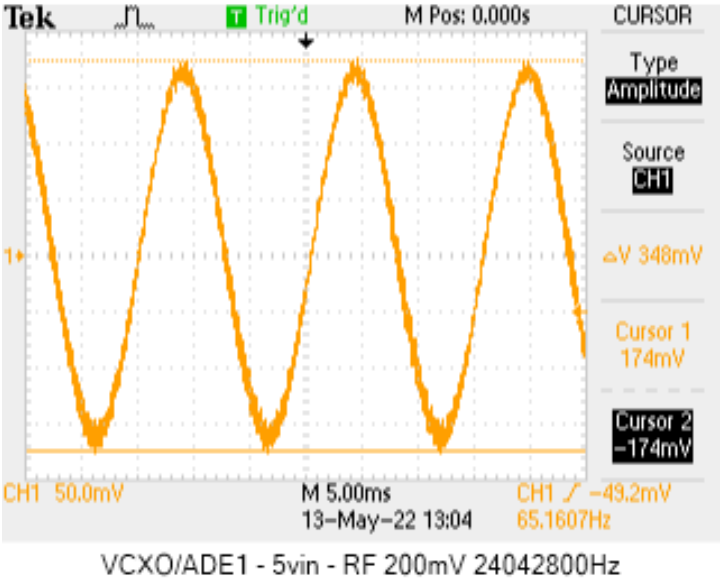

Figure 4. ADE-1 Output with the RF signal of 200mV, 24.042800 MHz

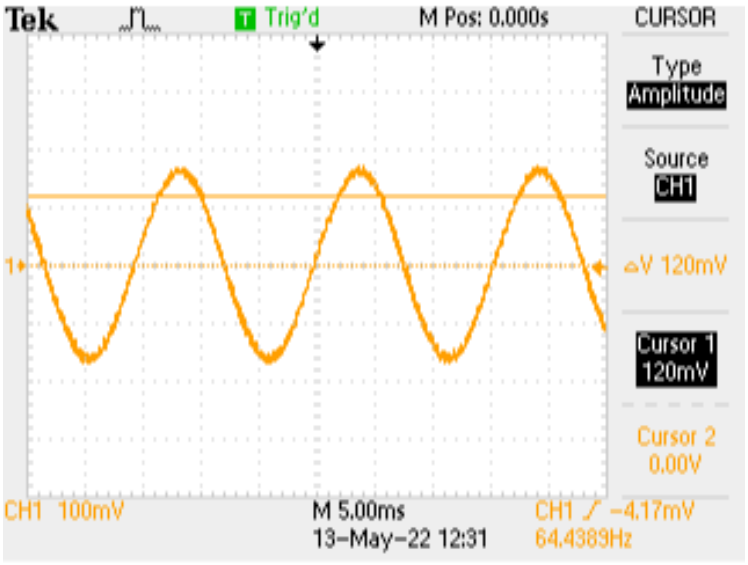

Figure 5. An estimation of k_{ϕ}

This measurement of k_{ϕ} yields about 120mV. With both k_{VCO} and k_{ϕ}, the capture range and lock range are about 80 Hz.

Understanding how a VCXO works

Part 1:

I simulated the transistor-resistor section of the VCXO using an operating point simulation to find the DC values at each node.

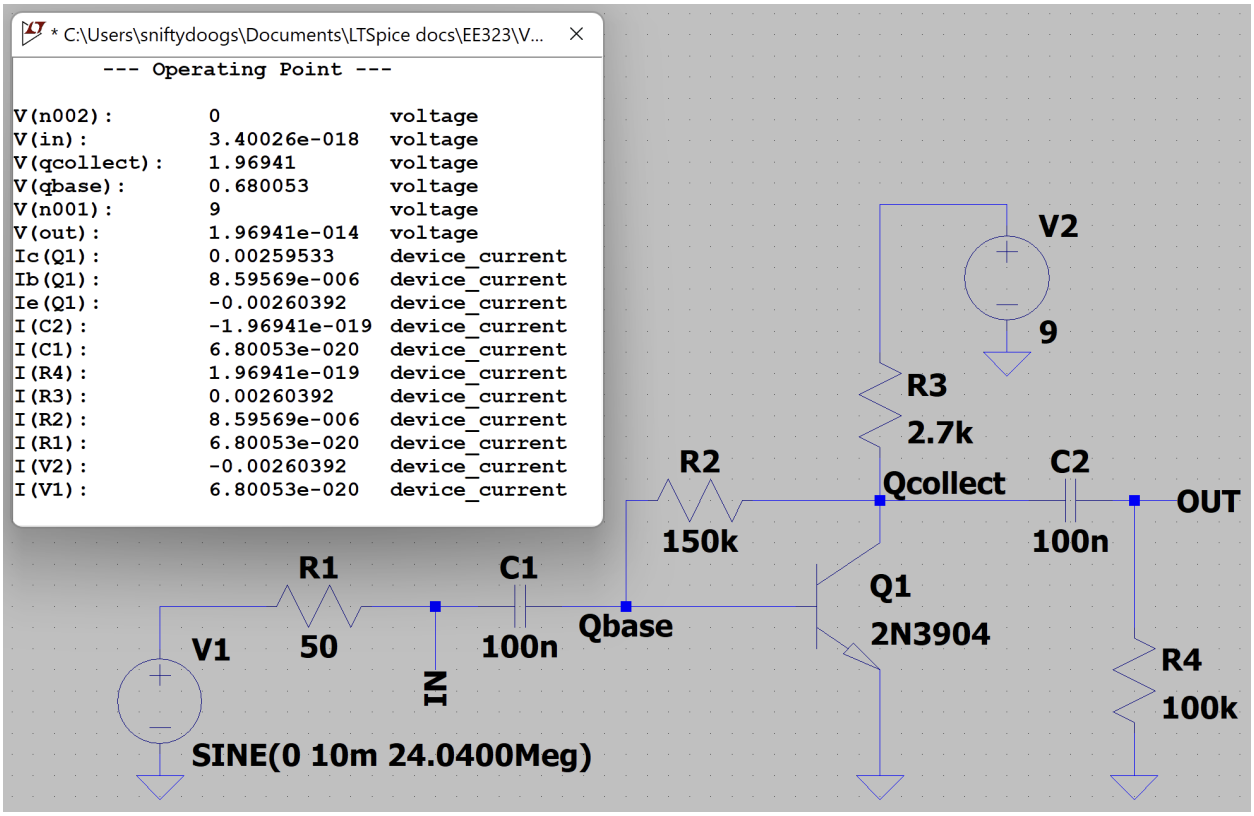

Figure 6: DC operating point simulation results

The current I_C is about the expected 2 mA for this design. The emitter current matches this value and the base current is about 10 μA. The rest of the DC currents are negligible. The collector voltage is the expected 2 V. These values are all expected from the general rule for BJT transistors that there is about a 0.7 V drop between the base voltage and emitter voltage, and the feedback resistor is relatively high compared to the collector resistance.

Part 2:

The quartz crystal oscillator acts similarly to an RLC resonant circuit, with the crystal behaving much like a capacitor with a specific resonant frequency and the transistor acting to reinforce and amplify that oscillation. The thickness of the quartz crystal determines the f_0 rated resonant frequency and the capacitance at either side of the crystal affects the frequency at which the 180° phase shift occurs. The crystal oscillator provides feedback to the amplifier to drive the resonant frequency at that phase shift.

The flute analogy reminded me of how a string on a guitar sets up a standing wave resonance to produce a pitch. The tension, thickness, and length of the string have to be balanced in such a way to determine the resonant frequency of that plucked string, just as the inductance, capacitance, and resistance of the crystal are such that when it is “plucked” by the input bias of the circuit, it resonates at a certain frequency.

I simulated the crystal oscillator and used values from the board we made and tested in the lab.

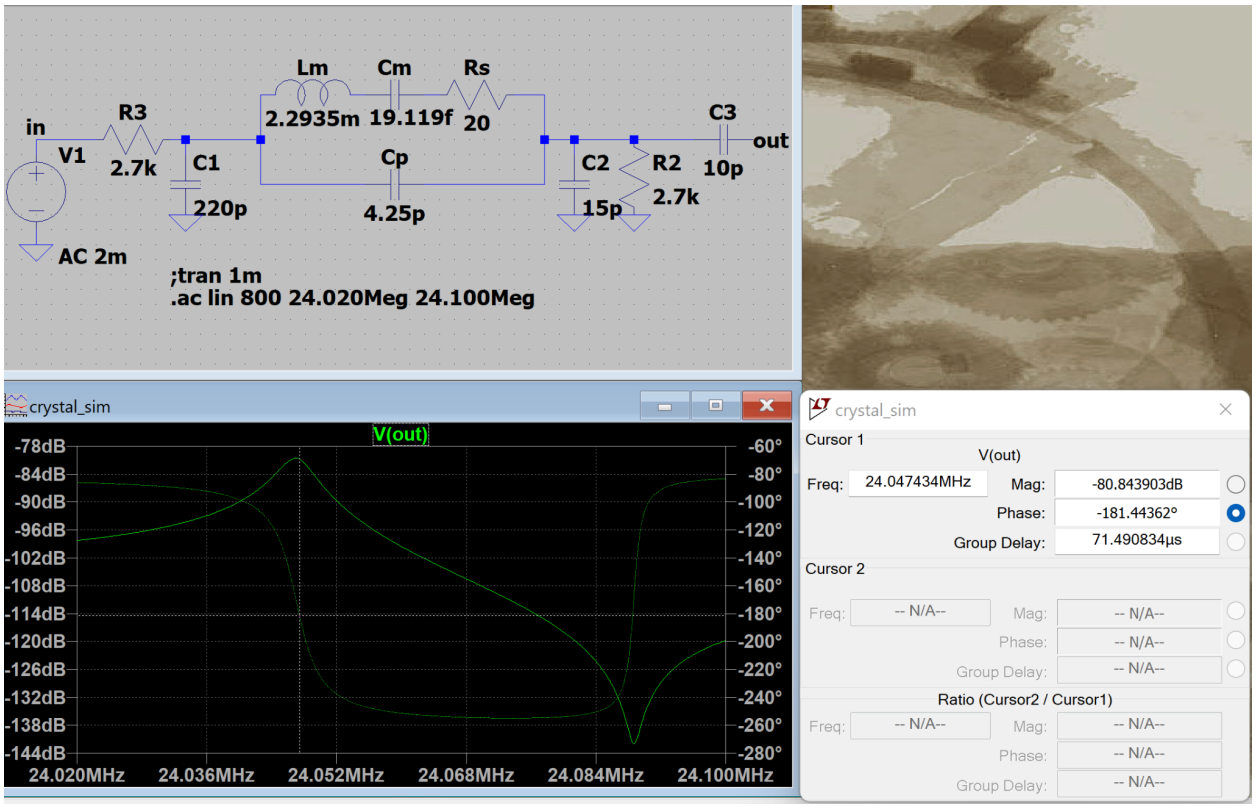

Figure 7: This simulated circuit peaks at about 24.047 MHz when the phase is around 180°

At 180° of phase shift, the output voltage peaks at about 24.047 MHz. This is in the ballpark, since the physical components and the circuit joining them will introduce variation in the final measured output.