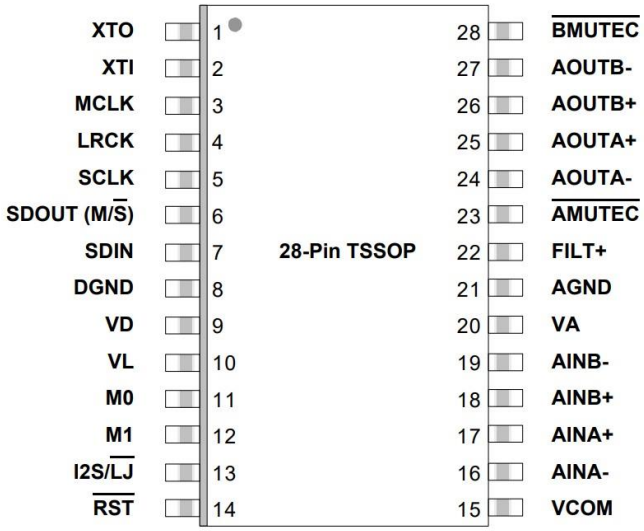
Things to note about using the CS4271

## 2. PIN DESCRIPTIONS - STAND-ALONE MODE




If we're using 44.1 kHz or 48 kHz sample rate, we'll use Single Speed mode.

**Table 1. Speed Modes**

| Mode | Sampling Frequency |
|---|---|
| ***Single Speed*** | 4-50 kHz |
| ***Double Speed*** | 50-100 kHz |
| ***Quad Speed*** | 100-200 kHz |

Since we're using the FPGA's clock, XTI should be connected to ground and XTO should be left unconnected (pg 24). MCLK is an input and must be driven externally with an appropriate speed clock of 512*Fs (e.g., 512*48kHz = 24.576 MHz).

**Table 4. Clock Ratios - Stand Alone Mode Without External Crystal**

| External Crystal Not Used, MCLK=Input | | | |
|---|---|---|---|
| ***Master Mode*** | | | |
| | **MCLK/LRCK** | **SCLK/LRCK** | **LRCK** |
| ***Single Speed*** | 256 | 64 | Fs |
| ***Double Speed*** | 128 | 64 | Fs |
| ***Quad Speed*** | 64 | 32 | Fs |
| ***Slave Mode*** | | | |
| | **MCLK/LRCK** | **SCLK/LRCK** | **LRCK** |
| ***Single Speed*** | 256 | 32, 64, 128 | Fs |
| | 384 | 32, 48, 64, 96, 128 | Fs |
| | 512 | 32, 64, 128 | Fs |
| ***Double Speed*** | 128 | 32, 64 | Fs |
| | 192 | 32, 48, 64 | Fs |
| | 256 | 32, 64 | Fs |
| ***Quad Speed*** | 64 | 32 | Fs |
| | 96 | 48 | Fs |
| | 128 | 32, 64 | Fs |

Clock ratios must be correct for the chip to not be muted.

Assuming we're using 44.1 kHz, pin M0 and M1 should be set to 0 and 0.

**Table 5. CS4272 Stand-Alone Mode Control**

| Mode 1 | Mode 0 | Mode | Sample Rate (Fs) | De-Emphasis |
|---|---|---|---|---|
| 0 | 0 | Single Speed Mode | 4 kHz - 50 kHz | 44.1 kHz |
| 0 | 1 | Single Speed Mode | 4 kHz - 50 kHz | Off |
| 1 | 0 | Double Speed Mode | 50 kHz - 100 kHz | Off |
| 1 | 1 | Quad Speed Mode | 100 kHz - 200 kHz | Off |

Since we're not using I2C, we need to place a 10kΩ pull-down to ground on pin 13 (I2S/$\overline{LJ}$) (pg. 26).

## Input Connections:

The analog module samples input at a 6.144 MHz rate and has the range 1.1V to 3.9V.

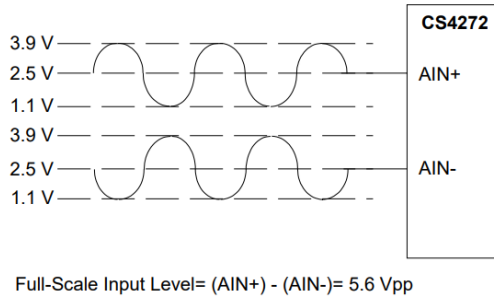



**Figure 13. Full-Scale Analog Input**

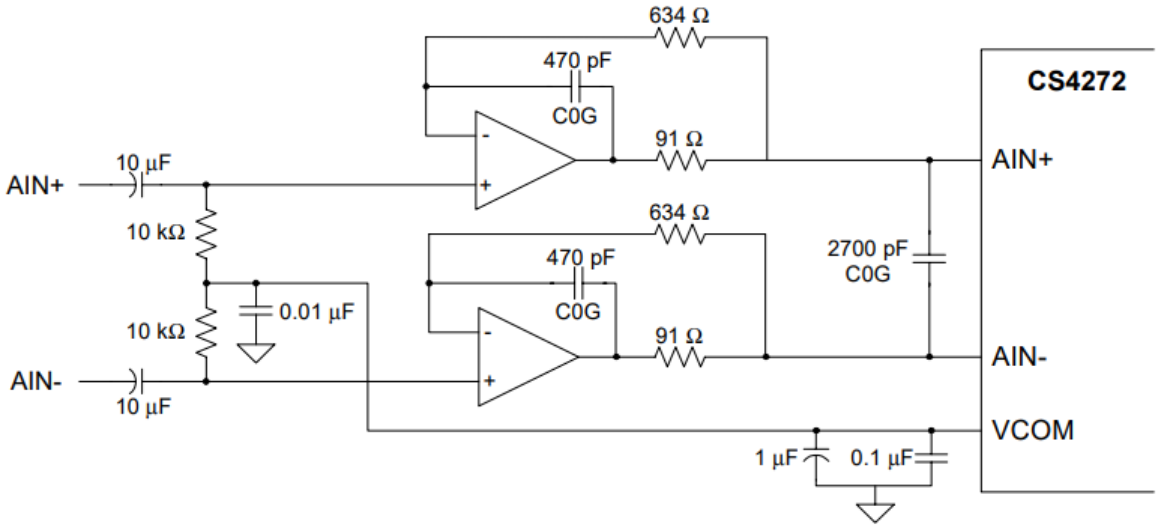



**Figure 12. CS4272 Recommended Analog Input Buffer**

## Output Connections:

We should consider filtering the output signal using their recommended circuit:

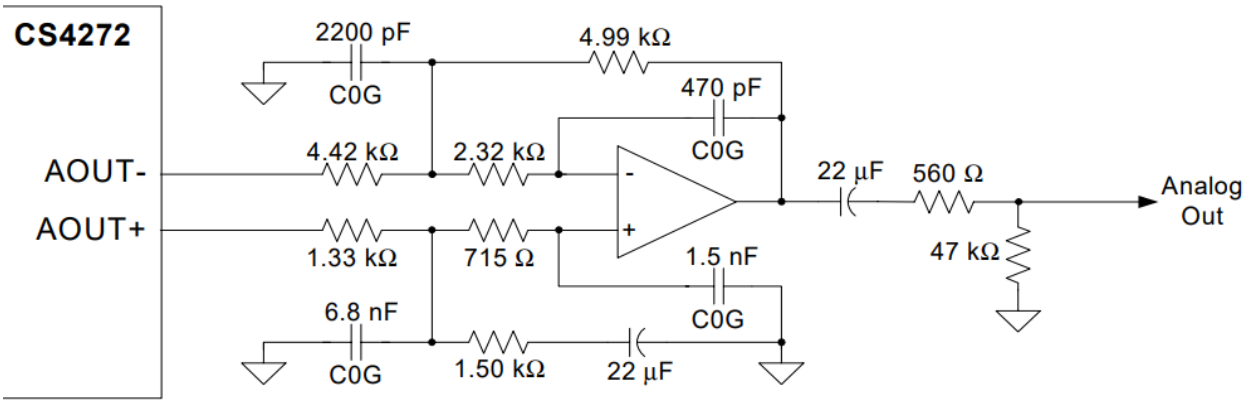



**Figure 14. CS4272 Recommended Analog Output Filter**

## Control Port Interface:

SPI mode will be selected when the AD0/$\overline{CS}$ (pin 13 I2S/$\overline{LJ}$?) transitions from high to low after power-up (pg 35) and control ports are write-only in SPI mode.

We might have to stall for 10ms after reset: "Upon release of the RST pin, the CS4272 will wait approximately 10 ms before it begins its start-up sequence" and also write 03h to register 07h before the end of the 10ms to avoid "noise" (pg 35). Then set CPEN and clear PDN to enter Control-Port Mode, now set all registers as desired before releasing the PDN bit.

To write to a register, bring $\overline{CS}$ (pin 5) low and the first 7 bits on CDIN (pin 7) must be 0010000 (chip address) and the eighth bit must be 0 (write). The next 8 bits is the address of the register to be updated. The next 8 bits is the data to be placed in the register. We can set bit INCR to write to successive registers.

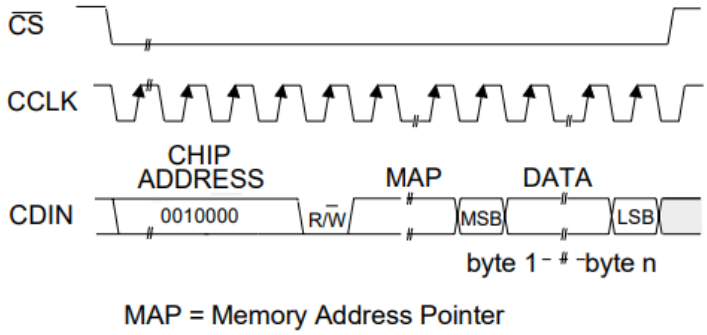



**Figure 17. Control Port Timing, SPI mode**

**Table 10. Memory Address Pointer (MAP)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INCR | Reserved | Reserved | Reserved | MAP3 | MAP2 | MAP1 | MAP0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

INCR - Auto MAP Increment Enable
Default = '0'.
0 - Disabled
1 - Enabled
MAP(3:0) - Memory Address Pointer
Default = '0000'.

If we're using 16-bit depth, enable the Dither16 bit in ADC control register 06h. This bit should not be set if we're using more than 16 bits.

Note that the ADC high pass filter is enabled by default. To disable, write 00 to the lower two bits in register 06h.