LAB 2 BEHAVIOURAL SIMULATION LAB REPORT

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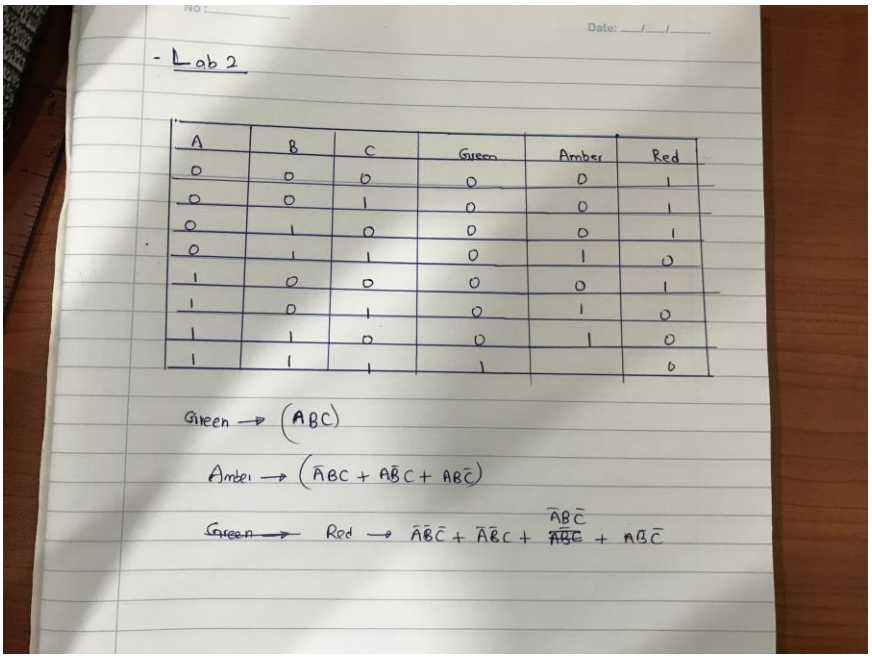
LAB TASK

We were assigned to run the simulation to indicate the correct functioning of three generators in a power station. The circuit should be designed in such a way that it indicates Green if all generators function, Amber if only 2 generators function and Red if 1 or no generators function. First we had create a design source and relate the hardware LEDs and pins by editing the constraint file. Finally we had to create a test bench file and complete the simulation.

Boolean Expression



- Lab 2

A	B	C	Green	Amber	Red
0	0	0	0	0	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1		0

Green → (ABC)

Amber → $(\bar{A}BC + A\bar{B}C + AB\bar{C})$

~~Green~~ → Red → $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \overline{\overline{ABC}} + AB\bar{C}$

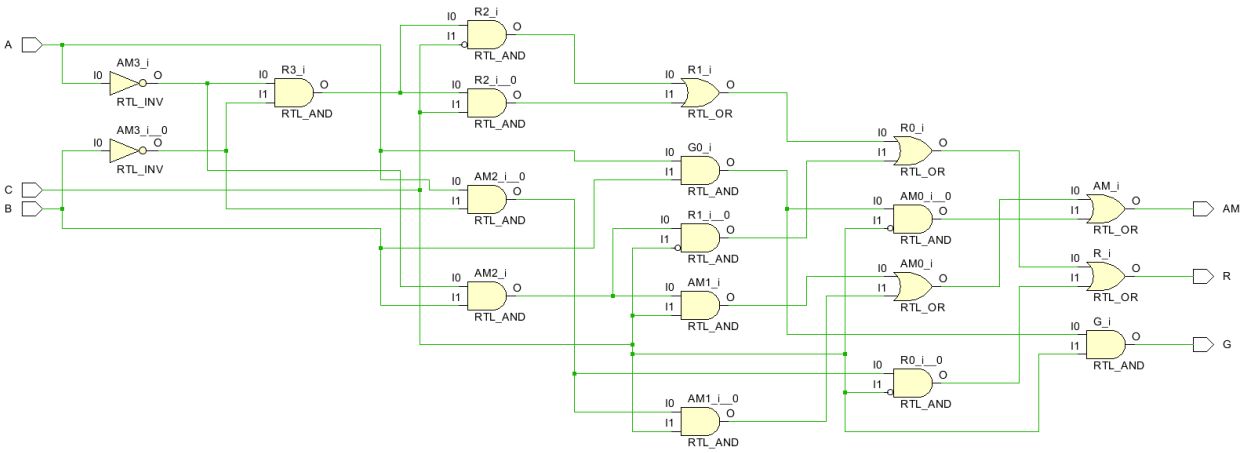
VHDL Design Source Code

Lab2.vhd | Basys3Labs.xdc | Circuit2Sim.vhd | Untitled 3

C:/Users/workshop/Documents/Lab2/Lab2.srcs/sources_1/new/Lab2.vhd

```
8       -- Project Name:
9       -- Target Devices:
10      -- Tool Versions:
11      -- Description:
12      --
13      -- Dependencies:
14      --
15      -- Revision:
16      -- Revision 0.01 - File Created
17      -- Additional Comments:
18      --
19      ----------------------------------------------------------------------------------
20
21
22      library IEEE;
23      use IEEE.STD_LOGIC_1164.ALL;
24
25      -- Uncomment the following library declaration if using
26      -- arithmetic functions with Signed or Unsigned values
27      --use IEEE.NUMERIC_STD.ALL;
28
29      -- Uncomment the following library declaration if instantiating
30      -- any Xilinx leaf cells in this code.
31      --library UNISIM;
32      --use UNISIM.VComponents.all;
33
34      entity Lab2 is
35          Port ( A : in STD_LOGIC;
36                 B : in STD_LOGIC;
37                 C : in STD_LOGIC;
38                 G : out STD_LOGIC;
39                 AM : out STD_LOGIC;
40                 R : out STD_LOGIC);
41      end Lab2;
42
43      architecture Behavioral of Lab2 is
44
45      begin
46          G <= A AND B AND C;
47         AM <= ((NOT A) AND B AND C) OR (A AND (NOT B) AND C) OR (A AND B AND (NOT C));
48         R <= ((NOT A) AND (NOT B) AND (NOT C)) OR ((NOT A) AND (NOT B) AND C) OR ((NOT A) AND B AND (NOT C)) OR (A AND (NOT B) AND (NOT C));
49
50      end Behavioral;
51
```

Schematic Circuit



Test Bench Code

Project Summary | Schematic | Lab2.vhd | Basys3Labs.xdc | Circuit2Sim.vhd

C:/Users/workshop/Documents/Lab2/Lab2.srcs/sim_1/new/Circuit2Sim.vhd

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/07/2023 02:02:19 PM
-- Design Name:
-- Module Name: Circuit2Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Circuit2Sim is
--  Port ( );
end Circuit2Sim;

architecture Behavioral of Circuit2Sim is
        COMPONENT Lab2
            PORT(  A, B, C : IN STD_LOGIC;
                   G,  Am,  R  : OUT STD_LOGIC);
        END COMPONENT;
```

```
        END COMPONENT;

        SIGNAL g0, g1, g2 : std_logic;
        SIGNAL g, a, r : std_logic;

begin
    UUT: Lab2 PORT MAP(
        A => g0,
        B => g1,
        C => G2,
        G => g,
        Am => a,
        R => r
);

process
begin
 g0 <= '0'; -- set initial values
 g1 <= '0';
 g2 <= '0';
 WAIT FOR 100 ns; -- after 100 ns change inputs
 g2 <= '1';
 WAIT FOR 100 ns; --change again
 g1 <= '1';
 g2 <= '0';
 WAIT FOR 100 ns; --change again
 g2 <= '1';
 WAIT FOR 100 ns; --change again
 g0 <= '1';
 g1 <= '0';
 g2 <= '0';
 WAIT FOR 100 ns; --change again
  g2 <= '1';
  WAIT FOR 100 ns; --change again
  g1 <= '1';
  g2 <= '0';
  WAIT FOR 100 ns; --change again
  g2 <= '1';
  WAIT; -- will wait forever
   end process;


end Behavioral;
```

Timing Diagram

Conclusions

- This lab was conducted to implement a logic circuit as stated at the beginning of this report and it was able to successfully simulate and provide exact results.
- Using Vivado software and creating respective design source codes, constraint files and a test bench code; we are able to create a simulation for any logic circuit.
- The most important role of simulation software was identified through this lab. When designing larger digital circuits, these simulation software can be very effective for debugging errors and reaching the final step.