LAB 3 – ADDER

B.A Nipun Viraj

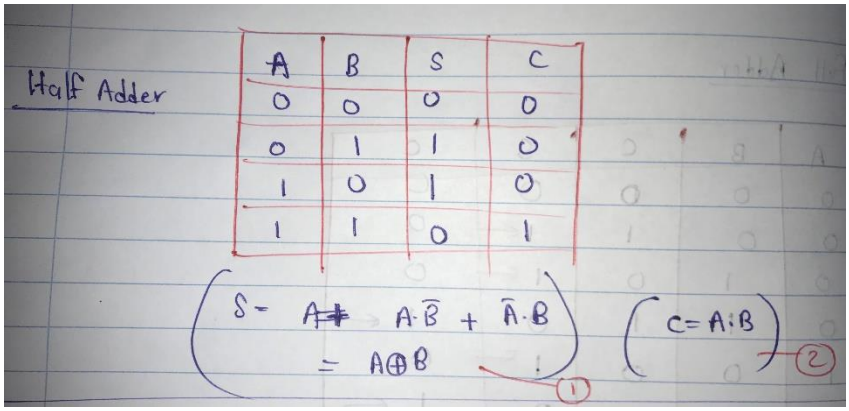
210495G

1. LAB TASK ASSIGNED

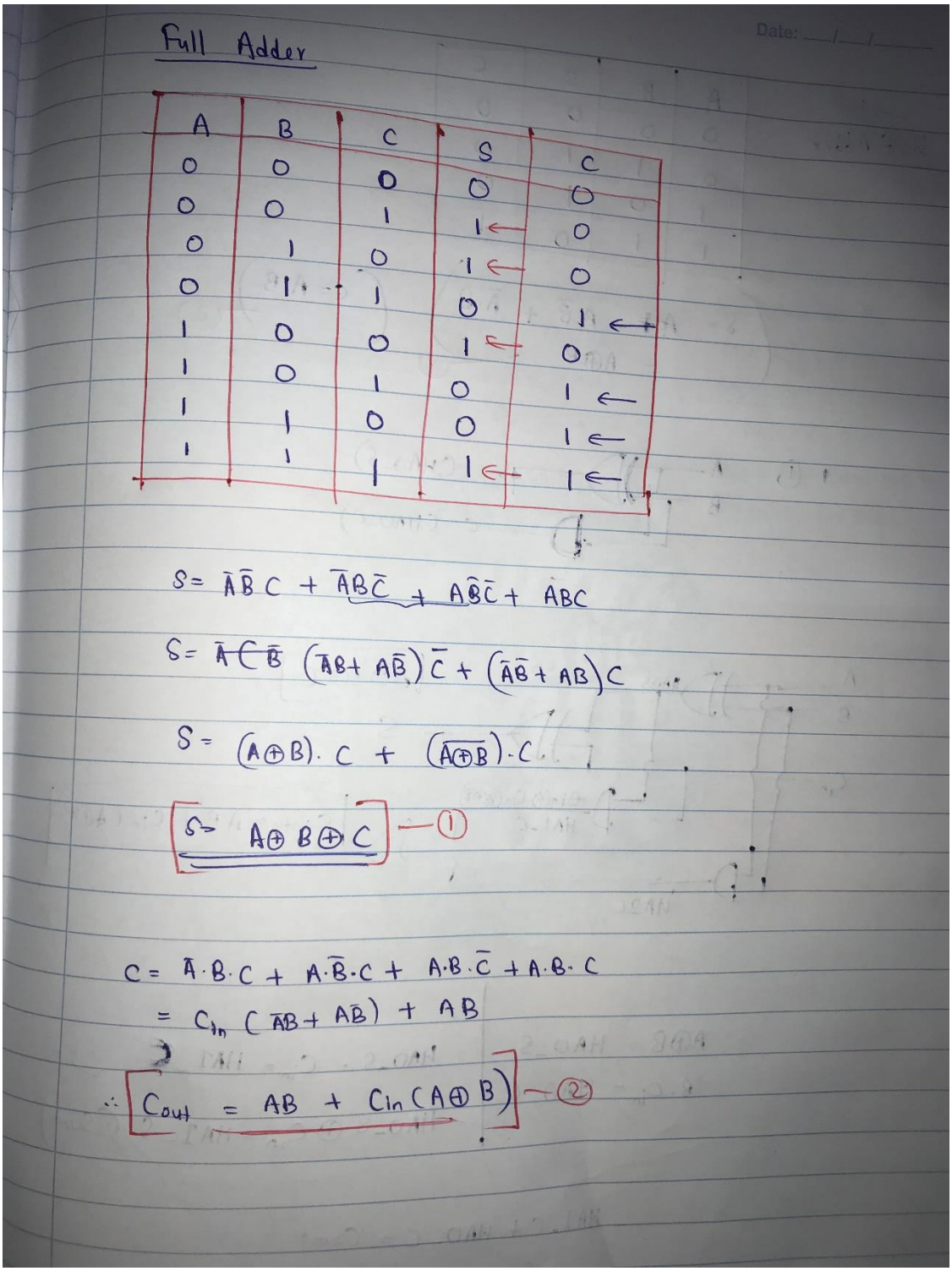
We were assigned to use Vivado Software to design a circuit as a half-bit adder, full bit adder and a ripple adder. Using appropriate inputs, a design file, a constraint file and a simulation file, we had to complete the circuit design.

2. TRUTH TABLES & SIMPLIFIED BOOLEAN EXPRESSION

1. **HALF ADDER**



2. **FULL ADDER**



Full Adder

Date: __/__/____

A	B	C	S	C
0	0	0	0	0
0	0	1	1 ←	0
0	1	0	1 ←	0
0	1	1	0	1 ←
1	0	0	1 ←	0
1	0	1	0	1 ←
1	1	0	0	1 ←
1	1	1	1 ←	1 ←

$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$S = \bar{A}(\bar{B}) + A(\bar{B})\bar{C} + (\bar{A}\bar{B} + AB)C$

$S = (A \oplus B) \cdot C + (\overline{A \oplus B}) \cdot C$

$S = A \oplus B \oplus C$ — (1)

$C = \bar{A} \cdot B \cdot C + A \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$

$= C_{in}(\bar{A}B + A\bar{B}) + AB$

$\therefore C_{out} = AB + C_{in}(A \oplus B)$ — (2)

3. VHDL FILES

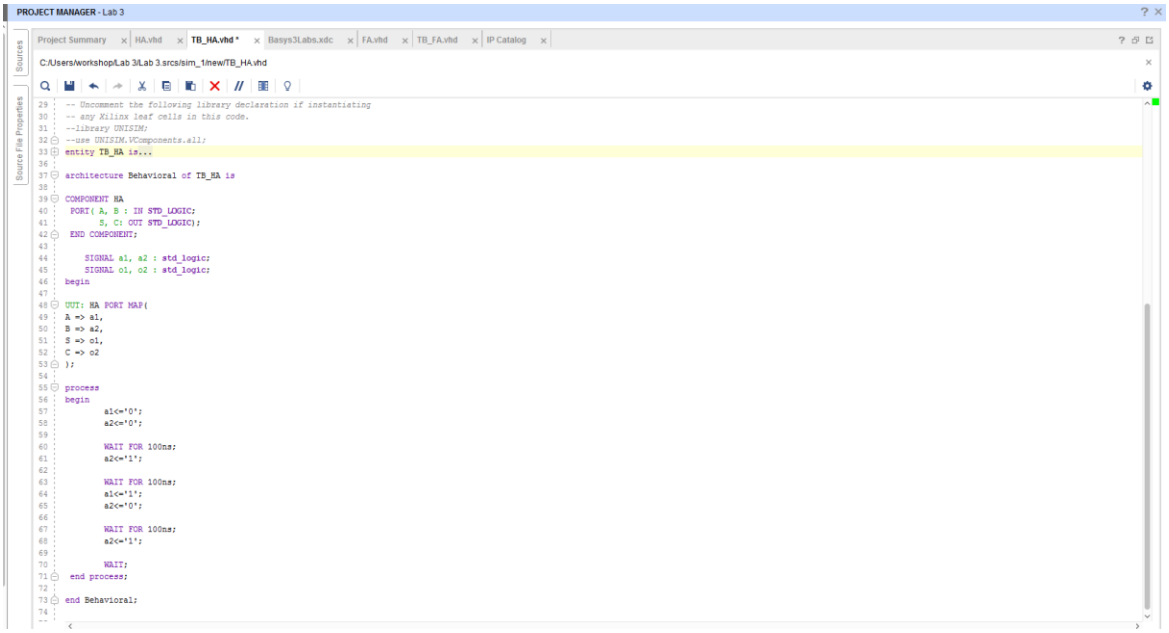
1. HA

Project Summary | HA.vhd | TB_HA.vhd | Basys3Labs.xdc | FA.vhd | TB_FA.vhd | IP Catalog

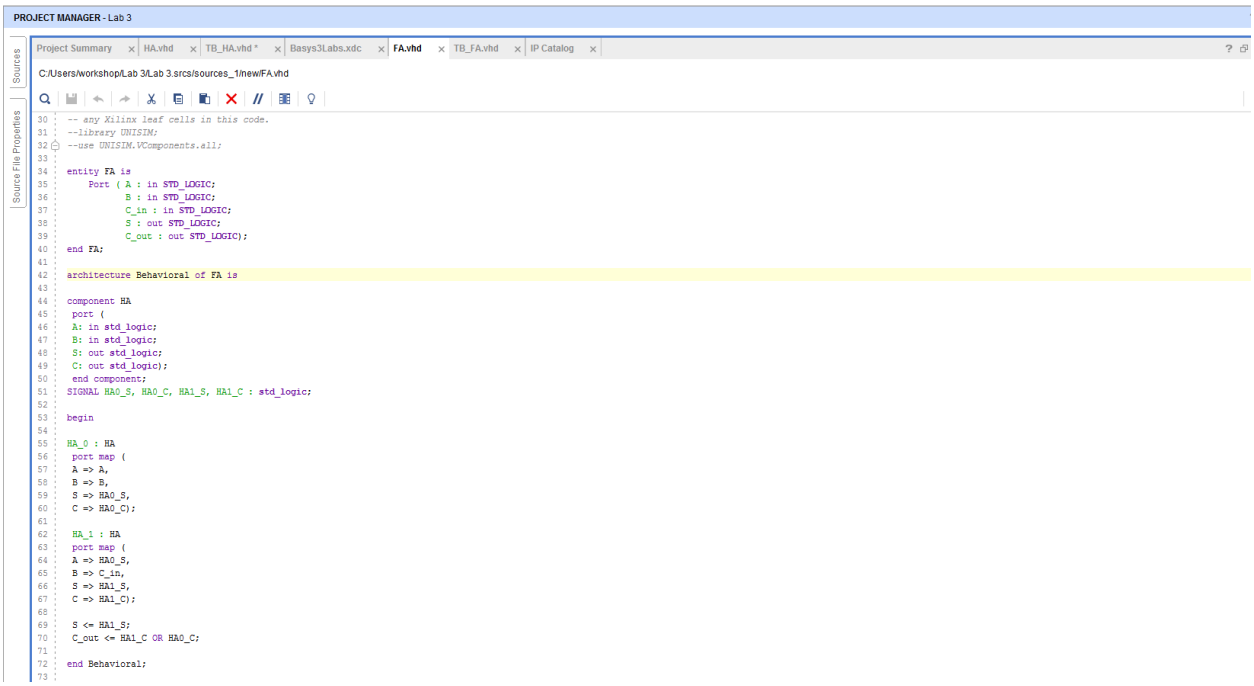
C:/Users/workshop/Lab 3/Lab 3.srcs/sources_1/new/HA.vhd

```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity HA is
35      Port ( A : in STD_LOGIC;
36             B : in STD_LOGIC;
37             S : out STD_LOGIC;
38             C : out STD_LOGIC);
39  end HA;
40
41  architecture Behavioral of HA is
42
43  begin
44
45  S <= A XOR B;
46  C <= A AND B;
47
48  end Behavioral;
49
```

2. TB_HA



3. FA


PROJECT MANAGER - Lab 3
Project Summary
HA.vhd
TB_HA.vhd *
Basys3Labs.xdc
FA.vhd
TB_FA.vhd
IP Catalog
C:/Users/workshop/Lab 3/Lab 3.srcs/sources_1/new/FA.vhd
Sources
Source File Properties
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity FA is
Port (A : in STD_LOGIC;
B : in STD_LOGIC;
C_in : in STD_LOGIC;
S : out STD_LOGIC;
C_out : out STD_LOGIC);
end FA;
architecture Behavioral of FA is
component HA
port (
A: in std_logic;
B: in std_logic;
S: out std_logic;
C: out std_logic);
end component;
SIGNAL HA0_S, HA0_C, HA1_S, HA1_C : std_logic;
begin
HA_0 : HA
port map (
A => A,
B => B,
S => HA0_S,
C => HA0_C);
HA_1 : HA
port map (
A => HA0_S,
B => C_in,
S => HA1_S,
C => HA1_C);
S <= HA1_S;
C_out <= HA1_C OR HA0_C;
end Behavioral;

4. TB_FA


```
19  ----------------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity TB_FA is
35  --  Port ( );
36  end TB_FA;
37
38  architecture Behavioral of TB_FA is
39
40  COMPONENT FA
41   PORT( A, B, C_in : IN STD_LOGIC;
42         S, C_out: OUT STD_LOGIC);
43   END COMPONENT;
44
45      SIGNAL i0, i1, i2 : std_logic;
46      SIGNAL o1, o2 : std_logic;
47  begin
48
49  UUT: FA PORT MAP(
50  A => i0,
51  B => i1,
52  C_in => i2,
53  S => o1,
54  C_out => o2
55  );
56
57  process
58  begin
59   i0 <= '0';
60   i1 <= '0';
61   i2 <= '0';
62   WAIT FOR 100 ns;
63   i2 <= '1';
64   WAIT FOR 100 ns;
65   i1 <= '1';
66   i2 <= '0';
67   WAIT FOR 100 ns;
68   i2 <= '1';
69   WAIT FOR 100 ns;
70   i0 <= '1';
71   i1 <= '0';
72   i2 <= '0';
73   WAIT FOR 100 ns;
74   i2 <= '1';
75   WAIT FOR 100 ns;
76   i1 <= '1';
77   i2 <= '0';
78   WAIT FOR 100 ns;
79   i2 <= '1';
80   WAIT;
81   end process;
82
83
84  end Behavioral;
85
86
```

5. TB_RCA_4

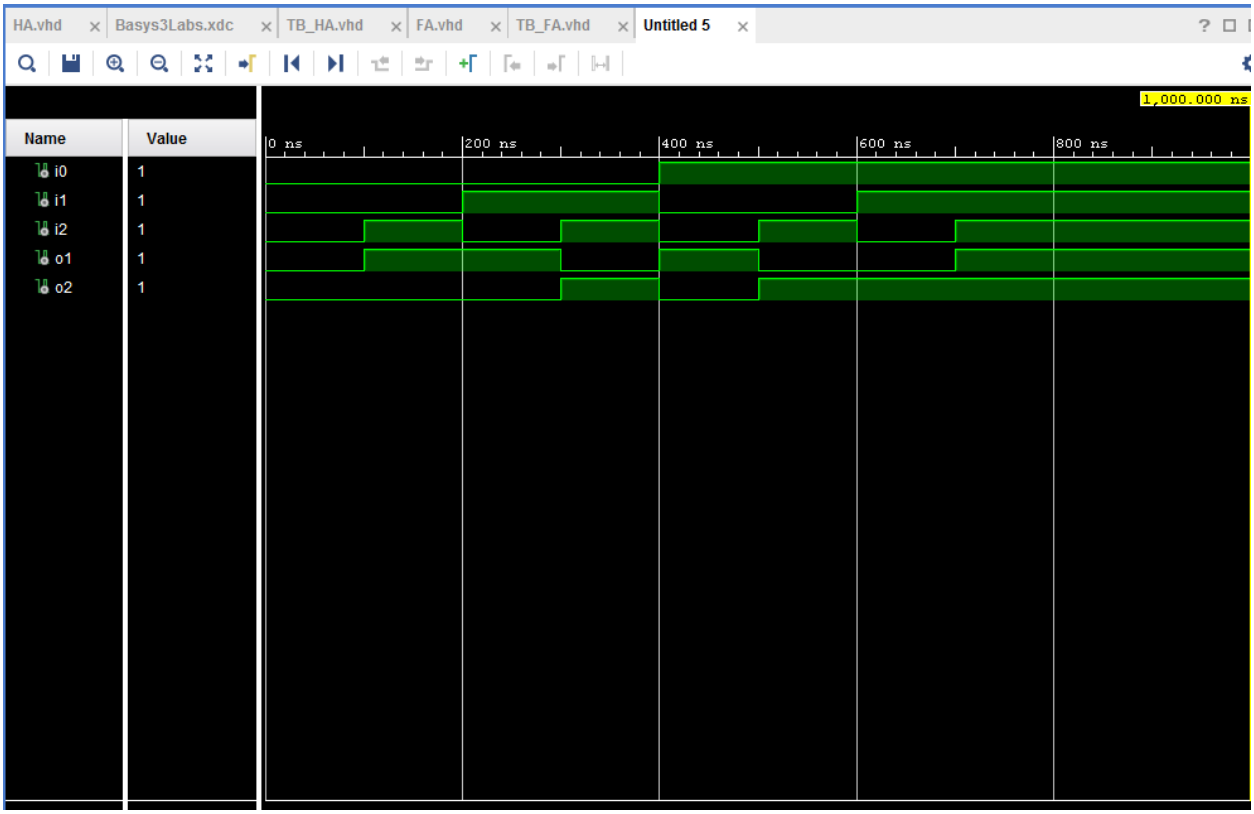
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_4_RCA is
--  Port ( );
end TB_4_RCA;

architecture Behavioral of TB_4_RCA is

COMPONENT RCA_4
 PORT( A0,A1,A2,A3,B0,B1,B2,B3,C_in : IN STD_LOGIC;
      S0,S1,S2,S3,C_out : OUT STD_LOGIC);
 END COMPONENT;
SIGNAL g0, g1, g2,g3,h0,h1,h2,h3,i0 : std_logic;
SIGNAL O0,O1,O2,O3,O4 : std_logic;

begin

UUT: RCA_4 PORT MAP(
A0 => g0,
A1 => g1,
A2 => g2,
A3 => g3,
B0=>h0,
B1 => h1,
B2=>h2,
B3=>h3,
C_in=>i0,
S0=>O0,
S1=>O1,
S2=>O2,
S3=>O3,
C_out => O4
 );

 process
 begin
   g0 <= '0'; -- set initial values
   g1 <= '0';
   g2 <= '1';
   g3 <= '1';
   h0 <= '0';
   h1 <= '0';
   h2 <= '1';
   h3 <= '1';
   i0 <= '0';
```

```
h2 <= '1';
h3 <= '1';
i0 <= '0';
WAIT FOR 100 ns; -- after 100 ns change inputs
g0 <= '0'; -- set initial values
g1 <= '0';
g2 <= '1';
g3 <= '1';
h0 <= '1';
h1 <= '1';
h2 <= '1';
h3 <= '1';
i0 <= '0';
WAIT FOR 100 ns; --change again
g0 <= '0'; -- set initial values
g1 <= '1';
g2 <= '0';
g3 <= '1';
h0 <= '1';
h1 <= '0';
h2 <= '1';
h3 <= '1';
i0 <= '0';
WAIT FOR 100 ns; --change again
```

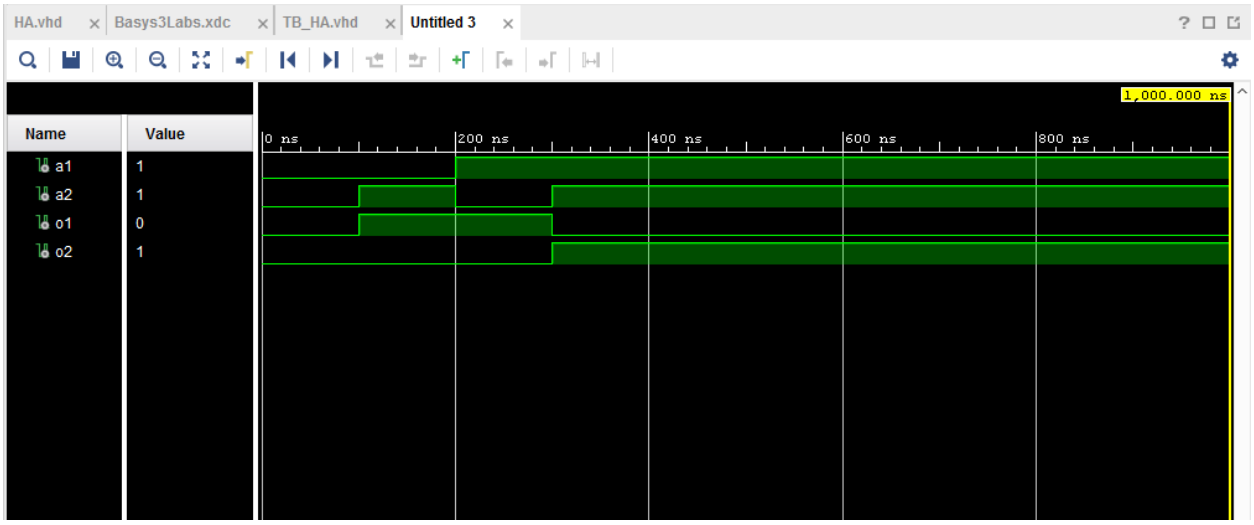
```
i0 <= '0';
WAIT FOR 100 ns; --change again
g0 <= '0'; -- set initial values
g1 <= '0';
g2 <= '1';
g3 <= '1';
h0 <= '1';
h1 <= '0';
h2 <= '1';
h3 <= '1';
i0 <= '1';
WAIT FOR 100 ns; --change again
g0 <= '0'; -- set initial values
g1 <= '1';
g2 <= '1';
g3 <= '1';
h0 <= '1';
h1 <= '1';
h2 <= '1';
h3 <= '1';
i0 <= '1';
WAIT FOR 100 ns; --change again
g0 <= '1'; -- set initial values
g1 <= '1';
g2 <= '1';
g3 <= '1';
h0 <= '1';
h1 <= '0';
h2 <= '0';
h3 <= '1';
i0 <= '1';
WAIT FOR 100 ns; --change again
```

```
  i0 <= '1';
  WAIT FOR 100 ns; --change again
  g0 <= '1'; -- set initial values
  g1 <= '1';
  g2 <= '0';
  g3 <= '0';
  h0 <= '0';
  h1 <= '0';
  h2 <= '0';
  h3 <= '0';
  i0 <= '0';
  WAIT FOR 100 ns; --change again
  g0 <= '1'; -- set initial values
  g1 <= '1';
  g2 <= '0';
  g3 <= '0';
  h0 <= '1';
  h1 <= '1';
  h2 <= '0';
  h3 <= '0';
  i0 <= '0';
  WAIT; -- will wait forever
end process;
```

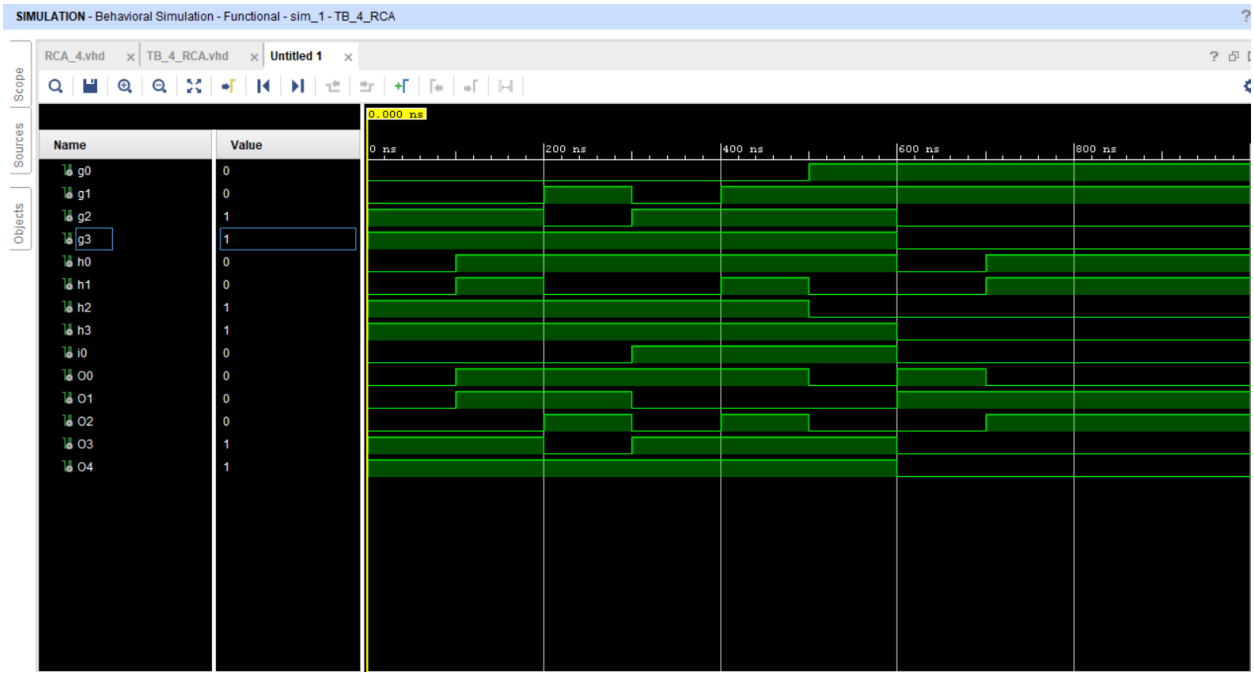
4. TIMING DIAGRAMS



HA TIMING DIAGRAM



FA TIMING DIAGRAM



RCA TIMING DIAGRAM

CONCLUSION

We can integrate many similar circuits into a main circuit and improve their performance to much larger tasks. (Like the half adder was developed to full adder and full adder was developed to ripple adder which can add any 4-bit number).