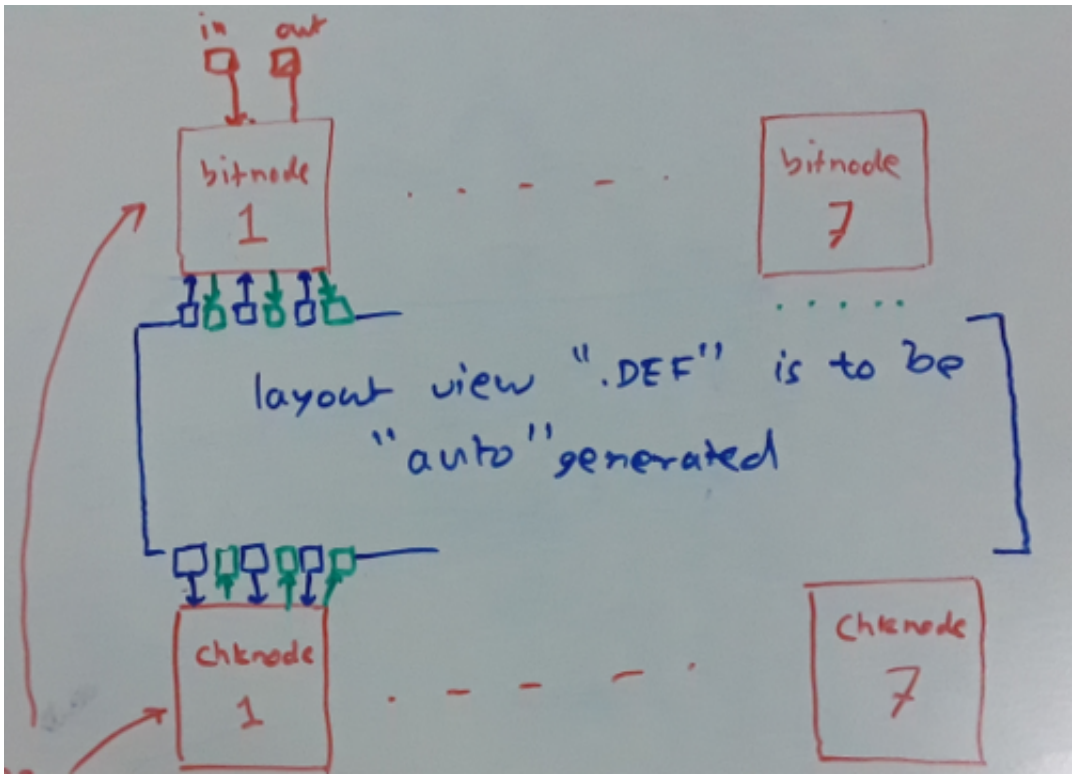
VLSI Layout of fully parallel LDPC decoder



"incidence fabric" (connectes bitnodes and checknodes as per tanner graph / provided incidence matrix)

Need to generate .DEF file.

Layout for bitnode and checknode can be generated using :
synopsys design compiler (behavioural to structural)
followed by
cadence soc encounter (netlist to automatic layout, routing etc.)

It is not necessary to place the bitnodes and checknodes in two rows as shown above.
They should be placed as per convenience -- dictated by the incidence fabric layout.

Note : Above diagram is just a sketch, e.g. CLK and RST signals are not shown above.

Can use PDK/CDK such as NCSU CDK, and cell library such as mudlib.
Free to use many metal layers.
To start with generation of layout of incidence fabric, can assume black box bit and check nodes of reasonable(!) sizes.
example incidence matrix of a PG(2, 2) based LDPC code :

	bitnode 1	bitnode 2	. . .				
checknode 1	1	1	0	1	0	0	0
checknode 2	0	1	1	0	1	0	0
.	0	0	1	1	0	1	0
.	0	0	0	1	1	0	1
.	1	0	0	0	1	1	0
	0	1	0	0	0	1	1
	1	0	1	0	0	0	1

7x7

'1' at row-i, column-j indicates a connection between checknode-i and bitnode-j