Exam 2

Practice Problems

```
(*TODO*)

vt = 0.9; k = 0.018; rl = 220;
(*With KVL we find VGS+VIN-VG=0
    and VGS≥VT keeps the MOSFET out of cutoff.
    So we plug in different values at the boundaries of the VIN range,
and pick one of them *)
vin = 1;
Solve[vg - vin == vt, vg]
vin = -2;
Solve[vg - vin == vt, vg](*Not sure why we don't pick this one, its the min(?)*)

vg = 3;
vin = 1;(*First try*)
vgs = vg - vin;
id = k/2 (vgs - vt)^2;
vdd = id rl(*Not sure why we don't pick this one, its the min(?)*)
vin = -2;(*Second try*)
vgs = vg - vin;
id = k/2 (vgs - vt)^2;
vdd = id rl

Clear[vg]
Solve[vg - vt == 0, vg]
vg = 0.9;(*This is our operating point,
at this point VGS=VG from our KVL expression above.*)
g = k (vg - vt)
```

Out[•]= {{vg → 1.9}}

Out[•]= {{vg → -1.1}}

Out[•]= 2.3958

Out[•]= 33.2838

Out[•]= {{vg → 0.9}}

Out[•]= 0.

Q2

0 points possible (ungraded)

The circuit shown below is intended to implement C as a logic function of A and B.

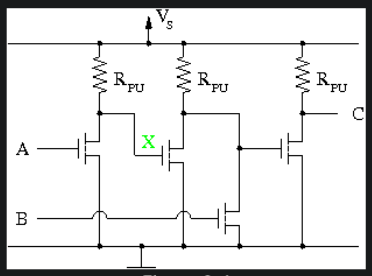


Figure 2-1

Three of the four following logic diagrams compute the same logic function as the circuit above.

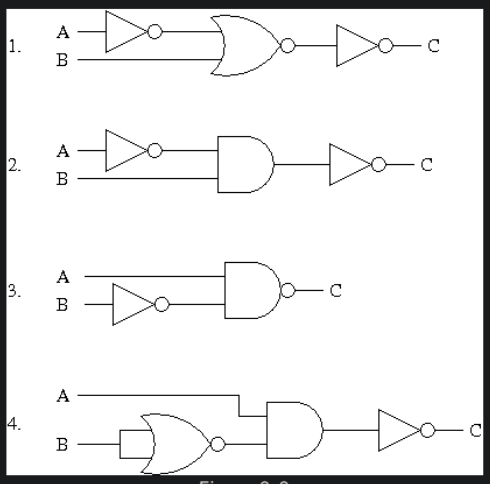


Figure 2-2

Which diagram computes something different?
Write the number of the incorrect diagram in the box below:

2 ✔ **Answer:** 2

The circuit is intended to obey the following static discipline:

$V_S = 5.0\text{V}, V_{OH} = 4.0\text{V}, V_{IH} = 2.8\text{V}, V_{IL} = 2.2\text{V}, V_{OL} = 1.4\text{V}.$

What is the low-level noise margin? (Express your answer in Volts.)

0.8 ✔ **Answer:** 0.8000000000000003

What is the high-level noise margin? (Express your answer in Volts.)

1.2 ✔ **Answer:** 1.2000000000000002

How big (in Volts) is the forbidden region?

0.6 ✔ **Answer:** 0.5999999999999996

Assume that $R_{ON} = 5.0\text{k}\Omega$ for our MOSFETS. What is the minimum value that R_{PU} can have, in kilOhms, and still satisfy

the static discipline?

12.8571 ✔ **Answer:** 12.85714285714286

We now have $R_{ON} = 5.0\text{k}\Omega$. Let's choose $R_{PU} = 14\text{k}\Omega$. What is the maximum amount of power, in milliWatts, that is consumed by this circuit for legitimate logic levels applied at A and B?

2.63445 ✔ **Answer:** 2.631578947368421

Given our choices of R_{ON} and R_{PU}, assume that the gate-to-source capacitance $C_{GS} = 50.0\text{fF}$. What is the rising edge time constant, in nanoseconds, for the signal at the node labeled X?

0.7 ✔ **Answer:** 0.7000000000000001

What is the falling edge time constant, in nanoseconds, for the signal at the node labeled X?

0.184211 ✔ **Answer:** 0.1842105263157895

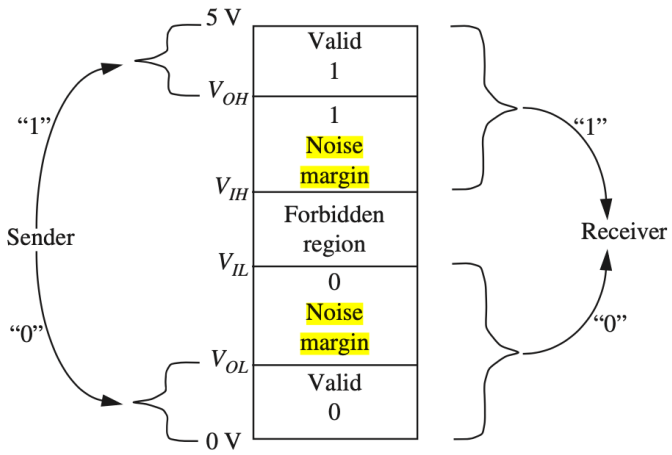
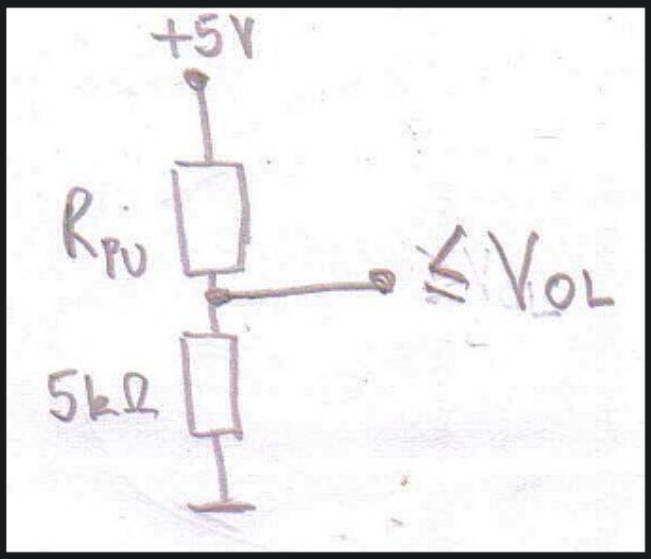


FIGURE 5.8 A mapping between voltage levels and logical signals that provides noise margins. For a logical high, senders must output values in the V_{OH} to 5-V range. For a logical low, senders must output values in the o V to V_{OL} range. Receivers must correspondingly interpret values greater than V_{IH} as a logical high, and output values lower than V_{IL} as a logical low.

I don't know how to find the minimun value of Rpu, can u help me how to see this?

This post is visible to everyone.

Grove (Community TA)
2 years ago - marked as answer 2 years ago by **MIT_Lover_UA** (Staff)



Why it must be less or equal than V_OL?

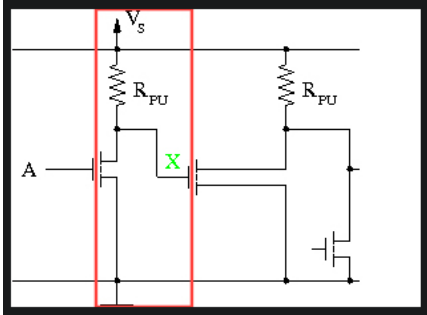
posted 2 years ago by **Pacories**

That is part of the static discipline.

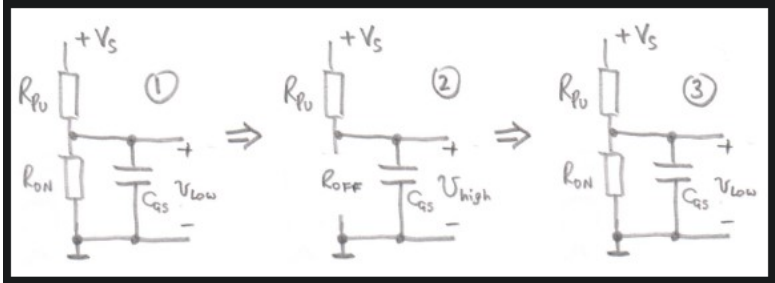
Any output voltage less than or equal to V_{OL} is to be taken as a **0** or **LOW** output from the device.

```
(*For the last 2 parts*)
```

The relevant part of the circuit is in the red rectangle and there is a capacitance C_{GS} between node X (the gate) and the ground (the source).



A sequence of events might be characterised by the following circuit diagrams.

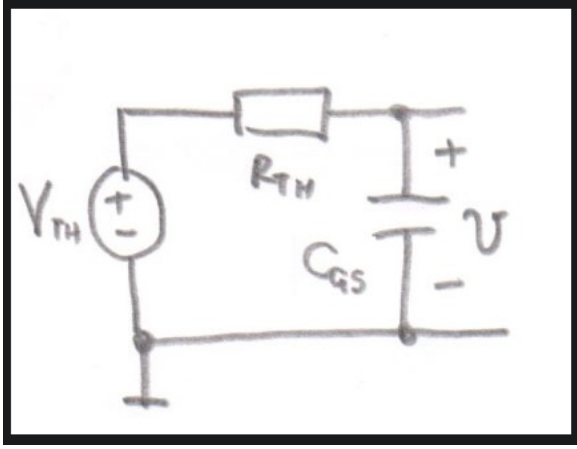


In diagram **1** the mosfet is ON the voltage across the capacitor is v_{low} determined by the potential divider network R_{PU} and R_{ON} and the supply voltage V_{S}.

If the mosfet is switched off then the voltage across the capacitor will rise with a time constant which is determined by C_{GS} and R_{PU} because R_{OFF} is so much larger than R_{PU} ie effectively an open circuit.
The capacitor charges up to reach v_{high} which will be V_{S} in this example as shown in diagram **2**.

After a time if the mosfet is now switched on the capacitor will now discharge with a time constant which depends on R_{PU}, R_{ON} and C_{GS} and it finally reaches a state as shown in diagram **3** (and **1**).

At each stage the voltage source and resistor network can be converted into the Thevenin equivalent as shown below.



In[•]:=
```
(*First write down explicitly what the diagram does,
then convert all of them to DNF then compare*)
c1 = BooleanConvert[! (! (! a || b))]
c2 = BooleanConvert[! (! a && b)]
c3 = BooleanConvert[! (! b && a)]
c4 = BooleanConvert[! (! (b || b) && a)]

vs = 5; voh = 4; vih = 2.8; vil = 2.2; vol = 1.4;
vil - vol
voh - vih
vih - vil

ron = 5*^3;
Solve[vol == ron / (ron + rpu) vs, rpu] (*Divide by 1000 for unit conversion*)

ron = 5*^3; rpu = 14*^3;
Rp[r_List] := 1 / Total[1 / r];
(*Resistance for a MOSFET in the ON state = R_PU||R_ON
   There are 4 legit logic levels for AB namely: 00,10,01,11.
  When we enumerate their resistive networks.
   00: 2(R_PU||R_ON)
   10: 2(R_PU||R_ON)
   01: (R_PU||R_ON||R_ON)+(R_PU||R_ON)
   11: R_ON+(R_PU||R_ON)
   Instead of following this I just turned on
   all MOSFETs and got something close to the official answer.
    TLDR; no idea*)
rth = Rp[{rpu, ron}] + Rp[{rpu, ron, ron}] + Rp[{rpu, ron}];
p = vs^2 / rth * 1000 // N(*Multiply by 1000 for unit conversion*)

ron = 5*^3; rpu = 14*^3; cgs = 50*^-15;
τ = rpu * cgs // N
τ = Rp[{rpu, ron}] * cgs // N
```

Out[•]= ! a || b

Out[•]= a || ! b

Out[•]= ! a || b

Out[•]= ! a || b

Out[•]= 0.8

Out[•]= 1.2

Out[•]= 0.6

••• Solve: Solve was unable to solve the system with inexact coefficients. The answer was obtained by solving a corresponding exact system and numericizing the result.

Out[•]= {{rpu → 12 857.1}}

Out[•]= 2.63445

Out[•]= $7. \times 10^{-10}$

Out[•]= 1.84211×10^{-10}

Q3

0 points possible (ungraded)

A junction field-effect transistor (JFET) with its gate and source connected together form a two terminal nonlinear device. The current in this device saturates to a current level I_{DSS} for v_D larger than V_P called the pinch-off voltage. The device and I-V characteristic are shown in Figure 3-1.

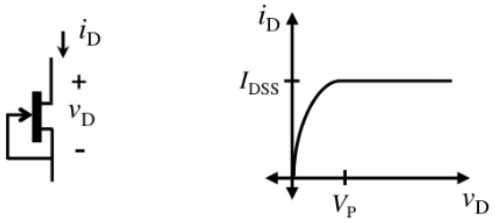


Figure 3-1

We can describe this relationship with the equation:

$$i_D = \begin{cases} I_{DSS}\left[2\left(\frac{v_D}{V_P}\right) - \left(\frac{v_D}{V_P}\right)^2\right] & \text{if } v_D \le V_P \\ I_{DSS} & \text{if } v_D > V_P \end{cases}$$

This device is used in the circuit in Figure 3-2, which includes a resistor, R, and voltage source, V_S.

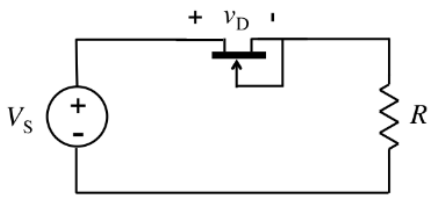


Figure 3-2

Assuming that $I_{DSS} = 0.004A$, $V_P = 2V$, $R = 1000\Omega$, and $V_S = 4V$, find the operating point of the circuit by evaluating v_D and i_D.

v_D (in Volts):

1 ✔ **Answer:** 1.0

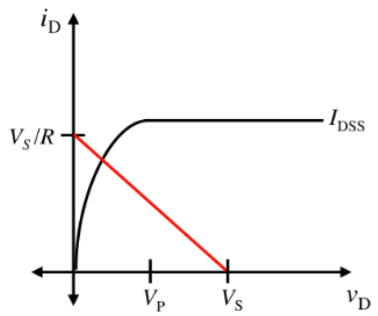
i_D (in Amps):

0.003 ✔ **Answer:** 0.003

At what value of V_S (in Volts) does the current through the JFET stabilize at I_{DSS}?

6 ✔ **Answer:** 6.0

Explanation:
Observing the V-I chart for the non-linear device in this question, we see two distinct modes of operation. The device is in a "quadratically increasing" mode when the voltage across it is less than V_P and the current through it is defined as $i_D = I_{DSS} \cdot \left(2\frac{v_D}{V_P} - \left(\frac{v_D}{V_P}\right)^2\right)$. If the voltage across it is greater than V_P, the device enters saturation and has a steady current of I_{DSS}.
For the first part to determine what mode the device is operating in, it is helpful to do a load line analysis. When the voltage drop across the JFET is 0, the voltage drop across the resistor is V_S and the current through the resistor is V_S/R, so the y-intercept (or i-intercept) of the load line is V_S/R. When the voltage drop across the JFET is V_S, the voltage drop across the resistor is 0 as is the current through it, so the x-intercept (or v-intercept) is V_S. The load line is drawn below. We can see that the operating point occurs when the JFET is not saturated.



We can apply KCL on the node between the resistor and JFET, which is operating in it's non-linear mode:

$$i_D = i_R$$
$$I_{DSS} \cdot \left(2\frac{v_D}{V_P} - \left(\frac{v_D}{V_P}\right)^2\right) = \frac{V_S - v_D}{R}$$

Substituting in $I_{DSS} = 0.004A$, $V_P = 2V$, $R = 1000\Omega$, and $V_S = 4V$:

$$0.004 \cdot \left(2\frac{v_D}{2V} - \left(\frac{v_D}{2V}\right)^2\right) = \frac{4V - v_D}{1000\Omega}(1.0) \cdot v_D^2 + (-5.0) \cdot v_D + (4) = 0$$

Solving for v_D:

$$v_D = 4.0V, 1.0V$$

We know that $v_D = 1.0V$, because the other solution implies there is current flowing through the JFET but no current through the resistor, which violates KCL.
Solving for i_D is straight foraward once we know v_D:

$$i_D = i_R = \frac{V_S - v_D}{R} i_D = \frac{4V - 1.0V}{1000\Omega} i_D = 0.003A$$

Finally we want to find what value of V_S gurantees that the JFET is in saturation. If the JFET is saturated, we know that $v_D > V_P$ and $i_D = I_{DSS}$. We can again use our best friend KCL with these assumptions:

$$i_D = i_R I_{DSS} = \frac{V_S - v_D}{R} v_D = V_S - R \cdot I_{DSS} v_D > V_P \Rightarrow V_S - R \cdot I_{DSS} > V_P V_S > V_P + R \cdot I_{DSS}$$

Again substituting in our known values:

$$V_S > 2V + (1000\Omega) \cdot (0.004A)\, V_S > 6.0V$$

Q4

0 points possible (ungraded)

This problem investigates how digital signals are distorted as they travel over real wires. A real wire is not a perfect short circuit, instead it has resistance, inductance and capacitance. In this problem we assume that the wire has been designed to have very low capacitance, so the capacitance can be ignored, and the wire can be modeled as shown in the figure below.

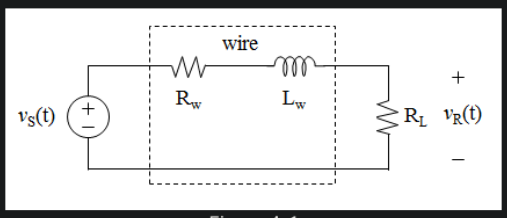


Figure 4-1

Here R_w and L_w model the series resistance and inductane of the wire. The voltage source $v_S\,(t)$ models the signal source and R_L is the resistance of the load where the signal is received. The signal source generates a square-wave voltage with period $2T$ and maximum value V_0, as shown below.

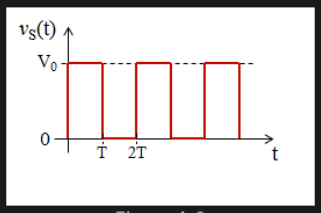


Figure 4-2

In steady state, the voltage signal measured across the load resistor appears as shown below

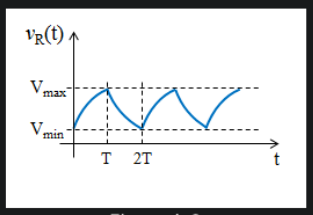


Figure 4-3

Assume that in the circuit above, $V_0 = 5V$, $T = 1ms$, $R_w = 1\Omega$, $L_w = 1mH$ and $R_L = 1\Omega$.

What is the time constant (in milliseconds) associated with the rise of voltage v_R?

0.5 ✔ **Answer:** 0.5

What is the time constant (in milliseconds) associated with the fall of voltage v_R?

0.5 ✔ **Answer:** 0.5

What is the value of V_{max} in Volts?

2.202 ✔ **Answer:** 2.202

What is the value of V_{min} in Volts?

0.298 ✔ **Answer:** 0.298

Explanation:
This is a first order LR system that requires a time-domain analysis to find the solutions.
(a) As with all linear LR systems, the rise time constant is defined as $\tau = \frac{L}{R}$. In this case, however, we have to consider both resistances R_w and R_L in series since they both share the same current with the inductor. Therefore, we find that:

$$\tau = \frac{L}{R_w + R_L} = 0.5ms$$

(b) The decay time constant in this case is the same as the rise time constant because the circuit is not changed during the transition. Therefore:

$$\tau = \frac{L}{R_w + R_L} = 0.5ms$$

(c) To find the maximum and minimum voltages of the output waveform we can use the typical expressions for the first order LR systems. Notice, however, that for each rising transistion the output voltage does not start at zero and for the decaying transition the voltage does not start at maximum voltage. When a system is operating like this, it is said to be in "periodic steady state."
First, let's consider both resistors R_L and R_w together as an equivalent resistor, and find the voltage across both of them. After that, we can just apply a voltage divider and find the voltage only across the load resistor R_L. A procedure to solve this is to state one equation for the rising transition assuming that it starts from zero at $t = 0$ and that it reaches V_{min} at some unknown time $t = t_0$. Then, it reaches V_{max} at time $t = t_0 + T$. We can write two equations for the voltage across both resistors:

$$V_{min} = V_0 \cdot \left(1 - e^{\frac{-t_0}{\tau}}\right)$$
$$V_{max} = V_0 \cdot \left(1 - e^{\frac{-(t_0+T)}{\tau}}\right)$$

Similarly for the decaying transition we can write an expression for V_{min} and V_{max} assuming that the decay starts at V_0, reaching V_{max} at an unknown time $t = t_1$ and V_{min} at time $t = t_1 + T$. The equations are:

$$V_{max} = V_0 \cdot e^{\frac{-t_1}{\tau}}$$
$$V_{min} = V_0 \cdot e^{\frac{-(t_1+T)}{\tau}} = V_0 \cdot e^{\frac{-t_1}{\tau}} \cdot e^{\frac{-T}{\tau}}$$

These last two equations can be used to get a relationship between V_{max} and V_{min}:

$$V_{max} = V_0 \cdot e^{\frac{-t_1-T+T}{\tau}} = V_0 \cdot e^{\frac{-t_1-T}{\tau}} \cdot e^{\frac{T}{\tau}} = V_{min} \cdot e^{\frac{T}{\tau}}$$

The other two equations can be used to solve for V_{max} and V_{min}. Start by solving for $e^{\frac{-t_0}{\tau}}$ with the expression for V_{min} found for the rising transition. This gives:

$$\left(1 - \frac{V_{min}}{V_0}\right) = e^{\frac{-t_0}{\tau}}$$

Then, substitute this value and the relationship between V_{max} and V_{min} found before, into the equation for V_{max} during the rising transition. This gives:

$$V_{min} \cdot e^{\frac{T}{\tau}} = V_0 \cdot \left(1 - e^{\frac{-T_0}{\tau}} \cdot e^{\frac{-T}{\tau}}\right) = V_0 \cdot \left(1 - \left(1 - \frac{V_{min}}{V_0}\right) \cdot e^{\frac{-T}{\tau}}\right)$$

This expression is only a function of V_0, V_{min}, T and τ so that we can solve for V_{min} as follows:

$$V_{min} \cdot e^{\frac{T}{\tau}} = V_0 \cdot \left((1 - e^{\frac{-T}{\tau}}) + \frac{V_{min}}{V_0} \cdot e^{\frac{-T}{\tau}}\right)$$

$$V_{min} \cdot e^{\frac{T}{\tau}} = V_0 \cdot \left(1 - e^{\frac{-T}{\tau}}\right) + V_{min} \cdot e^{\frac{-T}{\tau}}$$

$$V_{min} \cdot \left(e^{\frac{T}{\tau}} - e^{\frac{-T}{\tau}}\right) = V_0 \cdot (1 - e^{\frac{-T}{\tau}})$$

$$V_{min} = V_0 \cdot \frac{1 - e^{\frac{-T}{\tau}}}{e^{\frac{T}{\tau}} - e^{\frac{-T}{\tau}}}$$

Using the relationship between V_{max} and V_{min} found before, we get:

$$V_{max} = V_{min} \cdot e^{\frac{T}{\tau}} = V_0 \cdot \frac{1 - e^{\frac{-T}{\tau}}}{e^{\frac{T}{\tau}} - e^{\frac{-T}{\tau}}} \cdot e^{\frac{T}{\tau}}$$

$$V_{max} = V_0 \cdot \frac{e^{\frac{T}{\tau}} - 1}{e^{\frac{T}{\tau}} - e^{\frac{-T}{\tau}}}$$

Finally, we have to apply a voltage divider between the two resistors to find the voltage only across R_L:

$$V_{max} = \frac{R_L}{R_w + R_L} \cdot V_0 \cdot \left(\frac{e^{\frac{T}{\tau}} - 1}{e^{\frac{T}{\tau}} - e^{\frac{-T}{\tau}}}\right) = 2.202V$$

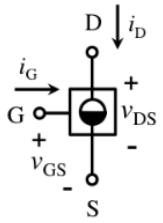
(d) Applying the voltage divider for the V_{min} equation we get:

$$V_{min} = \frac{R_L}{R_w + R_L} \cdot V_0 \cdot \left(\frac{1 - e^{\frac{-T}{\tau}}}{e^{\frac{T}{\tau}} - e^{\frac{-T}{\tau}}}\right) = 0.298V$$

Q5

0 points possible (ungraded)

A startup company TakaCorp has invented a new type of MOS-gated transistor called iMOSm. The symbol for iMOSm and its terminal voltage-current characteristics are given in Figure 5-1.



$$i_G = 0$$

$$i_D = \begin{cases} 0 & \text{if } v_{GS} < 0 \\ m \cdot v_{GS} & \text{if } v_{GS} \geq 0 \end{cases}$$

Figure 5-1

TakaCorp uses the iMOSm as an amplifier with the input biased with two gate resistors, R_G as shown in Figure 5-2.

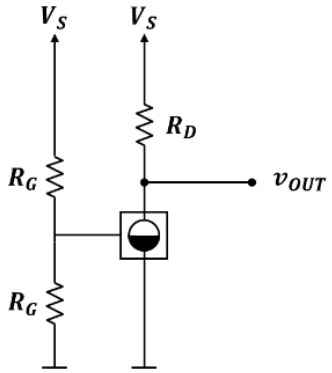


Figure 5-2

What is the expression for v_{OUT} in terms of V_S, R_D, and m?

VS*(1 - m*RD/2)

✔ **Answer:** VS*(1 - m*RD/2)

$$V_S \cdot \left(1 - m \cdot \frac{R_D}{2}\right)$$

Explanation:
Amplifier in Figure 5-2: Due to the fact that the gate of a MOSFET has no input current, the gate voltage of the iMOSm is set by the voltage divider consisting of the two R_G resistors and our supply voltage, so:

$$v_{GS} = V_S \cdot \frac{R_G}{R_G + R_G} = \frac{V_S}{2}$$

The current through R_D equals the current through the the iMOSm, so we write:

$$\frac{V_S - v_{OUT}}{R_D} = m \cdot v_{GS} \frac{V_S - v_{OUT}}{R_D} = m \cdot \frac{V_S}{2}$$

Solving for v_{OUT}:

$$v_{OUT} = V_S \cdot \left(1 - \frac{m \cdot R_D}{2}\right)$$

Q6

0 points possible (ungraded)

Here we analyze the time response of the circuit in Figure 6-1 which contains capacitive and resistive elements and a voltage source, V_S. The voltage source is switched between two nodes in the circuit, and we observe the voltage response across C_1. All answers in this problem are looking for expressions in terms of V_S, C_1, C_2, R_1, and R_2.

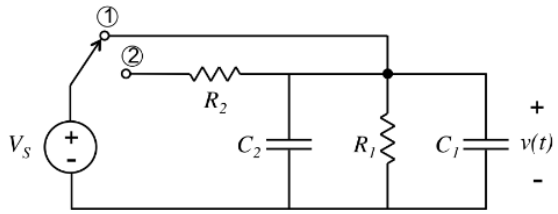


Figure 6-1

Initially for $t < 0$ the switch connects the voltage source, V_S to node 1 and the circuit is allowed to reach steady-state. What is the steady-state voltage, $v\,(t)$, across C_1 for $t < 0$?

VS

✔ **Answer:** VS

V_S

At $t = 0$, the switch is repositioned to connect the voltage source to node 2 and the circuit is allowed to reach steady-state again. What is the voltage, $v\,(t)$, across C_1 after the circuit reaches steady-state?

VS*R1/(R1+R2)

✔ **Answer:** VS*R1/(R1+R2)

$$V_S \cdot \frac{R_1}{R_1 + R_2}$$

We can use differential equations to write an expression for the voltage, $v\,(t)$, across C_1 for $t > 0$. The homogeneous and particular solutions can be used to express the voltage, $v\,(t) = H * e^{-t/\tau} + P$. Give expressions for H, P and τ.

τ

(C1+C2)*R1*R2/(R1+R2)

✔ **Answer:** (C1+C2)*R1*R2/(R1+R2)

$$(C_1 + C_2) \cdot R_1 \cdot \frac{R_2}{R_1 + R_2}$$

P

VS*R1/(R1+R2)

✔ **Answer:** VS*R1/(R1+R2)

$$V_S \cdot \frac{R_1}{R_1 + R_2}$$

H

VS*R2/(R1+R2)

✔ **Answer:** VS*R2/(R1+R2)

$$V_S \cdot \frac{R_2}{R_1 + R_2}$$

Explanation:
First, to find the steady state voltage across C_1 for $t < 0$, we realize capacitors act like open circuits in steady state.
Therefore, a simple KVL loop around C_1 confirms the answer:

Therefore, a simple KVL loop around C_1 confirms the answer:

$$v = V_S$$

When the switch is connected to node 2, we now realize that, in steady state, we will have a voltage divider between R_2 and R_1. Therefore:

$$v = V_S \cdot \frac{R_1}{R_1 + R_2}$$

To find the time constant τ , we can first reduce the two capacitors in parallel to one equivalent capacitor of capacitance $C_{TOT} = C_1 + C_2$. Then we find the equivalent resistance as seen through the terminals of that capacitor, which is $R_1 || R_2$. So the time constant is:

$$\tau = (R_1 || R_2) \cdot C_{TOT} = (C_1 + C_2) \cdot \frac{R_1 \cdot R_2}{R_1 + R_2}$$

The particular solution P is identical to the steady state voltage:

$$P = V_S \cdot \frac{R_1}{R_1 + R_2}$$

To find the homogeneous solution, H, we can simply plug in $t = 0$ into the given generic expression, and set it equal to its known initial value, which is V_S. We get:

$$H = V_S \cdot \frac{R_2}{R_1 + R_2}$$

Q7

0 points possible (ungraded)

The startup company TransGadget has also invented a MOS-gated transistor called SuperT, with the symbol and terminal voltage-current characteristics given below.

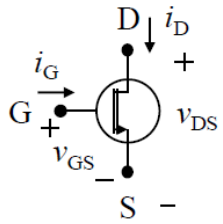


Figure 7-1

$$i_G = 0$$

$$i_D = \begin{cases} 0 & \text{if } v_{GS} < 0 \\ f \cdot (v_{GS})^3 & \text{if } v_{GS} \geq 0 \end{cases}$$

Engineers of TransGadget build a common source amplifier using SuperT as shown below.

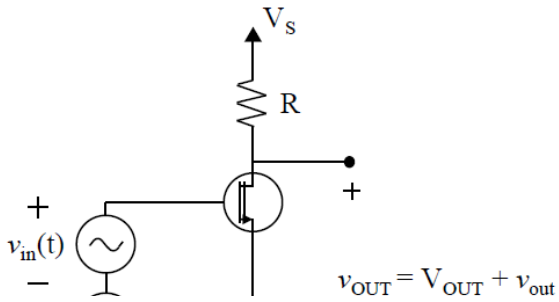


Figure 7-2

Here, $V_S = 100V$, $R = 1k\Omega$, and the transistor parameter $f = 1\frac{mA}{V^3}$. The amplifier is biased with $V_{IN} = 4V$.

What is the dc operating point (bias) output voltage V_{OUT} (in Volts) of this amplifier?

36 ✔ **Answer:** 36

What is the small signal gain ($\frac{v_{out}}{v_{in}}$) of this amplifier when it is biased as above?

-48 ✔ **Answer:** -48

Explanation:
We begin this problem by defining the overall input voltage v_{IN} and overall output voltage v_{OUT} as the summation of their large signal V_{IN} and V_{OUT} and their small signal v_{in} and v_{out} parts:

$$v_{IN} = V_{IN} + v_{in}$$
$$v_{OUT} = V_{OUT} + v_{out}$$

By inspection, we note that the source of the device connected to ground giving the relation:

$$v_{GS} = v_{IN}$$

Considering the drain and source of the device in series with the resistor R gives the second equation:

$$v_{DS} = v_{OUT} = V_S - i_D \cdot R$$

Substituting the device relations between v_{GS} and i_D combines these two equations to give a single relation:

$$v_{OUT} = V_S - R \cdot f \cdot (v_{IN})^3$$

To answer the first part of this question, we ignore the small-signal components so that $v_{IN} = V_{IN}$ and $v_{OUT} = V_{OUT}$. With $V_S = 100V$, $R = 1k\Omega$, $f = 1mA/V^3$ and $V_{IN} = 4V$, the dc operating point output voltage is:

$$V_{OUT} = (100V) - (1k\Omega) \cdot (1\frac{mA}{V^3}) \cdot (4V)^3 = 36V$$

In the second part of the question, the small signal gain is known to be the gradient of the v_{OUT}/v_{IN} characteristic, which can be obtained by simple differentiation:

$$\frac{dv_{OUT}}{dv_{IN}} = -3 \cdot R \cdot f \cdot (v_{IN})^2$$

Making the approximation that the small-signal component is negligible in determining its own gain:

$$v_{IN} = V_{IN} + v_{in} \approx V_{IN}$$

We can write:

$$\frac{v_{out}}{v_{in}} = -3 \cdot R \cdot f \cdot (V_{IN})^2.$$

With $R = 1k\Omega$, $f = 1\frac{mA}{V^3}$ and $V_{IN} = 4V$, the small signal gain is:

$$\frac{v_{out}}{v_{in}} = -3 \cdot (1k\Omega) \cdot (1\frac{mA}{V^3}) \cdot (4V)^2 = -48.$$