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## Week 3

S5 - Inside the Gate

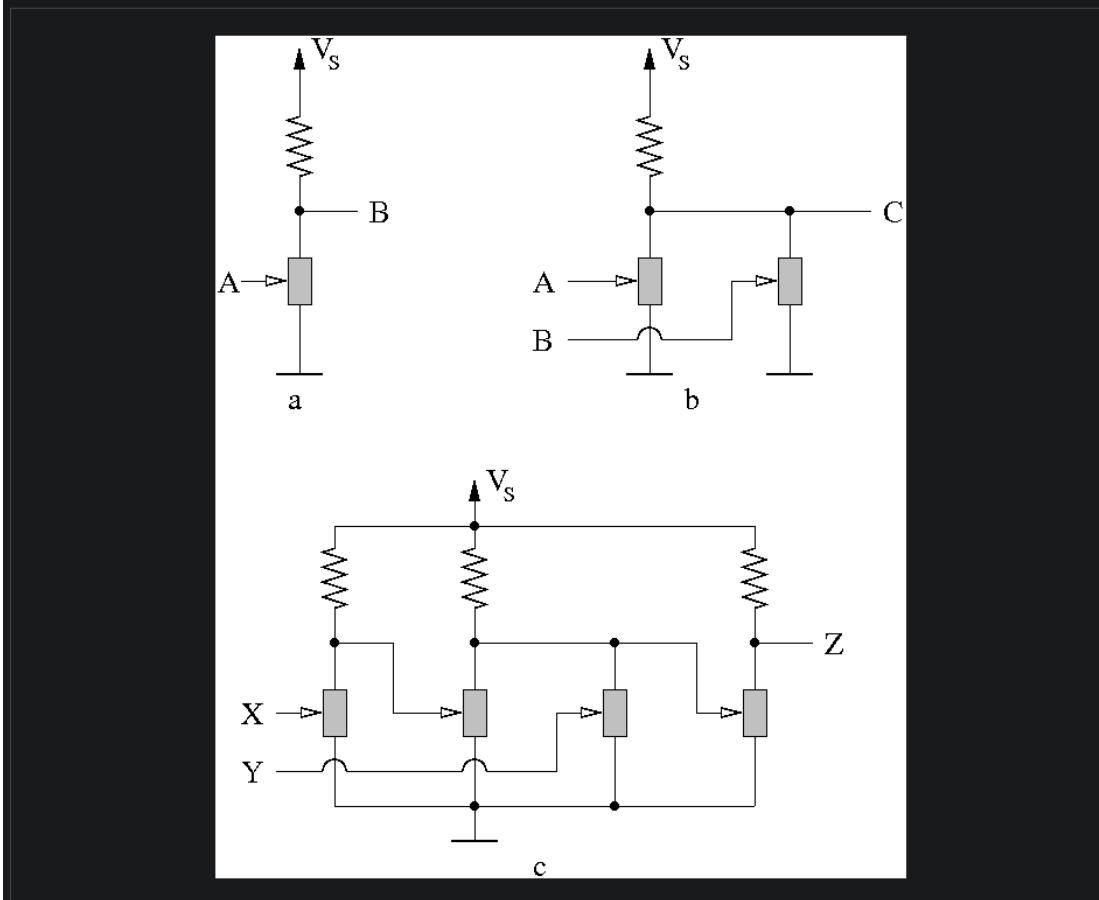
S6 - Circuits with Nonlinear Elements

Lectures

## S5E1: Logic with Switches

0 points possible (ungraded)

In the figure shown there are three circuits. The first two, labeled "a" and "b", are an inverter and a NOR gate, respectively. Circuit "c" is a bit more complex.



In the spaces provided below give the logical output at  $Z$  as a function of the inputs at  $X$  and  $Y$ .

When  $X=0$  and  $Y=0$ ,  $Z=$

✓ Answer: 1

When  $X=0$  and  $Y=1$ ,  $Z=$

✓ Answer: 1

When  $X=1$  and  $Y=0$ ,  $Z=$

✓ Answer: 0

When  $X=1$  and  $Y=1$ ,  $Z=$

✓ Answer: 1

```
In[®]:= ! ! (! x || y) // Simplify
```

```
Boole[BooleanTable[{x, y, ! x || y}, {x, y}]] // TableForm
```

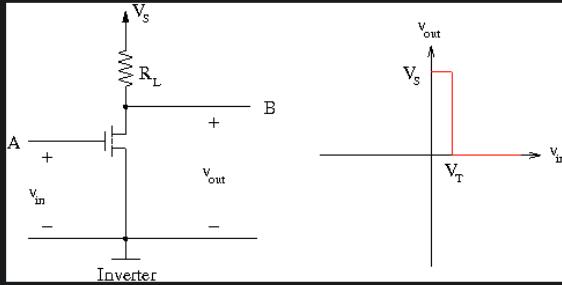
Out[®]=  $\neg x \mid\mid y$

Out[®]/TableForm=

1	1	1
1	0	0
0	1	1
0	0	1

### S5E2: Switch Model

0 points possible (ungraded)



The graph shows the input/output behavior of the inverter, given the S-model (perfect switch model) of the MOSFET. The inverter shown must meet the static discipline:  $0 \leq V_{OL} < V_{IL} < V_{IH} < V_{OH} \leq V_S$

The required discipline is:  $V_{OL} = 0.32V$ ,  $V_{IL} = 0.5760000000000001V$ ,  $V_{IH} = 2.6240000000000006V$ ,  $V_{OH} = 2.88V$ , and  $V_S = 3.2V$ .

For what values of the MOS threshold  $V_T$  can the design satisfy the static discipline?

What is the minimum possible value of  $V_T$  (in Volts)?

✓ Answer: 0.5760000000000001

What is the maximum possible value of  $V_T$  (in Volts)?

✓ Answer: 2.6240000000000006

### S5E3: SR Model

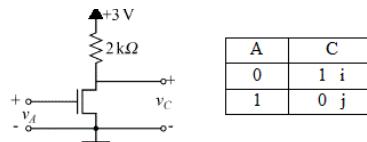
0 points possible (ungraded)

For this problem, consider the convention that a logical one corresponds to a high voltage level and a logical zero corresponds to a low voltage level. Thus, when the voltage  $v_A$  associated with the Boolean variable A is high, A is one. When  $v_A$  is low, A is zero. The same holds for  $v_B$  and B, and  $v_C$  and C. Assume also the following:

- The high voltage level is much greater than the threshold voltage,
- The "on" resistance of the MOSFET is  $50.0\Omega$ ,
- The "off" resistance of the MOSFET is  $10M\Omega$ .

For each of the following diagrams we provide a corresponding truth table. You will provide the value of the output voltage  $v_C$  for each row of the table. We will refer to a row by an index placed next to the logical value of C in the table.

--	--	--	--



A	C
0	1 i
1	0 j

What is the value of  $v_C$  (in Volts) at entry i?

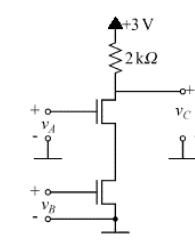
2.9994

✓ Answer: 2.9994001199760048

What is the value of  $v_C$  (in Volts) at entry j?

0.0731707

✓ Answer: 0.07317073170731708



A	B	C
0	0	1 k
0	1	1 l
1	0	1 m
1	1	0 n

What is the value of  $v_C$  (in Volts) at entry k?

2.9997

✓ Answer: 2.9997000299970003

What is the value of  $v_C$  (in Volts) at entry l?

2.9994

✓ Answer: 2.9994001199760048

What is the value of  $v_C$  (in Volts) at entry m?

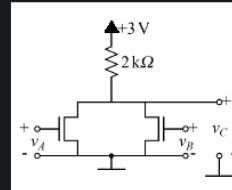
2.9994

✓ Answer: 2.9994001199760048

What is the value of  $v_C$  (in Volts) at entry n?

0.142857

✓ Answer: 0.14285714285714285



A	B	C
0	0	1 o
0	1	0 p
1	0	0 q
1	1	0 r

What is the value of  $v_C$  (in Volts) at entry o?

2.9988

✓ Answer: 2.998800479808077

What is the value of  $v_C$  (in Volts) at entry p?

0.0731704

✓ Answer: 0.07317073170731708

What is the value of  $v_C$  (in Volts) at entry q?  
 ✓ Answer: 0.07317073170731708

What is the value of  $v_C$  (in Volts) at entry r?  
 ✓ Answer: 0.037037037037037035

```
In[1]:= Vs = 3; Rl = 2^3; Ron = 50; Roff = 10^6;
Rp[r_List] := 1 / Total[1 / r];
(*NOT gate*)
i = Vs *  $\frac{Roff}{Roff + Rl}$  // N
j = Vs *  $\frac{Ron}{Ron + Rl}$  // N
(*NAND*)
k = Vs *  $\frac{2 Roff}{2 Roff + Rl}$  // N
l = Vs *  $\frac{Ron + Roff}{Ron + Roff + Rl}$  // N
m = l
n = Vs *  $\frac{2 Ron}{2 Ron + Rl}$  // N
(*NOR*)
o = Vs *  $\frac{Rp[\{Roff, Roff\}]}{Rp[\{Roff, Roff\}] + Rl}$  // N
p = Vs *  $\frac{Rp[\{Ron, Roff\}]}{Rp[\{Ron, Roff\}] + Rl}$  // N
q = p
r = Vs *  $\frac{Rp[\{Ron, Ron\}]}{Rp[\{Ron, Ron\}] + Rl}$  // N
```

Out[1]= 2.9994

Out[1]= 0.0731707

Out[1]= 2.9997

Out[1]= 2.9994

Out[1]= 2.9994

Out[1]= 0.142857

Out[1]= 2.9988

Out[1]= 0.0731704

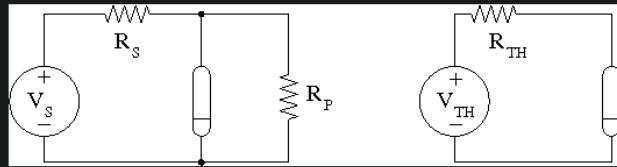
Out[1]= 0.0731704

Out[<sup>6</sup>] = 0.037037

## S6E0: Thevenin isolates nonlinear element

0 points possible (ungraded)

If we want to study the behavior of a circuit with linear resistors, independent sources, and an unfamiliar, perhaps nonlinear, element, it is to our advantage to package up everything but the unfamiliar element into a Thevenin or Norton model, so we can concentrate on the interaction of this simply-characterized circuit with the unfamiliar element. For example, the circuit on the left of the diagram can be summarized, from the point of view of the unfamiliar element, by the circuit on the right.



In the space provided, write the algebraic expressions for the Thevenin voltage and resistance.

 $V_{TH} =$ 

$$RP*VS/(RS+RP)$$

✓ Answer: RP\*VS/(RS+RP)
 $R_{TH} =$ 

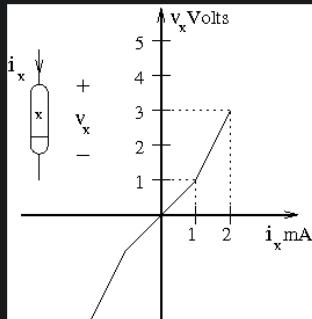
$$RS*RP/(RS+RP)$$

✓ Answer: RS\*RP/(RS+RP)

### S6E1: A Nonlinear Element

0 points possible (ungraded)

Lem E. Tweakit had a problem. He bought a mystery apparatus at an electrical flea market. One element in the apparatus was unmarked and not obviously identified, but when he measured its behavior in a curve tracer he found that it was a nonlinear resistor with the characteristic shown in the figure:



Lem was afraid to test this device with a current greater than 2mA.

What is the resistance (in kOhms) when the current is small: less than 1mA?

1

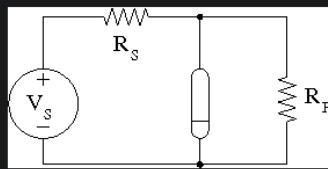
✓ Answer: 1

What is the resistance (in kOhms) when the current is outside that range? (Note that this refers to the incremental resistance, which relates an incremental change in voltage to an incremental change in current.)

2

✓ Answer: 2

In the circuit that Lem found this the strange element, it was connected to a power supply of  $V_s = 5.0V$  with a series resistance of  $R_s = 4700.0\Omega$  and it was shunted with a parallel resistance of  $R_p = 8200.0\Omega$ .



What is the current (in Amperes) through the strange object when it is in operation in the circuit?

0.00079

✓ Answer: 0.0007970451010886469

What is the voltage (in Volts) across the strange object when it is in operation in the circuit?

0.79

✓ Answer: 0.7970451010886469

```
In[1]:= (*Values are in kOhm, because current is in mA*)
1
3 - 1
-----
2 - 1
(*From above, we have two choices for the resistance, namely:
 1 kOhm (current should be [-1,1]mA) or
 2 kOhm (current should be [1,2]mA or [-2,-1]mA*)
```

$V_s = 5$ ;  $R_s = 4700$ ;  $R_p = 8200$ ;

```
(*From previous question*)
vth =  $\frac{R_p * V_s}{R_s + R_p}$ ;
rth =  $\frac{R_s * R_p}{R_s + R_p}$ ;
(*The unknown element (resistance rx) is in
series with the Thévenin resistor. Try rx=2 kOhm first*)
rx = 2*^3;
i =  $\frac{vth}{rth + rx}$ ;
(*Does not give current in the valid range, so try rx=1 kOhm*)
rx = 1*^3;
i =  $\frac{vth}{rth + rx}$  // N
v = i * rx // N
```

Out[1]= 1

Out[2]= 2

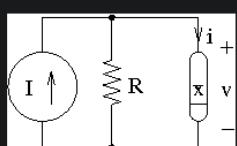
Out[3]= 0.000797045

Out[4]= 0.797045

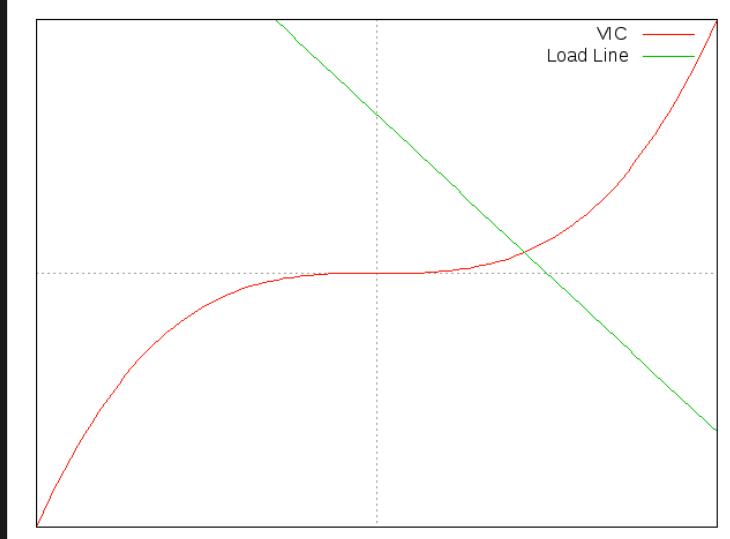
### S6E2: Load Line

0 points possible (ungraded)

In the circuit shown, the strange nonlinear device is specified to have the characteristic  $i = (1A/V^3) \cdot v^3$ . (Note that  $A/V^3$  represents the unit "amps per cubic volt". Admittedly, it is hard to find a device with this kind of characteristic in your junkbox.) The current supplied by the current source is  $I = 4.0A$ , and the resistance of the parallel resistor is  $R = 8.2\Omega$ .



In the graph the horizontal axis is the voltage across the nonlinear device and the vertical axis is the current through the device. The curve is the voltage-current characteristic of the device and the straight line is the load line.



(NOTE: The curves are not to scale and are used to exhibit the intersection indicating the operating point.)

What is the current (in Amperes) where the load line intercepts the vertical axis?

4

✓ Answer: 4.0

What is the voltage (in Volts) where the load line intercepts the horizontal axis?

32.8

✓ Answer: 32.8

Hint: use guess and check to solve for the operating point.

What is the operating voltage (in Volts) of the device in this circuit?

1.5618

✓ Answer: 1.5617947578430176

What is the operating current (in Amperes) of the device in this circuit?

3.80954

✓ Answer: 3.8095342488502437

Submit

Show answer

$\ln[=]:= r = 8.2;$

(\*Load line is  $v = (4 - i)r$ . Can get this from Norton method  
Keep in mind that  $i$  has reversed direction thus negative sign\*)

```
(*y-intercept*)
Solve[0 == (4 - i) r, i]
(*x-intercept*)
Solve[v == 4 r, v]
(*Operating point*)
Solve[v == (4 - i) r && i == v^3, {v, i}, Reals]
```

*Out[6]=* { { $i \rightarrow 4.$  } }

*Out[7]=* { { $v \rightarrow 32.8$ } }

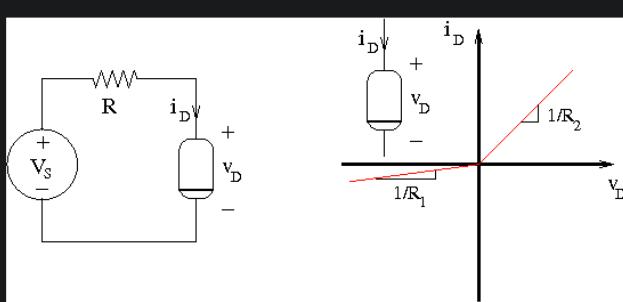
**Solve:** Solve was unable to solve the system with inexact coefficients. The answer was obtained by solving a corresponding exact system and numericizing the result.

*Out[8]=* { { $v \rightarrow 1.5618$ ,  $i \rightarrow 3.80954$ } }

### S6E3: Piecewise Linear

0 points possible (ungraded)

The characteristic of the nonlinear element shown in the circuit is made up of two linear segments. The resistance of one segment is  $R_1 = 1.0M\Omega$  and the resistance of the other segment is  $R_2 = 1.0\Omega$ . (Of course, the graph is not to a uniform scale. If it were, we would not see the slope of the segment with slope  $1/R_1$ .)



In the circuit, the resistor  $R = 1.2k\Omega$ .

If the voltage source has strength  $V = 9.0V$ , what is the current  $i_D$  (in Amperes)?

0.00749376

**Answer:** 0.00749375520399667

And what is the voltage  $v_D$  (in Volts)?

0.00749376

**Answer:** 0.00749375520399667

However, suppose the voltage source has strength  $V = -9.0V$ , what is now the current  $i_D$  (in Amperes)?

-8.98921e-6

**Answer:** -8.98921294446664e-06

And, in this case, what is the voltage  $v_D$  (in Volts)?

-8.98921

**Answer:** -8.98921294446664

```
r1 = 1*^6; r2 = 1; R = 1.2*^3;
(*There is just one current across all elements in series,
so we simply use Ohms law.*)
```

```
(*In this regime, resistance of nonlinear element is R2*)
V = 9;
id = V / (R + r2)
vd = id * r2
```

```
(*In this regime, resistance of nonlinear element is R1*)
V = -9;
id = V / (R + r1)
vd = id * r1
```

Out[=] 0.00749376

Out[=] 0.00749376

Out[=]  $-8.98921 \times 10^{-6}$

Out[=] -8.98921

## Homework

MITx 6.002.1x  
Circuits and Electronics 1: Basic Circuit Analysis

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### Homework 3

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Homework due Jul 26, 2022 02:56 +04 Completed

H3P1: A Logic Family

9/9 points (graded)

For many purposes of gate design, we can model a MOSFET used as a switch simply as an ideal switch and an "on-state resistor"  $R_{ON}$ . This is the SR model.

Assuming this model for the MOSFET, consider the inverter in the figure. This inverter is intended to be used as an element in a logic family with NAND and NOR gates.

The diagram shows three circuit models for logic gates. 
 1. Inverter: A single NMOS transistor with its drain terminal connected to the output node C. The source terminal is connected to ground. The gate terminal is connected to the input node A. A resistor  $R_{PD}$  is connected between the drain of the NMOS transistor and the output node C.
 2. NAND gate: Two NMOS transistors in series. Their drains are connected to the output node C. Their sources are connected to ground. Their gates are connected to the inputs A and B respectively. A resistor  $R_{PD}$  is connected between the drain of the top NMOS transistor and the output node C.
 3. NOR gate: Three NMOS transistors in parallel. Their drains are connected to the output node C. Their sources are connected to ground. Their gates are connected to the inputs A, B, and C respectively. A resistor  $R_{PD}$  is connected between the drain of the top NMOS transistor and the output node C.

The static discipline required for this family is:

$$V_S = 5.0\text{V}, V_{OH} = 4.5\text{V}, V_{IH} = 4.0\text{V}, V_{IL} = 1.5\text{V}, V_{OL} = 1.0\text{V}.$$

What is the low noise margin (in Volts)?

0.5

✓ Answer: 0.5

What is the high noise margin (in Volts)?

0.5

✓ Answer: 0.5

What is the width of the forbidden region (in Volts)?

2.5

✓ Answer: 2.5

Suppose that the threshold voltage for the MOSFET is  $V_T = 2.0\text{V}$  and  $R_{ON} = 7000.0\Omega$ .

What is the minimum value of the pullup resistor  $R_{PUI}$  (in Ohms) for which this inverter can obey the required static discipline?

28000

✓ Answer: 28000.0

Now, consider the NAND gate of this family. What is the minimum value of the pullup resistor  $R_{PNA}$  (in Ohms) for which this inverter can obey the required static discipline?

56000

✓ Answer: 56000.0

How about the NOR gate of this family. What is the minimum value of the pullup resistor  $R_{PNO}$  (in Ohms) for which this inverter can obey the required static discipline?

28000

✓ Answer: 28000.0

Assume that we implemented this family with the minimum pullup resistors that you have already calculated.

What is the maximum power (in Watts) consumed by the inverter?

0.000714286

✓ Answer: 0.0007142857142857143

What is the maximum power (in Watts) consumed by the NAND?

0.000357143

✓ Answer: 0.00035714285714285714

What is the maximum power (in Watts) consumed by the NOR?

0.000793651

✓ Answer: 0.0007936507936507937

#### Explanation:

$$V_S = 5.0 \text{V} \quad V_{OH} = 4.5 \text{V} \quad V_{IH} = 4.0 \text{V} \quad V_{IL} = 1.5 \text{V} \quad V_{OL} = 1.0 \text{V}$$

The low noise margin is defined as  $V_{IL} - V_{OL}$ . For this problem, it is  $0.5\text{V}$ . As an example, if an inverter outputs a valid voltage signal of  $1.0\text{V}$  ( $V_{OL}$ ) to another inverter, then that signal can rise by  $0.5\text{V}$  all the way to  $V_{IL}$ , before it becomes an invalid logical 0 input to the second inverter.

The high noise margin is defined as  $V_{OH} - V_{IH}$ . For this problem, it is  $0.5\text{V}$ . Again, if an inverter outputs a valid voltage signal of  $4.5\text{V}$  ( $V_{OH}$ ) to another inverter, then that signal can fall by  $0.5\text{V}$ , all the way to  $V_{IH}$  before it becomes an invalid logical 1 input to the second inverter.

The width of the forbidden region is defined as  $V_{IH} - V_{IL}$ . For this problem, it is  $2.5\text{V}$ . Valid inputs to our logic family are not allowed to fall between  $V_{IH}$  and  $V_{IL}$ .

When  $V_{GS}$  for the MOSFET is below  $V_T$ , the MOSFET behaves like an open circuit, and  $i_{DS} = 0$ . That means no voltage drops over  $R_{PUI}$  and the output voltage of our inverter is  $V_S$ , so this case is fine with out static discipline, since the output voltage is above  $V_{OH}$ . For  $V_{GS} \geq V_T$ , the MOSFET is on and behaves like a resistor with resistance  $R_{ON}$  with our model. To find  $R_{PUI}$ :

$$V_{OL} = \frac{V_S (R_{ON})}{R_{ON} + R_{PUI}}$$

$$1 = \frac{5 (7000.0)}{(7000.0 + R_{PUI})} \rightarrow R_{PUI} = 28000.0\Omega$$

Similar to the inverter case, when either MOSFET is off, no current can flow through the pullup resistor because the MOSFETs and pullup resistor are in series. So  $V_{OUT}$  for the NAND gate is simply  $V_S$  when either MOSFET is off. When both MOSFETs are on, they behave like resistors with resistance  $R_{ON}$ . The two MOSFETs are in series, so we calculate:

To find  $R_{PNA}$ :

$$V_{OL} = \frac{V_S (2R_{ON})}{2R_{ON} + R_{PNA}}$$

$$1 = \frac{5 (14000.0)}{(14000.0 + R_{PNA})} \rightarrow R_{PNA} = 56000.0\Omega$$

When both MOSFETs are off,  $V_{OUT}$  for the NOR gate is simply  $V_S$  because no current can flow through either MOSFET or  $R_{PNO}$ . When one MOSFET is on,  $V_{OUT}$  is:

$$V_S \cdot \frac{(0.5) R_{ON}}{(0.5) R_{ON} + R_{PNO}}$$

because the MOSFETs are in parallel with each other. For the cases with one MOSFET on or both MOSFETs on,  $V_{OUT}$  must be at least as small as  $V_{OL}$ . For the case with one MOSFET on,  $R_{PNO}$  must be at least  $28000.0\Omega$ . For the case with both

MOSFETs on,  $R_{PUO}$  must be at least 14000.0  $\Omega$ . So for our NOR gate to satisfy the static discipline,  $R_{PUO}$  must be at least 28000.0  $\Omega$ .

When the MOSFET in the inverter is off, no power is consumed because no current can flow as the MOSFET behaves like an open circuit. When it is on,  $V_S$  must drop over  $R_{PUI}$  and  $R_{ON}$ , so the power consumed is:

$$\frac{(V_S)^2}{R_{PUI} + R_{ON}}$$

Power consumed by inverter:

$$\frac{25V}{7000.0 + 28000.0\Omega} = 0.000714W$$

When either MOSFET is off, no current flows through the MOSFETs or  $R_{PUA}$ , so there is no power consumed. When both MOSFETs are on,  $V_S$  must drop over  $R_{PUA}$  and  $2R_{ON}$  because the MOSFETs are in series with each other. The power consumed in this case is:

$$\frac{(V_S)^2}{R_{PUA} + 2R_{ON}}$$

Power consumed by NAND:

$$\frac{25V}{2 \cdot 7000.0 + 56000.0\Omega} = 0.000357W$$

When both MOSFETs are off, no current can flow, so no power is consumed. When one MOSFET is on,  $V_S$  must drop over  $R_{PUO}$  and  $R_{ON}$ , so the power consumed is:

$$\frac{(V_S)^2}{R_{PUO} + R_{ON}}$$

When both MOSFETs are on,  $V_S$  must drop over  $R_{PUO}$  and  $\frac{1}{2} R_{ON}$  because the MOSFETs are in parallel, so the power consumed is:

$$\frac{(V_S)^2}{R_{PUO} + 0.5(R_{ON})}$$

The maximum power is consumed by the NOR gate in the latter case:

$$\frac{25V}{(7000.0 \parallel 7000.0) + 28000.0\Omega} = 0.000794W$$

You have used 3 of 25 attempts

|

Answers are displayed within the problem

### H3P2: Graphical Inverter Model

7/7 points (graded)

A calculator uses digital logic to perform math functions, but a calculator was malfunctioning and not adding correctly. After much debugging, we discovered there was an inverter that had been malfunctioning. To fix the calculator we need to replace the inverter with a new one. We can draw our calculator as the system shown in Figure 1, where Network A has an output that is the input to our inverter and the output of the inverter is the input to Network B.

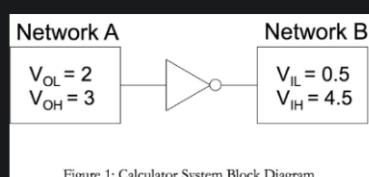
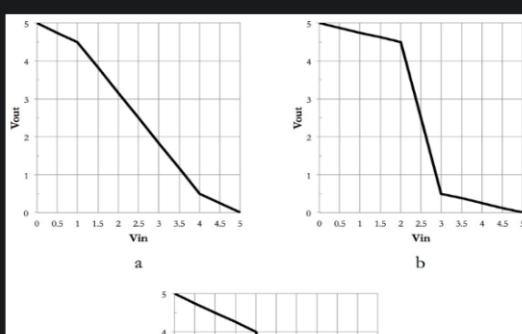


Figure 1: Calculator System Block Diagram

Figure 1 shows the relevant static disciplines for Networks A and B. Figure 2 shows the graphical models for three inverters.



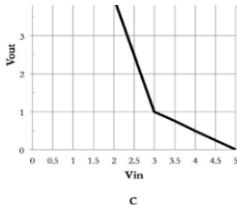


Figure 2: Inverter Graphical Models

Which one will ensure we invert correctly according to the static disciplines of the two networks? Enter the letter label of the correct inverter.

✓ Answer: B

Give the minimum value of  $V_{IL}$  (in Volts) for the inverter to ensure correct operation.

✓ Answer: 2

Give the maximum value of  $V_{IH}$  (in Volts) for the inverter to ensure correct operation.

✓ Answer: 3

Give the maximum value of  $V_{OL}$  (in Volts) for the inverter to ensure correct operation.

✓ Answer: 0.5

Give the minimum value of  $V_{OH}$  (in Volts) for the inverter to ensure correct operation.

✓ Answer: 4.5

What is the high noise margin,  $NM_H$  (in Volts), from the minimum and maximum values that you obtained?

✓ Answer: 1.5

What is the low noise margin,  $NM_L$  (in Volts), from the minimum and maximum values that you obtained?

✓ Answer: 1.5

#### Explanation:

We want the inverter to convert signals of "1" from network A to "0" in network B and vice-versa. According to the static discipline of network A, output voltages lower than  $2V$  will represent "0" and output voltages higher than  $3V$  will represent "1". Network B, on the other hand, will interpret inputs lower than  $0.5V$  as "0" and anything higher than  $4.5V$  as "1".

Now let's see how each of the transfer curves behaves. Graph "a" doesn't work out because when a signal anywhere from  $1V$  to  $2V$  gets sent by network A, the inverter converts this to something in the range of approximately  $4.5V$  to  $3.2V$  which doesn't get interpreted as a "1" by network B. Same logic applies for voltages in the range of  $3V$  to  $4V$  from network A.

Graph "c" doesn't meet our need for same reason as with graph "a". Say network A sends a valid output signal of  $3.5V$  it gets converted to approximately  $0.75V$  which doesn't lead to a "0" in network B.

This leaves us with graph "b" which satisfies our constraints.

The minimum value of  $V_{IL}$  is same as Networks A's  $V_{OL}$  since we want anything less than that to be interpreted by the inverter as a low input

The maximum value of  $V_{IH}$  is same as network A's  $V_{OH}$  since we want anything higher than that to be interpreted as a high input by the inverter

The maximum value of  $V_{OL}$  is same as Networks B's  $V_{IL}$  because signals higher than this would not be interpreted by network B as valid low inputs.

The minimum value of  $V_{OH}$  is same as Networks B's  $V_{IH}$  because signals lower than this would not be interpreted by network B as valid high inputs.

$$NM_H = V_{OH} - V_{IH} = 4.5 - 3 = 1.5V$$

$$NM_L = V_{IL} - V_{OL} = 2 - 0.5 = 1.5V$$

You have used 2 of 25 attempts

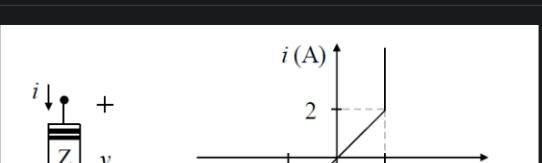
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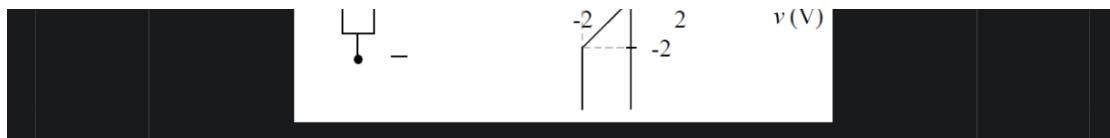
Answers are displayed within the problem

#### H3P3

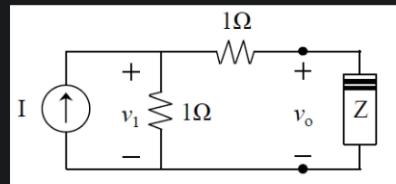
4/4 points (graded)

A nonlinear device Z has the i-v relationship shown below.





This device is used in the circuit shown below, where "I" is the value of the current source.



Assuming that  $I = 10A$ , what is the value of the voltage  $v_o$  (in Volts)?

2

✓ Answer: 2

Now assuming that  $I = -3A$ , what is the value of the voltage  $v_o$  (in Volts)?

-1

✓ Answer: -1

Finally, for the last two parts assume that  $I = 5A$ .

What is the value of the voltage  $v_o$  (in Volts)?

1.67

✓ Answer: 1.66

What is the value of the voltage  $v_1$  (in Volts)?

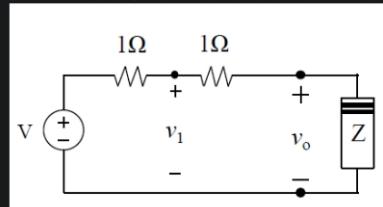
3.33

✓ Answer: 3.33

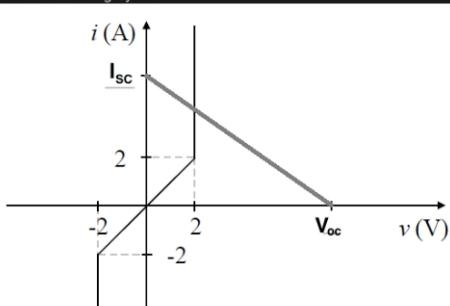
#### Explanation:

Observing the V-I chart for the non-linear device in this question, we see two distinct modes of operation. The device is in a "resistive mode" when the voltage across it is between 2V and -2V. In this mode, the device behaves like a simple  $1\Omega$  resistor, and obeys Ohm's law  $V = IR$ . Outside of this range, however, the device enters its "voltage limit mode", and becomes equivalent to a voltage source. Any additional current driven to the device will not increase its terminal voltage beyond 2V and -2V respectively.

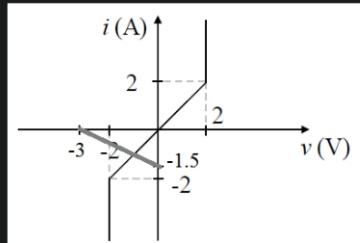
To determine whether the device is operating in its "resistive mode" or its "voltage limit mode", it is helpful to transform the circuit connected to its terminals into their Thevenin equivalent, in order to perform load line analyses. The current source on the left can be transformed via Norton / Thevenin equivalence into a voltage source and a resistor in series, with  $V = I \cdot 1\Omega$  and  $R = 1\Omega$ . The two series resistors can then be combined to form an overall Thevenin equivalent circuit of  $V = I \cdot 1\Omega$  and  $R = 2\Omega$ . This new circuit is shown below:



With the circuit drawn in its Thevenin equivalent, we can use load line analysis to determine the device's mode of operation in each part of the question. For the first part of the question,  $I = 10A$ , which gives an open circuit voltage  $V_{OC} = 10A \cdot 1\Omega = 10V$  and a short circuit current  $I_{SC} = V_{OC}/2\Omega = 5.0A$ . The load line for this circuit is as shown below as the thick gray line:



We can see at the intersection of the two lines, the non-linear device is operating in its "voltage limit mode", and so is restricted to having  $v_o = 2V$ .  
In the second part of the question,  $I = -3A$ , giving  $V_{OC} = -3V$  and  $I_{SC} = -1.5A$ . The load line for this circuit is shown below:



This time, the non-linear device is in its "resistive mode", and operates like a  $1\Omega$  resistor. Thinking of the three resistors as voltage dividers, we have  $v_o = -3V \div (1\Omega + 1\Omega + 1\Omega) \cdot 1\Omega = -1V$ .

In the last part of the question,  $I = 5A$ , giving  $V_{OC} = 5V$  and  $I_{SC} = 2.5A$ . By the same logic used in the previous sections, the non-linear device is operating in its "resistive mode". Once again considering the non-linear device as just another  $1\Omega$  resistor,  $v_o = 5 \div (1\Omega + 1\Omega + 1\Omega) \cdot 1\Omega = 1.66V$  and  $v_1 = 5 \div (3\Omega) \cdot (1\Omega + 1\Omega) = 3.33V$

Submit

You have used 10 of 25 attempts

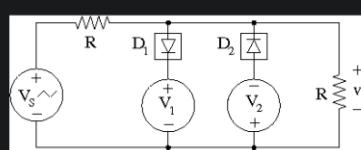
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 Answers are displayed within the problem

### H3P4: Diode Limiter

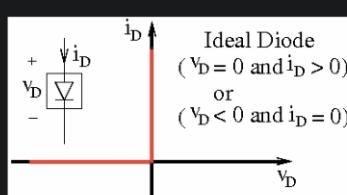
4/4 points (graded)

In the circuit shown there are two ideal diodes, two resistors, two DC voltage sources, and an AC voltage source.

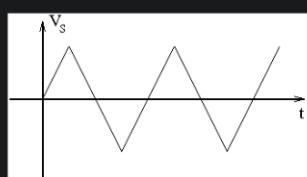


The resistors both have the resistance  $R = 5.6k\Omega$ . The voltage of the DC sources is  $V_1 = 3.25V$  and  $V_2 = 3.0V$ .

An ideal diode has the characteristic shown:



The AC voltage source puts out a symmetrical triangle wave that looks like:



The peak voltage of this waveform is 7.5V.

What is the maximum positive voltage (in Volts) that can appear at  $v$ ?

3.25

✓ Answer: 3.25

What is the minimum (negative) voltage (in Volts) that can appear at  $v$ ?

-3

✓ Answer: -3.0

What is the maximum current ( $A$ ) that can flow through diode D1?

What is the maximum current (in Amperes) that can go through diode  $D_1$ ?

0.000178571

✓ Answer: 0.00018

What is the maximum current (in Amperes) that can go through diode  $D_2$ ?

0.000267857

✓ Answer: 0.00027

**Explanation:**

The maximum positive voltage that can appear at  $v$  is limited by the source  $V_1$ .

$$V_{max} = 3.25$$

The maximum negative voltage that can appear at  $v$  is limited by the source  $V_2$ .

$$V_{min} = -3.0$$

Notice from the I-V characteristics of an ideal diode that the current through the diode  $i_D$  is always zero unless the voltage across the diode is  $0V$ . For diode  $D_1$ , this means that the voltage across it is  $0V$  and that  $v = V_1$ . This also means that no current flows through diode  $D_2$  when current can flow through  $D_1$  because the voltage across  $D_2$  is not zero. We can write KCL equations at the top-right node to get:

$$i_{D_1} = \frac{V_S - V_1}{R} - \frac{V_1}{R}$$

This is maximum when  $V_S = 7.5$  V. The maximum current that can go through diode 1 is:

$$i_{D_1} = \frac{V_{sPeak} - V_1 - V_1}{R} = \frac{7.5 - 3.25 - 3.25}{5600.0} = 0.00018A$$

As before, current can only go through a diode when the voltage drop across it is  $0V$ . This means that current only goes through  $D_2$  when  $v = -V_2$ . This also means no current goes through  $D_1$  because the voltage drop across it is non-zero. Writing KCL at the top-right node again, we get:

$$i_{D_2} = \frac{(-V_2) - V_S}{R} + \frac{-V_2}{R}$$

This is maximum when  $V_S = -7.5$  V. The maximum current that can go through diode 2 is:

$$i_{D_2} = \frac{-V_2 - -V_{sPeak} - V_2}{R} = \frac{-3.0 + 7.5 - 3.0}{5600.0} = 0.00027A$$

Submit

You have used 13 of 25 attempts

Save | Show answer

Answers are displayed within the problem

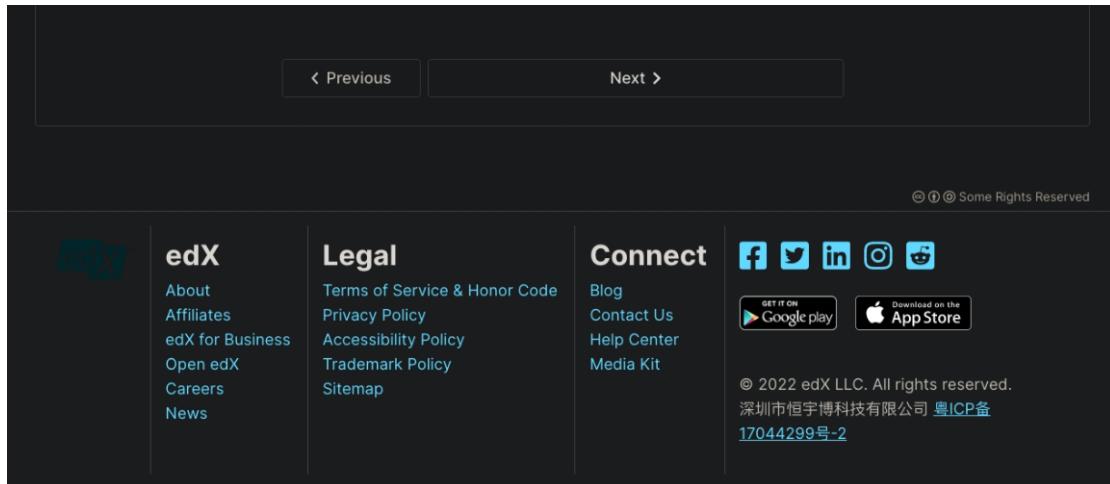
Discussion

Topic: Week 3 / Homework 3

Show Discussion

Calculator

Hide Notes



## Lab

The screenshot shows the 'Lab 3' page for the 'Circuits and Electronics 1: Basic Circuit Analysis' course. The page has a dark theme. At the top, it displays the course name 'MITx 6.002.1x Circuits and Electronics 1: Basic Circuit Analysis', the user 'venkatn93', and a 'Help' link. Below this is a navigation bar with tabs: Course (which is selected), Progress, Dates, Discussion, Notes, and FAQ. Underneath the navigation bar, the page title is 'Course / Week 3 / Lab 3'. There is a 'Previous' and 'Next' navigation bar at the top of the main content area. The main content starts with the heading 'Lab 3' and a 'Bookmark this page' link. It then shows a note: 'Lab due Jul 26, 2022 02:56 +04 Completed'. The lab title is 'Lab 3' and it is worth '1/1 point (graded)'. A note states: 'Your goal for this lab is to design a circuit that implements a 3-input logic gate that implements  $Z = \neg(C(A + B))$  where the  $\neg$  symbol stands for logical negation. This function is enumerated in the following truth table:' followed by three truth tables:

C	B	A		Z
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		1
1	0	1		0
1	1	0		0
1	1	1		0

C	B	A		Z
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		1
1	0	1		0
1	1	0		0
1	1	1		0

C	B	A		Z
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		1
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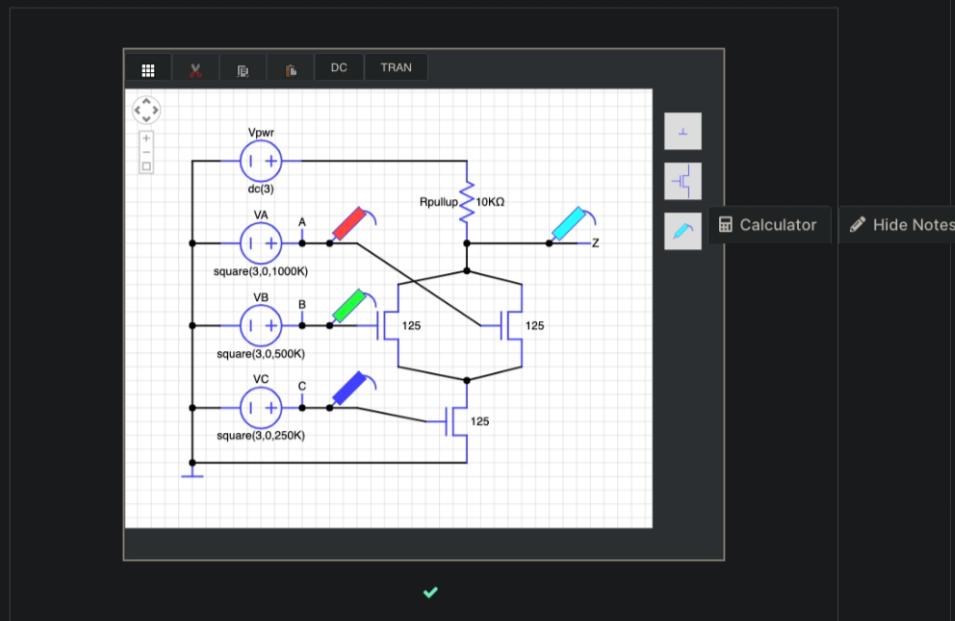
The schematic diagram below includes the resistive pullup for the logic gate and some voltage sources that serve as the power supply and generators for the signals that will be the inputs to the gate. The voltage sources generate the three input signals (A, B and C), timed so that all possible combinations of the inputs will be generated over a  $4\mu s$  interval.

Please add the appropriate pulldown network of mosfet switches connected to node Z to implement the truth table above, with  $R_{ON}$  of the mosfets chosen so that  $V_{dl}$  of the logic gate is less than  $0.25V$  for any combination of inputs. In the schematic tool, the mosfet model has  $V_{th} = 0.5V$ , so  $V_{dl} < 0.25V$  will ensure that when the output of the logic gate is 0, if it is used as the input to some other logic gate, the mosfet to which it connects will be off.

On Section 6.7 of the textbook (page 305) we see from Equation (6.4) that  $R_{ON} = R_n \frac{L}{W}$ . In the schematic tool, the mosfet model has  $R_n \approx 26.5k\Omega$  when using a  $3V$  power supply. To adjust  $R_{ON}$ , double click the mosfet and select an appropriate value for the W/L parameter. For example, setting a mosfet's W/L to 10 would result in  $R_{ON} = 2.65k\Omega$ .

Note that the "Plot offset" property of the scope probes on the A, B and C signals has been set so that the plots will not overlap, making it easier to see what's happening.

Please do not change the voltages of the voltage sources or the resistance of the pullup resistor.



When your circuit is ready for testing, run a  $4\mu s$  transient simulation to verify correct functionality and appropriate  $V_{dl}$  when the output of the gate is logic 0. To submit, please click CHECK. The checker will be verifying the voltage of the output node at several different times, so you'll earn a checkmark only *after* you've performed the transient simulation so that the checker will have a waveform to check!

Hint: you'll only need 3 mosfet switches to implement the gate.

When the gate is correctly implemented, the plot produced by the transient analysis should look similar to the following figure.

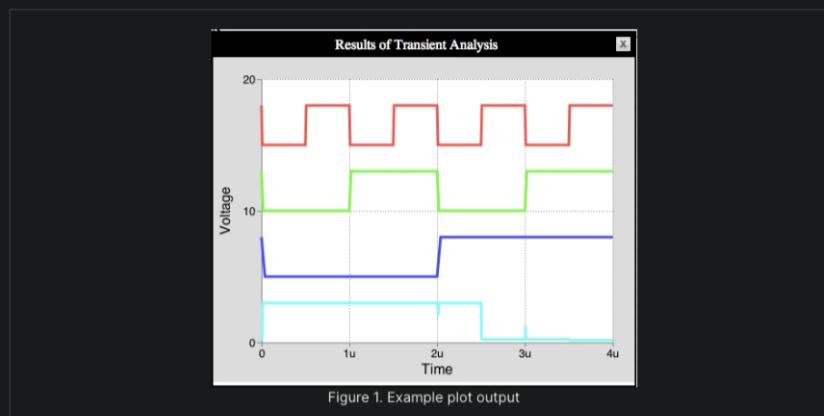


Figure 1. Example plot output

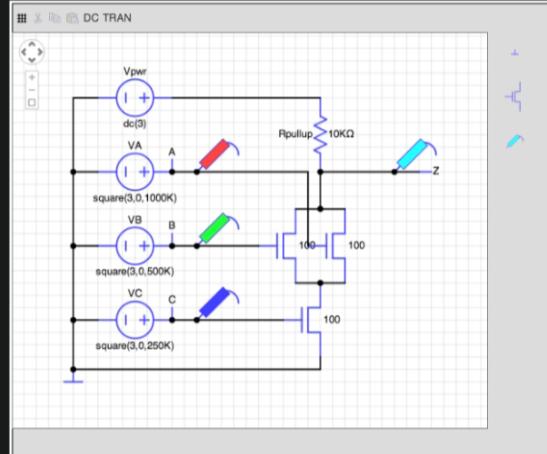
Food for thought: You'll notice there are little spikes, sometimes called *glitches*, in the output waveform (see the bottom cyan-colored waveform in Figure 1). These only occur when the A and B inputs are changing simultaneously and the C input is high. Can you explain why? Think about what is happening in the pulldown circuitry at the time the glitches occur.

Note: If you are getting the right answer and the system is marking it wrong, here are 6 things you can try.

- (1) Try a different browser. For example, if Chrome does not work well, try Firefox or Microsoft Edge.
- (2) Do not modify or replace any of the components that have been originally provided. For example the load resistor has been given. Therefore, you just need to provide the proper combination of MOSFETs which meet the given specifications.
- (3) Try clicking the "Reset" button at the bottom (next to "save", and below the "submit" button) to recover original circuit setup and then make the changes. Sometimes it is helpful to reset everything and start over.
- (4) Before you click the "submit" button, make sure that you have performed the correct transient analysis, and then keep up the window with the result.
- (5) Please verify that the values of all the LOW output states are less than 0.25V.
- (6) If you have any questions on 3-gate logic, please read the textbook Fig 6.25, page 295.

#### **Explanation:**

We are asked to implement the logic function  $\overline{C \cdot (A + B)}$ . This can be achieved with three transistors, as shown below; a series connection between  $C$  and  $(A + B)$  to implement the AND function, and a parallel connection between  $A$  and  $B$  to implement the OR function:



We are told that  $V_{DD} = 3V$  and that  $R_n = 26.5K\Omega$ . Furthermore, we are told that we are to use the switch-resistor model of the MOSFETs, treating them like resistors with resistances  $R_{ON}$  when they are given a high input.  $R_{ON}$  has the form  $R_{ON} = 26.5K \cdot \frac{L}{W}$ . We need to determine  $R_{ON}$  by choosing the ratio  $\frac{L}{W}$  such that  $V_{OL}$  is always  $< 0.25V$ . The first thing to do is to identify the scenario in which  $V_{OUT}$  takes on its maximum possible value in the context of a logical 0. This scenario corresponds to the worst-case  $V_{OL}$ . There must be a full conducting path from  $V_{OUT}$  to ground to have a logical 0, which imposes the first condition. And because  $V_{OUT}$  is in the middle of a voltage divider between  $R_{pullup}$  and the equivalent "on" resistance of the MOS-FETs, we should be able to convince ourselves that  $V_{OL}$  takes on its highest value whenever the equivalent resistance of the "on" MOSFET network is the LARGEST because it is still constrained by an existing conducting path from  $V_{DD}$  to ground.

existing conducting path from  $V_{OUT}$  to ground. Finding the largest combination of resistances is simple: if we replace "on" transistors with resistors of resistance  $R_{ON}$ , and "off" transistors with open circuits, we find the largest combination of resistance comes from a series connection between  $C$  and only one of  $A$  or  $B$ , but NOT both. This results in an equivalent resistance of  $R_{EQ} = 2 \cdot R_{ON}$ .

We now solve for REQ using the voltage divider formula:

$$\frac{V_{DD} \cdot R_{EQ}}{R_{pullup} + R_{EQ}} < 0.25$$

Plugging in our values, we end up with  $R_{ON} < 454.56$  as our constraint. Plugging in once more into the given form of  $R_{ON}$ , we end up with our final constraint on the transistor sizing:

$$\frac{W}{L} > 58.3$$

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**i** Answers are displayed within the problem.

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Lab 3 - some notes

## Lab 5 - Some notes

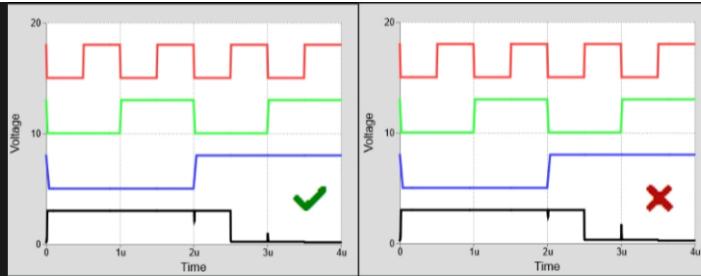
This problem has caused students some difficulties so if at first you don't succeed, try and try again.

Possibly getting the correct solution boils down to understanding why the left hand graph gets a green tick and the right hand graph gets a red cross.

Note that for improved legibility I have converted the colour of the  $y_{out}$  trace from cyan to black.

#### Results of Transient Analysis

## Results of Transient Analysis



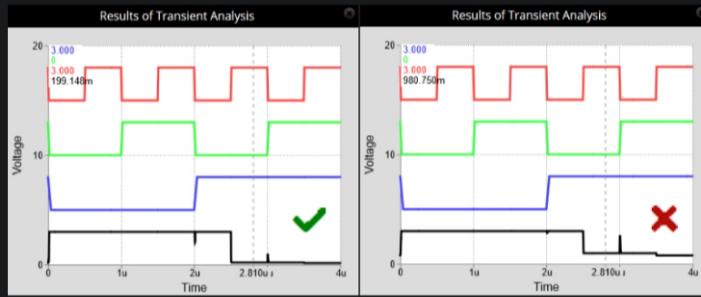
**Read no further before carefully inspecting the two graphs.**

Can you spot the subtle difference between the two graphs?

Read on.

One of the very useful feature of the Sandbox is that voltage readings can be made from the graph.

Passing the mouse cursor over the graph results in the voltages at a particular time being shown.



**Read no further before carefully inspecting the two graphs.**

Now can you spot the subtle difference between the two graphs?

Read on.

This illustrates one of the problems encountered by students in that they appear to get the correct output graphs but have actually not satisfied the  $v_{out}$  specification required for a LOW output,  $v_Z = v_{out} \leq 0.25V$ .

Note that  $\frac{W}{L} = 10$  is an example and in this lab you are required to find the value of  $\frac{W}{L}$  from a value of  $R_{ON}$  that you have evaluated to ensure that for LOW output  $v_Z = v_{out} \leq 0.25V$ .

Keep  $R_{pullup}$  at  $10\text{k}\Omega$ .

Using the truth table decide on the configuration of the three MOSFETS.

Note that connections between circuit elements can cross one another without making electrical contact.

You are interested in the last three entries of the truth table when  $Z = 0$  and this is when the condition  $v_Z = v_{out} \leq 0.25V$  must be satisfied.

C	B	A		Z
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		1
1	0	1		0
1	1	0		0
1	1	1		0

Which combination(s) of inputs that produce an output  $Z = 0$  result in the resistance between output  $Z$  and ground being the highest?

This configuration will produce the highest value of  $v_{out}$  as a LOW output.

Given that  $v_{out} \leq 0.25V$  what is the value of  $R_{ON}$  for an individual MOSFET?

Use the equation  $R_{ON} = R_n \frac{L}{W}$  to evaluate the required value of  $\frac{W}{L}$  for the three mosfets.

If you still encounter difficulties then read the last "troubleshooting" paragraph.

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1 response

MIT\_Lover\_UA (Staff)

2 years ago

Thank Grove for his great notes!

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