

Week 6

S11 - Small-Signal Circuit Models

S12 - Capacitors and First-Order Circuits

Lectures

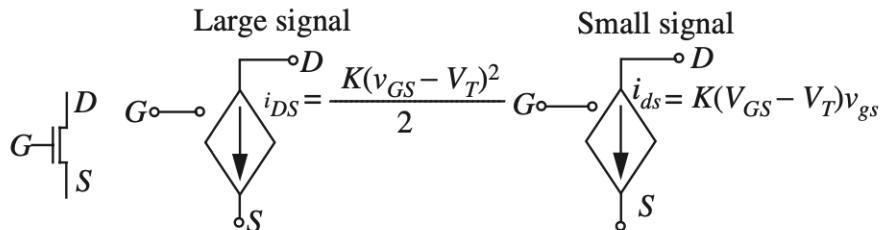
S11E1: Small-Signal MOSFET Model

0 points possible (ungraded)

When operating in the saturated region we have $i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2$.

In the space provided below write an algebraic expression for the small-signal current i_{ds} for the MOSFET. Your expression should be in terms of device parameters K and V_T , the bias voltage V_{GS} , and the incremental voltage v_{gs} . Remember that algebraic expressions are case sensitive.

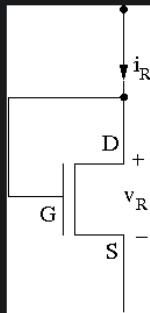
✓ Answer: K*(VGS-VT)*vgs



S11E2: Small-Signal Model of Diode-Connected MOSFET

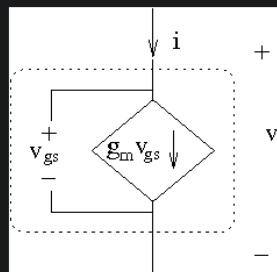
0 points possible (ungraded)

In exercise S10E2 we saw the two-terminal device formed by connecting the gate to the drain of a MOSFET, as illustrated in the figure below.



As usual, the MOSFET is specified in terms of two parameters, K and V_T .

A small-signal model of the MOSFET can be used to make a small-signal model of the two-terminal device, as illustrated below:



The coefficient g_m of the incremental voltage v_{gs} in the linear dependent current source is called the "transconductance" of the MOSFET. Given that the bias voltage across the MOSFET is V , write an algebraic expression for the transconductance of the MOSFET in this circuit. Your expression should be expressed in terms of K , V_T , and V . Enter your expression in the space provided below:

K*(V-VT)

✓ Answer: K*(V-VT)

$K \cdot (V - V_T)$

The two-terminal device can be interpreted as a resistor for small signals.

In the space provided below, write an algebraic expression for the incremental resistance presented by this two-terminal device, in terms of K , V_T and the bias voltage V .

$1/(K*(V-VT))$

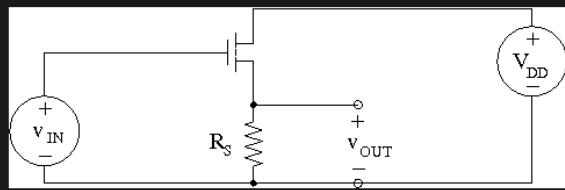
✓ Answer: $1/(K*(V-VT))$

$\frac{1}{K \cdot (V - V_T)}$

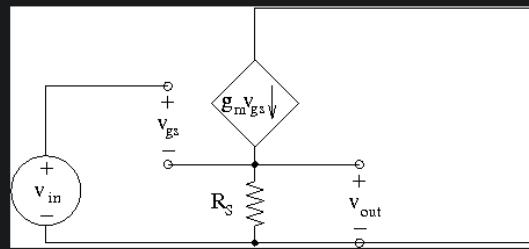
S11E3: Source Follower, Again!

0 points possible (ungraded)

We have been studying the source follower in H5P2 and H5P3.



Now we have a small-signal model of the MOSFET. Using this model of the MOSFET the small-signal model of the source-follower looks like:



where g_m is the transconductance of the MOSFET at the operating point.

Notice that the small-signal circuit is linear with independent sources.

Assume that you have already determined the operating point of the MOSFET: it is saturated; the input bias voltage is V_{IN} , and the bias current is I_{DS} .

In the space provided below write an algebraic expression for the transconductance g_m in terms of the device parameters K , V_T , R_S , and the bias conditions V_{IN} , and I_{DS} .

Although the answer can be expressed in multiple ways, note that the grader will only accept as correct an algebraic expression that has each of the variables K , V_T , R_S , V_{IN} , and I_{DS} .

Transconductance $g_m =$

Answer: K*(V_{IN} - VT - RS*IDS)

In the space provided below, write an algebraic expression for the incremental gain $a = \frac{v_{out}}{v_{in}}$ of this circuit in terms of g_m and R_S .

Incremental gain $a =$

Answer: gm*RS/(1 + gm*RS)

Now let's get the output resistance of this source follower.

To do this:

1. Suppress the independent source v_{in} . (Short it out.) Remember, you may not suppress the dependent source.
2. Add an independent current source to inject a current into the output port. Analyze the resulting circuit to get the voltage across the output port.
3. The ratio of the voltage you obtained and the current you injected is the effective output resistance of this circuit.

In the space provided below write an algebraic expression for the output resistance $r_{out} = \frac{v_{out}}{i_{out}}$ in terms of a_m and

R_S .

Output resistance $r_{out} =$

$RS/(1 + gm \cdot RS)$

✓ Answer: $RS/(1 + gm \cdot RS)$

$\frac{R_S}{1 + g_m \cdot R_S}$

Note that the input resistance $r_i = \frac{v_i}{i_i} = \infty$ because in our model there is no current allowed into the gate of a MOSFET. For low frequencies this is a good estimate. But a real MOSFET has capacitance between its gate and its other terminals. So there are better models that allow us to estimate the input "resistance" (impedance). But you will have to wait until we introduce capacitance!

S12E1: Scaling Capacitors

0 points possible (ungraded)

A capacitor is a device that stores energy in the electric field between its two conductive plates. The characteristic parameter C of a capacitor is called "capacitance", which is measured in units of Farads, after Michael Faraday, who invented fields as a way of understanding electromagnetic phenomena. See [Faraday](#) for more historical information about this great scientist/engineer. For a mechanical analogy, if we think of charge in an electrical system as analogous to displacement in a mechanical system, so current is analogous to velocity, and voltage in an electrical system as analogous to force in a mechanical system then the law for a linear capacitor is analogous to the law for a linear spring:

$$v = \frac{1}{C}Q \iff F = kx$$

and

$$i = C \frac{dv}{dt}$$

The capacitance of a parallel-plate capacitor is determined by its geometry and the material (called the dielectric) that is between its plates. As you just seen in the lecture segment, the capacitance of a parallel-plate capacitor is directly proportional to the area of the plates and inversely proportional to the distance between the plates.

$$C = \frac{\epsilon A}{d}$$

The constant of proportionality ϵ is called the "permittivity". The permittivity is a property of the material between the plates.

Suppose we double the length, width, and depth of a capacitor, by what multiple does the capacitance increase?

2

Answer: 2

The permittivity of the vacuum is $\epsilon_0 \approx 8.854 \times 10^{-12} \text{ F/m}$. This is also called the [electric constant](#). Non-conductive materials that can be put between the plates, such as polyethylene, have higher permittivity than the vacuum. The ratio of the permittivity of a material to the permittivity of the vacuum is called the "relative permittivity" or the "dielectric constant" of the material. For example, the dielectric constant of polyethylene is 2.25. For more information [see](#).

As a consequence of the very small permittivity of the vacuum, most common capacitors have a capacitance of only a tiny part of a Farad. For example, what is the capacitance (in Farads) of a parallel-plate capacitor with plates 100.0m long, 1.0 cm wide, and separated by 0.01mm of polyethylene?

1.99215e-6

Answer: 1.992149999999996e-06

Of course, for such a capacitor the plates would be thin foil or metal deposited on the dielectric film. The result would be rolled up into a tight package, with wire leads bonded to the foil plates, and hermetically sealed.

So commonly available approximately linear capacitors range from picoFarads (pF) through microFarads (uF). Electrolytic capacitors, which are not very linear, can easily be obtained in the thousands of microFarad range.

S12E2: Capacitors Store Energy

0 points possible (ungraded)

We have just learned the v-i characteristic for a linear capacitor:

$$i = C \frac{dv}{dt}$$

So the power entering the capacitor (as in any two-terminal device) is:

$$P = vi = Cv \frac{dv}{dt}$$

If we integrate this between two times we get the energy change in the capacitor over the interval:

$$\Delta E = \int_{t_0}^{t_1} P(t) dt = \int_{t_0}^{t_1} Cv(t) \frac{dv(t)}{dt} dt = \frac{1}{2}C(v(t_1))^2 - \frac{1}{2}C(v(t_0))^2$$

So the energy stored in a capacitor, as a function of the voltage across it, is:

$$E = \frac{1}{2}Cv^2$$

A typical photographic flash unit charges a capacitor of about $470.0\mu F$ to a voltage of about $260.0V$. The energy in the capacitor is then dumped into the flash tube on a scale of about $1ms$.

How much energy (in Joules) is stored in this capacitor?

7943/500

✓ Answer: 15.886000000000001

If the discharge time is actually $1ms$ what is the power (in Watts) delivered to the flash tube?

15886

✓ Answer: 15886.0

Wow!

In[6]:= $\epsilon_0 = 8.854 \times 10^{-12}; l = 100; w = 1 \times 10^{-2}; d = 0.01 \times 10^{-3};$

(*Dielectric constant = $\frac{\text{permittivity of a material}}{\text{permittivity of vacuum}}$ *)

$dc = 2.25;$

$$c = \frac{\epsilon_0 * dc * l * w}{d}$$

Out[6]:= 1.99215×10^{-6}

```
In[1]:= c = 470*^-6; v = 260;
```

$$e = \frac{1}{2} c v^2$$

$$(*\text{Power} = \frac{\text{Energy}}{\text{Time}} *)$$

$$t = 1*^-3;$$

$$p = e / t$$

$$7943$$

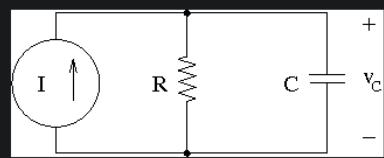
$$\text{Out}[1]= \frac{7943}{500}$$

$$\text{Out}[1]= 15886$$

S12E3: Norton Capacitor Circuit

0 points possible (ungraded)

For the circuit shown below



write an algebraic expression for the rate of change of the capacitor voltage in terms of I , R , C , and v_C . Be careful, algebraic expressions are case sensitive.

Rate of change of capacitor voltage $\frac{dv_C}{dt} =$

Answer: $(I*R - vC) / (R*C)$

$$\frac{I \cdot R - v_C}{R \cdot C}$$

Let $R = 1.0\text{k}\Omega$ and $C = 1.0\mu\text{F}$. If at some time t we have $I(t) = 1\text{mA}$ and $v_C(t) = 0\text{V}$ what is the rate of change of capacitor voltage? Express your answer in Volts/millisecond.

Answer: 1.0

$$\text{Solve}\left[-c v' + i - \frac{v}{r} = 0, v'\right]$$

(*Just trying it out, not being asked to solve DE here.*)

$$\text{DSolve}\left[\left\{-c v'[t] + i - \frac{v[t]}{r} = 0, v[0] = V_0\right\}, v[t], t\right]$$

$$r = 1*^3; c = 1*^-6; i = 1*^-3; v = 0;$$

$\frac{i r - v}{c r * 1000}$ (*Factor of 1/1000 is for conversion to V/ms*)

$$\text{Out}[]= \left\{ \left\{ v' \rightarrow \frac{i r - v}{c r} \right\} \right\}$$

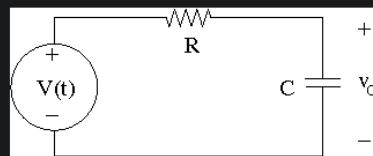
$$\text{Out}[]= \left\{ \left\{ v[t] \rightarrow e^{-\frac{t}{c r}} \left(-i r + e^{\frac{t}{c r}} i r + V_0 \right) \right\} \right\}$$

$$\text{Out}[]= 1$$

S12E4: First-Order Capacitor Examples

0 points possible (ungraded)

We have a circuit with a capacitor and a resistor driven by an independent voltage source with a voltage that is a function of time $V(t)$.



The resistance of the resistor is $R\Omega$ and the capacitance of the capacitor is $C\text{F}$.

Suppose the drive V rises in a step from 0V to 5V at the initial time $t = 0$. Also suppose that the capacitor's initial voltage $v_C(0) = 0\text{V}$.

In the space provided below write an algebraic expression for the capacitor voltage as a function of time, $v_C(t)$ for $t > 0$.

5-5*e^(-t/(R*C))

✓ Answer: 5-5*e^(-t/(R*C))

5 - 5 · $e^{-\frac{t}{R \cdot C}}$

Now, suppose the drive falls in a step from 5V to 0V at the initial time $t = 0$. Also suppose that the capacitor's initial voltage $v_C(0) = 5\text{V}$.

In the space provided below write an algebraic expression for the capacitor voltage as a function of time, $v_C(t)$ for $t > 0$.

5*e^(-t/(R*C))

✓ Answer: 5*e^(-t/(R*C))

5 · $e^{-\frac{t}{R \cdot C}}$

(*The RC solution when capacitor charges from $V_0 \rightarrow V_I$ is $v_c = V_I + (V_0 - V_I) e^{-t/RC}$ *)

`DSolve[{r c v'[t] + v[t] == V, v[0] == V0}, v[t], t]`

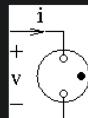
$$\text{Out}[=] = \left\{ \left\{ v[t] \rightarrow e^{-\frac{t}{cr}} \left(-V + e^{\frac{t}{cr}} V + V_0 \right) \right\} \right\}$$

S12E5: Neon Relaxation Oscillator

0 points possible (ungraded)

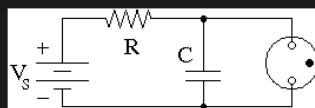
It is fun to make and to understand a neon-lamp relaxation oscillator.

A small neon indicator lamp such as an NE-2 is a pair of electrodes closely spaced in a low-pressure atmosphere of neon gas.



The lamp starts out as an open circuit. We raise the voltage v across the lamp. When the voltage across the lamp exceeds a striking voltage threshold $V_U \approx 77V$ the gas ionizes and becomes a conductor with a resistance of about $R_B \approx 10k\Omega$. However, if the voltage across the lamp decreases to a value below the sustaining threshold $V_D \approx 35V$ the gas loses its ionization and the lamp becomes an open circuit again.

The following circuit can oscillate.



The voltage of the battery $V_s = 92V$ is greater than the striking threshold of the lamp. However, initially the capacitor is at 0V. The battery charges up the capacitor through the resistor. When the voltage on the capacitor, which is the voltage across the lamp, exceeds the striking threshold of the lamp, the lamp turns on. The current through the lamp is larger than the current through the resistor from the battery, so the voltage on the capacitor decreases. When the voltage across the lamp goes below the sustaining threshold the lamp turns off, and the capacitor starts to charge again.

So after the initial transient from 0V the voltage across the capacitor oscillates between the two thresholds and the lamp flashes.

Let $R = 1.5M\Omega$ and $C = 1.0\mu F$.

How much time, in seconds, does it take for the capacitor to charge from the sustaining threshold to the striking threshold?

2.0025

✓ Answer: 2.00250160009851

How much time, in seconds, does it take for the capacitor to discharge from the striking threshold to the sustaining threshold?

0.00792789

✓ Answer: 0.00783235788441328

What is the duty cycle of the lamp? (The duty cycle is the ratio of the time it is lit to the total time.)

0.00394338

✓ Answer: 0.003896048143300483

The following algebraic solution was provided by the Community TA Irrational_Kongt:

$$\text{Time to charge capacitor: } t_1 = -RC \cdot \ln \left(\frac{V_s - V_U}{V_s - V_D} \right)$$

$$V_{TH} = \frac{R_B}{R+R_B} \cdot V_S$$

$$R_{TH} = R_B || R$$

Time to discharge capacitor: $t_2 = -R_{TH} \cdot C \cdot \ln \left(\frac{V_D - V_{TH}}{V_U - V_{TH}} \right)$

Duty cycle: $\frac{t_2}{t_1 + t_2}$

Here is the approximation used in the numerical response:

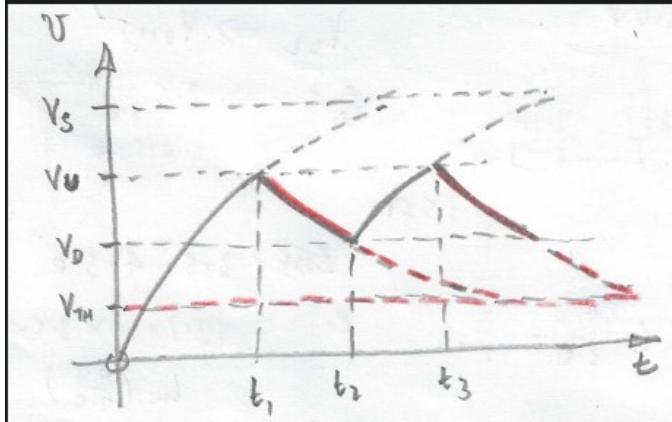
$$t_2 = -R_{TH} \cdot C \cdot \ln \left(\frac{V_D}{V_U} \right)$$

Grove (Community TA)

2 years ago

This is not an easy question.

The graph of voltage across the neon and the capacitor, v , against time, t , looks something like this.



Initially, $t = 0$, the capacitor is uncharged and it charges with a time constant which depends on R and C . When the voltage reaches V_U at $t = t_1$, the neon becomes a conductor.

The capacitor discharges with a time constant which depends on R , R_B and C until the voltage across the neon reaches V_D at time $t = t_2$.

Note that in this phase if the capacitor was allowed to discharge for ever it would then have the Thevenin voltage, V_{TH} across it.

The capacitor starts to charge again reaching V_H at time $t = t_3$.

So after the first charging interval t_1 , the time interval for discharge is $t_2 - t_1$ and that for charging is $t_3 - t_2$.

The cycle then repeats itself.

After the initial charging phase the next charging time interval is $t_{\text{charge}} = t_3 - t_2$.

The voltage across the capacitor starts at V_D and increases asymptotically towards V_S but stops at V_U .

You have decided to offset the voltages by V_S so that the voltage increase asymptotically towards zero, starting at $V_D - V_S$ and reaching the voltage $V_U - V_S$ after a time interval of $t_{\text{charge}} = t_3 - t_2$. The equation that you obtained then follows.

I think that the given solution has missed a step which showed the inversion of the subtractions to make the top and bottom of the fraction both positive?

```

vu = 77; rb = 10*^3; vd = 35; vs = 92; r = 1.5*^6; c = 1*^-6;
(*The RC solution when capacitor charges from V0 → VI is vc=VI+(V0-VI)e-t/RC.)

```

For the capacitor to charge from the sustaining threshold to the striking threshold, we sub:
 $v_c=vu$, $V_0=vd$ and $V_I=vs$)

```
Solve[vu == vs + (vd - vs) Exp[-t/(r c)], t]
```

(*Next we are asked to find the time for the capacitor to discharge from the striking threshold to the sustaining threshold. We sub:

$v_c=vd$, $V_0=vu$ and $V_I=vth$. We don't use that numerical approximation for t2 here. *)

$$vth = \frac{rb}{r + rb} vs;$$

$$rth = \frac{1}{1/rb + 1/r};$$

```
Solve[vd == vth + (vu - vth) Exp[-t/(rth c)], t]
```

(*Duty cycle*)

$$\frac{t2}{t1 + t2} /. \{t1 \rightarrow 2.00250160009851^\circ, t2 \rightarrow 0.007927890663213926^\circ\}$$

... Solve: Inverse functions are being used by Solve, so some solutions may not be found; use Reduce for complete solution information.

```
Out[6]= { {t \rightarrow 2.0025} }
```

... Solve: Inverse functions are being used by Solve, so some solutions may not be found; use Reduce for complete solution information.

```
Out[7]= { {t \rightarrow 0.00792789} }
```

```
Out[8]= 0.00394338
```

Homework

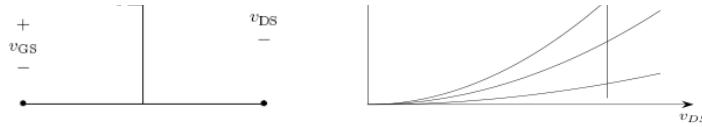
Homework due Sep 2, 2022 15:54 +04

H2P1: The NewFET device

4/4 points (graded)

This problem examines the behavior and application of a new field effect transistor (NewFET) with large-signal electrical characteristics as described in the Figure 1, where $v_{DS} \geq 0$. Note that the coefficient K and the threshold voltage V_T are both positive and constant.





$$i_D = \begin{cases} 0 & \text{for } v_{GS} < V_T \text{ (Cutoff Region)} \\ K(v_{GS} - V_T)v_{DS}^2 & \text{for } v_{GS} \geq V_T \text{ (Active Region)} \end{cases}$$

Figure 1: Large-signal characteristics of the NewFET

An amplifier is constructed with the NewFET as shown in Figure 2.

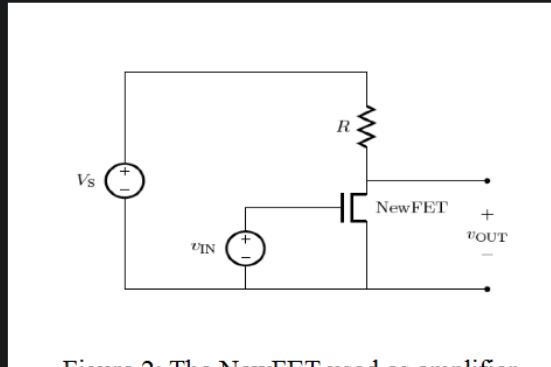


Figure 2: The NewFET used as amplifier

Derive an expression of v_{OUT} as a function of v_{IN} in terms of the power supply voltage V_S , the resistance R , and the NewFET parameters, K and V_T . Do so for the NewFET biased into the active region $0 < V_T \leq v_{IN} \leq V_S$.

Write your expression in the space provided below. Remember that algebraic expressions are case sensitive.

(-1+sqrt(1+4*R*K*(vIN-VT)*VS))/(2*R*K*(vIN-VT))



Answer: (-1 + sqrt(1 + 4 * R * K * VS * (vIN - VT))) / (2 * R * K * (vIN - VT))

$$\frac{-1 + \sqrt{1 + 4 \cdot R \cdot K \cdot (v_{IN} - V_T) \cdot V_S}}{2 \cdot R \cdot K \cdot (v_{IN} - V_T)}$$

Hint: You will get a quadratic expression. Which is the correct root? Think about what happens when $v_{IN} = V_T$. You will need to use l'Hospital's rule.

With the NewFET biased into its active region, its small-signal model is as shown in Figure 4.

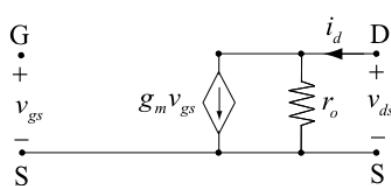


Figure 3: Small-signal-model of the NewFET when biased in its active region

Using this model, find i_d in terms of g_m , r_o , v_{gs} , and v_{ds} . Write your expression in the space provided below.

$$g_m \cdot v_{gs} + v_{ds}/r_o$$

✓ Answer: $v_{ds}/r_o + g_m \cdot v_{gs}$

$$g_m \cdot v_{gs} + \frac{v_{ds}}{r_o}$$

Assuming that the NewFET is biased into its active region, derive expressions for the small-signal-model parameters g_m and r_o in terms of the large-signal model parameters K and V_T and the bias voltages V_{GS} and V_{DS} .

Transconductance g_m =

$$K \cdot V_{DS}^2$$

✓ Answer: $K \cdot V_{DS}^2$

$$K \cdot V_{DS}^2$$

Output resistance r_o =

$$1/(K \cdot (V_{GS} - V_T) \cdot 2 \cdot V_{DS})$$

✓ Answer: $1/(2 \cdot K \cdot V_{DS} \cdot (V_{GS} - V_T))$

$$\frac{1}{K \cdot (V_{GS} - V_T) \cdot 2 \cdot V_{DS}}$$

Explanation:

(a) Equating two expressions for the drain current i_D :

$$\frac{V_s - v_{OUT}}{R} = K \cdot (v_{IN} - V_T) \cdot (v_{OUT})^2$$

Simplifying to quadratic form:

$$v_{OUT}^2 + \frac{v_{OUT}}{K \cdot R \cdot (v_{IN} - V_T)} - \frac{V_s}{K \cdot R \cdot (v_{IN} - V_T)} = 0$$

Applying the quadratic formula to solve this quadratic equation, we get the following expression:

$$v_{OUT} = \frac{-1 \pm \sqrt{\frac{1}{K \cdot R \cdot (v_{IN} - V_s)^2} + \frac{4 \cdot V_s}{K \cdot R \cdot (v_{IN} - V_T)}}}{2}$$

With a little algebra to get common denominators, the expression can be simplified to:

$$v_{OUT} = \frac{-1 \pm \sqrt{1 + 4 \cdot K \cdot R \cdot V_s \cdot (v_{IN} - V_T)}}{2 \cdot K \cdot R \cdot (v_{IN} - V_T)}$$

Now how do we figure out which root to take? When $v_{IN} = V_T$ we have a $\frac{0}{0}$ case. Using l'Hopital's rule and taking derivatives of the numerator and denominator of the fraction, we end up with $v_{OUT} = \pm V_s$ in the limit of v_{IN} approaching V_T . Thus it makes sense that we should take the positive root; there is no circumstance in this circuit where the output voltage should ever fall below 0, let alone to the negative of the supply rail.

(b) Using KCL at node A, we can find i_D by inspection: $i_D = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o}$

(c), (d) As we can see, i_D is a function of both v_{GS} and v_{DS} . The transconductance is found by taking the derivative of the current with respect to v_{GS} and evaluating it at the DC operating point (V_{GS}, V_{DS}) , and $\frac{1}{r_o}$ is found by taking the derivative of the current with respect to v_{DS} and also evaluating it at the DC operating point. Thus:

$$g_m = K \cdot (V_{DS})^2$$

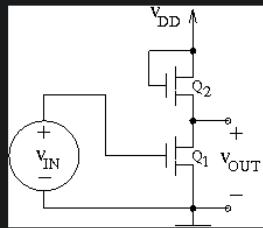
$$r_o = \frac{1}{2 \cdot K \cdot (V_{DS}) \cdot (V_{GS} - V_T)}$$

H2P2: Phase Inverter

6/6 points (graded)

The circuit shown below has two MOSFETs. The input signal is presented to the gate of Q_1 . Q_2 is configured as the two-

terminal device that you explored in exercise S10E2. Here, Q_2 , with its gate connected to its drain, is used as a replacement for the load resistor in a common-source amplifier.



Assume that the MOSFETs are identical, with parameters K and V_T . Note that it is hard to get close to identical transistors if they are discrete components, but one can get pretty good matched pairs on an integrated circuit chip.

We want to set the input bias V_{IN} high enough to keep Q_1 out of cutoff. If we want to be able to swing the input voltage up and down by Dv , what is the minimum value for the input bias voltage? Write an algebraic expression involving Dv and V_T for this minimum value of V_{IN} .

VT+Dv

✓ Answer: VT+Dv

What is the minimum value that the power supply voltage V_{DD} must be to ensure that both transistors are operating in the saturated region? Write an algebraic expression involving V_{IN} and V_T for this minimum value of V_{DD} in the space provided below:

2*V_{IN}-V_T

✓ Answer: 2*V_{IN}-V_T

$2 \cdot V_{IN} - V_T$

Notice that K did not appear in this answer... Hmmmmmm, very interesting...

Now, consider the small-signal model of this circuit. What is the transconductance g_{m1} of transistor Q_1 at the operating point? Write an algebraic expression for g_{m1} in terms of the parameters K and V_T , and the bias voltage V_{IN} .

$K*(V_{IN}-V_T)$

✓ Answer: $K*(V_{IN}-V_T)$

$K \cdot (V_{IN} - V_T)$

What is the transconductance g_{m2} of transistor Q_2 at the operating point? Write an algebraic expression for g_{m2} in terms of the parameters K and V_T , and the bias voltage V_{IN} .

$K*(V_{IN}-V_T)$

✓ Answer: $K*(V_{IN}-V_T)$

$K \cdot (V_{IN} - V_T)$

Hmmmmmm...

What is the Thevenin equivalent open-circuit voltage of the small-signal circuit, as seen from the output port? Write an algebraic expression for this v_{out} in terms of the parameters K and V_T , the bias voltage V_{IN} , and the incremental input voltage v_{in} .

-vin

✓ Answer: -vin

$-v_{in}$

What is the Thevenin equivalent resistance of the small-signal circuit, as seen from the output port? Write an algebraic expression for this resistance in terms of the parameters K and V_T , and the bias voltage V_{IN} .

$1/(K*(V_{IN}-V_T))$

✓ Answer: $1/(K*(V_{IN}-V_T))$

$\frac{1}{K \cdot (V_{IN} - V_T)}$

Notice that, for the approximations we use in this class, the behavior of this circuit is quite independent of the detailed properties of the MOSFETs. This is very useful.

Explanation:

(a) To remain in saturation, $V_{IN} \geq V_T$ must ALWAYS hold true. Since $V_{IN} - D_V$ is the minimum possible input voltage, we have:

$$V_{IN} - D_v \geq V_T$$

Therefore,

$$V_{IN} \geq V_T + D_v$$

(b) As both MOSFETs must satisfy the equation $i_{D2} = i_{D1}$, we write the following equation:

$$\frac{K}{2} \cdot [(V_{DD} - V_{OUT}) - V_T]^2 = \frac{K}{2} \cdot (V_{IN} - V_T)^2$$

Simplifying,

$$V_{DD} = V_{IN} + V_{OUT}$$

For Q1 to be in saturation, $V_{OUT} \geq V_{IN} - V_T$. Substituting this in the above relation for V_{OUT} , we get:

$$V_{DD} \geq 2 \cdot V_{IN} - V_T$$

(c) Transconductance g_{m1} is found through the following equation: $g_{m1} = \frac{\partial i_{D1}}{\partial V_{GS}}$ evaluated at the DC operating point $v_{in} = V_{IN}$. Carrying out this derivative, we get:

$$g_m = K \cdot (V_{IN} - V_T)$$

(d) As $i_{D1} = i_{D2}$, the answers to parts (c) and (d) are identical.

(e) Using KVL, we get: $-g_{m2} \cdot v_{OUT} = g_{m1} \cdot v_{IN}$. Since $g_{m1} = g_{m2}$, we see that $v_{out} = -v_{in}$

(f) We can find the output resistance by shorting all the independent voltage sources (in this case, v_{in}), and then, applying a test voltage v_{test} and measuring the resulting i_{test} .

$$i_{test} = g_m \cdot v_{test}$$

Thus the output resistance is:

$$r_o = \frac{v_{test}}{i_{test}} = \frac{v_{test}}{g_m \cdot v_{test}} = \frac{1}{g_m} = \frac{1}{K \cdot (V_{IN} - V_T)}$$

We can also find the output resistance by finding the ratio of the open-circuit voltage to the short-circuit current on the small-signal model. We already have the open-circuit voltage:

$$v_{oc} = v_{out} = -v_{in}$$

And shorting the output node to ground and performing KCL at that node:

$$i_{sc} = -g_m \cdot v_{in}$$

Thus the output resistance is:

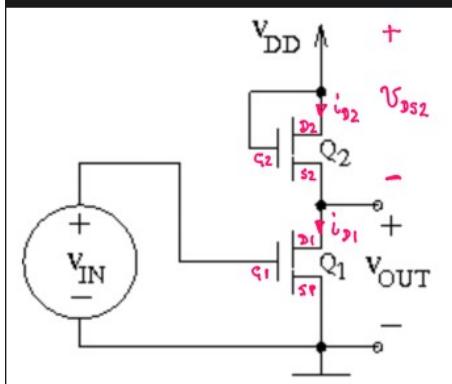
$$\frac{v_{oc}}{i_{sc}} = \frac{-v_{in}}{-g_m \cdot v_{in}} = \frac{1}{g_m} = \frac{1}{K \cdot (V_{IN} - V_T)}$$

This agrees with the result we got from the first method!

There are two conditions which relate to cut off which are $v_{GS} \geq V_T$ and $v_{DS} \geq (v_{GS} - V_T)$.

Use one of them to answer part 1.

Here is the circuit under investigation.



You know of an equation for $i_D = K(v_{GS} - V_T)^2$ so use it to generate equations for i_{D1} and i_{D2} in terms of voltages given in the circuit diagram.

Looking at the circuit diagram what do you know about i_{D1} and i_{D2} ?

Use that knowledge to find a relationship between V_{DD} , v_{IN} and v_{OUT} and then, using one of the cut off conditions, answer part 2.

The relationship between V_{DD} , v_{IN} and v_{OUT} can also be found by using KVL.

(*Help with Thevenin part, after finding relationship

transconductance and output (Thevenin) resistance $g_m=1/r_o^*$)

Grove (Community TA)

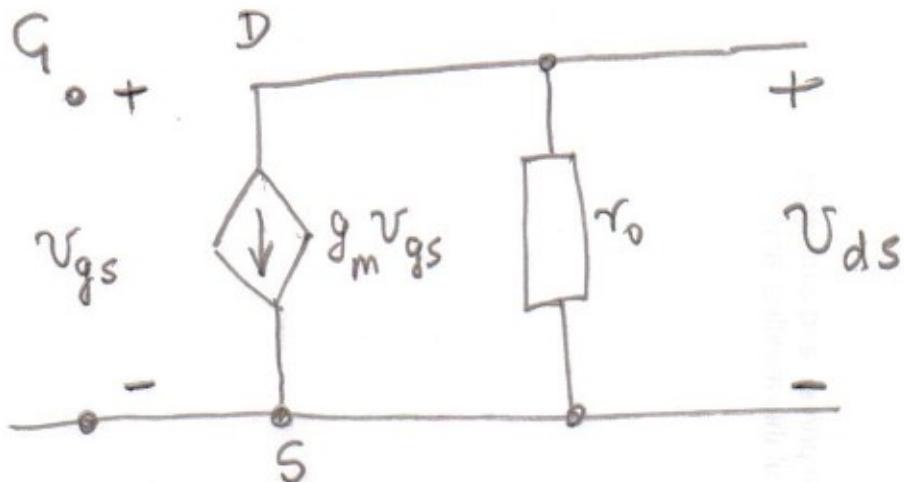
3 years ago

In your travels you have found a simple relationship between V_{DD} , v_{IN} and v_{OUT} .

Differentiate this expression to get a simple relationship for $\Delta v_{OUT} = v_{out}$ in terms of $\Delta v_{IN} = v_{in}$.

Now use the small signal equivalent circuit to find another simple relationship between v_{out} (open circuit) and v_{in} .

(*We found $V_{IN}=V_{DD}-V_{OUT}$, so we differentiate as hinted to get $v_{in}=-v_{out}$ *)



H2P3: Series and Parallel Capacitors

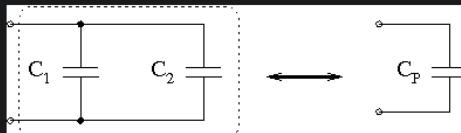
6/6 points (graded)

Now we know that the voltage-current behavior of a capacitor of capacitance C is:

$$i_C = C \frac{dv_C(t)}{dt}$$

It turns out that, just like with resistors, various combinations of capacitors are terminal-equivalent to a single capacitor with a capacitance determined from the capacitances of the parts of the combination. For each of the following circuits give the capacitance of an equivalent capacitor, as seen from the exposed terminals.

First, let's look at two capacitors in parallel:



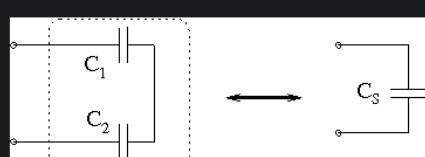
Think in terms of the geometry: how can two capacitors in parallel be thought of as one?

In the space provided below give an algebraic expression for C_P in terms of C_1 and C_2 that makes these terminal equivalent.

Parallel capacitance $C_P =$

✓ Answer: $C_1 + C_2$

Next, let's look at two capacitors in series:



Think in terms of the geometry: how can two capacitors in series be thought of as one?

In the space provided below give an algebraic expression for C_S in terms of C_1 and C_2 that makes these terminal equivalent.

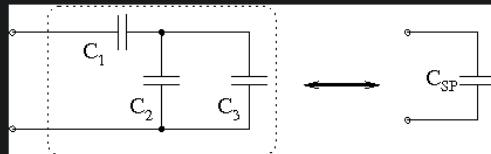
Series capacitance $C_S =$

$$1/(1/C_1+1/C_2)$$

✓ Answer: $(C_1 \cdot C_2) / (C_1 + C_2)$

$$\frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}$$

Next, let's look at a combination



In the space provided below give an algebraic expression for C_{SP} in terms of C_1 , C_2 , and C_3 that makes these terminal equivalent.

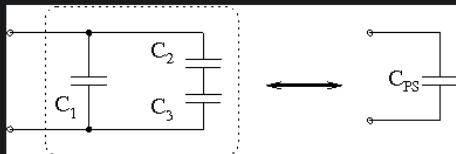
Equivalent capacitance $C_{SP} =$

$$1/(1/C_1+1/(C_2+C_3))$$

✓ Answer: $(C_1 \cdot (C_2 + C_3)) / (C_1 + C_2 + C_3)$

$$\frac{1}{\frac{1}{C_1} + \frac{1}{C_2 + C_3}}$$

Next, let's look at another combination



In the space provided below give an algebraic expression for C_{PS} in terms of C_1 , C_2 , and C_3 that makes these terminal equivalent.

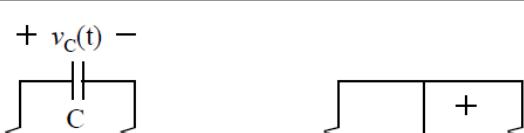
Equivalent capacitance $C_{PS} =$

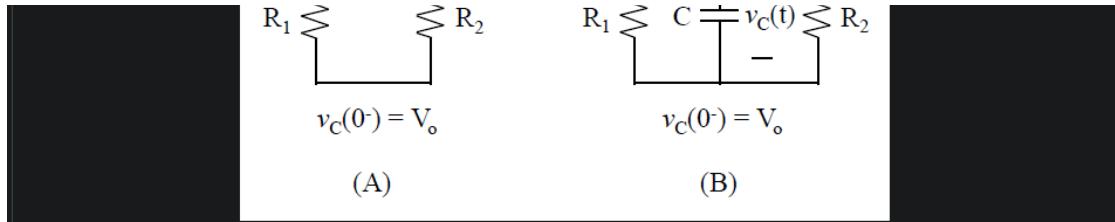
$$C_1 + 1/(1/C_2+1/C_3)$$

✓ Answer: $C_1 + (C_2 \cdot C_3) / (C_2 + C_3)$

$$C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3}}$$

The capacitor in each network shown below has a non-zero initial voltage at $t = 0^-$, as indicated in the figure. For each network, determine the time constant with which this capacitor voltage decays. Hint: Consider the Thevenin resistance seen by each capacitor.





What is the decay time constant associated with network A in terms of the circuit parameters?

$$(R_1+R_2)\cdot C$$

Answer: $C \cdot (R_1 + R_2)$

$$(R_1 + R_2) \cdot C$$

What is the decay time constant associated with network B in terms of the circuit parameters?

$$C/(R_1+R_2)$$

Answer: $C \cdot ((R_1 \cdot R_2) / (R_1 + R_2))$

$$\frac{C}{\frac{1}{R_1} + \frac{1}{R_2}}$$

Explanation:

(a) The equivalent capacitance of capacitors in parallel is the sum of the capacitances. Therefore:

$$C_P = C_1 + C_2$$

(b) The equivalent capacitance of capacitors in series is the product of the capacitances divided by the sum of the capacitances. Therefore:

$$C_{SP} = \frac{(C_1 + C_2) \cdot C_3}{C_1 + C_2 + C_3}$$

(c) The equivalent capacitance of C_1 in parallel with the series combination of C_2 and C_3 is expressed as:

$$\frac{C_2 \cdot C_3}{C_2 + C_3} + C_1$$

(d) The decay time constant associated with network A is found by multiplying the capacitance by the equivalent resistance.

$$\tau = (R_1 + R_2) \cdot C$$

(e) The decay time constant associated with network B is found by multiplying the capacitance by the equivalent resistance.

$$\tau = \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C$$

Lab

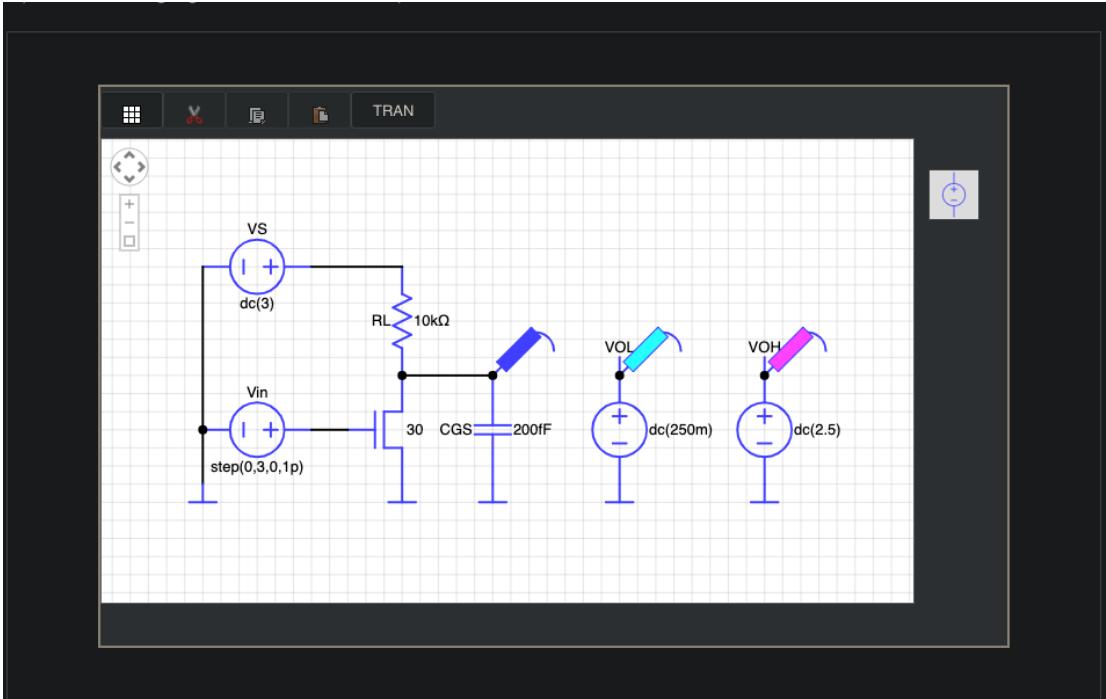
Lab due Sep 2, 2022 15:54 +04

Lab 2

7/7 points (graded)

The goal of this lab is to measure the propagation delay of an inverter. You may find it useful to review [Section 10.4](#) in the text.

The circuit below contains an inverter designed to be used in a system where $V_S = 3V$, $V_{OL} = 0.25V$ and $V_{OH} = 2.5V$. The input to the inverter is hooked to a voltage source that makes a $0 \rightarrow 1$ transition at $t = 0$. The performance of the inverter is measured as it drives a $200fF$ capacitive load, which represents the parasitic capacitance of the wiring and the inputs of other logic gates hooked to the output of the inverter.



Run a 5ns transient analysis on this circuit and use measurements from the plot to answer the following questions:

1. Measure final output voltage of the inverter when the input is high and use that to estimate R_{ON} for the mosfet switch.

Estimate for R_{ON} in ohms:

686.783

✓ Answer: 683

2. When the input to the inverter is high, the Thevenin equivalent for the circuit is as shown in Figure 10.22 in the text. Using your measurements, estimate V_{TH} and R_{TH} for the Thevenin equivalent circuit.

Estimate for V_{TH} in volts:

0.192794

✓ Answer: .192

Estimate for R_{TH} in ohms:

642.647

✓ Answer: 639

3. Using Equation 10.66 in the text and the parameters above, compute an estimate for $t_{pd,0 \rightarrow 1}$, the time it takes for the inverter output to fall from V_S to V_{OL} when driving a 200fF capacitive load.

Estimate for t_{pd} in nanoseconds:

0.500401

✓ Answer: .496

4. Using the plot of the inverter's output voltage from the transient analysis, enter the measured value of $t_{pd,0 \rightarrow 1}$.

Measurement for t_{pd} for a rising input in nanoseconds:

0.595

✓ Answer: .6

You'll notice that the measured value is longer than the estimated value. To understand why, remember that the value you used for R_{ON} in the calculation was based on the steady-state output voltage of the inverter after the output transition was complete, i.e., when the mosfet switch is in its triode region of operation. However the transition started with the mosfet switch in its saturation region, where the effective resistance ($\frac{V_{DS}}{I_{DS}}$) was higher. Hence the actual propagation delay will be somewhat longer than the calculated propagation delay.

5. Finally, change the V_{in} voltage source so that input is making a $1 \rightarrow 0$ transition (just interchange the initial and

8. Finally, change the V_{IN} voltage source so that input is making a 1 → 0 transition (just interchange the initial and plateau voltages) and measure the value of $t_{pd,1 \rightarrow 0}$, the time it takes for the inverter's output to reach V_{OH} .

Measurement for t_{pd} for a falling input in nanoseconds:

3.45

✓ Answer: 3.4

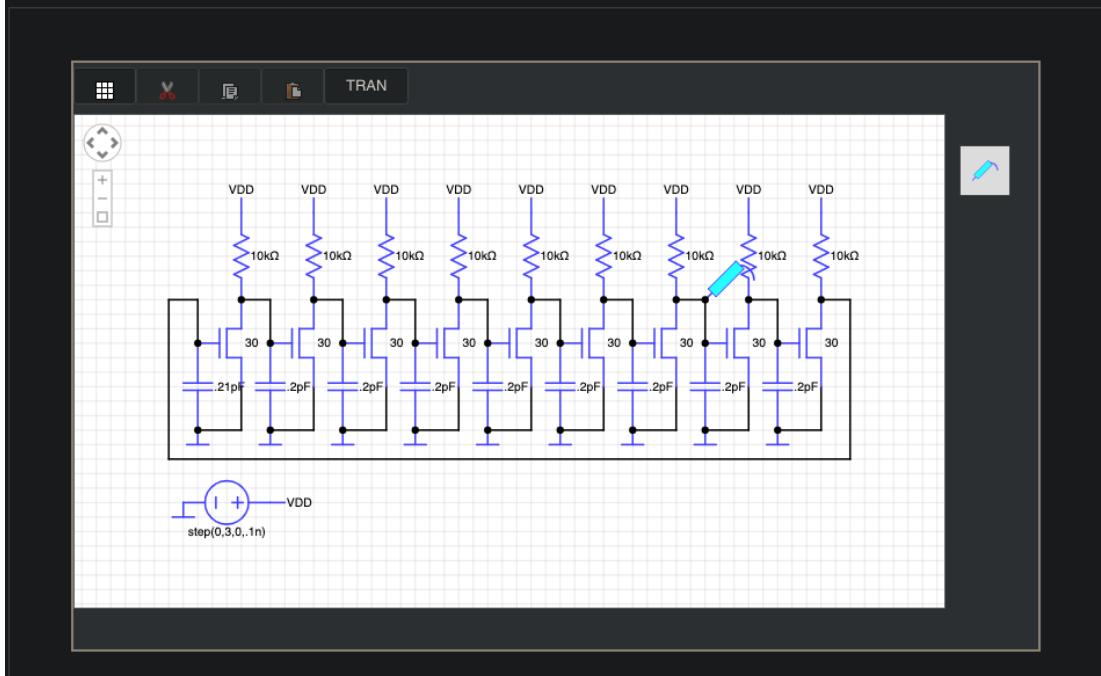
If you compute an estimate for $t_{pd,1 \rightarrow 0}$ using [Equation 10.71](#) and the appropriate parameters, you'll find it agrees quite well with the measurement. This time the resistance used in the calculation (R_L) was exactly the resistance in the circuit throughout the entire transition.

These measurements and calculations of the inverter's propagation delay are *worst-case* values. When there are many logic gates in series, the actual measured signal delay is often considerably smaller than the sum of the worst-case delays for each gate. This is because the gates will start their transitions long before their inputs have reached their final value, e.g., the mosfet switch in the inverter turns on when its input exceeds V_T , long before the input reaches V_{OH} .

To see this effect, let's build a 9-stage *ring oscillator*, a chain of 9 inverters hooked in a loop as shown in the circuit below. Here's how it works:

1. Think about 9 inverters hooked in series: if we set the input of the first inverter to a "0" logic value, it produces a "1" on its output after a short delay. This causes the second inverter to produce a "0" after another short delay, and so on, until the ninth inverter produces a "1" on its output after a delay that reflects how long it takes for the original input to propagate through all nine inverters. Since there are an odd number of inverters, the output signal will be the negation of the input signal.
2. Now suppose the output of the ninth inverter is hooked to the input of the first. Things proceed as explained above, until the ninth inverter produces a "1" on its output. But this output is hooked to the input of the first inverter and this new value propagates through the inverter chain as before, producing a "0" on the output of the ninth inverter. This cycle repeats itself over and over: the value of each input/output alternates between "0" and "1" as each new value propagates through the chain and then back to the start.
3. What happens when the circuit powers on is a bit more complicated since, if all the nodes start at 0 volts, each inverter has a "0" on its input as starts to drive its output to "1". But any small asymmetry will cause some inverters to do this more slowly than the others -- this asymmetry happens naturally in a manufactured circuit where, e.g., the long wire that completes the loop has a bit more capacitance than the other wires. It takes a cycle for the inverters to get themselves sorted out. You can see this happening in the little hiccup at the beginning of the transient simulation of the circuit below. Add some additional voltage probes if you'd like to see in more detail what is happening.

We have to use two tricks to ensure the oscillator will oscillate in the perfect world of the simulator: introduce a small asymmetry in the parasitic capacitances and turn "on" the circuit after time 0 by using a step voltage source for the power supply.



Because there are an odd number of inverters in the loop, the node voltages will oscillate between high and low, the period of oscillation being determined by the time it takes for a signal to propagate *twice* around the loop (think about why). If we consider the voltage for a particular node, the period of oscillation represents one $0 \rightarrow 1$ transition and one $1 \rightarrow 0$ transition, separated by the propagation time of 9 inverters.

Run a 50ns transient simulation on the ring oscillator and measure the period of oscillation. Be patient! It can take a moment for the simulation to complete. Divide the result by 9 to get an estimate for the time it takes one inverter to make a $0 \rightarrow 1$ transition followed by a $1 \rightarrow 0$ transition.

Estimate for time for both transitions, in nanoseconds:

1.80556

✓ Answer: 1.8

Compare this time to the sum of your answers for questions (4) and (5) above.

Explanation:

- From the transient plot we find that the output voltage of the inverter when the input is high is $V_{out} = 192mV$. The measurement has to be done after the transient due to the capacitor. Since the MOSFET is behaving as a resistor, the equivalent circuit is a voltage divider with the output voltage calculated on the R_{on} resistance. Therefore:

$$V_{out} = \frac{R_{on}}{R_L + R_{on}} \cdot V_S$$

Solving for R_{on} we get:

$$\begin{aligned} R_{on} &= R_L \cdot \frac{V_{out}}{V_S} \cdot \left(1 - \frac{V_{out}}{V_S}\right)^{-1} = (10k\Omega) \cdot \left(\frac{0.192V}{3V}\right) \cdot \left(1 - \frac{0.192V}{3V}\right)^{-1} \\ &= 683\Omega \end{aligned}$$

- From Figure 10.22, the Thevenin voltage is given by the equation:

$$V_{th} = \frac{R_{on}}{R_L + R_{on}} \cdot V_S = \frac{683\Omega}{10000\Omega + 683\Omega} \cdot 3V = 0.192V$$

Also from figure 10.22, the Thevenin resistance is:

$$R_{th} = R_L \parallel R_{on} = \frac{R_L \cdot R_{on}}{R_L + R_{on}} = \frac{683\Omega \cdot 10000\Omega}{10000\Omega + 683\Omega} = 639.33\Omega$$

- From equation 10.66, we get that the time it takes for the transition to occur is approximately:

$$t > -R_{th}C_{GS2} \cdot \ln\left(\frac{V_{OL} - V_{th}}{V_S - V_{th}}\right)$$

Using the values found above:

$$t > -(639.33\Omega) \cdot (200 \times 10^{-15}) \cdot \ln\left(\frac{0.25V - 0.192V}{3V - 0.192V}\right) = 0.496ns$$

- From the transient analysis plot we see that the output voltage reaches $V_{OL} = 0.25V$ after approximately 0.60ns. As expected, this value is larger than the calculated value.

- Changing the input voltage to make a 1 to 0 transition and extending the simulation time to 5ns, we can see that the output voltage takes about 3.4ns to reach a value of V_{OH}

- Now, we compute the turn on and off time of the MOSFET connected on a ring oscillator configuration. By running the simulation for 50ms, we can see that the output voltage in all the node oscillate between high and low with a particular frequency. Measuring the time it takes for the output voltage to complete one cycle (i.e start at a low value, change to high, and return to low) is approximately 16.125ns. Therefore, the addition of the turn on and off transitions for one inverter is the period divided by nine, so that the result is 1.79ns.

$$v_2 = \frac{R_2}{R_1 + R_2} V. \quad (2.48)$$

This completes the analysis of the two-resistor voltage divider.

(*Using this voltage divider equation and reading off v2= 192.794m from the transient*)

In[6]:= v2 = 192.794*^-3; Rl = 10*^3; Vs = 3;

Solve[v2 == $\frac{R_{ON}}{R_L + R_{ON}}$ Vs, Ron]

... Solve: Solve was unable to solve the system with inexact coefficients. The answer was obtained by solving a corresponding exact system and numericizing the result.

ans =

{ {Ron → 686.783} }

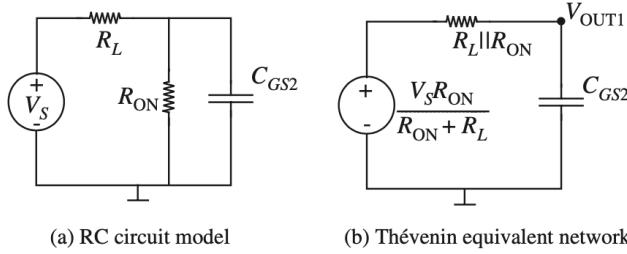


FIGURE 10.22 Equivalent circuit when C_{GS2} is discharging.

In[7]:= Vth = $\frac{Vs R_{ON}}{R_{ON} + R_L}$ /. {Ron → 686.7825161388228`}

Rth = $\frac{1}{\frac{1}{R_L} + \frac{1}{R_{ON}}}$ /. {Ron → 686.7825161388228`}

Vth =

0.192794

Rth =

642.647

Substituting the initial condition $v_C(0) = V_S$, we obtain the final solution:

$$v_C(t) = V_{TH} + (V_S - V_{TH})e^{-t/R_{TH}C_{GS2}}. \quad (10.66)$$

How long does it take for v_C to drop below 1 volt? To obtain this duration, we must solve for the value of t that satisfies

$$V_{TH} + (V_S - V_{TH})e^{-t/R_{TH}C_{GS2}} < 1.$$

In other words,

$$t > -R_{TH}C_{GS2} \ln \left(\frac{1 - V_{TH}}{V_S - V_{TH}} \right).$$

```
In[1]:= Vol = 0.25; c = 200*^-15;
t0to1 = -Rth c Log[Vol - Vth]
          Vs - Vth
```

```
t0to1 =
5.00401 × 10^-10
```

```
In[2]:= period = (46.25 - 30)/9
```

```
period =
1.80556
```