User's Manual

32

RH850 Evaluation Platform

RH850/U2A 516pin

User's Manual: PiggyBack Board

Y-RH850-U2A-516PIN-PB-T1-V1

The newest version of this document can be obtained from the following web location:
Y-RH850-U2A-516PIN-PB-T1-V1 Documents

Renesas Electronics
www.renesas.com

Rev.1.00 Feb 2019

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   – The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2A 516pin PiggyBack Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2A 516pin microcontrollers.

Notes

1. This document describes the functionality of the PiggyBack Board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document low active signals are marked by an appended 'Z' to the pin or signal name. E.g. the reset pin is named RESETZ.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2A-516PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2A-516PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2A-516PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2A-516PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2A-516PIN-PB-T1-V1

Item	Description	Quantity
D016345#0080	RH850/U2A 516pin Adapter Board	1
D016563	Documentation CD	1
D010816-24	China RoHS document	1
D016345-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	49
Red Hirschmann 4 mm power lab sockets	In the bag	3
Black Hirschmann 4 mm power lab sockets	In the bag	1
16MHz Resonator	In the bag	1
20MHz Resonator	In the bag	1
24MHz Resonator	In the bag	1

Note

Please keep the Y-RH850-U2A-516PIN-PB-T1-V1 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-U2A-516PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported MainBoards

This PiggyBack Board can be used as a standalone board, or it can be mated with a MainBoard. The following MainBoards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1

1.3 Main features

- Burn-in socket for mounting of the device
- Several power setup-up options
  - Combined operation with powering from Main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.12 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.
- Debugging, tracing and programming capability via two interfaces:
  - 14-pin LPD/JTAG Debug Connector (e.g. for using E2 OCD Emulator or PG-FP6 Flash Programmer)
  - 34-pin ERF8 AURORA Trace Connector (e.g. for using 3rd Party Off-chip Trace Emulator Solutions)
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 16/20/24/40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Gigabit Ethernet Port 100/1000BASE-TX
- On-board interface connector for
  - Renesas High-Speed Serial I/F (RHSIF)

  or
  - Multichannel Serial Peripheral Interface (MSPI)
- Operating temperature from 0 °C to +40 °C

1.4 PiggyBack Board views

Following figures provide the top and bottom views of the PiggyBack Board.

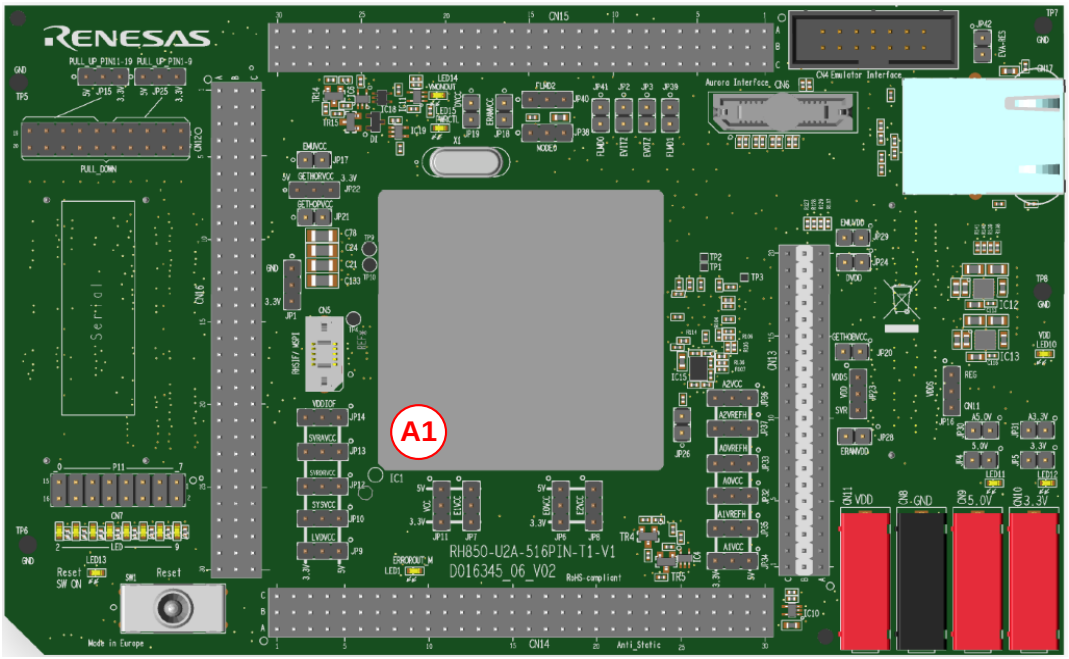


Figure 1.1 PiggyBack Board top view

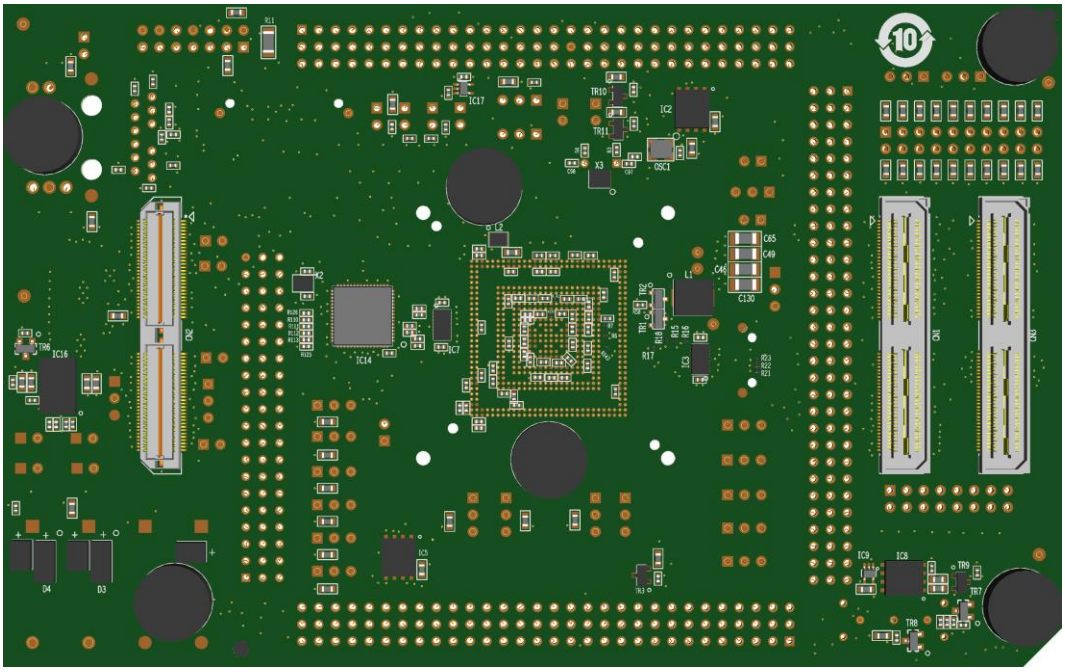


Figure 1.2 PiggyBack Board bottom view

Following figures provide the top and bottom views of the PiggyBack Board.

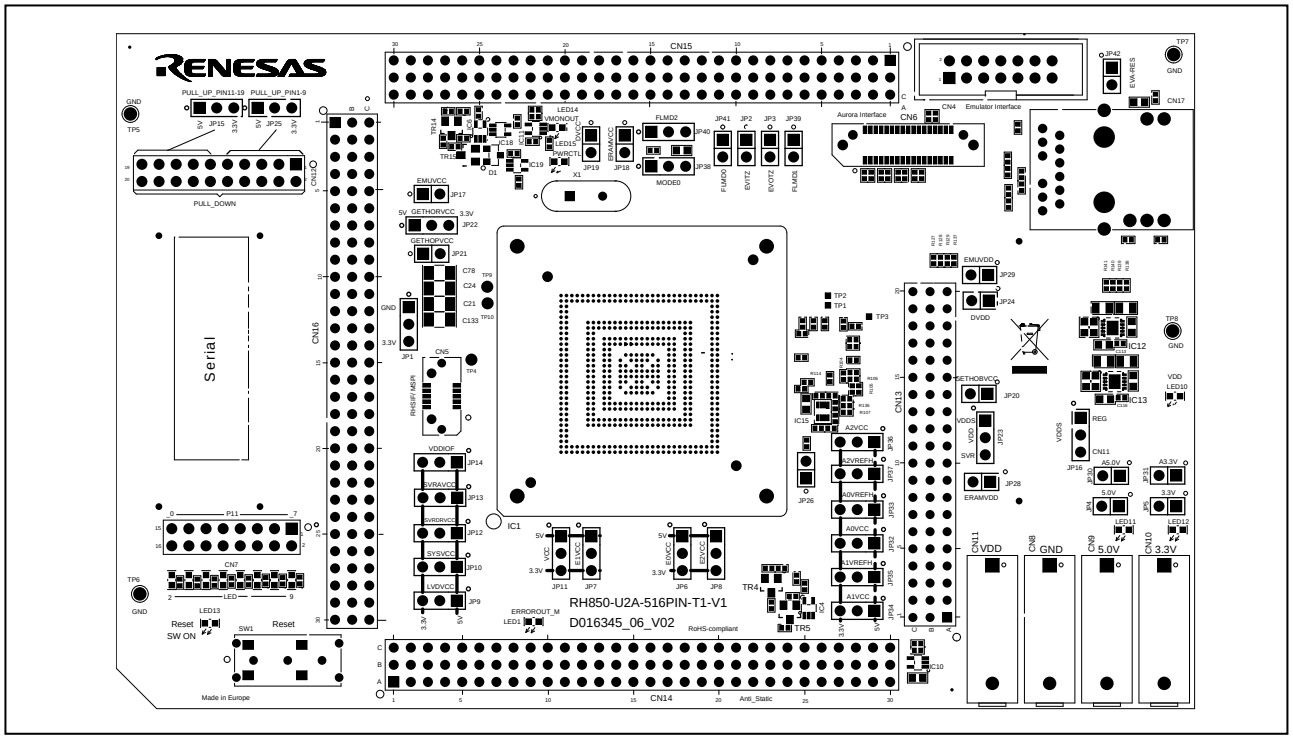


Figure 1.3 PiggyBack Board top view

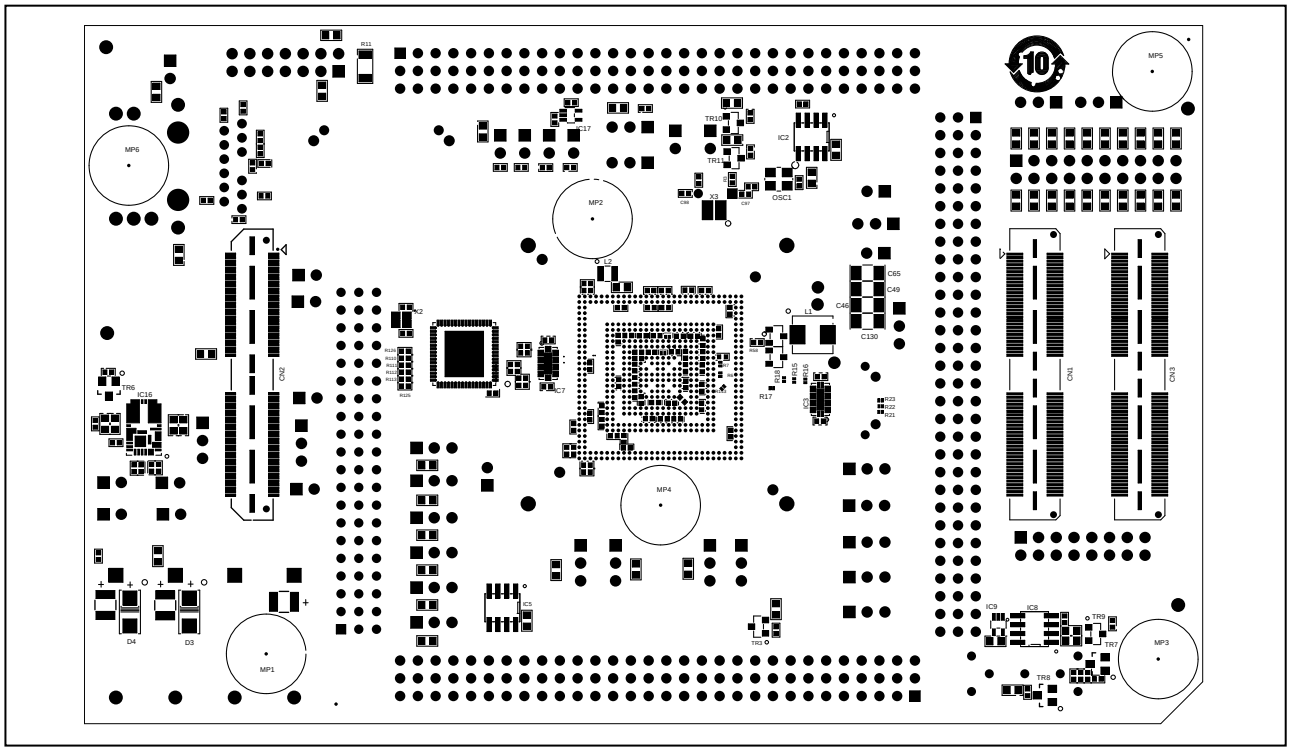


Figure 1.4 PiggyBack Board bottom view

1.5 Mounting of the device

The board is designed for use with the following devices:

- R7F702Z19EDBG (RH850/U2A-EVA)
- R7F702300EABG (RH850/U2A16)

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the A1 pin of the socket.
The A1pin of the socket is marked with a circle near to the “IC1” label (see also red A1 circle in *Figure 1.1 PiggyBack Board top view*).
The A1 pin of the device is marked by a white triangle on the package (see white circle in the figure below).

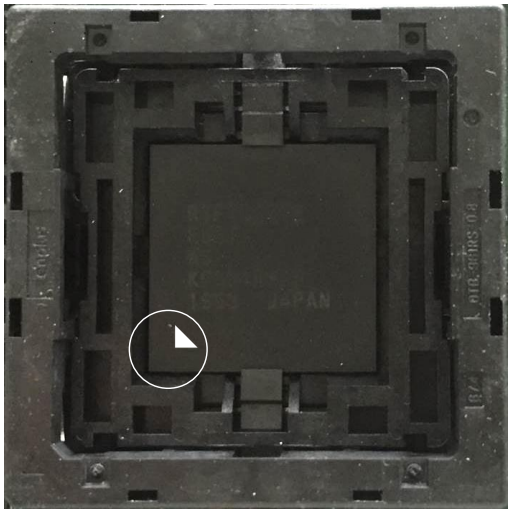


Figure 1.5 Enplas OTP-516(961RS)-0.8-048S-00 socket with mounted device

CAUTION

Be careful with the device placement in the socket to avoid damage of the device.

2. Jumpers, Connectors and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figure below.

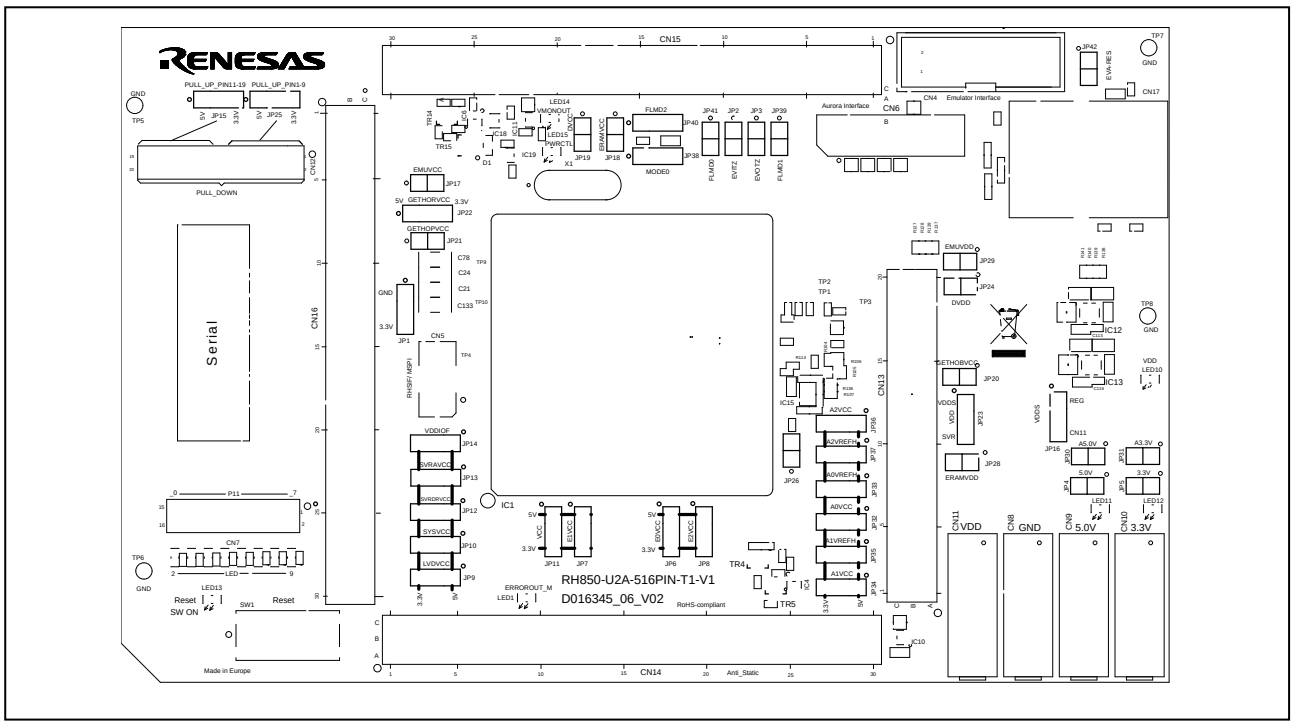


Figure 2.1 Placement of jumpers, connectors and LEDs

The placement of these components on the board is depicted in the figure below.

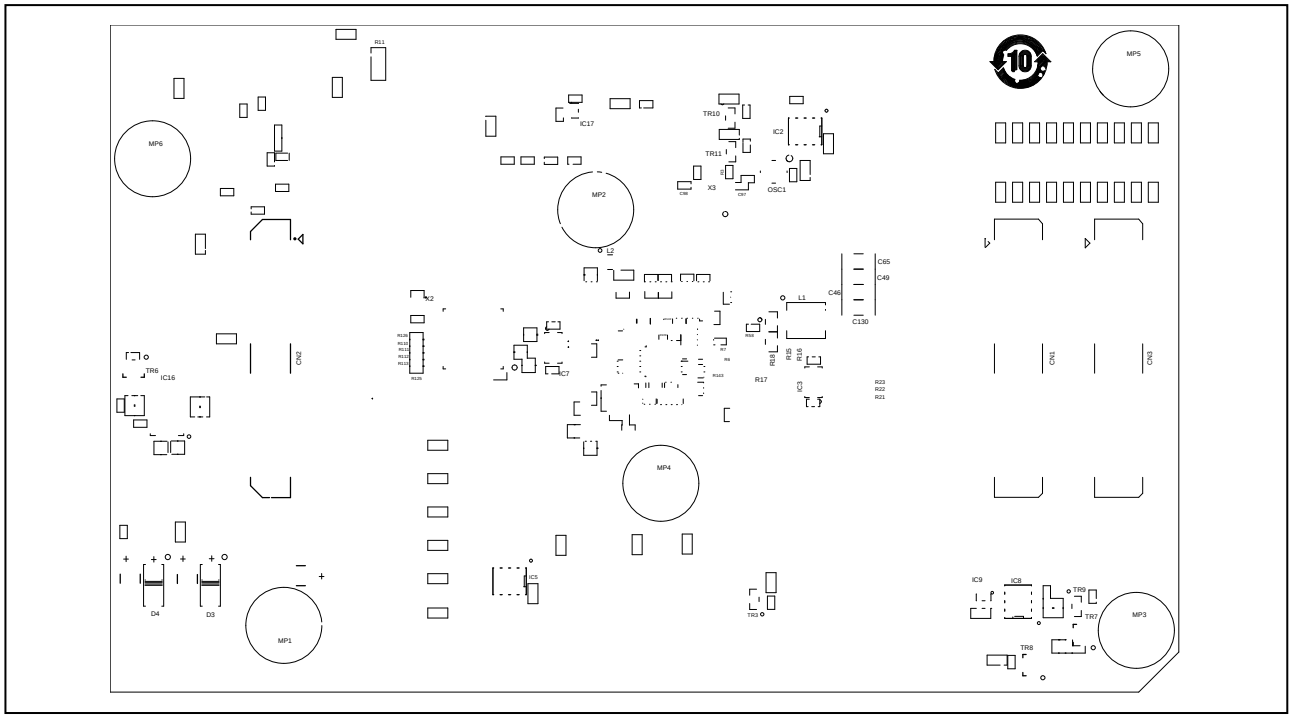


Figure 2.2 Placement of connectors on bottom side

2.1 Jumpers overview

The following table provides an overview of all jumpers.

Table 2.1 Jumpers overview

Jumper	Function	Remark
JP1	RHSIF I/F Rx/Tx signals swap • JP1[2-1]: RXDP/RXDN at pins 7 and 9 of CN5, TXDP/TXDN at pins 1 and 3 of CN5 • JP1[2-3]: RXDP/RXDN at pins 1 and 3 of CN5, TXDP/TXDN at pins 7 and 9 of CN5	refer to *6.7 Renesas High-Speed Serial I/F (RHSIF) / Multichannel Serial Peripheral Interface (MSPI)*
JP2	Nexus I/F EVTIZ level • JP2[2-1]: EVTIZ = H level • JP2[OPEN]: EVTIZ = CN6 pin 16 level	refer to *5.2 Aurora trace*
JP3	Nexus I/F EVTO level • JP3[2-1]: EVTO = H level • JP3[OPEN]: EVTO = CN6 pin 18 level	
JP4	Current measurement bridge of 5.0 V power rail	refer to *3.4 Current measurement bridges*
JP5	Current measurement bridge of 3.3 V power rail	refer to *3.4 Current measurement bridges*
JP6	voltage selection for E0VCC • JP6[2-1]: 5.0 V • JP6[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP7	voltage selection for E1VCC • JP7[2-1]: 5.0 V • JP7[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP8	voltage selection for E2VCC • JP8[2-1]: 5.0 V • JP8[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP9	voltage selection for LVDVCC • JP9[2-1]: 5.0 V • JP9[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP10	voltage selection for SYSVCC • JP10[2-1]: 5.0 V • JP10[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP11	voltage selection for VCC • JP11[2-1]: 5.0 V • JP11[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP12	voltage selection for SVRDRVCC • JP12[2-1]: 5.0 V • JP12[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP13	voltage selection for SVRAVCC • JP13[2-1]: 5.0 V • JP13[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP14	voltage selection for VDDIOF • JP14[2-1]: 5.0 V • JP14[2-3]: 3.3 V	refer to *3.2 Voltage distribution*

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP15	voltage selection for Pull-up/Pull-down pin header CN12 pins 11, 13, 15, 17, 19 • JP15[2-1]: 5.0 V • JP15[2-3]: 3.3 V	refer to *6.5 Pull-up/Pull-down pin header*
JP16	voltage selection for 1.12 V VDDs * • JP16[2-1]: reg_vcc_VDD • JP16[2-3]: IN_1v12	refer to *3.3 Device core voltages (xVDD) selection*
JP17	voltage selection for EMUVCC • JP17[2-1]: 3.3 V • JP17[OPEN]: off	refer to *3.2 Voltage distribution*
JP18	voltage selection for ERAMVCC • JP18[2-1]: 3.3 V • JP18[OPEN]: off	refer to *3.2 Voltage distribution*
JP19	voltage selection for DVCC • JP19[2-1]: 3.3 V • JP19[OPEN]: off	refer to *3.2 Voltage distribution*
JP20	voltage selection for GETH0BVCC • JP20[2-1]: 3.3 V • JP20[OPEN]: off	refer to *3.2 Voltage distribution*
JP21	voltage selection for GETH0PVCC • JP21[2-1]: 3.3 V • JP21[OPEN]: off	refer to *3.2 Voltage distribution*
JP22	voltage selection for GETH0RVCC • JP22[2-1]: 5.0 V • JP22[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP23	voltage selection for VDD • JP23[2-1]: VDDs • JP23[2-3]: SVR_OUTPUT	refer to *3.3 Device core voltages (xVDD) selection*
JP24	voltage selection for DVDD • JP24[2-1]: VDDs • JP24[OPEN]: off	refer to *3.2 Voltage distribution*
JP25	voltage selection for Pull-up/Pull-down pin header CN12 pins 1, 3, 5, 7, 9 • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V	refer to *6.5 Pull-up/Pull-down pin* header

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP26	Device Ethernet I/F Rx/Tx signals swap • JP26[OPEN]: – device pins N21/P21 used as Ethernet Tx signals – device pins P22/R22 used as Ethernet Rx signals • JP26[2-1]: – device pins N21/P21 used as Ethernet Rx signals – device pins P22/R22 used as Ethernet Tx signals	refer to *6.6 Gigabit Ethernet interface*
JP28	voltage selection for ERAMVDD • JP28[2-1]: VDDs • JP28[OPEN]: off	refer to *3.2 Voltage distribution*
JP29	voltage selection for EMUVDD • JP29[2-1]: VDDs • JP29[OPEN]: off	refer to *3.2 Voltage distribution*
JP30	Current measurement bridge of 5.0 V A/D Converter power supply	refer to *3.4 Current measurement bridges*
JP31	Current measurement bridge of 3.3 V A/D Converter power supply	refer to *3.4 Current measurement bridges*
JP32	voltage selection for A0VCC • JP32[2-1]: 5.0 V • JP32[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP33	voltage selection for A0VREFH • JP33[2-1]: 5.0 V • JP33[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP34	voltage selection for A1VCC • JP34[2-1]: 5.0 V • JP34[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP35	voltage selection for A1VREFH • JP35[2-1]: 5.0 V • JP35[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP36	voltage selection for A2VCC • JP36[2-1]: 5.0 V • JP36[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP37	voltage selection for A2VREFH • JP37[2-1]: 5.0 V • JP37[2-3]: 3.3 V	refer to *3.2 Voltage distribution*
JP38	MODE0 level selection • JP38[2-1]: H level • JP38[2-3]: L level	refer to *6.1 Operation mode selection*

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP39	FLMD1 level selection • JP39[2-1]: H level • JP39[OPEN]: L level	refer to *6.1 Operation mode selection*
JP40	FLMD2 level selection • JP40[2-1]: H level • JP40[2-3]: L level	refer to *6.1 Operation mode selection*
JP41	FLMD0 level selection • JP41[2-1]: H level • JP41[OPEN]: – if no debug/programming tool connected: L level – controlled by debug/programming tool, if tool connected:	refer to *6.1 Operation mode selection*
JP42	RESETZ_EVA connection • JP42[2-1]: RESETZ_EVA = RESETZ • JP42[OPEN]: RESETZ_EVA ≠ RESETZ	refer to *6.3 RESETZ-EVA signal*

Note: * Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

2.2 Connectors overview

The following table provides an overview of all connectors.

Table 2.2 Connectors overview

Connector	Function	Remark
CN1	MainBoard connectors	refer to *7.1 Connectors to the MainBoard CN1 to CN3*
CN2		
CN3		
CN4	debug connector	refer to *5.1 Debug connector* and *7.2 Debug connector CN4*
CN5	RHSIF & MSPI connector	refer to *6.7 Renesas High-Speed Serial I/F (RHSIF) / Multichannel Serial Peripheral Interface (MSPI)* and *7.3 RHSIF/MSIP connector CN5*
CN6	Aurora trace unit connector	refer to *5.2 Aurora trace* and *7.4 Aurora interface connector CN6*
CN7	Signaling LEDs pin header	refer to *6.4 Signaling LEDs*
CN8	GND for external power supply	refer to *3.1 Board power connection,* connectors are not assembled on the board
CN9	+5.0 V external power supply	
CN10	+3.3 V external power supply	
CN11	+1.12 V external power supply *	
CN12	Pull-up/Pull-down pin header	refer to *6.5 Pull-up/Pull-down pin header* and *7.6 Pull-up/Pull-down pin header* CN12
CN13	Device ports connectors	refer to *7.5 Device ports connectors CN13 to CN16*
CN14		
CN15		
CN16		
CN17	Ethernet interface connector	refer to *6.6 Gigabit Ethernet interface* and *7.7 Ethernet connector CN17*

Note: * Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

2.3 LEDs overview

The following table provides an overview of all LEDs.

Table 2.3 LEDs overview

LED	Function	Color	Remark
LED1	device ERROROUT signal	red	
LED2	Signaling LED	yellow	connection via CN7, refer to *6.4 Signaling LEDs*
LED3	Signaling LED		
LED4	Signaling LED		
LED5	Signaling LED		
LED6	Signaling LED		
LED7	Signaling LED		
LED8	Signaling LED		
LED9	Signaling LED		
LED10	1.09 V device core voltage VDD	green	refer to *3.5 Power supply LEDs*
LED11	5.0 V power supply P5V0	green	
LED12	3.3 V power supply P3V3	green	
LED13	reset switch SW1 on	red	
LED14	device VMONOUT signal	red	
LED15	device PWRCTL signal	red	

3. Power Supply

3.1 Board power connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5 V in case some ports shall be operated with 5 V I/O voltage
- 1.12 V for the device's VDD core voltage supply
  Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

Note

Within this document all voltage values are considered as ‘typical’.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm ‘banana-type’ connectors are used to connect external power supplies:
  - black connector CN8 for GND (VSS)
  - red connector CN9 for 5 V
  - red connector CN10 for 3.3 V
  - red connector CN11 for 1.12 V
    Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

  These connectors are not assembled at delivery of the board, but separately supplied with the board package.

In case the PiggyBack Board is mounted on a MainBoard, all voltages are supplied by the MainBoard.

CAUTION

Do not supply the 5 V (CN9) and 3.3 V (CN10) voltage directly to the PiggyBack Board in case it is mounted on the MainBoard.

Connecting external 1.12 V via CN11 (and GND via CN8) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

3.2 Voltage distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC	3.3 V, 5 V	power supply for I/O ports
LVDVCC	3.3 V, 5 V	power supply for LVDS ports
SYSVCC	3.3 V, 5 V	power supply for • system Logic and internal voltage regulator power • I/O ports
VCC	3.3 V, 5 V	power supply for on-chip flash memory
SVRDRVCC	3.3 V, 5 V	power supply for on-chip Switching Voltage Regulator (SVR)
SVRAVCC	3.3 V, 5 V	
VDDIOF	3.3 V, 5 V	I/O voltage supply for the MainBoard
GETH0PVCC	3.3 V	power supply for Ethernet domain
GETH0BVCC	3.3 V	
GETH0RVCC	3.3 V	
A0VCC, A1VCC, A2VCC	3.3 V, 5 V	A/D Converter's power supplies and reference voltages
A0VREFH, A1VREFH, A2VREFH,	3.3 V, 5 V	
DVDD	1.12 V *	power supply for on-chip debug circuits
DVCC	3.3 V	
EMUVDD	1.12 V *	power supply for Aurora emulator interface signals
EMUVCC	3.3 V	
ERAMVDD	1.12 V *	ERAM circuits of FLASH
ERAMVCC	3.3 V	

Note: * Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

Each of the above voltages can be selected from

- 5.0 V, 3.3 V (where applicable, see table above)
- off

by a set of jumpers. For details refer to the figure below and *Table 2.1 Jumpers overview (cont'd)*.

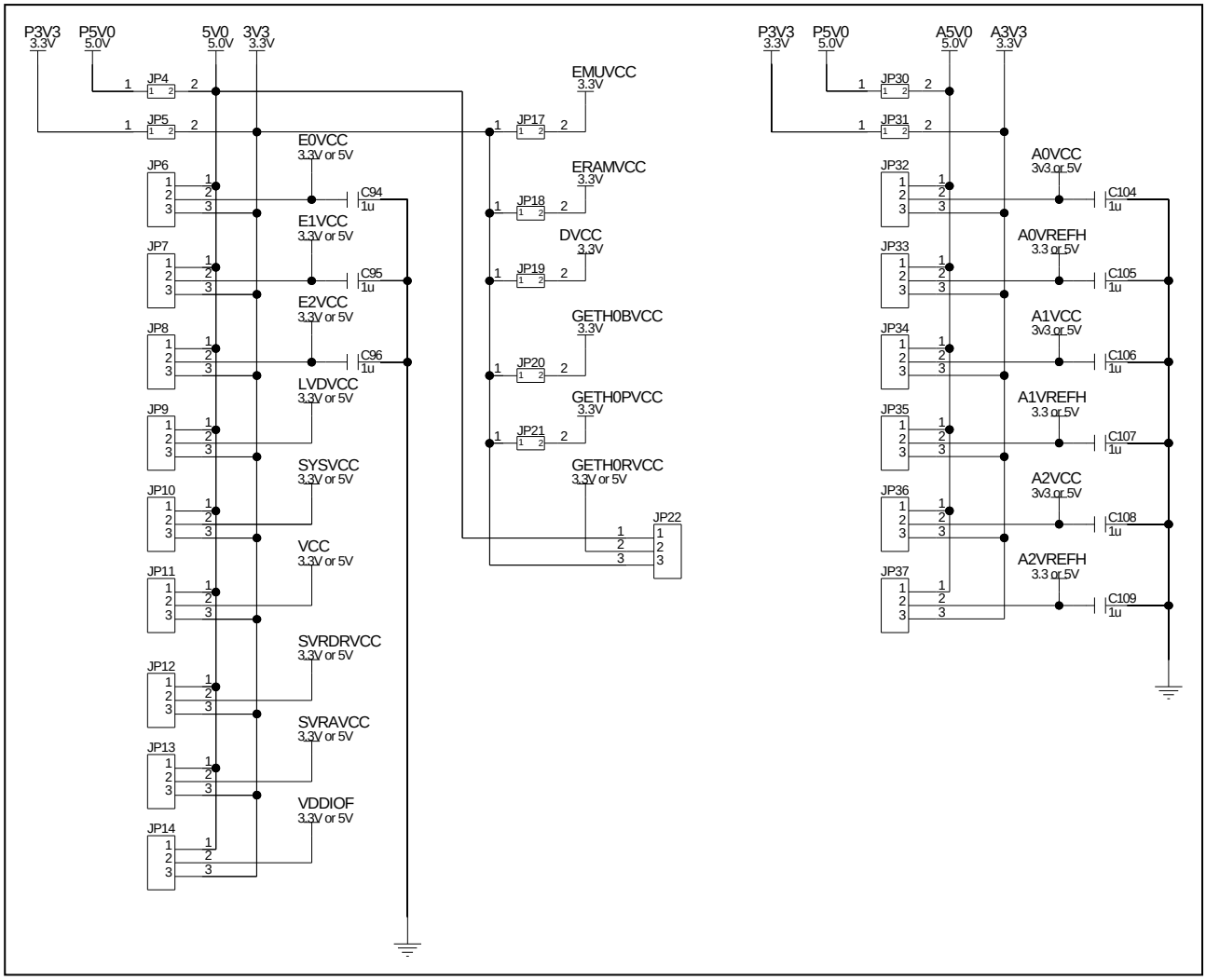


Figure 3.1 Voltage distribution

3.3 Device core voltages (xVDD) selection

The following VDD voltages must be supplied to the devices:

- RH850/U2A16: VDD
- RH850/U2A-EVA: VDD, DVDD, ERAMVDD, EMUVDD

The device core voltage VDD (typ.1.09 V) can be

- supplied from external via CN11 (voltage In_1v12)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC16 (voltage reg_vss_VDD)
- generated by the on-chip Switching Voltage Regulator (SVR) in combination with device external power transistors TR1, TR2 (voltage SVR_OUTPUT)

Note

The In_1v12 and reg_vss_VDD voltages have a level of typical 1.12 V, which is higher than the typical device core voltages VDD of 1.09 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

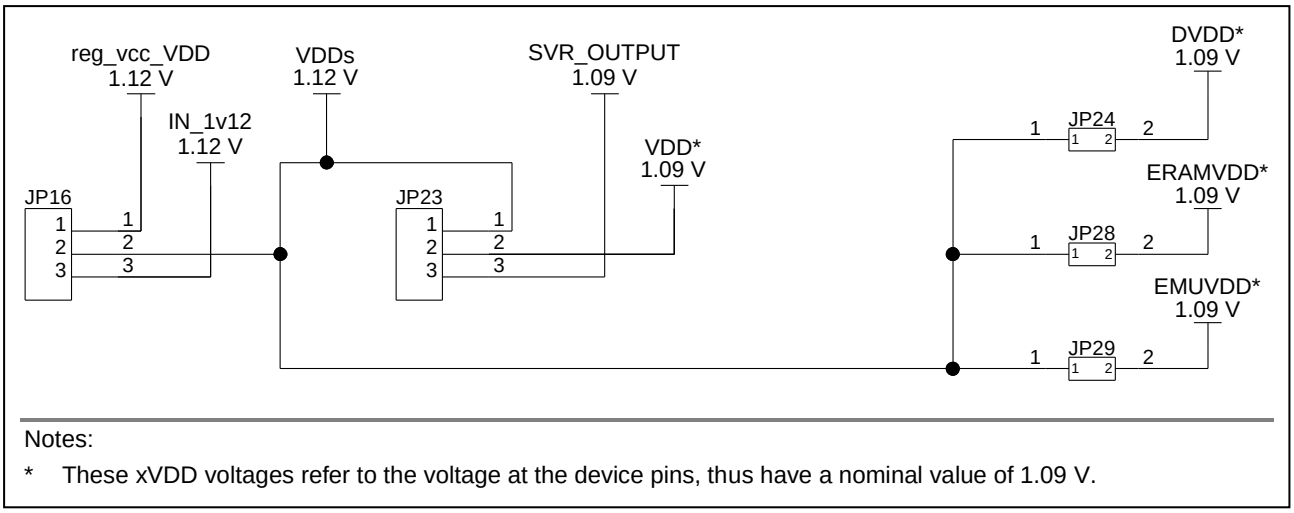
Selection of the VDD source is achieved by use of the jumpers JP23 and JP16:

- JP23[2-1]: VDD = 1.12 V (VDDs) from
  - JP16[2-1]: VDDs = reg_vss_VDD from on-board voltage regulator IC16
  - JP16[2-3]: VDDs = IN_1v12 from external supply CN11
- JP23[2-3]: VDD = 1.09 V (SVR_OUTPUT)

Note

All other - RH850/U2A-EVA related - VDD voltages are always sourced from the 1.12 V voltages reg_vss_VDD (JP16[2-1]) or IN_1v12 (JP16[2-3]).

Note that the nominal voltages DVDD, ERAMVDD and EMUVDD at the device pins are also 1.09 V.



Notes:

* These xVDD voltages refer to the voltage at the device pins, thus have a nominal value of 1.09 V.

Figure 3.2 Device core voltages (xVDD) selection

3.4 Current measurement bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP4 and JP5 with a current meter.

Accordingly, the total current via the A/D Converter's supply voltages A5V0 and A3V3 can be measured via the jumpers JP30 and JP31 respectively.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.1 Voltage distribution*.

3.5 Power supply LEDs

The following green LEDs indicate the presence of various voltages on the PiggyBack Board:

- LED11 for 5.0 V power rail P5V0
- LED12 for 3.3 V power rail P3V3
- LED10 for 1.09 V device core voltage VDD

4. Clock Supply

The device's operation clock can be generated by

- the on-chip oscillator MainOsc circuit in combination with an off-chip resonator, connected to the X1, X2 terminals
- an off-chip oscillator, the clock is fed into the X1 terminal

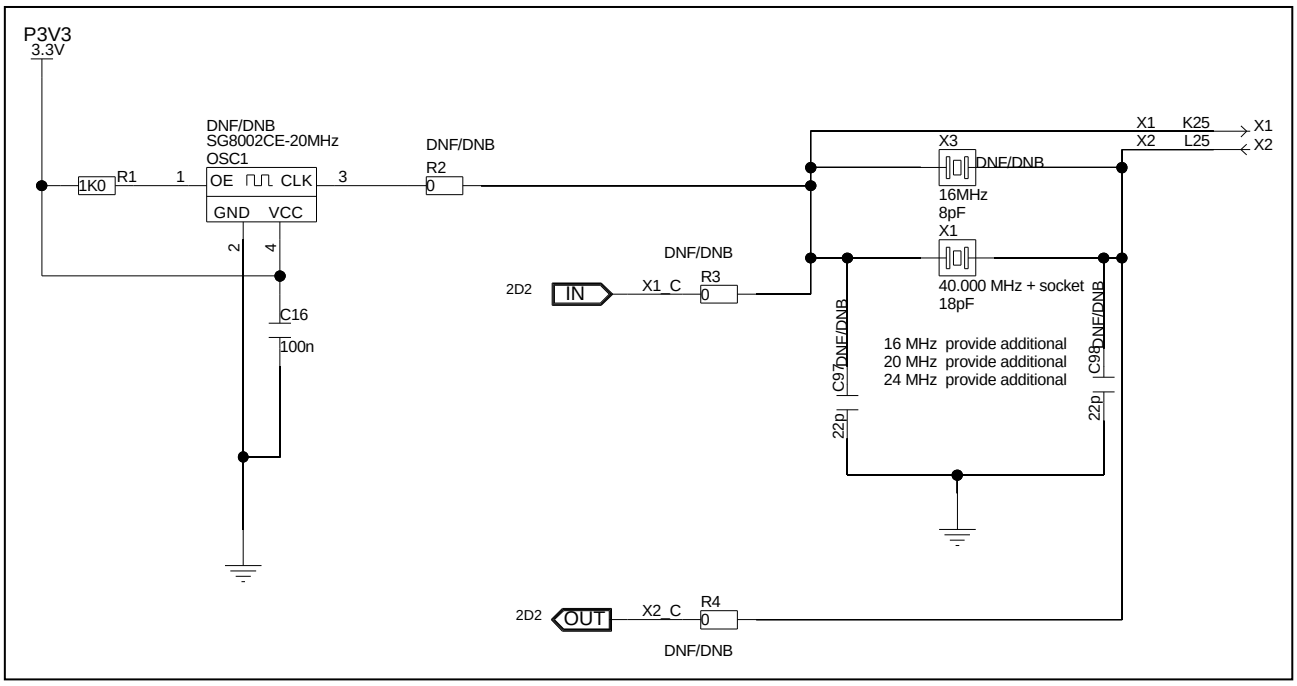


Figure 4.1 Clock supply

4.1 MainOsc

For operating the on-chip MainOsc the PiggyBack Board provides a socket (X1) for a resonator.

Optionally a resonator (X3) can be soldered on the board, refer to the figure above.

Several resonators for various MainOsc frequencies (16 MHz, 20 MHz, 24 MHz, 40 MHz) are included in the board package. For package content please refer to *1.1 Package Components*

4.2 Programmable oscillator

Instead of using the on-chip MainOsc a programmable crystal oscillator (OSC1) circuit can be soldered on the board.

The available footprint and circuitry is designed for a SG-8002CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via resistor R2.

The SG-8002CE is neither mounted on nor provided with the board. For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 or soldered on X3 must not be used in parallel to another clock source.

4.3 X1 and X2 on CN15

To minimize disturbance on the resonator signal the signals X1 and X2 are by default not connected to a pin header. If needed the signals can be connected to CN15 via 0 Ω resistors:

- X1: A19 pin of CN15 to supply an external clock to the device via R3
- X2: A18 pin of CN15 for measurement purposes of the clock via R4

Note

By default the X1 and X2 signals are not connected to CN15 in order to minimize signal integrity disturbance. Upon demand they can be connected via 0 Ω resistors R3 and R4.

5. Debug, Trace and Flash Programming Interfaces

5.1 Debug connector

For debugging and flash programming purposes debug and flash programming tools can be connected to the CN4 connector.

Refer to *7.2 Debug connector CN4* for details about the CN4 pin assignment.

5.2 Aurora trace connector

A trace unit can be connected via the CN6 connector.

Refer to *7.4 Aurora interface connector CN6* for details about the CN4 pin assignment.

5.3 EVTI and EVTO signals

Depending on the used tool output it might be necessary to pull the EVTI and/or EVTO signal to H level via a pull-up resistor:

- JP2 set: EVTI pulled up to H level
- JP3 set: EVTO pulled up to H level

Note

Please refer to the documentation of the used tool, whether this is needed.

6. Other Circuitry

6.1 Operation mode selection

The PiggyBack Board gives the possibility to configure the following jumpers for selection of the device operation mode:

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP38	MODE0 pin level • JP38[2-1]: MODE0 = H level • JP38[2-3]: MODE0 = GND
JP41	FLMD0 pin level • JP41[SHORT]: FLMD0 = H level • JP41[OPEN]: FLMD0 – controlled by debugger or programming tool, if a tool is connected via CN4 or CN6 – GND, if no tool connected
JP39	FLMD1 pin level • JP39[SHORT]: FLMD1 = H level • JP39[OPEN]: FLMD1 = GND
JP40	FLMD2 pin level • JP40[2-1]: FLMD2 = H level • JP40[2-3]: FLMD2 = GND

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In the very most cases the 'Normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'Normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP41.

All other jumpers related to the mode selection can be left open.

6.2 RESET switch

The SW1 is used to issue a RESET to the device.

The SW1 toggle switch allows to activate the RESET in two different ways:

- SW1 in left '2-1(ON)' position: temporary reset
  Releasing the switch's lever returns the switch into its middle 'OFF' position and thus releases the reset.
- SW1 in right '2-3 ON' position: permanent reset
  For reset release the switch has to be moved back manually into its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

The lighted red LED13 indicates that SW1 is "on", i.e. in position '2-1 (ON)' or '2-3 ON'.

Note

LED13 does not light up when RESET is asserted by any other means than SW1.

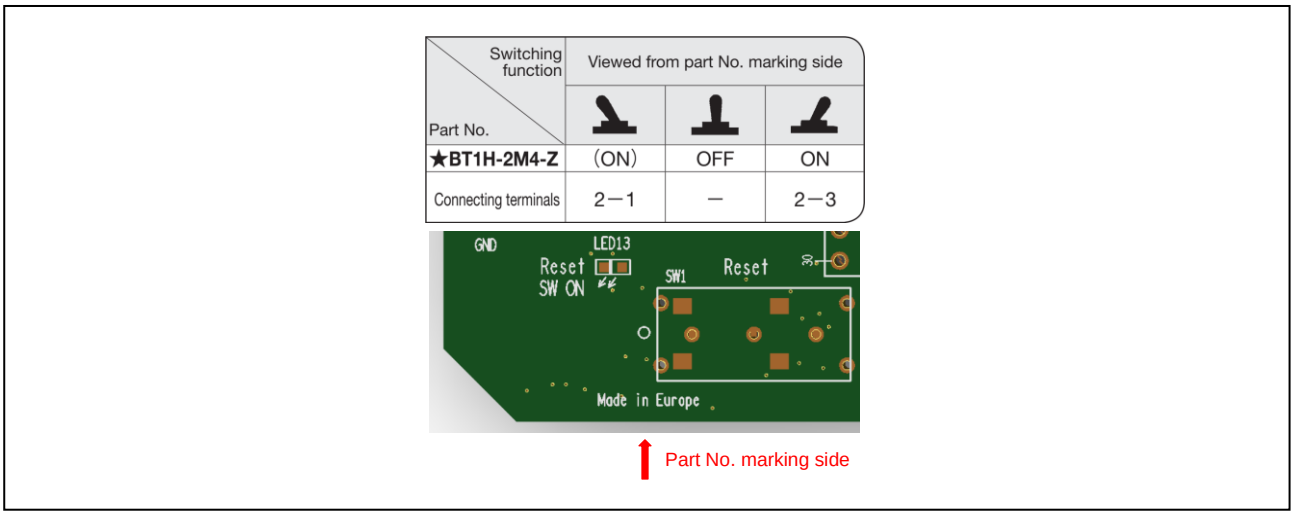


Figure 6.1 RESET switch SW1

6.3 RESETZ-EVA signal

By closing the jumper JP42 the device reset RESETZ asserts also following other resets (RESETZ_EVA):

- AURORES1Z
- AURORES2Z
- ERAMRESPDZ
- ERAMRES2Z

Note

The RESETZ_EVA signal affects board components which are used by an Aurora debugger interacting with the RH850/U2A-EVA device.

Thus, remove JP42 when the board is equipped with the RH850/U2A16 device.

Refer to chapter 9.3 for precautions possibly affecting your board revision.

6.4 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

Device pins P11_0 to P11_7 are connected to the odd pins of the pin header CN7, while the LEDs 2 to 9 are connected to the even CN7 pins.

Thus, the LEDs can be either connected to

- the device port pins P11_0 to P11_7 by closing the connection on CN7 using a jumper, or
- any device pin by connecting directly with the even CN7 pins using a separate cable.

6.5 Pull-up/Pull-down pin header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN12 pin to the signal via a separate cable.

The CN12 pins have following pull-up or pull-down voltage levels:

- all even numbered pins are connected to L level, i.e. to GND
- odd numbered pins 1, 3, 5, 7, 9, can be connected to
  - 5.0 V, if JP25[2-1] is set
  - 3.3 V, if JP25[2-3] is set
- odd numbered pins 11, 13, 15, 17, can be connected to
  - 5.0 V, if JP15[2-1] is set
  - 3.3 V, if JP15[2-3] is set

Refer to *7.6 Pull-up/Pull-down pin header* CN12 for CN12 details.

6.6 Gigabit Ethernet interface

The PiggyBack Board features a Marvell 88E1112-XX-NNC-I000 Gigabit Ethernet PHY (IC14) for using the device's Gigabit Ethernet SGMII interface (ETNB1) via the RJ45 type connector CN17.

Notes

1. For ETNBx initial setup please refer to the device UM. For ETNB1 operation the ETNB1SGCLKSEL register must be set to ETNB1SGCLKSEL=0x01 to select the Internal MOSC clock of 20MHz.
   For an internal MOSC clock of 20MHz the crystal X1 has to be replaced by the 20MHz crystal included in the package.
   For package content please refer to *Table 1.1 Package Components for the Y-RH850-U2A-516PIN-PB-T1-V1*
2. The signals of the device's Fast Ethernet (R)MII interface (ETNB0) are available on the MainBoard connectors. Thus, ETNB0 can control an Ethernet PHY on the MainBoard.
3. Alternatively, ETNB1 can also be used to operate the MainBoard's 100 MB Ethernet PHY. In this case the ETNB1 Fast Ethernet mode is selected by Option Bytes settings and the pin multiplexing needs to be configured accordingly.

Refer to *7.7 Ethernet connector CN17* for the CN17 pin assignment.

The device's LVDS Rx and Tx signals of the Ethernet interface can be swapped towards the Ethernet PHY by setting the jumper JP26. The correct JP26 setting depends on the device on the PiggyBack Board:

- JP26[OPEN]: for RH850/U2A-EVA
  - device pins N21/P21 (TX_DATAP/TX_DATAN) used as Ethernet Tx signals
  - device pins P22/R22 (RX_DATAP/RX_DATAN) used as Ethernet Rx signals
- JP26[2-1]: for RH850/U2A16

- device pins N21/P21 (TX_DATAP/TX_DATAN) used as Ethernet Rx signals
- device pins P22/R22 (RX_DATAP/RX_DATAN) used as Ethernet Tx signals

6.7 Renesas High-Speed Serial I/F (RHSIF) / Multichannel Serial Peripheral Interface (MSPI)

The CN5 connector can be used to connect to the device's RHSIF and MSPI0 interface.

Refer to *7.3 RHSIF/MSIP connector CN5* for the CN5 pin assignment.

The MSPI0 interface at CN5 is operated in LVDS mode.

The CN5 Rx and Tx signals of the RHSIF can be swapped by setting the jumper JP1:

- JP1[2-1]:
  - RXDP/RXDN at CN5 pins 1 and 3
  - TXDP/TXDN at CN5 pins 7 and 9
- JP1[2-3]:
  - RXDP/RXDN at CN5 pins 7 and 9
  - TXDP/TXDN at CN5 pins 1 and 3

Notes

1. By default all signals are not connected to the CN5 in order to minimize signal integrity disturbance. Upon demand they can be connected via 0 Ω resistors R15 to R18 and R21 to R23.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another PiggyBack Board via separate cables.

7. Connectors

7.1 Connectors to the MainBoard CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the PiggyBack Board to a MainBoard.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the MainBoard, please refer to the User's Manual of any supported MainBoard.

Refer to *1.2 Supported MainBoards* for a list of supported MainBoards.

7.1.1 MainBoard connector CN1

Table 7.1 MainBoard connector CN1

Pin	MainBoard function	PiggyBack Board device port	Pin	MainBoard function	PiggyBack Board device port
1	VDDA	–	2	VDDA	–
3	VDDA	–	4	VDDA	–
5	RESET	RESETZ	6	NMI	P4_7
7	–	–	8	–	–
9	INT0	P10_12	10	INT1	P22_0
11	INT2	P21_7	12	INT3	P2_8
13	–	–	14	–	–
15	UART0TX	P6_6	16	UART1TX	P6_3
17	UART0RX	P6_5	18	UART1RX	P6_2
19	LIN0TX	P4_8	20	LIN1TX	P2_5
21	LIN0RX	P4_9	22	LIN1RX	P2_4
23	IIC0SCL	P17_3	24	IIC1SCL	P22_4
25	IIC0SDA	P17_2	26	IIC1SDA	P22_3
27	CAN0TX	P6_14	28	CAN1TX	P6_8
29	CAN0RX	P6_13	30	CAN1RX	P6_7
31	SENT0RX	P21_1	32	SENT1RX	P21_0
33	SENT0SPCO	P24_6	34	SENT1SPCO	P24_7
35	PSI5SRX0	P3_6	36	PSI5RX0	P5_4
37	PSI5STX0	P3_7	38	PSI5TX0	P5_6
39	PSI5SCLK0	P3_8	40	–	–
41	FLX0TX	P20_7	42	FLX0EN	P20_5
43	FLX0RX	P20_2	44	FLXSTPWT	P20_4
45	FLX1TX	P20_6	46	FLX1EN	P20_8
47	FLX1RX	P20_3	48	FLX CLK	P10_8
49	–	–	50	–	–
51	ETH0MDIO	P20_3	52	ETH0MDC	P20_6

Table 7.1 MainBoard connector CN1 (cont'd)

Pin	MainBoard function	PiggyBack Board device port
53	ETH0RXD0	P10_3
55	ETH0RXD1	P10_4
57	ETH0RXD2	P10_5
59	ETH0RXD3	P10_6
61	ETH0RXCLK	P10_2
63	ETH0RXER	P10_0
65	ETH0CRSDV	P20_7
67	ETH0RXDV	P10_7
69	ETH0RESET	P20_0
71	–	–
73	USB0UDMF	–
75	USB0UDPF	–
77	–	–
79	–	–
81	–	–
83	–	–
85	DIGIO_0	P21_2
87	DIGIO_2	P21_4
89	DIGIO_4	P21_6
91	DIGIO_6	P22_0
93	DIGIO_8	P22_2
95	DIGIO_10	P10_8
97	DIGIO_12	P10_10
99	DIGIO_14	P10_12
101	–	–
103	MUX0	P6_0
105	MUX2	P6_3
107	ADC0	AP4_0
109	ADC2	AP4_2
111	ADC4	AP4_4
113	ADC6	AP4_6
115	VDDIOF	–
117	VDDB	–
119	VDDB	–

Pin	MainBoard function	PiggyBack Board device port
54	EH0TXD0 or ETNB0TXD0	P20_9
56	EH0TXD1 or ETNB0TXD1	P20_10
58	EH0TXD2 or ETNB0TXD2	P20_12
60	EH0TXD3 or ETNB0TXD3	P20_13
62	ETH0TXCLK	P10_1
64	ETH0TXER	P20_8
66	ETH0TXEN	P20_14
68	ETH0COL	–
70	ETH0LINK	P20_1
72	–	–
74	USB0UDMH	–
76	USB0UDPH	–
78	–	–
80	–	–
82	–	–
84	–	–
86	DIGIO_1	P21_3
88	DIGIO_3	P21_5
90	DIGIO_5	P21_7
92	DIGIO_7	P22_1
94	DIGIO_9	P22_3
96	DIGIO_11	P10_9
98	DIGIO_13	P10_11
100	DIGIO_15	P10_13
102	–	–
104	MUX1	P6_2
106	–	–
108	ADC1	AP4_1
110	ADC3	AP4_3
112	ADC5	AP4_5
114	ADC7	AP4_7
116	VDDIOF	–
118	VDDB	–
120	VDDB	–

7.1.2 MainBoard connector CN2

Table 7.2 MainBoard connector CN2

Pin	Function	Device port
1	CAN2TX	P3_2
3	CAN2RX	P3_3
5	CAN4TX	P4_6
7	CAN4RX	P4_7
9	LIN2TX	P2_0
11	LIN2RX	P2_1
13	LIN4TX	P6_12
15	LIN4RX	P6_15
17	LIN6TX	P2_7
19	LIN6RX	P2_6
21	LIN8TX	P4_0
23	LIN8RX	P4_1
25	LIN10TX	P6_5
27	LIN10RX	P6_4
29	LIN12TX	P0_1
31	LIN12RX	P0_0
33	LIN14TX	P0_5
35	LIN14RX	P0_3
37	–	–
39	CAN12Tx	P1_8
41	CAN12Rx	P1_9
43	CAN14Tx	P8_0
45	CAN14Rx	P8_1
47	CAN6TX	P4_14
49	CAN6RX	P4_15
51	CAN8TX	P1_0
53	CAN8RX	P1_1
55	CAN10TX	P1_4
57	CAN10RX	P1_5
59	–	–
61	LIN16TX	P0_10
63	LIN16RX	P0_8
65	LIN18TX	P1_13
67	LIN18RX	P1_12
69	LIN20TX	P3_1
71	LIN20RX	P3_0
73	LIN22TX	P3_12
75	LIN22RX	P3_11

Pin	Function	Device port
2	CAN3TX	P4_4
4	CAN3RX	P4_5
6	CAN5TX	P4_11
8	CAN5RX	P4_12
10	LIN3TX	P4_14
12	LIN3RX	P4_15
14	LIN5TX	P2_2
16	LIN5RX	P2_3
18	LIN7TX	P3_5
20	LIN7RX	P3_4
22	LIN9TX	P5_3
24	LIN9RX	P5_2
26	LIN11TX	P3_8
28	LIN11RX	P3_7
30	LIN13TX	P0_4
32	LIN13RX	P0_2
34	LIN15TX	P0_7
36	LIN15RX	P0_6
38	–	–
40	CAN13Tx	P1_10
42	CAN13Rx	P1_11
44	CAN15Tx	P8_2
46	CAN15Rx	P8_3
48	CAN7TX	P3_4
50	CAN7RX	P3_5
52	CAN9TX	P1_2
54	CAN9RX	P1_3
56	CAN11TX	P1_6
58	CAN11RX	P1_7
60	–	–
62	LIN17TX	P0_11
64	LIN17RX	P0_9
66	LIN19TX	P1_15
68	LIN19RX	P1_14
70	LIN21TX	P3_10
72	LIN21RX	P3_9
74	LIN23TX	P3_14
76	LIN23RX	P3_13

Table 7.2 MainBoard connector CN2 (cont'd)

Pin	Function	Device port
77	–	–
79	SFMA0CLK	P17_5
81	SFMA0IO0	P17_3
83	SFMA0IO2	P17_1
85	–	–
87	MMCA0CLK	P24_4
89	MMCA0DAT0	P24_6
91	MMCA0DAT2	P24_8
93	MMCA0DAT4	P24_10
95	MMCA0DAT6	P24_12
97	–	–
99	ETH1MDIO	P3_7
101	ETH1RXD0	P23_3
103	ETH1RXD1	P23_4
105	ETH1RXD2	P23_5
107	ETH1RXD3	P23_6
109	ETH1RXCLK	P23_2
111	ETH1RXER	P23_0
113	ETH1CRSDV	–
115	ETH1RXDV	P23_1
117	ETH1RESET	P9_0
119	–	–

Pin	Function	Device port
78	–	–
80	SFMA0SSL	P17_4
82	SFMA0IO1	P17_2
84	SFMA0IO3	P17_0
86	–	–
88	MMCA0CMD	P24_5
90	MMCA0DAT1	P24_7
92	MMCA0DAT3	P24_9
94	MMCA0DAT5	P24_11
96	MMCA0DAT7	P24_13
98	–	–
100	ETH1MDC	P3_6
102	ETH1TXD0	P23_10
104	ETH1TXD1	P23_11
106	ETH1TXD2	P23_12
108	ETH1TXD3	P23_13
110	ETH1TXCLK	P23_9
112	ETH1TXER	P23_7
114	ETH1TXEN	P23_8
116	ETH1COL	–
118	ETH1LINK	P21_13
120	–	–

7.1.3 MainBoard connector CN3

Table 7.3 MainBoard connector CN3

Pin	Function	Device port
1	CSI0CS0	P21_7
3	CSI0CS1	P21_6
5	CSI0CS2	P21_5
7	CSI0CS3	P21_4
9	–	–
11	–	–
13	PSI5SRX1	P6_13
15	PSI5STX1	P6_14
17	PSI5SCLK1	P6_15
19	–	–
21	CSI1CS2	P24_9

Pin	Function	Device port
2	CSI0CLK	P22_4
4	CSI0SI	P22_1
6	CSI0SO	P22_0
8	–	–
10	CSI1CS1	P24_8
12	–	–
14	PSI5RX1	P5_2
16	PSI5TX1	P5_3
18	–	–
20	–	–
22	CSI1CS3	P4_8

Table 7.3 MainBoard connector CN3 (cont'd)

Pin	Function	Device port
23	–	–
25	–	–
27	–	–
29	CSI1SCLK	P24_4
31	–	–
33	–	–
35	–	–
37	–	–
39	–	–
41	–	–
43	–	–
45	–	–
47	–	–
49	–	–
51	–	–
53	–	–
55	AD1_0	AP2_0
57	AD1_2	AP2_2
59	AD1_4	AP2_4
61	AD1_6	AP2_6
63	PWM0	P24_4
65	PWM2	P24_6
67	PWM4	P24_8
69	PWM6	P24_10
71	DIGIO16	P11_8
73	DIGIO18	P11_10
75	DIGIO20	P11_12
77	DIGIO22	P11_14
79	ENC0	P10_8
81	–	–
83	–	–
85	–	–
87	–	–
89	–	–
91	–	–
93	–	–
95	–	–
97	–	–
99	–	–

Pin	Function	Device port
24	CSI1CS0	P24_7
26	DIGIO_24	P17_6
28	CSI1SO	P24_6
30	CSI1SI	P24_5
32	–	–
34	–	–
36	–	–
38	–	–
40	–	–
42	–	–
44	–	–
46	–	–
48	–	–
50	–	–
52	–	–
54	–	–
56	AD1_1	AP2_1
58	AD1_3	AP2_3
60	AD1_5	AP2_5
62	AD1_7	AP2_7
64	PWM1	P24_5
66	PWM3	P24_7
68	PWM5	P24_9
70	PWM7	P24_11
72	DIGIO17	P11_9
74	DIGIO19	P11_11
76	DIGIO21	P11_13
78	DIGIO23	P11_15
80	ENC1	P10_9
82	–	–
84	–	–
86	–	–
88	–	–
90	–	–
92	–	–
94	–	–
96	–	–
98	–	–
100	–	–

Table 7.3 MainBoard connector CN3 (cont'd)

Pin	Function	Device port
101	–	–
103	–	–
105	–	–
107	–	–
109	–	–
111	–	–
113	–	–
115	–	–
117	–	–
119	–	–

Pin	Function	Device port
102	–	–
104	–	–
106	–	–
108	–	–
110	–	–
112	–	–
114	–	–
116	–	–
118	–	–
120	–	–

7.2 Debug connector CN4

Table 7.4 On-Chip Debugger connector CN4

Pin	Function	Device port
1	TDCK / LPDCLK / FPCK	JP0_2
3	TRSTZ	
5	TDO / LPDO / FPDT	JP0_1
7	TDI / LPDIO / FPDR	JP0_0
9	TMS	JP0_3
11	RDY / LPDCLKOUT	JP0_5
13	RESETZ	

Pin	Function	Device port
2	GND	
4	FLMD0	
6	–	
8	E0VCC	
10	EVTOZ	
12	GND	
14	GND	

7.3 RHSIF/MSIP connector CN5

Table 7.5 RHSIF/MISP connector CN5

Pin	JP1[2-1]		JP1[2-3]	
	Device port	Function	Device port	Function
1	P2_13	HSIF0_TXDP / MSPI0_SOP	P2_11	HSIF0_RXDP / MSPI0_SIP
2	P2_15	MSPI0_SCKP	P2_15	GND
3	P2_12	HSIF0_TXDN / MSPI0_SON	P2_10	HSIF0_RXDN / MSPI0_SIN
4	P2_14	MSPI0_SCKN	P2_14	MSPI0_SCKN
5	–	GND	–	GND
6	P2_9	HSIF0_REFCLK / MSPI0CSS4	P2_9	HSIF0_REFCLK
7	P2_11	HSIF0_RXDP / MSPI0_SIP	P2_13	HSIF0_TXDP / MSPI0_SOP
8	–	GND	–	GND

Table 7.5 RHSIF/MISP connector CN5 cont'd

Pin	JP1[2-1]		JP1[2-3]	
	Device port	Function	Device port	Function
9	P2_10	HSIF0_RXDN / MSPI0_SIN	P2_12	HSIF0_TXDN / MSPI0_SON
10	–	GND	–	GND
11	–	GND	–	GND
12	–	GND	–	GND

Note

By default all signals are not connected to CN5 in order to minimize signal integrity disturbance. Upon demand they can be connected via 0 Ω resistors R15 to R18 and R21 to R23.

7.4 Aurora interface connector CN6

Table 7.6 Aurora interface connector CN6

Pin	Function	Device port
1	TODP0	
3	TODN0	
5	GND	
7	TODP1	
9	TODN1	
11	GND	
13	TODP2	
15	TODN2	
17	GND	
19	TODP3	
21	TODN3	
23	GND	
25	NC	
27	NC (WDTDIS)	–
29	GND	
31	NC (ETK-BREQ)	–
33	NC (ETK-BGNT)	–

Pin	Function	Device port
2	E0VCC	
4	TCK / LPDCLKI	JP0_2
6	RMS	JP0_3
8	TDI / LPDI	JP0_0
10	TDO / LPDO	JP0_1
12	TRSTZ	
14	FLMD0	
16	EVTIZ	
18	EVTOZ	
20	FLMD1	P6_13
22	RESETZ	
24	GND	
26	CICREFP	
28	CICREFN	
30	GND	
32	RDYZ / LPDCLKO	JP0_5
34	RESETOUTZ	P6_10

7.5 Device ports connectors CN13 to CN16

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.5.1 Device ports connector CN13

Table 7.7 Device ports connector CN13

Pin	Device port	Pin	Device port	Pin	Device port
A1	P1_1	B1	P1_0	C1	P1_3
A2	P1_2	B2	AP0_7	C2	P1_5
A3	P1_4	B3	AP0_13	C3	P1_7
A4	P1_6	B4	AP0_12	C4	P1_9
A5	P1_8	B5	AP0_10	C5	P1_11
A6	P1_10	B6	AP0_9	C6	P1_13
A7	P1_12	B7	P3_2	C7	P24_7
A8	P24_4	B8	AP0_11	C8	P1_14
A9	P3_3	B9	P4_0	C9	P4_1
A10	P4_4	B10	P24_5	C10	P4_5
A11	P4_6	B11	P24_6	C11	P24_11
A12	P24_8	B12	P24_9	C12	P1_15
A13	P4_8	B13	P24_10	C13	P4_3
A14	P4_2	B14	P4_7	C14	P4_9
A15	P4_10	B15	P24_12	C15	P4_11
A16	P4_12	B16	P24_13	C16	P3_15
A17	P3_14	B17	P4_14	C17	P3_13
A18	P3_12	B18	P4_13	C18	P3_11
A19	P3_10	B19	P4_15	C19	P3_1
A20	GND	B20	–	C20	–

7.5.2 Device ports connector CN14

Table 7.8 Device ports connector CN14

Pin	Device port
A1	P11_15
A2	P21_5
A3	P21_6
A4	P21_7
A5	P17_6
A6	P17_5
A7	P17_2
A8	P17_4
A9	P17_3
A10	P18_2
A11	P18_1
A12	P18_0
A13	P9_8
A14	AP2_6
A15	AP2_4
A16	AP2_2
A17	P9_7
A18	P9_5
A19	P9_3
A20	P9_1
A21	AP2_0
A22	AP3_0
A23	P12_4
A24	P12_2
A25	P12_0
A26	AP0_0
A27	AP0_2
A28	AP0_4
A29	AP0_5
A30	AP0_8

Pin	Device port
B1	P19_1
B2	P19_3
B3	P19_5
B4	P18_14
B5	P18_12
B6	P18_10
B7	P18_8
B8	P18_6
B9	P18_4
B10	P18_3
B11	P10_10
B12	P10_12
B13	P10_14
B14	P17_1
B15	AP2_10
B16	AP2_8
B17	P9_6
B18	P9_4
B19	P9_2
B20	P9_0
B21	AP2_14
B22	AP2_15
B23	AP3_3
B24	AP3_1
B25	AP2_12
B26	AP1_3
B27	AP1_2
B28	AP1_0
B29	AP0_6
B30	ERAMRES2Z

Pin	Device port
C1	P19_0
C2	P19_2
C3	P19_4
C4	P18_15
C5	P18_13
C6	P18_11
C7	P18_9
C8	P18_7
C9	P18_5
C10	P10_9
C11	P10_11
C12	P10_13
C13	P17_0
C14	AP2_13
C15	AP2_11
C16	AP2_9
C17	AP2_7
C18	AP2_5
C19	AP2_3
C20	AP2_1
C21	AP3_2
C22	P12_5
C23	P12_3
C24	P12_1
C25	AP0_1
C26	AP1_1
C27	AP0_3
C28	ERAMRESPDZ
C29	AP0_15
C30	AP0_14

7.5.3 Device ports connector CN15

Table 7.9 Device ports connector CN15

Pin	Device port
A1	AP4_12
A2	AP4_10
A3	AP4_8
A4	AP4_6
A5	P3_5
A6	P6_11
A7	P6_2
A8	P6_3
A9	P6_5
A10	P6_7
A11	P6_9
A12	P6_15
A13	P6_13
A14	JP0_5
A15	JP0_2
A16	JP0_0
A17	GETH0VCL
A18	X2_C *
A19	X1_C *
A20	AURORES1Z
A21	AURORES2Z
A22	AURORESPDZ
A23	P2_1
A24	P0_4
A25	P0_3
A26	P5_6
A27	P2_0
A28	P2_2
A29	P2_3
A30	P2_5

Pin	Device port
B1	P3_0
B2	AP5_3
B3	AP4_11
B4	AP4_9
B5	AP4_7
B6	AP4_5
B7	P3_4
B8	P6_4
B9	P6_6
B10	P6_8
B11	P6_12
B12	P6_10
B13	P6_14
B14	JP0_3
B15	JP0_1
B16	TRSTZ
B17	GND
B18	PWRCTL
B19	P5_2
B20	P5_4
B21	P0_11
B22	P0_9
B23	P0_7
B24	P0_5
B25	P0_1
B26	AWOVCL
B27	MSYNZ
B28	EVTIZ
B29	AUDATA0
B30	AUDATA2

Pin	Device port
C1	P3_9
C2	AP5_2
C3	AP5_1
C4	AP5_0
C5	AP4_15
C6	AP4_14
C7	AP4_13
C8	AP4_4
C9	AP4_0
C10	AP4_3
C11	AP4_2
C12	AP4_1
C13	P6_0
C14	P3_6
C15	P3_7
C16	RESETZ
C17	P3_8
C18	VMONOUTZ
C19	P5_3
C20	FLMD0
C21	P0_12
C22	P0_10
C23	P0_8
C24	P0_6
C25	P0_2
C26	P0_0
C27	P2_4
C28	P2_6
C29	EVTOZ
C30	AUDATA1

Note * By default these signals are not connected to CN15 in order to minimize signal integrity disturbance. Upon demand they can be connected via 0 Ω resistors R3 and R4.

7.5.4 Device ports connector CN16

Table 7.10 Device ports connector CN16

Pin	Device port
A1	P2_7
A2	CN_P2_9 *
A3	P2_8
A4	CN_P2_12 *
A5	CN_P2_11 *
A6	CN_P2_13 *
A7	CN_P2_15 *
A8	P22_3
A9	P22_4
A10	P22_1
A11	P22_2
A12	P22_0
A13	P20_0
A14	P20_2
A15	P20_4
A16	P20_6
A17	P20_8
A18	P20_10
A19	P20_13
A20	P20_14
A21	ERROROUTZ
A22	P21_12
A23	P11_0
A24	P11_2
A25	P11_4
A26	P11_6
A27	P11_8
A28	P11_10
A29	P11_12
A30	P11_14

Pin	Device port
B1	AUDATA3
B2	AUDSYNCZ
B3	CN_P2_10 *
B4	CN_P2_14 *
B5	P8_10
B6	P8_8
B7	P8_6
B8	P8_4
B9	P8_2
B10	P20_1
B11	P20_3
B12	P20_5
B13	P20_7
B14	P20_9
B15	P20_12
B16	P23_12
B17	P23_10
B18	P23_8
B19	P23_6
B20	P23_4
B21	P23_2
B22	P20_15
B23	P10_1
B24	P10_2
B25	P10_3
B26	P10_4
B27	P10_5
B28	P10_6
B29	P10_7
B30	P10_8

Pin	Device port
C1	AUDRSTZ
C2	AUDCK
C3	P8_9
C4	P8_7
C5	P8_5
C6	P8_3
C7	P8_1
C8	P8_0
C9	P21_0
C10	P21_1
C11	P21_2
C12	P21_3
C13	P21_4
C14	P23_13
C15	P23_11
C16	P23_9
C17	P23_7
C18	P23_5
C19	P23_3
C20	P23_1
C21	P23_0
C22	P21_13
C23	P10_0
C24	P11_1
C25	P11_3
C26	P11_5
C27	P11_7
C28	P11_9
C29	P11_11
C30	P11_13

Note * By default these signals are not connected to CN16 in order to minimize signal integrity disturbance. Upon demand they can be connected via 0 Ω resistors R15 to R18 and R21 to R23.

7.6 Pull-up/Pull-down pin header CN12

Pin	Function
1	fixed H level, depends on JP25: • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V
3	
5	
7	
9	
11	fixed H level, depends on JP15: • JP15[2-1]: 5.0 V • JP15[2-3]: 3.3 V
13	
15	
17	
19	

Pin	Function
2	fixed L level
4	
6	
8	
10	
12	
14	
16	
18	
20	

7.7 Ethernet connector CN17

Table 7.11 Ethernet connector CN17

Pin	Function
1	TRCT3
2	TRD3_MINUS
3	TRD3_PLUS
4	TRD2_PLUS
5	TRD2_MINUS
6	TRCT2
7	TRCT4

Pin	Function
8	TRD4_PLUS
9	TRD4_MINUS
10	TRD1_MINUS
11	TRD1_PLUS
12	TRCT1
13	YEL_MINUS
14	YEL_PLUS

Pin	Function
15	ORN_MINUS
16	COM_PLUS
17	GRN_MINUS
18	GND
19	GND

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set on the board.

For a complete list of jumpers refer to *2.1 Jumpers overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation mode selection*.

The following sections show some jumper settings, that allow to operate the PiggyBack Board in different power supply configurations.

8.1 Stand-alone operation with power supply by the tool

In principle the PiggyBack Board can also exclusively be powered via a connected debugger. However the debug tool would need to deliver sufficient currents on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the PiggyBack Board with the tool is possible.

CAUTION

If a debugger or a programming tool is connected disable the 3.3 V/5 V voltage output of the tool.

8.2 RH850/U2A-EVA vs. RH850/U2A16

The following voltages are only used when the board is equipped with a RH850/U2A-EVA device and thus the mentioned jumpers must be set:

EMUVCC (JP17), ERAMVCC (JP18), - DVCC (JP19), DVDD (JP24), ERAMVDD (JP28), EMUVDD (JP29)

If the board is equipped with a RH850/U2A16 device remove the above jumpers.

8.3 Configuration examples

8.3.1 General settings

All of the following board configurations are based on these conditions:

- Normal device operation mode (JP41[OPEN]: FLMD0 = L).
- All voltages for all functions are activated.
- Current measurements are not carries out, hence JP4, JP5, JP30 and JP31 are set.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 to CN11 must be assembled on the board.

8.3.2 Jumper indicators

- The green jumper JP41 for FLMDO0 must always be open for a ‘normal’ (user mode and debug) operation of the device.
- The red jumpers are related to the power supply configuration.
- The blue jumpers are only set if the board is equipped with a RH850/U2A-EVA device.

Following jumper symbols are used:

–  : open jumper

– 

: jumper must be set in the indicated position

– 

: jumper must be set, *italic* position indicator is optional, see description above the figure

Note

The pin 1 of a jumper can be identified by a

- small circle near the jumper
- square soldering pad.

8.3.3 Stand-alone operation with single external power supply: minimum configuration

This example enables to operate the board with only the 3.3 V external power supply.
Since no 5 V voltage is available, all I/O ports can only use 3.3 V.

- CN8: GND connection
- CN10: 3.3 V
- CN9: not connected, no 5.0 V
- CN11: not connected, no IN_1v12
  - JP16[2-1]: use reg_vcc_VDD from on-board voltage regulator xVDD voltages
  - VDD from reg_vcc_VDD (JP23[2-1]) or from SVR_OUTPUT (JP23[2-3]) from on-chip Switching Voltage Regulator

  Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

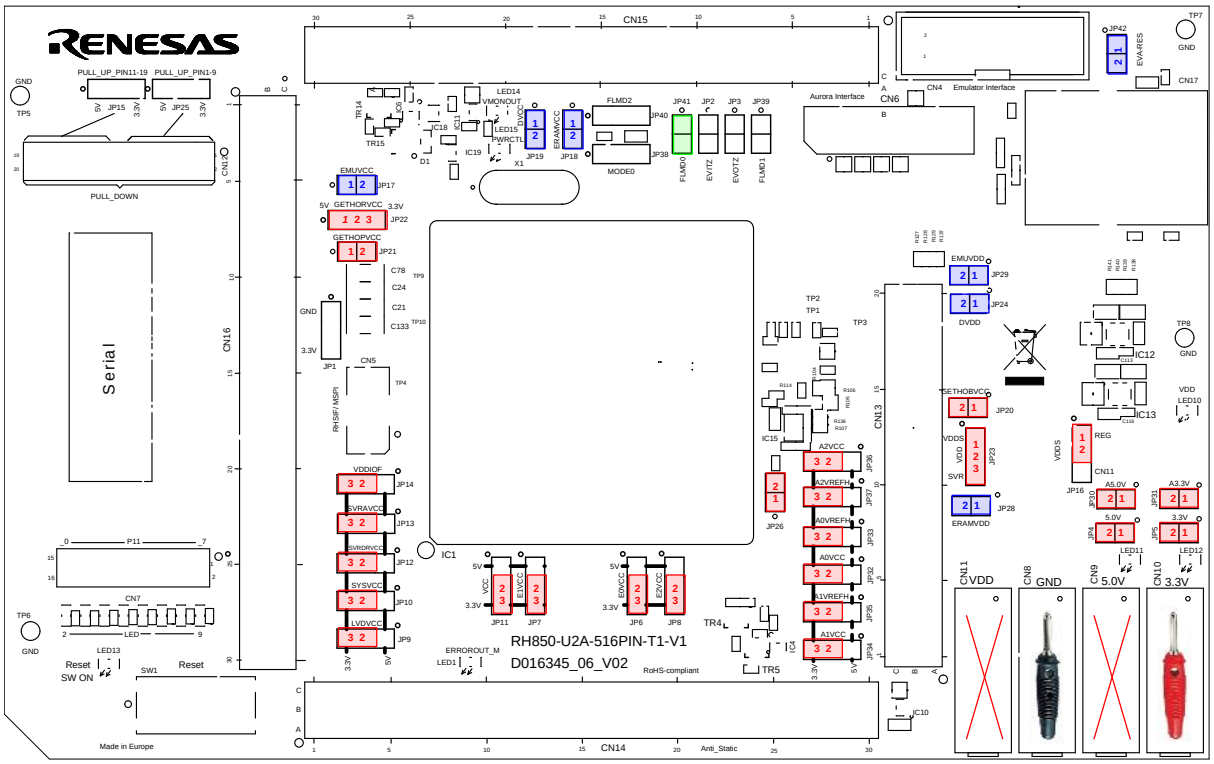


Figure 8.1 Stand-alone operation with minimum external power supply

8.3.4 Stand-alone operation with all external power supplies: maximum configuration

This example assumes all external power supplies are connected and used.

- CN8: GND connection
- CN10: 3.3 V
- CN9: 5 V
  - select desired 3.3 V/5.0 V via jumpers JP6 to JP14 and JP32 to JP37
- CN11: 1.12 V (IN_1v12)
  - JP16[2-3], JP23[2-1]: use IN_1v12 for all xVDD voltages

  Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

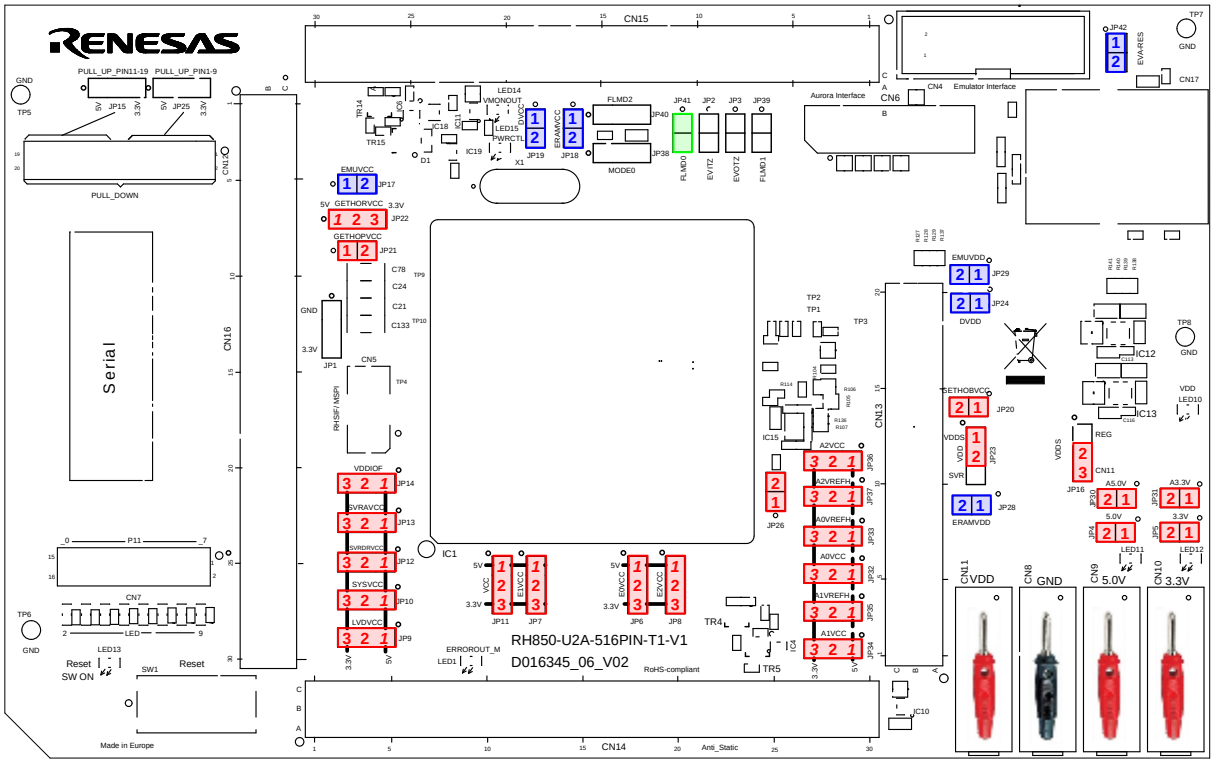


Figure 8.2 Stand-alone operation with maximum external power supply

8.3.5 Operation on the MainBoard: no external supply

This example assumes the PiggyBack Board is plugged onto a MainBoard, which provides 3.3 V and 5.0 V.

- CN8 to CN11: not connected, no external 5.0 V, 3.3 V, 1.12 V
- select desired 3.3 V/5.0 V via jumpers JP6 to JP14 and JP32 to JP37
- xVDD supply:
  - JP16[2-1]: use reg_vcc_VDD from on-board voltage regulator xVDD voltages
  - VDD from reg_vcc_VDD (JP23[2-1]) or SVR_OUTPUT (JP23[2-3]) from on-chip Switching Voltage Regulator

  Refer to *3.3 Device core voltages (xVDD) selection* for further details about xVDD voltages.

Note

This configuration still allows to utilize an external IN_1v12 voltage (connected to CN8, CN11) as the source for all xVDD voltages. In this case set JP16[2-3] and JP23[2-1].

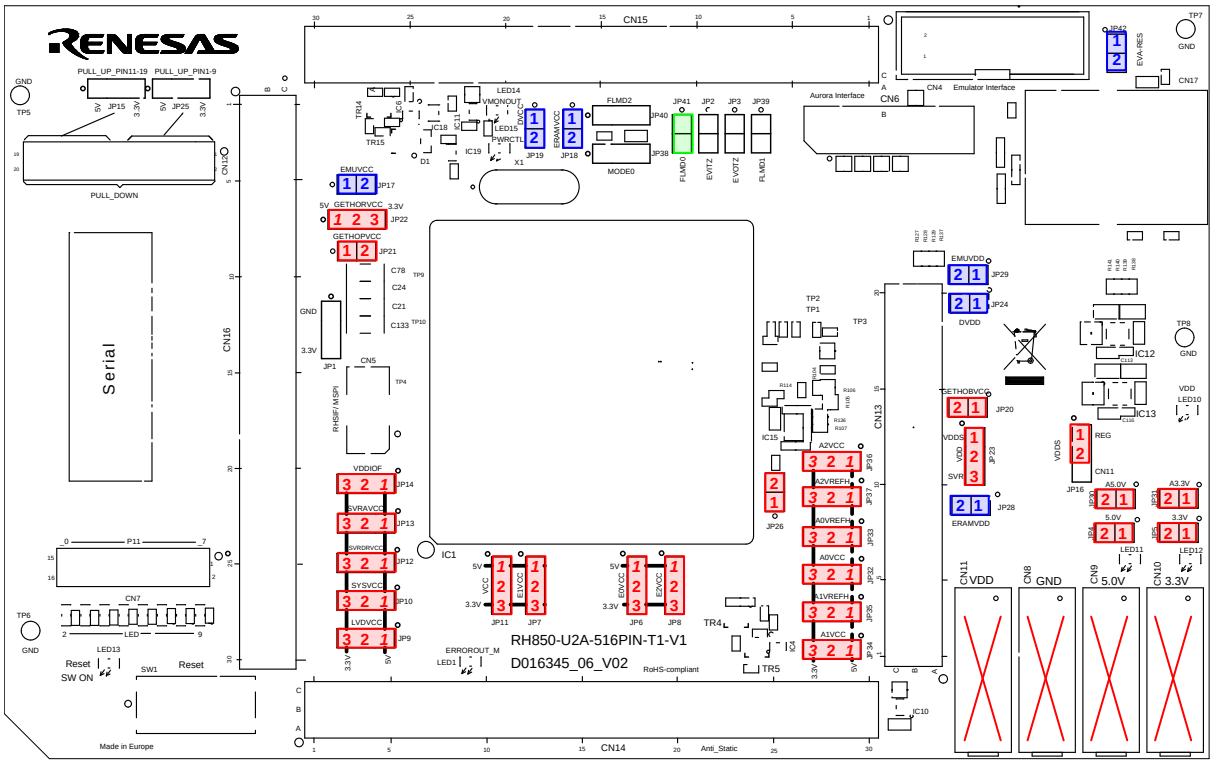


Figure 8.3 Main board operation without external power supply

9. Precautions

9.1 Power-Off sequence

A dedicated sequence needs to be applied, when the power supplied to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '2-3 ON' position, so that RESET is permanently asserted. Alternatively keep SW1 manually in' 2-1 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, deassert RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to section *6.2 RESET switch*.

9.2 Gigabit Ethernet interface

- **Affected products:** Some boards with hardware version D016345_06_V01
- **Not affected products:** All boards with hardware version D016345_06_V02 and above

For using the Ethernet interface (CN17) 0 Ω resistors R127 to R129 and R137 to R141 must be soldered onto the board.

The following figure shows the related schematics excerpt and indicate the resistor's locations on the board.

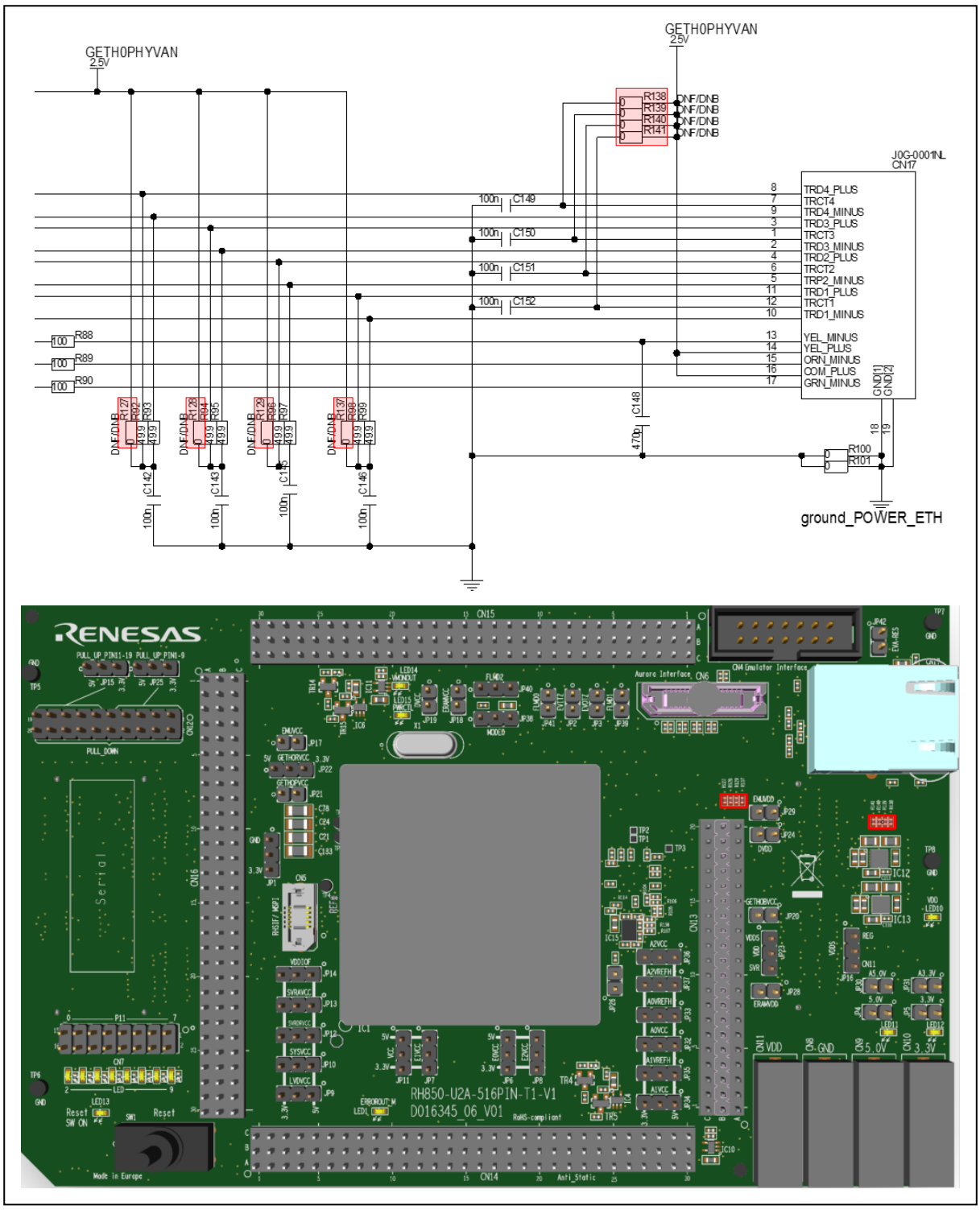


Figure 9.1 0 Ω resistors R127 to R129 and R137 to R141

9.3 Generation of AURORA RESETx Signals

The generation of the signals AURORES1Z and AURORESPDZ is different for board version V01 and V02

For board version D016345_06_V01 the signal generation is shown in figure Figure 9.2:

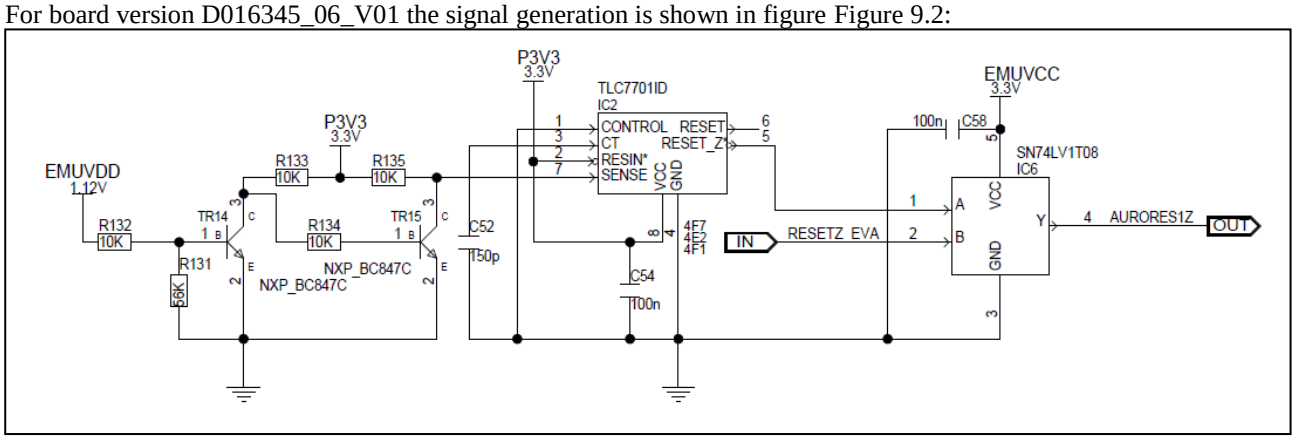


Figure 9.2 AURORES1Z generation board version V01

For board version D016345_06_V02 the signal generation is shown in figure Figure 9.3:

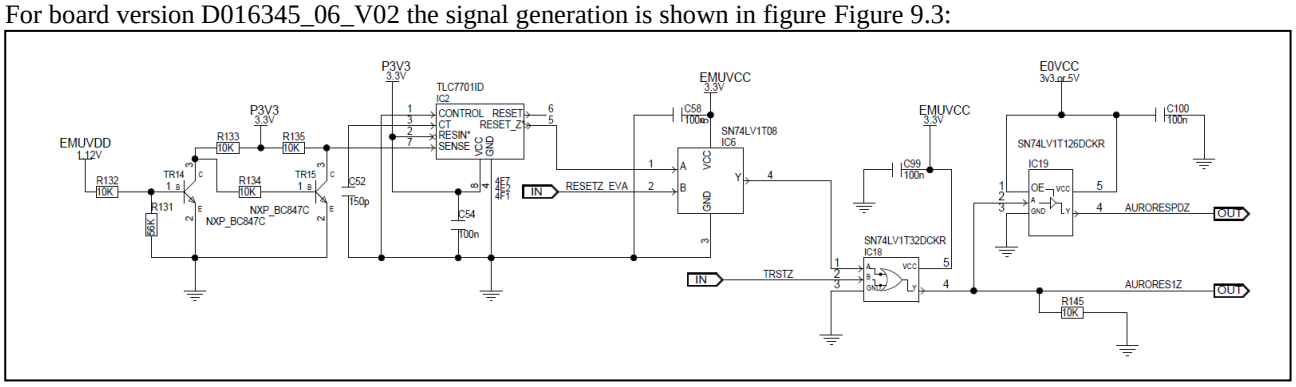


Figure 9.3 AURORES1Z and AURORESPDZ generation board version V02 and above

9.4 Erroneous Silkscreen print of CN15 and CN16

- **Affected products:** Boards with hardware version D016345_06_V01
- **Not affected products:** Boards with hardware version D016345_06_V02 and above

The numbering along CN15 and CN16 indicating the pin number is slipped one digit beginning with number “5”.

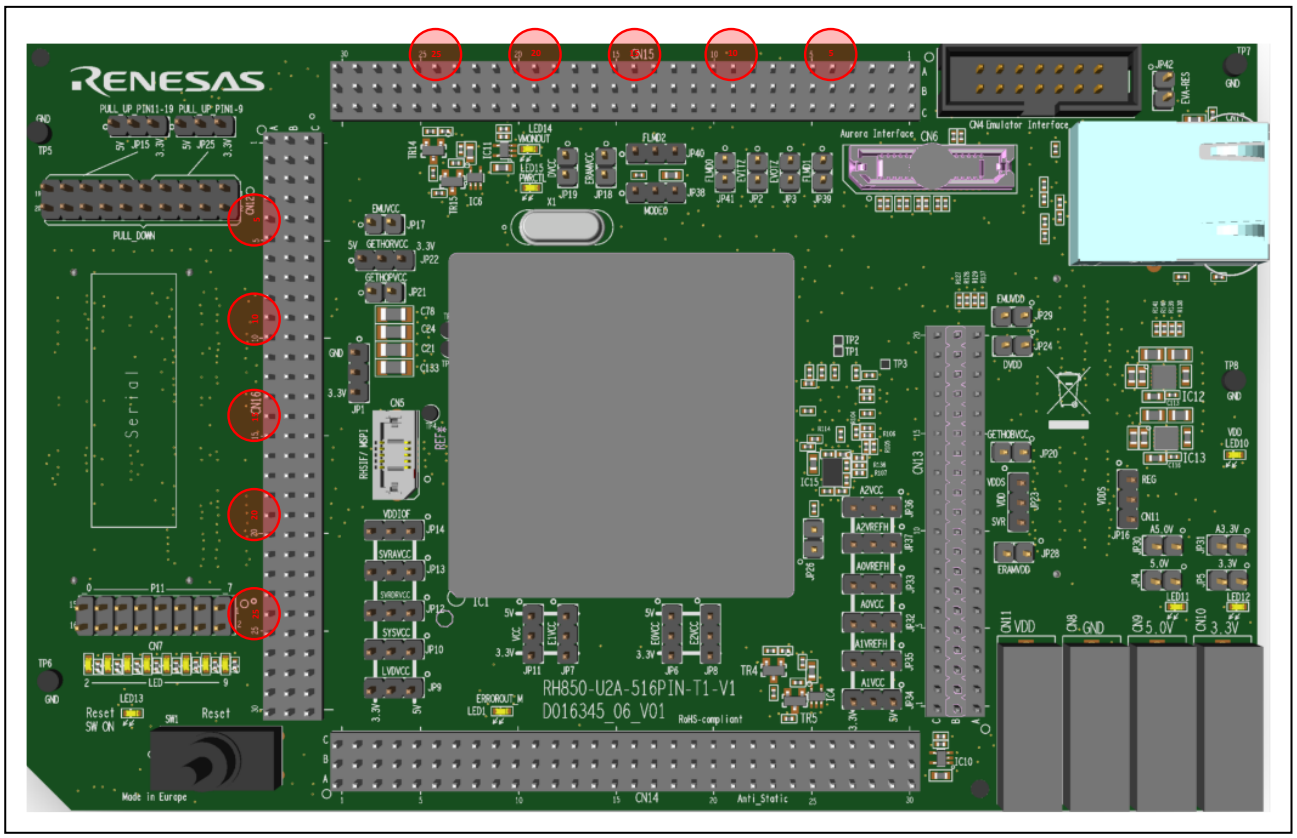


Figure 9.4 Numbering of CN15 and CN16 board version V01

9.5 Erroneous Silkscreen print of part name

- **Affected products:** All boards

The product name is missing “PB” in the middle.

It must be “RH850-U2A-512PIN-PB-T1-V1”

9.6 CAN0RX is shared with FLASH Programmer signal FLMD1

When using this product plugged into a motherboard where CAN0 is connected to the CAN-transceiver the FLASH programmer will not work.

This is because the CAN0RX function is shared with the FLMD1 function on the same device PIN.

Most CAN-transceiver are driving the RX line actively and the FLASH programmer then is not able to change signal level as required for flashing.

9.7 Displacement of JP39 and CN6

- **Affected products:** Boards with hardware version D016345_06_V01
- **Not affected products:** Boards with hardware version D016345_06_V02 and above

JP39 is located very close to CN6. To plug the AURORA-cable into CN6 the jumper-flag needs to be bend away.

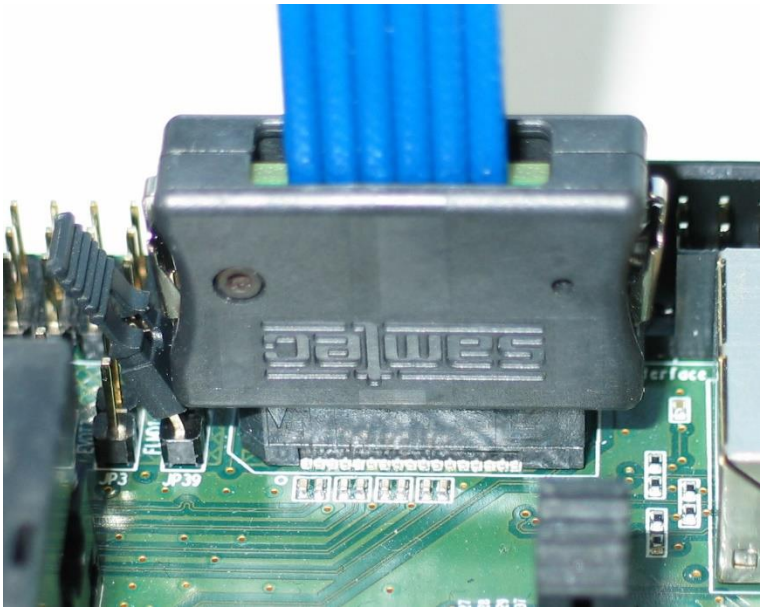


Figure 9.5: OPC displacement of JP39 and CN6

Figure 9.6: OPC displacement of JP39 and CN6 solved new board revision

10. Mechanical Dimensions

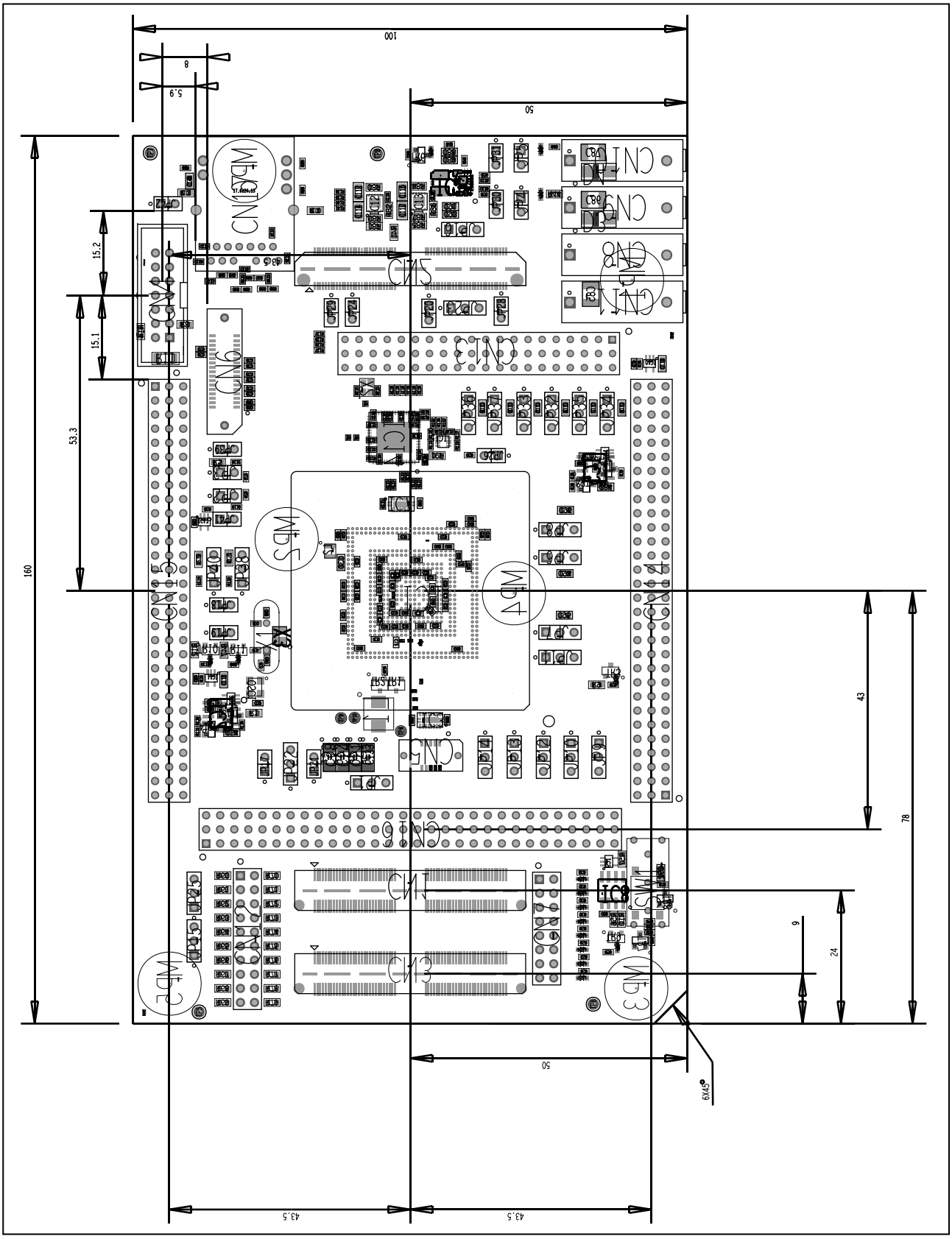


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Oscillators and resonators: OSC1, X3
- Capacitors: C97, C98, C113, C116,
- Resistors: R2 – R4, R6, R15 – R18, R21 – R23, R104 – R107, R127 – R129, R137, R138 – R141, R143,

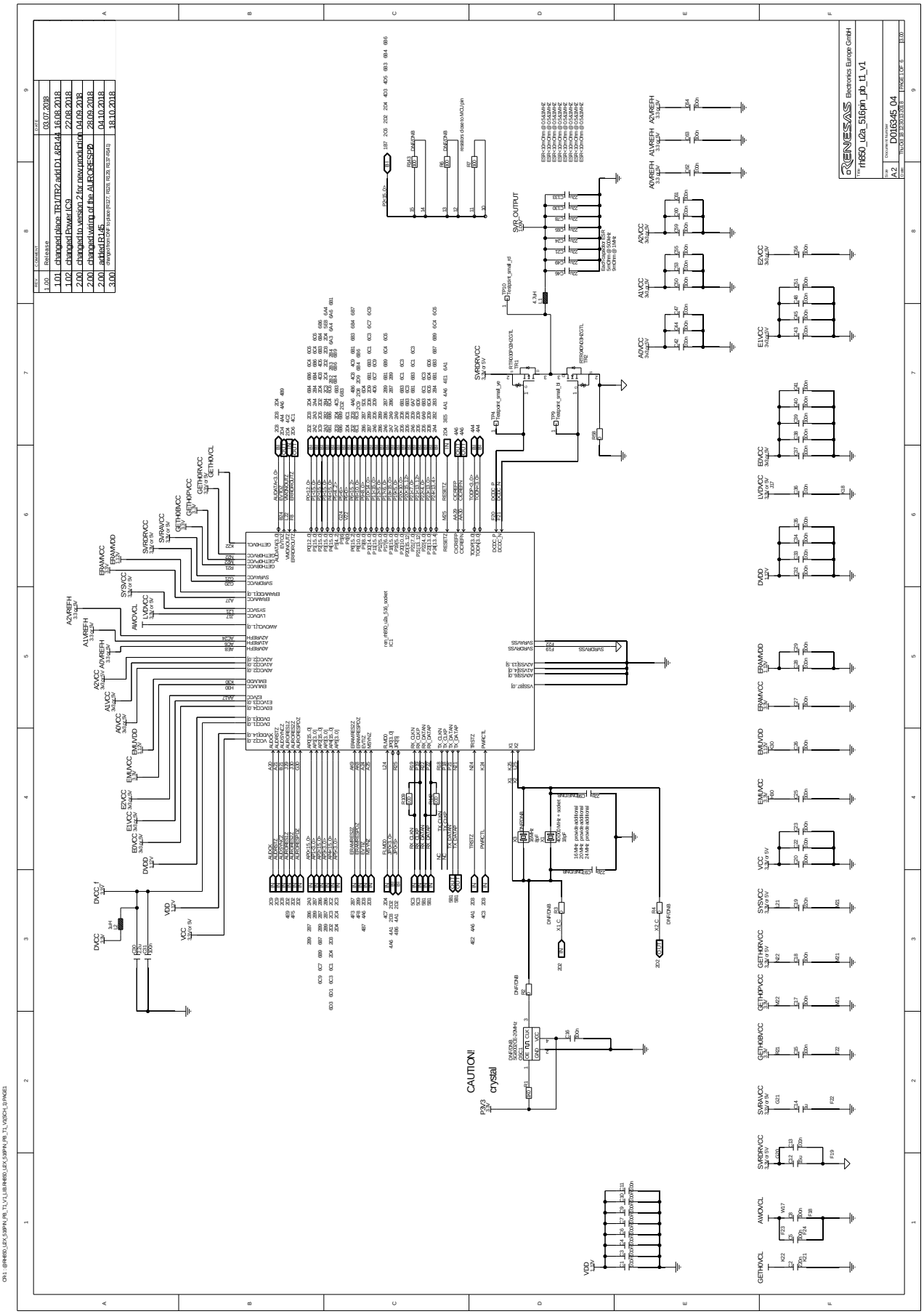
The above components are indicated with "DNF/DNB" in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

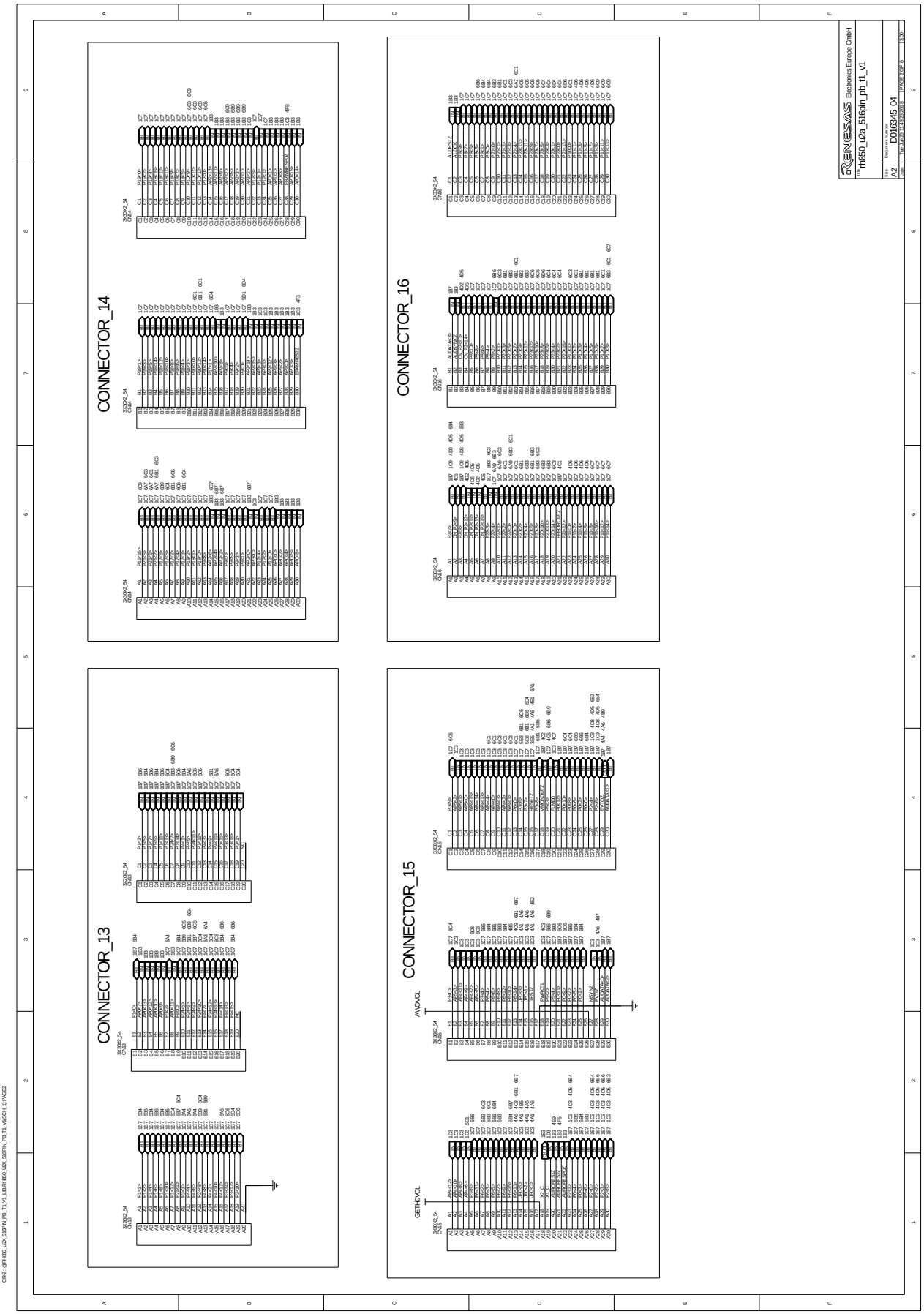
- 3 Hirschmann 4 mm power lab sockets, red for CN9 – CN11
- 1 Hirschmann 4 mm power lab sockets, black for CN8
- three resonators HC49 (16/20/24 MHz)
- 49 jumpers, 2.54 mm, black

The above components are indicated with "DO NOT FIT / TO DELIVER WITH THE BOARD" in the schematics.

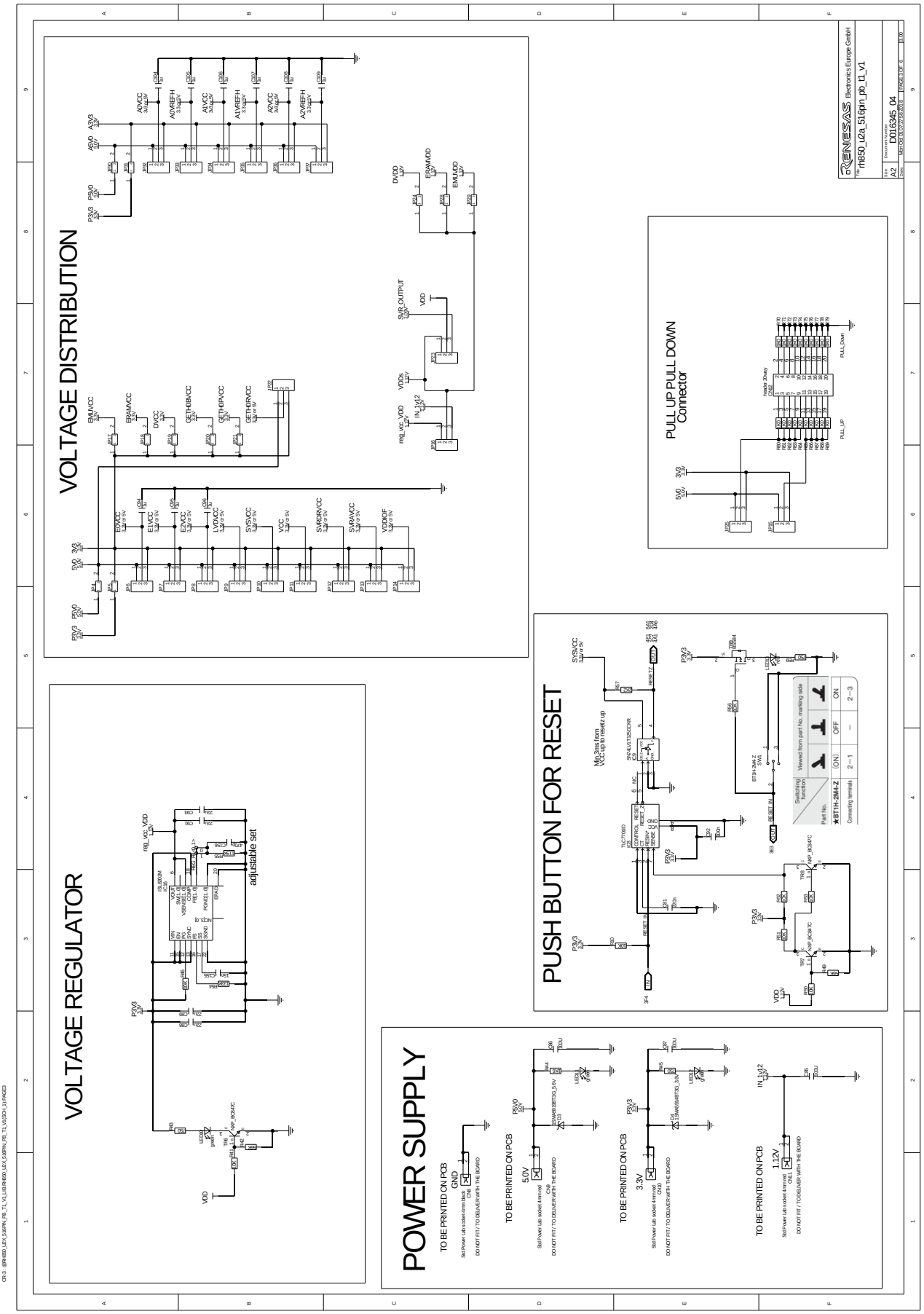
11.1 Page 1



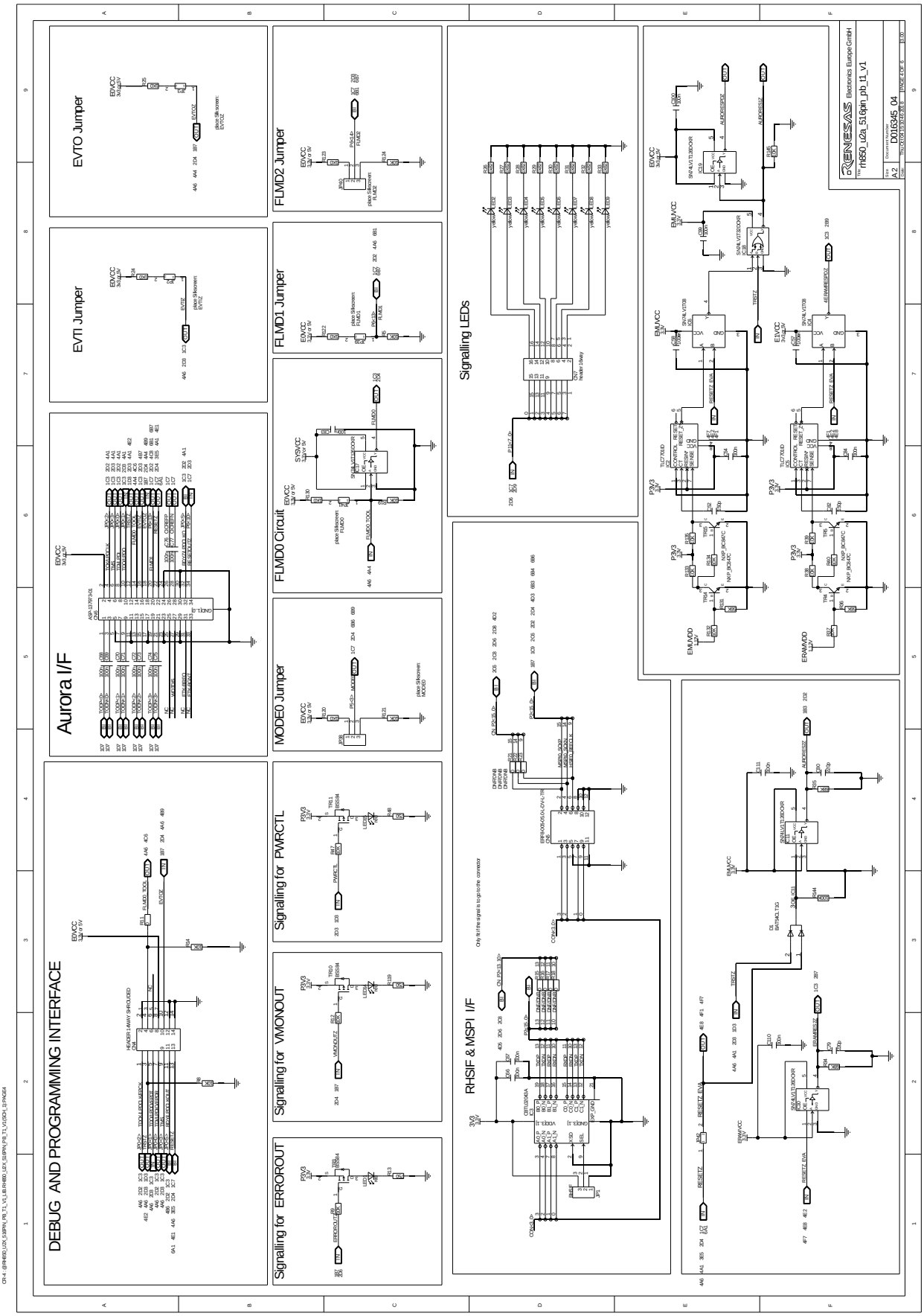
11.2 Page 2


CONNECTOR_14
CONNECTOR_16
CONNECTOR_13
CONNECTOR_15
RENESAS Electronics Europe GmbH
rh850_u2a_516pin_pb_t1_v1
Document number
R20UT0345_04
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

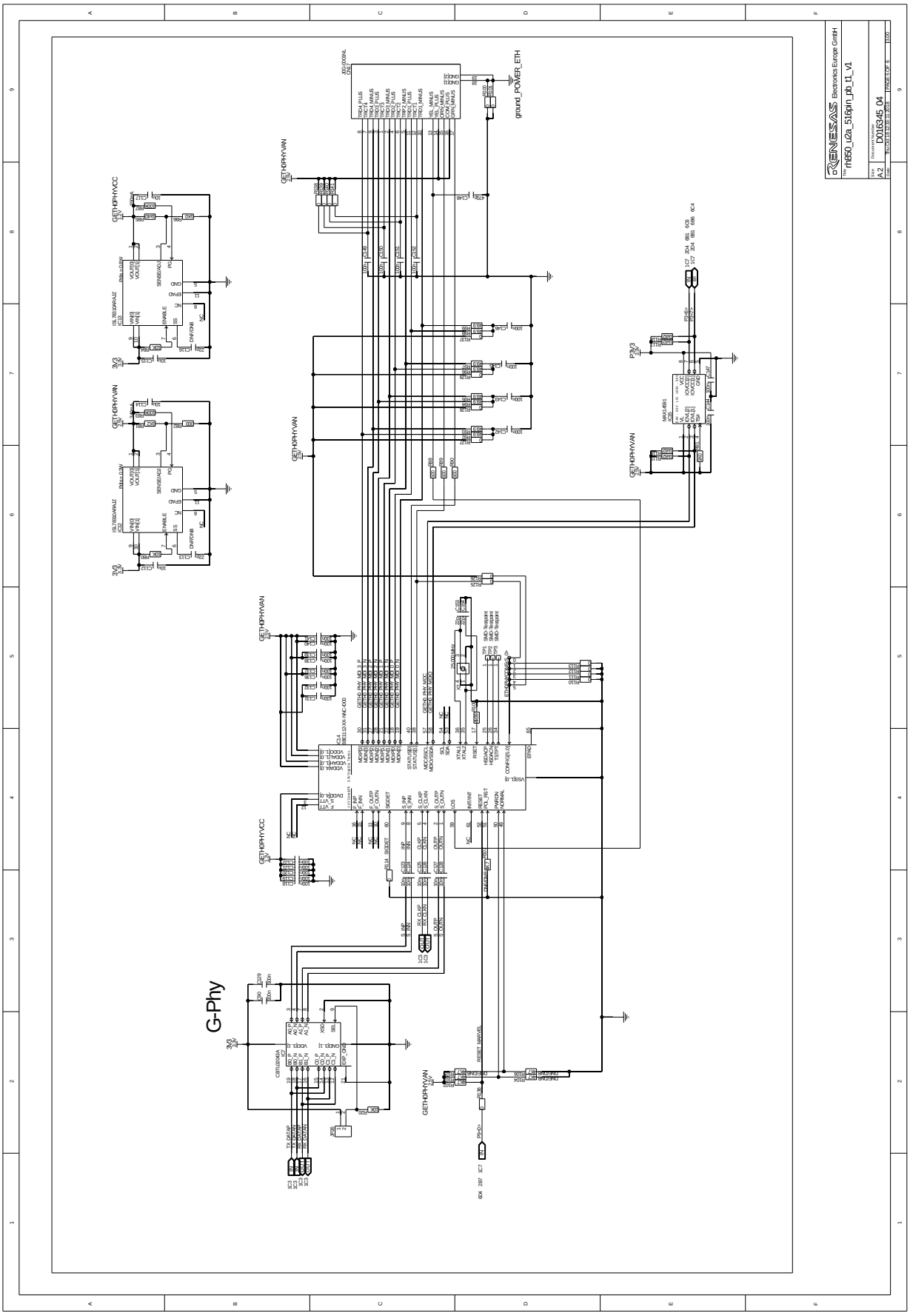
11.3 Page 3


VOLTAGE DISTRIBUTION
PULL UP PULL DOWN Connector
PUSH BUTTON FOR RESET
VOLTAGE REGULATOR
POWER SUPPLY
adjustable set
TO BE PRINTED ON PCB
GND
5.0V
3.3V
1.12V
RENESAS Electronics Europe GmbH
rh850_U2a_516pin_pb_t1_v1
D0163345_04
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

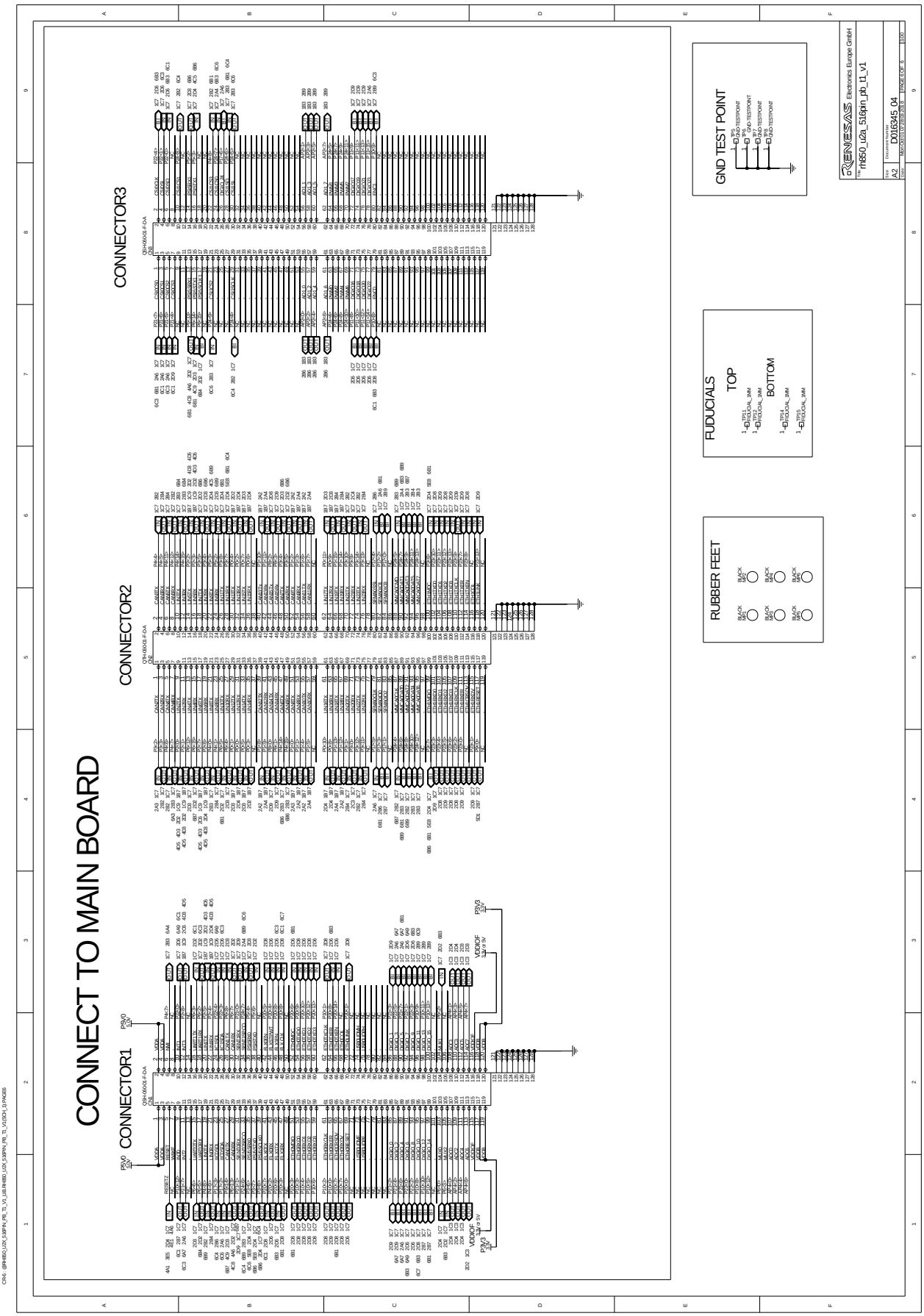
11.4 Page 4


DEBUG AND PROGRAMMING INTERFACE
Aurora I/F
EVTO Jumper
EVTI Jumper
FLMD2 Jumper
FLMD1 Jumper
FLMD0 Circuit
MODE0 Jumper
Signalling for PWRCTL
Signalling for VMONOUT
Signalling for ERROROUT
Signalling LEDs
RHSIF & MSPI I/F
RENESAS Electronics Europe GmbH
rh850_u2a_516pin_pb_t1_v1
D016345_04
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

11.5 Page 5


RENESAS Electronics Europe GmbH
rh850_u2a_516pin_pb_r1_v1
D0016945_04
ground_POWER_ETH
G-Phy
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

11.6 Page 6


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
GND TEST POINT
FUDUCIALS
TOP
BOTTOM
RUBBER FEET
RENESAS Electronics Europe GmbH
rh850_u2a_516pin_pb_t1_v1
D016345_04
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V0.01	2018-08-31	–	Initial release
V1.00	2019-02-20		• Schematics update • OPC Section added

RH850/U2A 516pin PiggyBack Board V1 User's Manual: PiggyBack Board

Publication Date: Rev.1.00 Feb 20, 2019

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 5.0

RH850/U2A 516pin

Renesas Electronics Corporation

R20UT4371ED0100