Automotive & Embedded Info

Never Forget Basics Whether its Life or Anything Else ... Basics are Cores. While seeing a Tree how can we forget Seed...

I2C

I2C:

What is I2C?

Inter integrated circuit. I2c is a 2 wire bus that is use to communicate between different types of IC's on a PCB board. Multi master communication protocol. Half duplex communication.

LINES\SIGNALS OF I2C:

2 lines. Signal involves in i2c: SDA (data line) and SCL (clock line).

STANDARD AND MAXIMUM SPEED: –

Maximum speed: – 400 kbit/sec

Standard speed: – 100 kbit/sec

MODES OF OPERATION: –

1. Master transmits
2. Master receives
3. Slave transmits
4. Slave receives.

Read and Write on I2C bus: –

READ:

S(1BIT-1)-> SLAVE-ADDRESS(7BIT-SLV ADD)->R/W(1BIT-1)-> A-> DATA(8BIT-DATA-SLV REG ADD) A-> DATA(8BIT-DATA)-> NA-> P(1BIT-0)

WRITE:

S(1BIT-1)-> SLAVE-ADDRESS(7BIT-SLV ADD)-> R/W(1BIT-0)-> A-> DATA(8BIT-SLV REG ADD)-> A-> DATA(8BIT-DATA)-> NA/A-> P(1BIT-0)

READ-WRITE:

S(1BIT-1)-> SLAVE-ADDRESS(7BIT-SLV ADD)-> R/W(1BIT-0)-> A-> DATA(8BIT-SLV REG ADD)-> A-> DATA(8BIT-DATA)-> NA/A-> SR(1BIT-1)-> SLAVE-ADDRESS(7BIT-SLV ADD)-> R/W(1BIT-0)-> A-> DATA(8BIT-SLV REG ADD)-> A->DATA(8BIT-DATA)-> NA/A P(1BIT-0)

Start and Stop Condition: –

START:

SCL->H WITH SDA->H-L,

STOP:

SCL->H WITH SDA->L-H.

I2C Bus Arbitration: –

Every master monitors the bus for start and stop bits and does not start a message while another master is keeping busy. However two master can start transmission at the same time, in this case arbitration occurs. I2c has deterministic arbitration policy. Each transmitter check the level of data line(SDA) and compare with the level it expects, if they do not match, that transmitter has lost arbitration and drops out of this protocol interaction.

If one transmitter sets SDA to 1 (not a driving signal) and second transmitter sets SDA to 0(pull to ground), the result is that line is low. The first transmitter observe that the level of line is different than expected, and conclude that another node is transmitting. The first node to notice such a difference is one that loses arbitration: it stops driving SDA. If it's a master it also stop driving SCL and waits for a stop, then it may try to reissue its entire message.

In the meantime the other node has not noticed any difference between actual and expected levels on SDA and therefore continue transmission. It can do so without problem so far the signal has been exactly as it expected; no other transmitter has disturbed its message.

If two master are sending a message to two different slaves, the one

sending the lower slave address always wins the arbitration in the address stage.

Slave Acknowledgement: –

Slave ACK pulls the **SDA** line low immediately after reception of the 8th bit transmitted; this means that as soon as the master pulls **SCL** low to complete the transmission of the bit, **SDA** will be pulled low by the slave. The master now issues a clock pulse on the **SCL** line. The slave will release the **SDA** line upon completion of this clock pulse.

I2C Clock Stretching: –

An addressed slave device may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master that is communicating with the slave may not finish the transmission of the current bit, but must wait until the clock line actually goes high.

The master must wait until it observes the clock line going high, and an additional minimum time (4 us for standard 100 kbit/s i^2c) before pulling the clock low again.

Although the master may also hold the SCL line low for as long as it desires, the term "clock stretching" is normally used only when slaves do it. Although in theory any clock pulse may be stretched, generally it is the intervals before or after the acknowledgment bit which are used. For example, if the slave is a microcontroller, its i^2c interface could stretch the clock after each byte, until the software decides whether to send a positive acknowledgment or a NACK.

slaves do not need to clock stretch and thus treat SCL as strictly an input with no circuitry to drive it.

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