User's Manual

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RH850 Evaluation Platform

RH850/U2A 292pin

User's Manual: Piggyback Board

Y-RH850-U2A-292PIN-PB-T1-V1

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Y-RH850-U2A-292PIN-PB-T1-V1 Documents

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1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   – The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2A 292pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2A 292pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document low active signals are marked by an appended 'Z' to the pin or signal name. E.g. the reset pin is named RESETZ.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2A-292PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2A-292PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2A-292PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2A-292PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2A-292PIN-PB-T1-V1

Item	Description	Quantity
D016636	RH850/U2A 292pin piggyback board	1
D017007	Documentation CD	1
D010816-24	China RoHS document	1
D017006-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	44
Red Hirschmann 4 mm power lab sockets	In the bag	3
Black Hirschmann 4 mm power lab sockets	In the bag	1
Würth PCB Terminal Block connector	In the bag	1
TE MATEnet 1000BASE-T1 Ethernet Port connector	In the bag	1
TE MATEnet 1000BASE-T1 Ethernet connection cable [1m]	In the bag	1
16MHz Resonator	In the bag	1
20MHz Resonator	In the bag	1
24MHz Resonator	In the bag	1

Note

Please keep the Y-RH850-U2A-292PIN-PB-T1-V1 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-U2A-292PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with powering from main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.12 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
  - 14-pin LPD/JTAG Debug Connector (e.g. for using E2 OCD Emulator or PG-FP6 Flash Programmer)
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 16/20/24/40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Automotive Ethernet Port 100/1000BASE-T1
- On-board interface connector for
  - Renesas High-Speed Serial I/F (RHSIF)

  or
  - Multichannel Serial Peripheral Interface (MSPI)
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

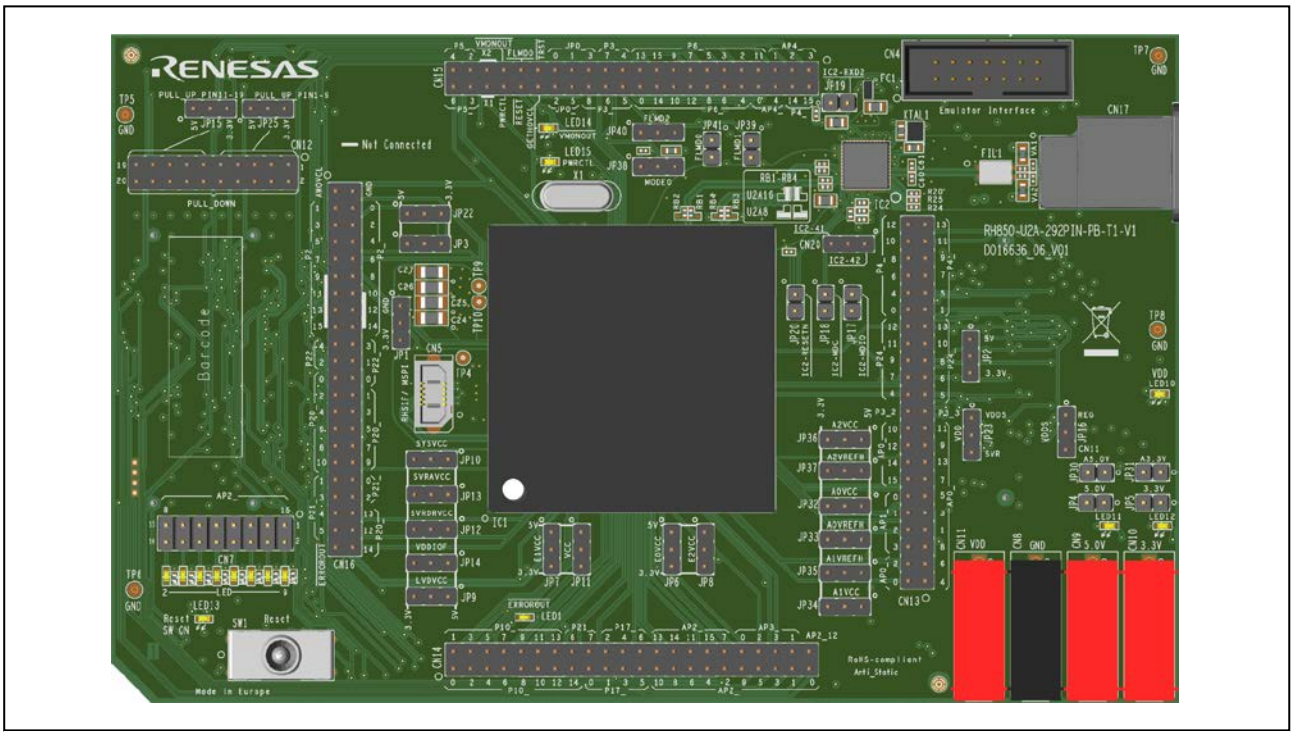


Figure 1.1 Piggyback board top view

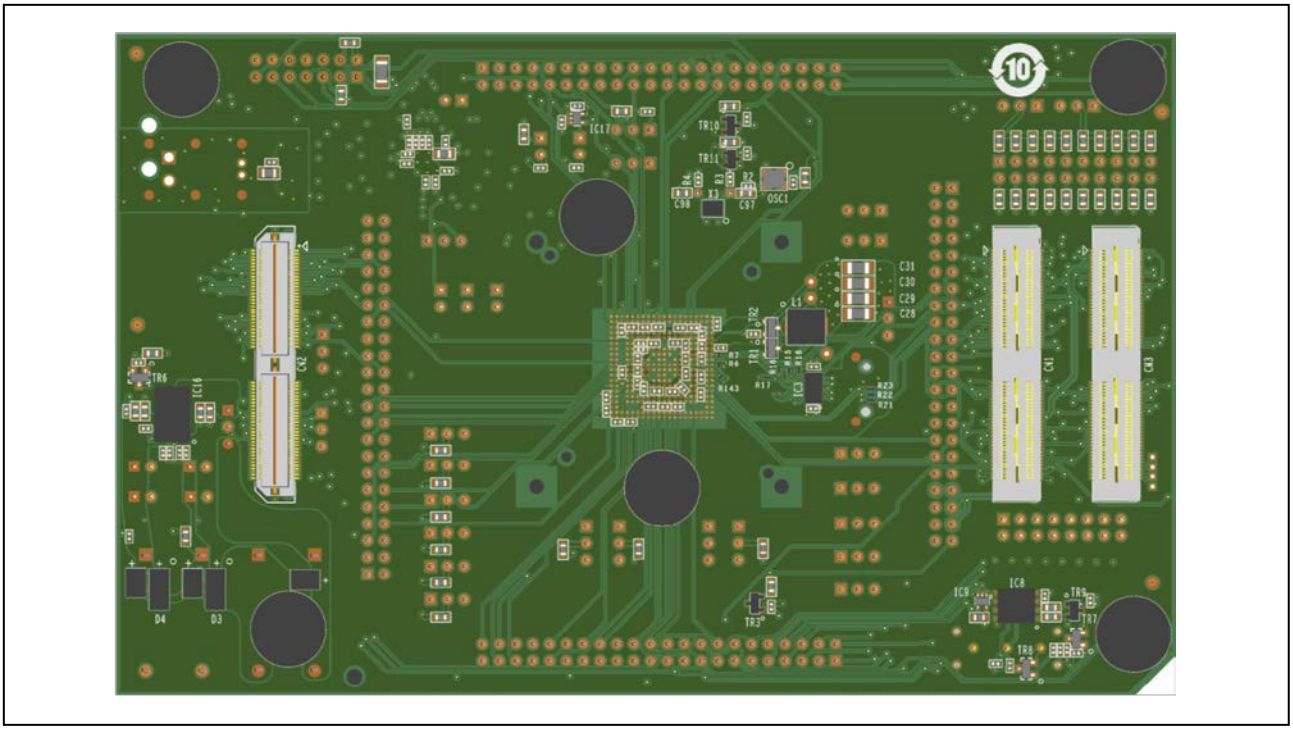


Figure 1.2 Piggyback board bottom view

Following figures provide the drawing of top and bottom views of the piggyback board.

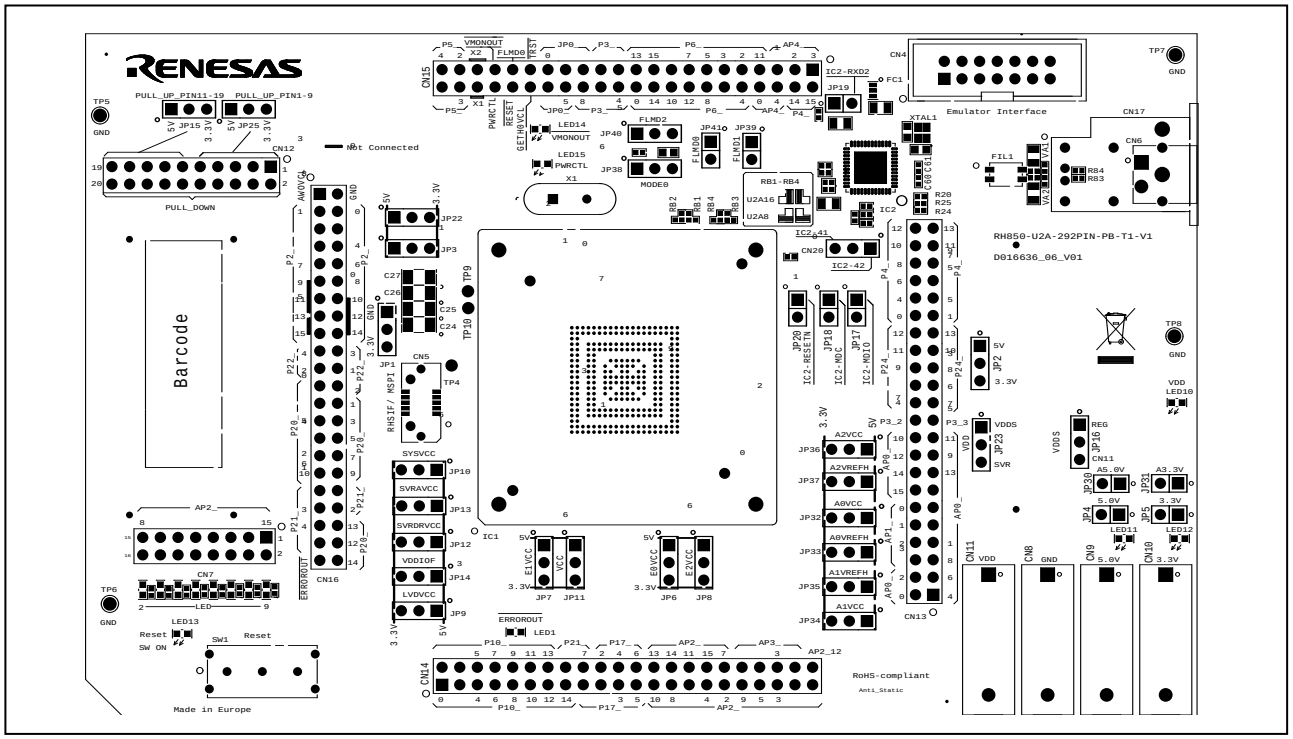


Figure 1.3 PiggyBack Board top view

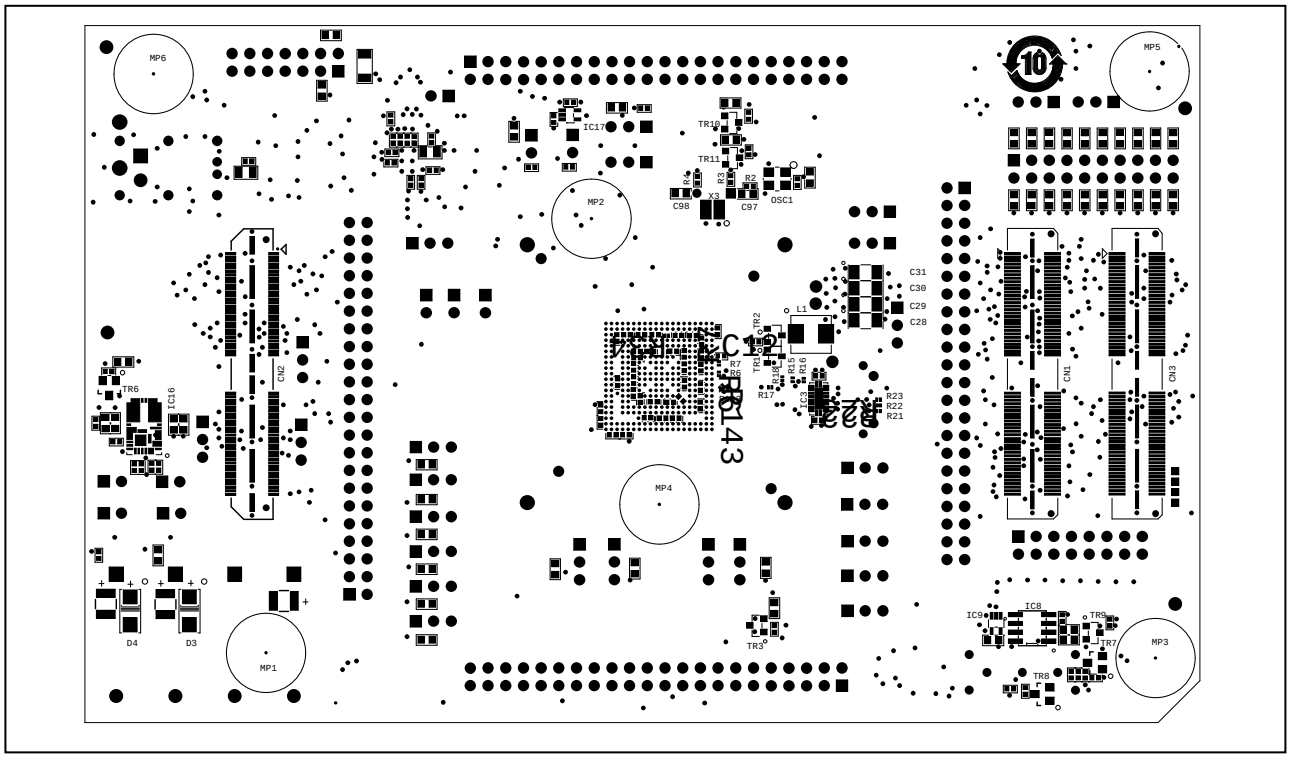


Figure 1.4 PiggyBack Board bottom view

1.5 Mounting of the Device

The board is designed for use with the following devices:

- R7F702300EABA (RH850/U2A16)
- R7F702301EABG (RH850/U2A8)

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking of the socket.
The A1pin of the socket is marked with a circle near to the “IC1” label (see also white point in *Figure 1.1 Piggyback board top view*).
The A1 pin of the device is marked by a white triangle on the package (see white circle in the figure below).

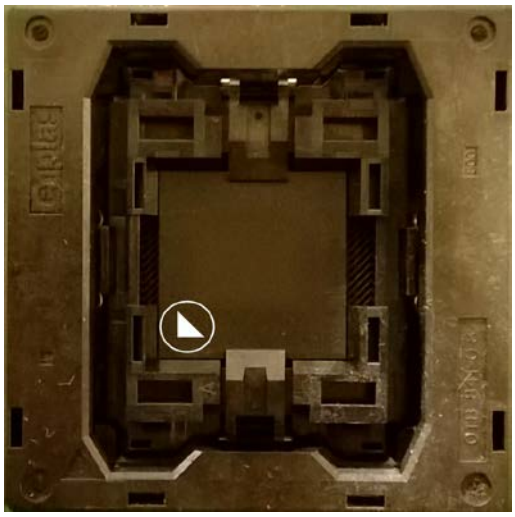


Figure 1.5 Enplas OTB-292(841R)-0.8-099-00 socket with mounted device

CAUTION

Be careful with the device placement in the socket to avoid damage of the device.

2. Jumpers, Connectors and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figure below.

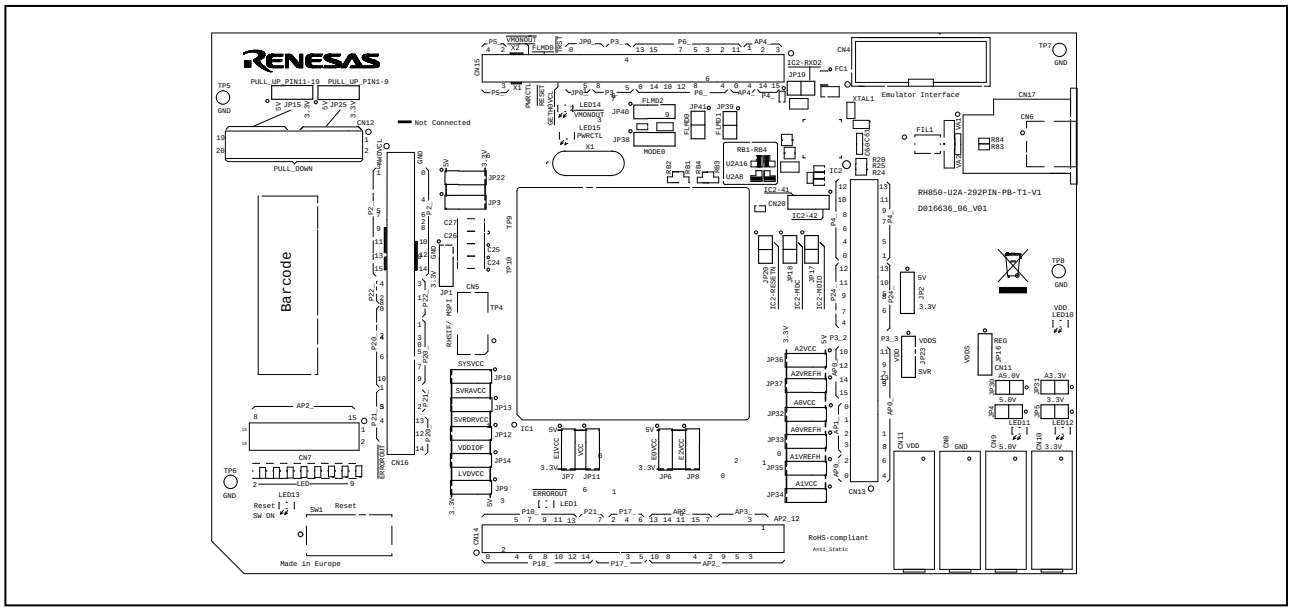


Figure 2.1 Placement of jumpers, connectors and LEDs

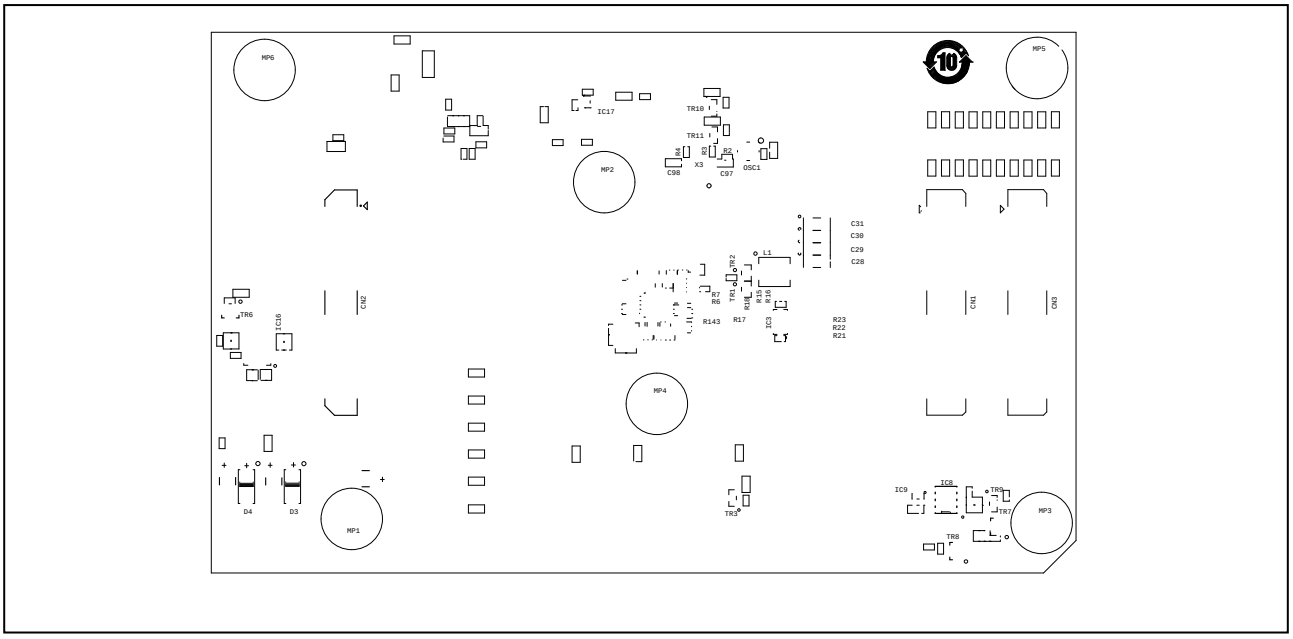


Figure 2.2 Placement of connectors on bottom side

2.1 Jumpers Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumpers overview

Jumper	Function	Remark
JP1	RHSIF I/F Rx/Tx signals swap • JP1[2-1]: RXDP/RXDN at pins 7 and 9 of CN5, TXDP/TXDN at pins 1 and 3 of CN5 • JP1[2-3]: RXDP/RXDN at pins 1 and 3 of CN5, TXDP/TXDN at pins 7 and 9 of CN5	refer to *6.6 Renesas High-Speed Serial I/F (RHSIF) / Multichannel Serial Peripheral Interface (MSPI)*
JP2	For processor U2A16: Voltage selection for GETH0BVCC • JP2[2-3]: 3.3 V For processor U2A8: Voltage selection for E0VCC (must be same as JP6) • JP2[2-1]: 5.0 V • JP2[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP3	For processor U2A16: Voltage selection for GETH0PVCC • JP3[2-3]: 3.3 V For processor U2A8: Voltage selection for E0VCC (must be same as JP6) • JP3[2-1]: 5.0 V • JP3[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP4	Current measurement bridge of 5.0 V power rail	refer to *3.4 Current Measurement Bridges*
JP5	Current measurement bridge of 3.3 V power rail	refer to *3.4 Current Measurement Bridges*
JP6	Voltage selection for E0VCC • JP6[2-1]: 5.0 V • JP6[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP7	Voltage selection for E1VCC • JP7[2-1]: 5.0 V • JP7[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP8	Voltage selection for E2VCC • JP8[2-1]: 5.0 V • JP8[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP9	Voltage selection for LVDVCC • JP9[2-1]: 5.0 V • JP9[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP10	Voltage selection for SYSVCC • JP10[2-1]: 5.0 V • JP10[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP11	Voltage selection for VCC • JP11[2-1]: 5.0 V • JP11[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP12	Voltage selection for SVRDRVCC • JP12[2-1]: 5.0 V • JP12[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP13	Voltage selection for SVRAVCC • JP13[2-1]: 5.0 V • JP13[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP14	Voltage selection for VDDIOF • JP14[2-1]: 5.0 V • JP14[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP15	Voltage selection for Pull-up/Pull-down pin header CN12 pins 11, 13, 15, 17, 19 • JP15[2-1]: 5.0 V • JP15[2-3]: 3.3 V	refer to *6.4 Pull-Up/Pull-Down Pin Header*
JP16	Voltage selection for 1.12 V VDDs * • JP16[2-1]: reg_vcc_VDD • JP16[2-3]: IN_1v12	refer to *3.3 Device Core Voltage (VDD) Selection*
JP17	Marvell MDIO – U2A P3_7 • JP17[2-1]: Connected • JP17[OPEN]: Open	
JP18	Marvell MDC – U2A P3_6 • JP18[2-1]: Connected • JP18[OPEN]: Open	
JP19	Marvel RxD2 Pull down • JP19[2-1]: Connected • JP19[OPEN]: Open	refer to *3.2 Voltage Distribution*
JP20	Marvell RESETn - U2A AP0_8 • JP20[2-1]: Connected • JP20[OPEN]: Open	
JP22	For processor U2A16: Voltage selection for GETH0RVCC • JP22[2-1]: 5.0 V • JP22[2-3]: 3.3 V For processor U2A8: Voltage selection for E0VCC (must be same as JP6) • JP22[2-1]: 5.0 V • JP22[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP23	Voltage selection for VDD • JP23[2-1]: VDDs • JP23[2-3]: SVR_OUTPUT	refer to *3.3 Device Core Voltage (VDD) Selection*
JP25	Voltage selection for Pull-up/Pull-down pin header CN12 pins 1, 3, 5, 7, 9 • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V	refer to *6.4 Pull-Up/Pull-Down Pin* Header
JP30	Current measurement bridge of 5.0 V A/D Converter power supply	refer to *3.4 Current Measurement Bridges*

Table 2.1 Jumpers overview (cont'd)

Jumper	Function	Remark
JP31	Current measurement bridge of 3.3 V A/D Converter power supply	refer to *3.4 Current Measurement Bridges*
JP32	Voltage selection for A0VCC • JP32[2-1]: 5.0 V • JP32[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP33	Voltage selection for A0VREFH • JP33[2-1]: 5.0 V • JP33[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP34	Voltage selection for A1VCC • JP34[2-1]: 5.0 V • JP34[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP35	Voltage selection for A1VREFH • JP35[2-1]: 5.0 V • JP35[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP36	Voltage selection for A2VCC • JP36[2-1]: 5.0 V • JP36[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP37	Voltage selection for A2VREFH • JP37[2-1]: 5.0 V • JP37[2-3]: 3.3 V	refer to *3.2 Voltage Distribution*
JP38	MODE0 level selection • JP38[2-1]: H level • JP38[2-3]: L level	refer to *6.1 Operation Mode Selection*
JP39	FLMD1 level selection • JP39[2-1]: H level • JP39[OPEN]: L level	refer to *6.1 Operation Mode Selection*
JP40	FLMD2 level selection • JP40[2-1]: H level • JP40[2-3]: L level	refer to *6.1 Operation Mode Selection*
JP41	FLMD0 level selection • JP41[2-1]: H level • JP41[OPEN]: – if no debug/programming tool connected: L level – controlled by debug/programming tool, if tool connected:	refer to *6.1 Operation Mode Selection*

Note: * Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

2.2 Connectors Overview

The following table provides an overview of all connectors.

Table 2.2 Connectors overview

Connector	Function	Remark
CN1	Main Board connectors	refer to *7.1 Connectors to the Main Board CN1 to* CN3
CN2		
CN3		
CN4	Debug connector	refer to *5 Debug and Flash Programming Interfaces* and *7.2 Debug Connector CN4*
CN5	RHSIF & MSPI connector	refer to *6.6 Renesas High-Speed Serial I/F (RHSIF) / Multichannel Serial Peripheral Interface (MSPI)* and *7.3 RHSIF/MSIP Connector CN5*
CN6	Ethernet interface connector	refer to *6.5 Automotive Ethernet Interface* and *7.6 Ethernet Connector CN6* and CN17
CN7	Signaling LEDs pin header	refer to *6.3 Signaling LEDs*
CN8	GND for external power supply	refer to *3.1 Board Power Connection,* connectors are not assembled on the board
CN9	+5.0 V external power supply	
CN10	+3.3 V external power supply	
CN11	+1.12 V external power supply *	
CN12	Pull-up/Pull-down pin header	refer to *6.4 Pull-Up/Pull-Down Pin Header* and *7.5 Pull-Up/Pull-Down Pin Header* CN12
CN13	Device ports connectors	refer to *7.4 Device Ports Connectors CN13 to CN16*
CN14		
CN15		
CN16		
CN17	Ethernet interface connector	refer to *6.5 Automotive Ethernet Interface* and *7.6 Ethernet Connector CN6* and CN17
CN20	GPIO/LED output	Refer to *7.7 GPIO/LED Connector CN20*

Note: * Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

2.3 LED Overview

The following table provides an overview of all LED.

Table 2.3 LED overview

LED	Function	Color	Remark
LED1	Device ERROROUT signal	red	
LED2	Signaling LED	yellow	connection via CN7, refer to *6.3 Signaling LEDs*
LED3	Signaling LED		
LED4	Signaling LED		
LED5	Signaling LED		
LED6	Signaling LED		
LED7	Signaling LED		
LED8	Signaling LED		
LED9	Signaling LED		
LED10	1.12 V device core voltage VDD	green	refer to *3.5 Power Supply LEDs*
LED11	5.0 V power supply P5V0	green	
LED12	3.3 V power supply P3V3	green	
LED13	Reset switch SW1 on	red	
LED14	Device VMONOUTZ signal	red	
LED15	Device PWRCTL signal	red	

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5 V in case some ports shall be operated with 5 V I/O voltage
- 1.12 V for the device's VDD core voltage supply
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as ‘typical’.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm ‘banana-type’ connectors are used to connect external power supplies:
  - black connector CN8 for GND (VSS)
  - red connector CN9 for 5 V
  - red connector CN10 for 3.3 V
  - red connector CN11 for 1.12 V
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

  These connectors are not assembled at delivery of the board, but separately supplied with the board package.

In case the piggyback board is mounted on a Main Board, all voltages except for 1.12 V (VDD) are supplied by the Main Board.

CAUTION

Do not supply the 5 V (CN9) and 3.3 V (CN10) voltage directly to the piggyback board in case it is mounted on the Main Board.

Connecting external 1.12 V via CN11 (and GND via CN8) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC	3.3 V, 5 V	Power supply for I/O ports
LVDVCC	3.3 V, 5 V	Power supply for LVDS ports
SYSVCC	3.3 V, 5 V	Power supply for • System Logic and internal voltage regulator power • I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SVRDRVCC	3.3 V, 5 V	Power supply for on-chip Switching Voltage Regulator (SVR)
SVRAVCC	3.3 V, 5 V	
VDDIOF	3.3 V, 5 V	I/O voltage supply for the Main Board
GETH0PVCC	3.3 V, 5V	Power supply for Ethernet domain (for U2A16 only)
GETH0BVCC	3.3 V, 5V	
GETH0RVCC	3.3 V, 5V	
A0VCC, A1VCC, A2VCC	3.3 V, 5 V	A/D Converter's power supplies and reference voltages
A0VREFH, A1VREFH, A2VREFH,	3.3 V, 5 V	
VDD	1.12 V *	Core supply voltage

Note: * Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Each of the above voltages can be selected from

- 5.0 V, 3.3 V (where applicable, see table above)

by a set of jumpers. For details refer to the figure below and *Table 2.1 Jumpers overview*

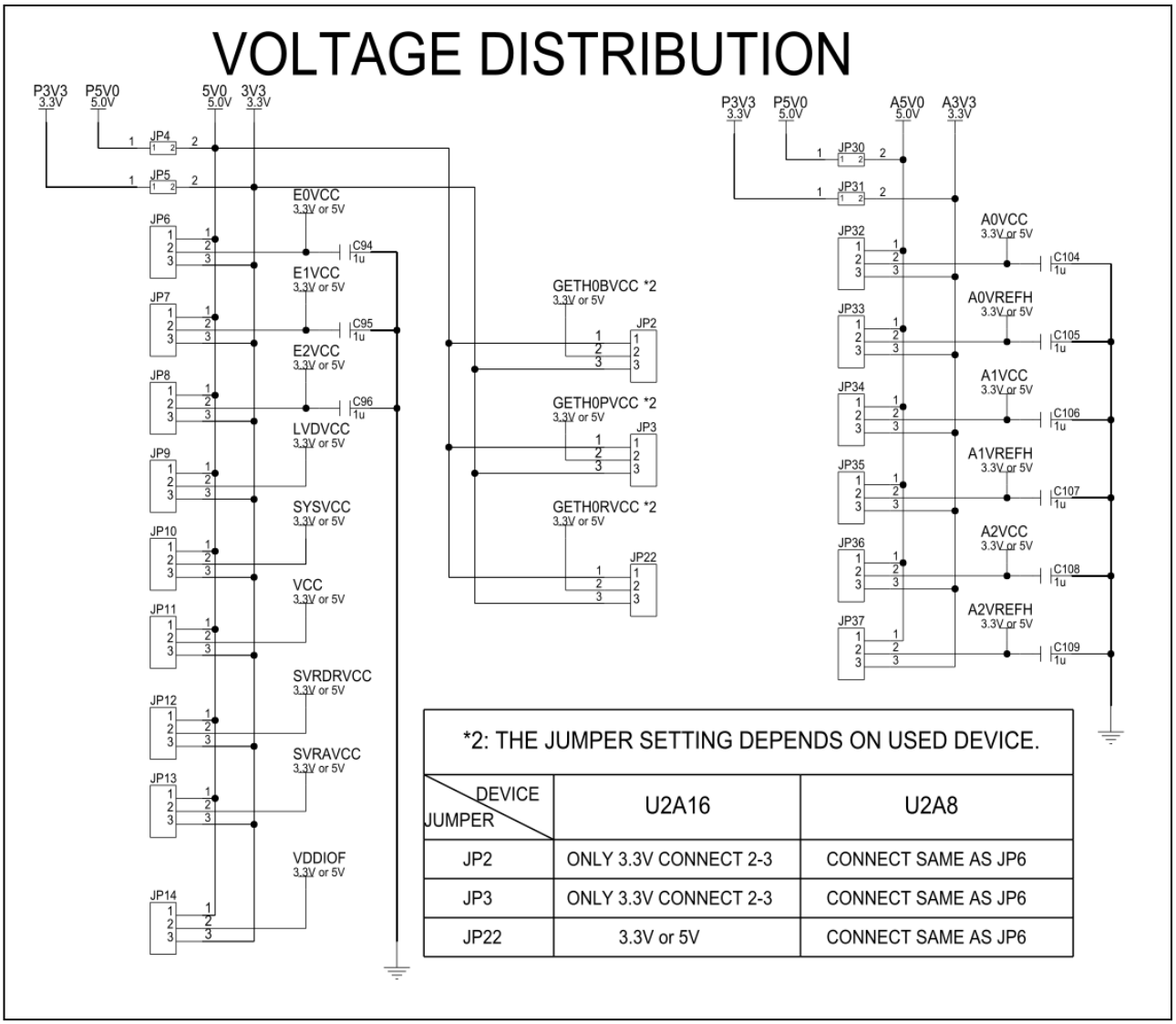


Figure 3.1 Voltage distribution

3.3 Device Core Voltage (VDD) Selection

The device core voltage VDD (typ.1.12 V) can be

- supplied from external via CN11 (voltage IN_1v12)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC16 (voltage reg_vcc_VDD)
- generated by the on-chip Switching Voltage Regulator (SVR) in combination with device external power transistors TR1, TR2 (voltage SVR_OUTPUT)

Note

The IN_1v12 and reg_vcc_VDD voltages have a level of typical 1.12 V, which is higher than the typical device core voltage VDD of 1.09 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

Selection of the VDD source is achieved by use of the jumpers JP23 and JP16:

- JP23[2-1]: VDD = 1.12 V (VDDs) from
  - JP16[2-1]: VDDs = reg_vcc_VDD from on-board voltage regulator IC16
  - JP16[2-3]: VDDs = IN_1v12 from external supply CN11
- JP23[2-3]: VDD = 1.09 V (SVR_OUTPUT)

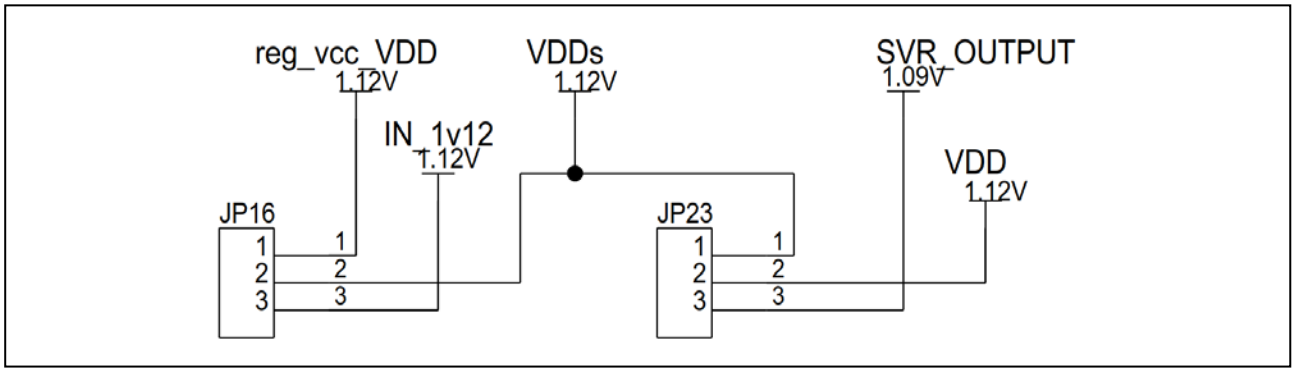


Figure 3.2 Device core voltage (VDD) selection

3.4 Current Measurement Bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP4 and JP5 with a current meter.

Accordingly, the total current via the A/D Converter's supply voltages A5V0 and A3V3 can be measured via the jumpers JP30 and JP31 respectively.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.1 Voltage distribution.*

3.5 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED11 for 5.0 V power rail P5V0
- LED12 for 3.3 V power rail P3V3
- LED10 for 1.12 V device core voltage VDD

4. Clock Supply

The device's operation clock can be generated by

- the on-chip oscillator main oscillator circuit in combination with an off-chip resonator, connected to the X1, X2 terminals
- an off-chip oscillator, the clock is fed into the X1 terminal

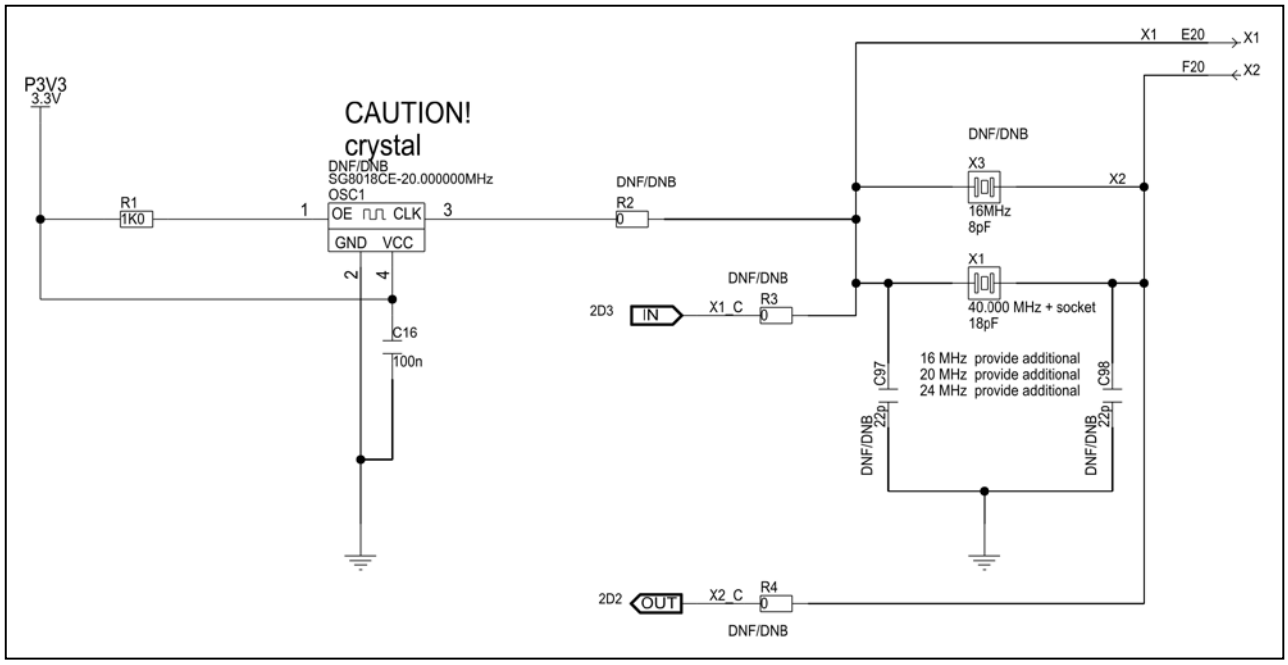


Figure 4.1 Clock supply

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

Optionally a resonator (X3) can be soldered on the board, refer to the figure above.

Several resonators for various main oscillator frequencies (16 MHz, 20 MHz, 24 MHz, 40 MHz) are included in the board package.

The 40MHz resonator is by default mounted to X1.

For package content please refer to *1.1 Package Components*

CAUTION

Only one oscillator, either X1 or X3, can be used at any one time for the main oscillator.

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be soldered on the board.

The available footprint and circuitry is designed for a SG-8002CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via resistor R2.

The SG-8002CE is neither mounted on nor provided with the board. For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 or soldered on X3 must not be used in parallel to another clock source.

4.3 X1 and X2 on CN15

To minimize disturbance on the resonator signal the signals X1 and X2 are by default not connected to a pin header. If needed the signals can be connected to CN15 via 0 Ω resistors:

- X1: Pin 40 of CN15 to supply an external clock to the device via R3
- X2: Pin 39 of CN15 for measurement purposes of the clock via R4

5. Debug and Flash Programming Interfaces

For debugging and flash programming purposes debug and flash programming tools can be connected to the CN4 connector.

Refer to *7.2 Debug Connector CN4* for details about the CN4 pin assignment.

The Renesas standard emulator for RH850/U2A is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers for selection of the device operation mode:

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP38	MODE0 pin level • JP38[2-1]: MODE0 = H level • JP38[2-3]: MODE0 = GND
JP41	FLMD0 pin level • JP41[SHORT]: FLMD0 = H level • JP41[OPEN]: FLMD0 – controlled by debugger or programming tool, if a tool is connected via CN4 – GND, if no tool connected
JP39	FLMD1 pin level • JP39[SHORT]: FLMD1 = H level • JP39[OPEN]: FLMD1 = GND
JP40	FLMD2 pin level • JP40[2-1]: FLMD2 = H level • JP40[2-3]: FLMD2 = GND

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP41.

All other jumpers related to the mode selection can be left open.

6.2 RESET Switch

The SW1 is used to issue a RESET to the device.

The SW1 toggle switch allows to activate the RESET in two different ways:

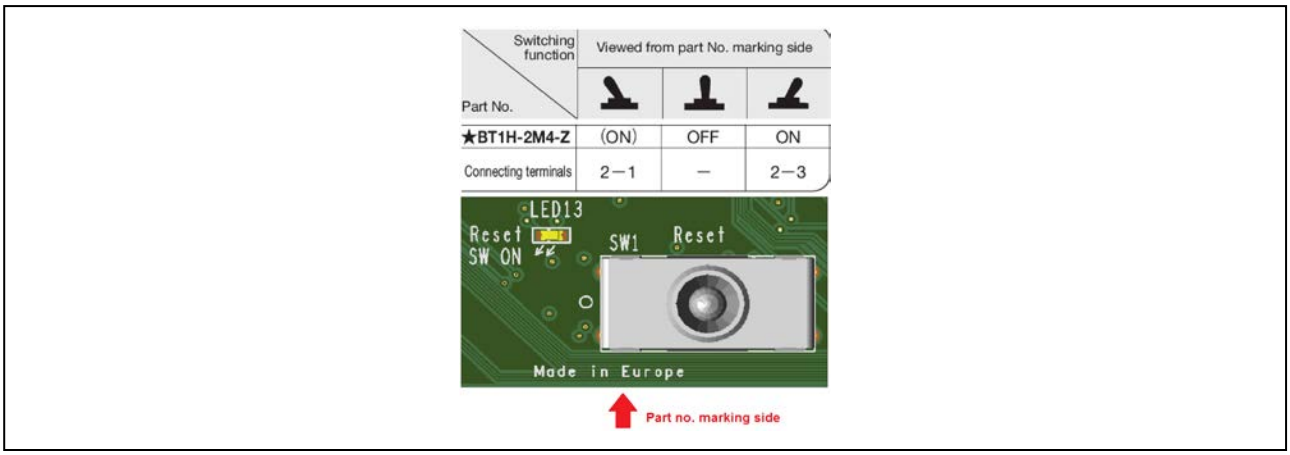
- SW1 in left '2-1(ON)' position: temporary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW1 in right '2-3 ON' position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

The lighted red LED13 indicates that SW1 is "on", i.e. in position '2-1 (ON)' or '2-3 ON'.

Note

LED13 does not light up when RESET is asserted by any other means than SW1.



6.3 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

Device pins AP2_8 to AP2_15 are connected to the odd pins of the pin header CN7, while the LEDs 2 to 9 are connected to the even CN7 pins.

Thus, the LEDs can be either connected to

- the device port pins Ap2_8 to AP2_15 by closing the connection on CN7 using a jumper, or
- any device pin by connecting directly with the even CN7 pins using a separate cable.

6.4 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN12 pin to the signal via a separate cable.

The CN12 pins have following pull-up or pull-down voltage levels:

- all even numbered pins are connected to L level, i.e. to GND
- odd numbered pins 1, 3, 5, 7, 9 can be connected to
  - 5.0 V, if JP25[2-1] is set
  - 3.3 V, if JP25[2-3] is set

- odd numbered pins 11, 13, 15, 17, 19 can be connected to
  - 5.0 V, if JP15[2-1] is set
  - 3.3 V, if JP15[2-3] is set

Refer to *7.5 Pull-Up/Pull-Down Pin Header CN12* for CN12 details.

6.5 Automotive Ethernet Interface

The piggyback board features a Marvell 88Q2112 Automotive Ethernet PHY (IC2) for using the device's SGMII interface (ETNB1) via the TE MateNet connector on CN17 or straight wires on block connector CN6.

If the TE MateNet connector should be used connector CN17 has to be assembled with the connector included in the delivery.

Please refer to *Figure 6.1 Ethernet connector CN17* for the placement of the connector.

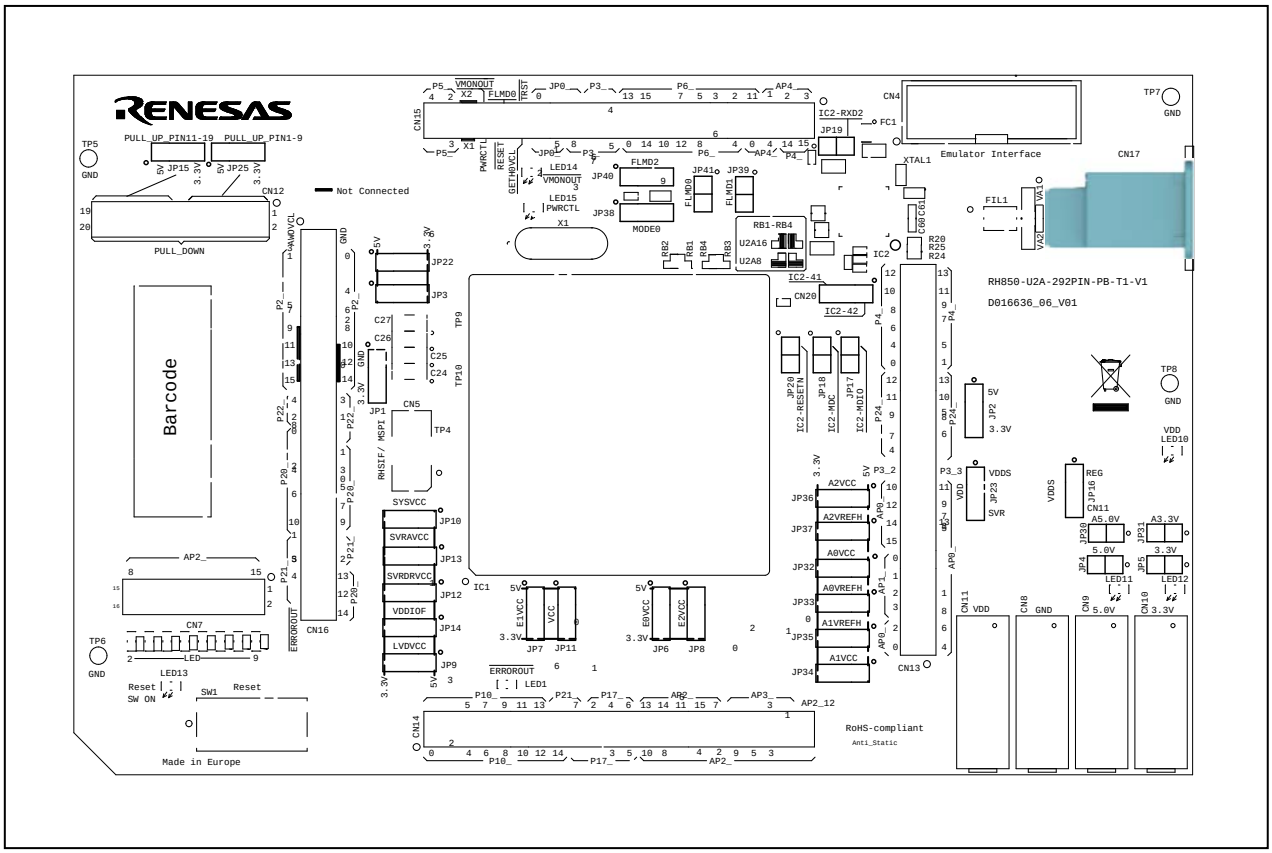


Figure 6.1 Ethernet connector CN17

If a 2-wire connection should be used connector CN6 has to be assembled with the Würth block connector included in the delivery.

In order to use CN6 it is necessary to populate the resistors R83 and R84 with 0 Ω resistors.

Please refer to *Figure 6.2 Ethernet connector CN6* for the placement of the connector.

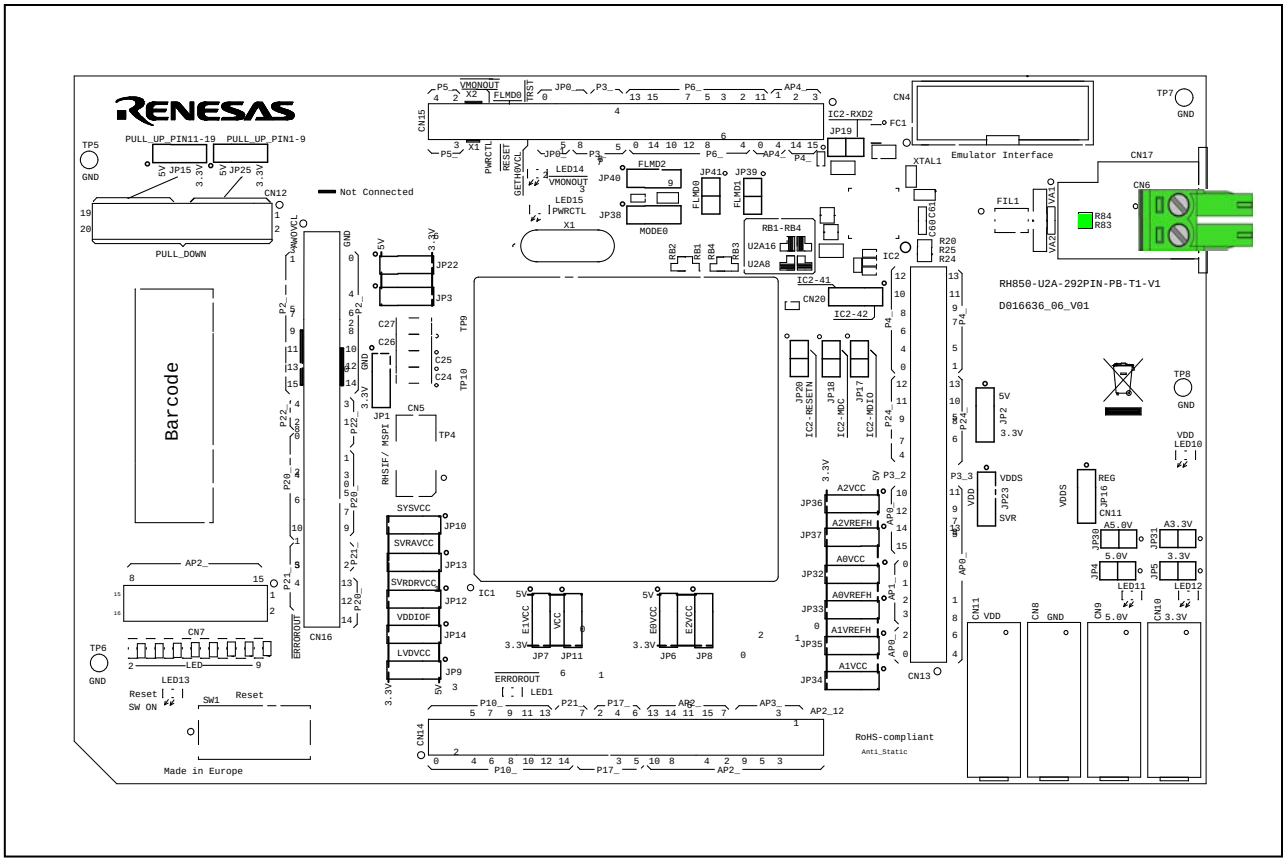


Figure 6.2 Ethernet connector CN6

Notes

1. For ETNBx initial setup please refer to the device UM. For ETNB1 operation the ETNB1SGCLKSEL register must be set to ETNB1SGCLKSEL=0x01 to select the Internal MOSC clock of 20MHz.
   For an internal MOSC clock of 20MHz the crystal X1 has to be replaced by the 20MHz crystal included in the package.
   For package content please refer to *Table 1.1 Package Components for the Y-RH850-U2A-292PIN-PB-T1-V1*
2. The signals of the device's Fast Ethernet (R)MII interface (ETNB0) are available on the Main Board connectors. Thus, ETNB0 can control an Ethernet PHY on the Main Board.
3. Alternatively, ETNB1 can also be used to operate the Main Board's 100 MB Ethernet PHY. In this case the ETNB1 Fast Ethernet mode is selected by Option Bytes settings and the pin multiplexing needs to be configured accordingly.

Refer to *7.6 Ethernet Connector CN6 and CN17* for the CN6 and CN17 pin assignment.

6.6 Renesas High-Speed Serial I/F (RHSIF) / Multichannel Serial Peripheral Interface (MSPI)

The CN5 connector can be used to connect to the device's RHSIF and MSPI0 interface.

Refer to *7.3 RHSIF/MSIP Connector CN5* for the CN5 pin assignment.

RHSIF and MSPI0 interface at CN5 are operated in LVDS mode.

Rx and Tx signals available at CN5 can be swapped by setting the jumper JP1:

- JP1[2-1]:
  - RXDP/RXDN at CN5 pins 7 and 9
  - TXDP/TXDN at CN5 pins 1 and 3
- JP1[2-3]:
  - RXDP/RXDN at CN5 pins 1 and 3
  - TXDP/TXDN at CN5 pins 7 and 9

Notes

1. In order to minimize signal interference no signals from CN5 are connected to CN16. If required they can be connected via 0 Ω resistors R15 to R18 and R21 to R23.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a Main Board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the Main Board, please refer to the User's Manual of any supported Main Board.

Refer to *1.2 Supported Main Boards* for a list of supported Main Boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Main Board function	Piggyback board device port	Pin	Main Board function	Piggyback board device port
1	VDDA	–	2	VDDA	–
3	VDDA	–	4	VDDA	–
5	RESET	RESETZ	6	NMI	P4_7
7	–	–	8	–	–
9	INT0	P10_12	10	INT1	P22_0
11	INT2	P21_7	12	INT3	P2_8
13	–	–	14	–	–
15	UART0TX	P6_6	16	UART1TX	P6_3
17	UART0RX	P6_5	18	UART1RX	P6_2
19	LIN0TX	P4_8	20	LIN1TX	P2_5
21	LIN0RX	P4_9	22	LIN1RX	P2_4
23	IIC0SCL	P17_3	24	IIC1SCL	P22_4
25	IIC0SDA	P17_2	26	IIC1SDA	P22_3
27	CAN0TX	P6_14	28	CAN1TX	P6_8
29	CAN0RX	P6_13	30	CAN1RX	P6_7
31	SENT0RX	P21_1	32	SENT1RX	P21_0
33	SENT0SPCO	P24_6	34	SENT1SPCO	P24_7
35	PSI5SRX0	P3_6	36	PSI5RX0	P5_4
37	PSI5STX0	P3_7	38	PSI5TX0	P5_6
39	PSI5SCLK0	P3_8	40	–	–
41	FLX0TX	P20_7	42	FLX0EN	P20_5
43	FLX0RX	P20_2	44	FLXSTPWT	P20_4
45	FLX1TX	P20_6	46	FLX1EN	P20_8
47	FLX1RX	P20_3	48	FLX CLK	P10_8
49	–	–	50	–	–
51	ETH0MDIO	P20_3	52	ETH0MDC	P20_6

Table 7.1 Main board connector CN1 (cont'd)

Pin	Main Board function	Piggyback board device port
53	ETH0RXD0	P10_3
55	ETH0RXD1	P10_4
57	ETH0RXD2	P10_5
59	ETH0RXD3	P10_6
61	ETH0RXCLK	P10_2
63	ETH0RXER	P10_0
65	ETH0CRSDV	P20_7
67	ETH0RXDV	P10_7
69	ETH0RESET	P20_0
71	–	–
73	USB0UDMF	–
75	USB0UDPF	–
77	–	–
79	–	–
81	–	–
83	–	–
85	DIGIO_0	P21_2
87	DIGIO_2	P21_4
89	DIGIO_4	P21_6
91	DIGIO_6	P22_0
93	DIGIO_8	P22_2
95	DIGIO_10	P10_8
97	DIGIO_12	P10_10
99	DIGIO_14	P10_12
101	–	–
103	MUX0	P6_0
105	MUX2	P6_3
107	ADC0	AP4_0
109	ADC2	AP4_2
111	ADC4	AP4_4
113	ADC6	AP3_2
115	VDDIOF	–
117	VDDB	–
119	VDDB	–

Pin	Main Board function	Piggyback board device port
54	ETH0TXD0	P20_9
56	ETH0TXD1	P20_10
58	ETH0TXD2	P20_12
60	ETH0TXD3	P20_13
62	ETH0TXCLK	P10_1
64	ETH0TXER	P20_8
66	ETH0TXEN	P20_14
68	ETH0COL	–
70	ETH0LINK	P20_1
72	–	–
74	USB0UDMH	–
76	USB0UDPH	–
78	–	–
80	–	–
82	–	–
84	–	–
86	DIGIO_1	P21_3
88	DIGIO_3	P21_5
90	DIGIO_5	P21_7
92	DIGIO_7	P22_1
94	DIGIO_9	P22_3
96	DIGIO_11	P10_9
98	DIGIO_13	P10_11
100	DIGIO_15	P10_13
102	–	–
104	MUX1	P6_2
106	–	–
108	ADC1	AP4_1
110	ADC3	AP4_3
112	ADC5	AP3_1
114	ADC7	AP3_3
116	VDDIOF	–
118	VDDB	–
120	VDDB	–

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function	Device port
1	CAN2TX	P3_2
3	CAN2RX	P3_3
5	CAN4TX	P4_6
7	CAN4RX	P4_7
9	LIN2TX	P2_0
11	LIN2RX	P2_1
13	LIN4TX	P6_12
15	LIN4RX	P6_15
17	LIN6TX	P2_7
19	LIN6RX	P2_6
21	LIN8TX	P4_0
23	LIN8RX	P4_1
25	LIN10TX	P6_5
27	LIN10RX	P6_4
29	LIN12TX	–
31	LIN12RX	–
33	LIN14TX	–
35	LIN14RX	–
37	–	–
39	CAN12TX	P24_10
41	CAN12RX	P24_11
43	CAN14TX	P17_3
45	CAN14RX	P17_4
47	CAN6TX	P4_14
49	CAN6RX	P4_15
51	CAN8TX	P10_6
53	CAN8RX	P10_5
55	CAN10TX	P24_6
57	CAN10RX	P24_7
59	–	–
61	LIN16TX	–
63	LIN16RX	–
65	LIN18TX	–
67	LIN18RX	–
69	LIN20TX	–
71	LIN20RX	–
73	LIN22TX	–
75	LIN22RX	–

Pin	Function	Device port
2	CAN3TX	P4_4
4	CAN3RX	P4_5
6	CAN5TX	P4_11
8	CAN5RX	P4_12
10	LIN3TX	P4_14
12	LIN3RX	P4_15
14	LIN5TX	P2_2
16	LIN5RX	P2_3
18	LIN7TX	P3_5
20	LIN7RX	P3_4
22	LIN9TX	P5_3
24	LIN9RX	P5_2
26	LIN11TX	P3_8
28	LIN11RX	P3_7
30	LIN13TX	–
32	LIN13RX	–
34	LIN15TX	–
36	LIN15RX	–
38	–	–
40	CAN13TX	P24_12
42	CAN13RX	P24_13
44	CAN15TX	P17_5
46	CAN15RX	P17_6
48	CAN7TX	P3_4
50	CAN7RX	P3_5
52	CAN9TX	P24_4
54	CAN9RX	P24_5
56	CAN11TX	P24_8
58	CAN11RX	P24_9
60	–	–
62	LIN17TX	–
64	LIN17RX	–
66	LIN19TX	–
68	LIN19RX	–
70	LIN21TX	–
72	LIN21RX	–
74	LIN23TX	–
76	LIN23RX	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function	Device port
77	–	–
79	SFMA0CLK	P17_5
81	SFMA0IO0	P17_3
83	SFMA0IO2	P17_1
85	–	–
87	MMCA0CLK	P24_4
89	MMCA0DAT0	P24_6
91	MMCA0DAT2	P24_8
93	MMCA0DAT4	P24_10
95	MMCA0DAT6	P24_12
97	–	–
99	ETH1MDIO	–
101	ETH1RXD0	–
103	ETH1RXD1	–
105	ETH1RXD2	–
107	ETH1RXD3	–
109	ETH1RXCLK	–
111	ETH1RXER	–
113	ETH1CRSDV	–
115	ETH1RXDV	–
117	ETH1RESET	–
119	–	–

Pin	Function	Device port
78	–	–
80	SFMA0SSL	P17_4
82	SFMA0IO1	P17_2
84	SFMA0IO3	P17_0
86	–	–
88	MMCA0CMD	P24_5
90	MMCA0DAT1	P24_7
92	MMCA0DAT3	P24_9
94	MMCA0DAT5	P24_11
96	MMCA0DAT7	P24_13
98	–	–
100	ETH1MDC	–
102	ETH1TXD0	–
104	ETH1TXD1	–
106	ETH1TXD2	–
108	ETH1TXD3	–
110	ETH1TXCLK	–
112	ETH1TXER	–
114	ETH1TXEN	–
116	ETH1COL	–
118	ETH1LINK	–
120	–	–

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function	Device port
1	CSI0CS0	P21_7
3	CSI0CS1	P21_6
5	CSI0CS2	P21_5
7	CSI0CS3	P21_4
9	–	–
11	–	–
13	PSI5SRX1	P6_13
15	PSI5STX1	P6_14
17	PSI5SCLK1	P6_15
19	–	–
21	CSI1CS2	P24_9

Pin	Function	Device port
2	CSI0CLK	P22_4
4	CSI0SI	P22_1
6	CSI0SO	P22_0
8	–	–
10	CSI1CS1	P24_8
12	–	–
14	PSI5RX1	P5_2
16	PSI5TX1	P5_3
18	–	–
20	–	–
22	CSI1CS3	P4_8

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
23	–	–
25	–	–
27	–	–
29	CSI1SCLK	P24_4
31	–	–
33	–	–
35	–	–
37	–	–
39	–	–
41	–	–
43	–	–
45	–	–
47	–	–
49	–	–
51	–	–
53	–	–
55	AD1_0	AP2_0
57	AD1_2	AP2_2
59	AD1_4	AP2_4
61	AD1_6	AP2_6
63	PWM0	P24_4
65	PWM2	P24_6
67	PWM4	P24_8
69	PWM6	P24_10
71	DIGIO16	AP0_0
73	DIGIO18	AP0_2
75	DIGIO20	AP0_4
77	DIGIO22	AP0_6
79	ENC0	P10_8
81	–	–
83	–	–
85	–	–
87	–	–
89	–	–
91	–	–
93	–	–
95	–	–
97	–	–
99	–	–

Pin	Function	Device port
24	CSI1CS0	P24_7
26	DIGIO_24	P17_6
28	CSI1SO	P24_6
30	CSI1SI	P24_5
32	–	–
34	–	–
36	–	–
38	–	–
40	–	–
42	–	–
44	–	–
46	–	–
48	–	–
50	–	–
52	–	–
54	–	–
56	AD1_1	AP2_1
58	AD1_3	AP2_3
60	AD1_5	AP2_5
62	AD1_7	AP2_7
64	PWM1	P24_5
66	PWM3	P24_7
68	PWM5	P24_9
70	PWM7	P24_11
72	DIGIO17	AP0_1
74	DIGIO19	AP0_3
76	DIGIO21	AP0_5
78	DIGIO23	AP0_7
80	ENC1	P10_9
82	–	–
84	–	–
86	–	–
88	–	–
90	–	–
92	–	–
94	–	–
96	–	–
98	–	–
100	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
101	–	–
103	–	–
105	–	–
107	–	–
109	–	–
111	–	–
113	–	–
115	–	–
117	–	–
119	–	–

Pin	Function	Device port
102	–	–
104	–	–
106	–	–
108	–	–
110	–	–
112	–	–
114	–	–
116	–	–
118	–	–
120	–	–

7.2 Debug Connector CN4

Table 7.4 On-chip debug connector CN4

Pin	Function	Device port
1	TDCK / LPDCLK / FPCK	JP0_2
3	TRSTZ	
5	TDO / LPDO / FPDT	JP0_1
7	TDI / LPDIO / FPDR	JP0_0
9	TMS	JP0_3
11	RDY / LPDCLKOUT	JP0_5
13	RESETZ	

Pin	Function	Device port
2	GND	
4	FLMD0	
6	–	
8	E0VCC	
10	–	
12	GND	
14	GND	

7.3 RHSIF/MSIP Connector CN5

Table 7.5 RHSIF/MISP connector CN5

Pin	JP1[2-1]		JP1[2-3]	
	Device port	Function	Device port	Function
1	P2_13	HSIF0_TXDP / MSPI0_SOP	P2_11	HSIF0_RXDP / MSPI0_SIP
2	P2_15	MSPI0_SCKP	P2_15	MSPI0_SCKP
3	P2_12	HSIF0_TXDN / MSPI0_SON	P2_10	HSIF0_RXDN / MSPI0_SIN
4	P2_14	MSPI0_SCKN	P2_14	MSPI0_SCKN
5	–	GND	–	GND
6	P2_9	HSIF0_REFCLK / MSPI0CSS4	P2_9	HSIF0_REFCLK / MSPI0CSS4
7	P2_11	HSIF0_RXDP / MSPI0_SIP	P2_13	HSIF0_TXDP / MSPI0_SOP
8	–	GND	–	GND

Table 7.5 RHSIF/MISP connector CN5 cont'd

Pin	JP1[2-1]		JP1[2-3]	
	Device port	Function	Device port	Function
9	P2_10	HSIF0_RXDN / MSPI0_SIN	P2_12	HSIF0_TXDN / MSPI0_SON
10	–	GND	–	GND
11	–	GND	–	GND
12	–	GND	–	GND

Note

In order to minimize signal interference no signals from CN5 are connected to CN16. If required they can be connected via 0 Ω resistors R15 to R18 and R21 to R23.

7.4 Device Ports Connectors CN13 to CN16

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.4.1 Device Ports Connector CN13

Pin	Device port
1	AP0_4
3	AP0_6
5	AP0_8
7	AP0_1
9	AP0_3
11	AP0_5
13	AP0_7
15	AP0_13
17	AP0_9
19	AP0_11
21	P3_3
23	P24_5
25	P24_6
27	P24_8
29	P24_10
31	P24_13
33	P4_1
35	P4_5
37	P4_7
39	P4_9
41	P4_11
43	P4_13

Pin	Device port
2	AP0_0
4	AP0_2
6	AP1_3
8	AP1_2
10	AP1_1
12	AP1_0
14	AP0_15
16	AP0_14
18	AP0_12
20	AP0_10
22	P3_2
24	P24_4
26	P24_7
28	P24_9
30	P24_11
32	P24_12
34	P4_0
36	P4_4
38	P4_6
40	P4_8
42	P4_10
44	P4_12

7.4.2 Device Ports Connector CN14

Table 7.6 Device ports connector CN14

Pin	Device port	Pin	Device port
1	P10_0	2	P10_1
3	P10_2	4	P10_3
5	P10_4	6	P10_5
7	P10_6	8	P10_7
9	P10_8	10	P10_9
11	P10_10	12	P10_11
13	P10_12	14	P10_13
15	P10_14	16	P21_6
17	P17_0	18	P21_7
19	P17_1	20	P17_2
21	P17_3	22	P17_4
23	P17_5	24	P17_6
25	AP2_10	26	AP2_13
27	AP2_8	28	AP2_14
29	AP2_6	30	AP2_11
31	AP2_4	32	AP2_15
33	AP2_2	34	AP2_7
35	AP2_9	36	AP3_0
37	AP2_5	38	AP3_2
39	AP2_3	40	AP3_3
41	AP2_1	42	AP3_1
43	AP2_0	44	AP2_12

7.4.3 Device Ports Connector CN15

Table 7.7 Device ports connector CN15

Pin	Device port	Pin	Device port
1	AP4_3	2	P4_15
3	AP4_2	4	P4_14
5	AP4_1	6	AP4_4
7	P6_11	8	AP4_0
9	P6_2	10	P6_4
11	P6_3	12	P6_6
13	P6_5	14	P6_8
15	P6_7	16	P6_12
17	P6_9	18	P6_10
19	P6_15	20	P6_14
21	P6_13	22	P6_0
23	P3_4	24	P3_5
25	P3_7	26	P3_6
27	JP0_3	28	P3_8
29	JP0_1	30	JP0_5
31	JP0_0	32	JP0_2
33	TRSTZ	34	GETH0VCL
35	FLMD0	36	RESETZ
37	VMONOUTZ	38	PWRCTL
39	X2_C *	40	X1_C *
41	P5_2	42	P5_3
43	P5_4	44	P5_6

Note * By default these signals are not connected to CN15 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R3 and R4.

7.4.4 Device Ports Connector CN16

Table 7.8 Device ports connector CN16

Pin	Device port	Pin	Device port
1	AWOVCL	2	GND
3	P2_1	4	P2_0
5	P2_3	6	P2_2
7	P2_5	8	P2_4
9	P2_7	10	P2_6
11	CN_P2_9 *	12	P2_8
13	CN_P2_11 *	14	CN_P2_10 *
15	CN_P2_13 *	16	CN_P2_12 *
17	CN_P2_15 *	18	CN_P2_14 *
19	P22_4	20	P22_3
21	P22_2	22	P22_1
23	P20_0	24	P22_0
25	P20_2	26	P20_1
27	P20_4	28	P20_3
29	P20_6	30	P20_5
31	P20_8	32	P20_7
33	P20_10	34	P20_9
35	P21_1	36	P21_0
37	P21_3	38	P21_2
39	P21_4	40	P20_13
41	P21_5	42	P20_12
43	ERROROUTZ	44	P20_14

Note * By default these signals are not connected to CN16 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R15 to R18 and R21 to R23.

7.5 Pull-Up/Pull-Down Pin Header CN12

Pin	Function
1	fixed H level, depends on JP25: • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V
3	
5	
7	
9	
11	fixed H level, depends on JP15: • JP15[2-1]: 5.0 V • JP15[2-3]: 3.3 V
13	
15	
17	
19	

Pin	Function
2	fixed L level
4	
6	
8	
10	
12	
14	
16	
18	
20	

7.6 Ethernet Connector CN6 and CN17

Please refer to *6.5 Automotive Ethernet Interface* for details on the function of these pins.

Table 7.9 Ethernet connector CN6

Pin	Function
1	MDIN_cn
2	MDIP_cn

Table 7.10 Ethernet connector CN17

Pin	Function
1	MDIN_cn
2	MDIP_cn
3	GND
4	GND
5	GND
6	GND
7	GND

7.7 GPIO/LED Connector CN20

Please refer to the data sheet of “Marvell 88Q2112 Automotive 100/1000BASE-T1 Transceiver” for details on the function of these pins.

Table 7.11 GPIO/LED connector CN20

Pin	JP1[2-1]	
	Device port	Function
1	GPIO, pin 42	GPIO output of Marvell PHY
2	NC	Not connected
3	LED, pin 41	LED output of Marvell PHY

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumpers Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings, that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool is able to provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Configuration Examples

8.2.1 General Settings

All of the following board configurations are based on these conditions:

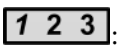
- Normal device operation mode (JP41[OPEN]: FLMD0 = L).
- All voltages for all functions are activated.
- Current measurements are not carried out, hence JP4, JP5, JP30 and JP31 are set.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 to CN11 must be assembled on the board.

8.2.2 Jumper Indicators

- The green jumper JP41 for FLMDO0 must always be open for a ‘normal’ (user mode and debug) operation of the device.
- The red jumpers are related to the power supply configuration.

Following jumper symbols are used:

–  : open jumper
– 

: jumper must be set in the indicated position
– 

: jumper must be set, *italic* position indicator is optional, see description above the figure

Note

The pin 1 of a jumper can be identified by a

- small circle near the jumper
- square soldering pad.

8.2.3 Stand-Alone Operation with Single External Power Supply: Minimum Configuration

This example enables to operate the board with only the 3.3 V external power supply.
Since no 5 V voltage is available, all I/O ports can only use 3.3 V.

- CN8: GND connection
- CN9: not connected, no 5.0 V
  - jumpers JP2, JP3, JP6 to JP14, JP22 and JP32 to JP37 are set to 3.3 V position [2-3]
- CN10: 3.3 V
- CN11: not connected, no IN_1v12
  - JP16[2-1]: use reg_vcc_VDD from on-board voltage regulator for supply of VDD voltage
  - VDD from reg_vcc_VDD (JP23[2-1]) or from SVR_OUTPUT (JP23[2-3]) from on-chip Switching Voltage Regulator

  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

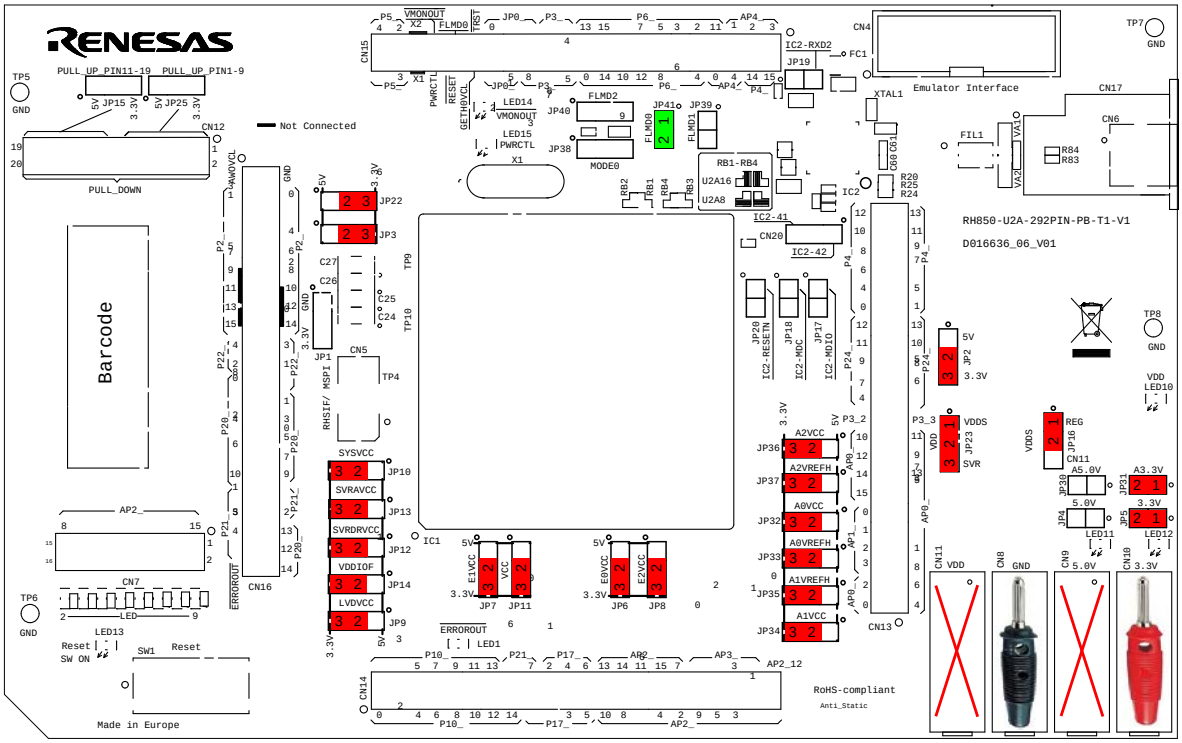


Figure 8.1 Stand-alone operation with minimum external power supply

8.2.4 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

- CN8: GND connection
- CN9: 5 V
  - select desired 3.3 V/5.0 V via jumpers JP2, JP3, JP6 to JP14, JP22 and JP32 to JP3

  Refer to *3.2Voltage Distribution* for further details about VDD voltage and possible settings of jumpers JP2, JP3 and JP22.
- CN10: 3.3 V
- CN11: 1.12 V (IN_1v12)
  - JP16[2-3], JP23[2-1]: use IN_1v12 for VDD voltage

  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

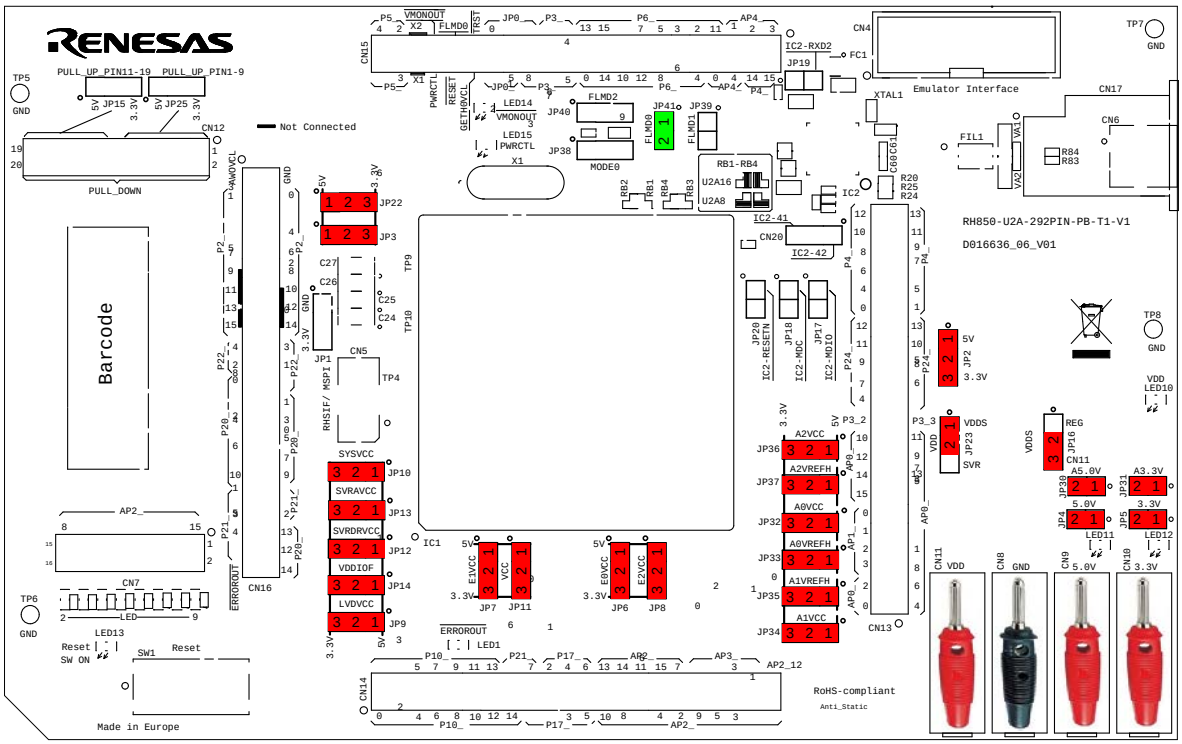


Figure 8.2 Stand-alone operation with maximum external power supply

8.2.5 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

Do not supply the 5V (CN9) and 3.3V (CN10) voltage directly to the piggyback board

- CN8 to CN11: not connected, no external 5.0 V, 3.3 V, 1.12 V
- select desired 3.3 V/5.0 V via jumpers JP2, JP3, JP6 to JP14, JP22 and JP32 to JP3

  Refer to *3.2Voltage Distribution* for further details about VDD voltage and possible settings of jumpers JP2, JP3 and JP22.
- VDD supply:
  - JP16[2-1]: use reg_vcc_VDD from on-board voltage regulator for supply of VDD voltage
  - VDD from reg_vcc_VDD (JP23[2-1]) or SVR_OUTPUT (JP23[2-3]) from on-chip Switching Voltage Regulator

  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

This configuration still allows to utilize an external IN_1v12 voltage (connected to CN8, CN11) as the source for VDD voltage. In this case set JP16[2-3] and JP23[2-1].

CAUTION

Do not supply 5V (CN9) and 3.3V (CN10) directly to the piggyback board if these voltages are already supplied by the main board.

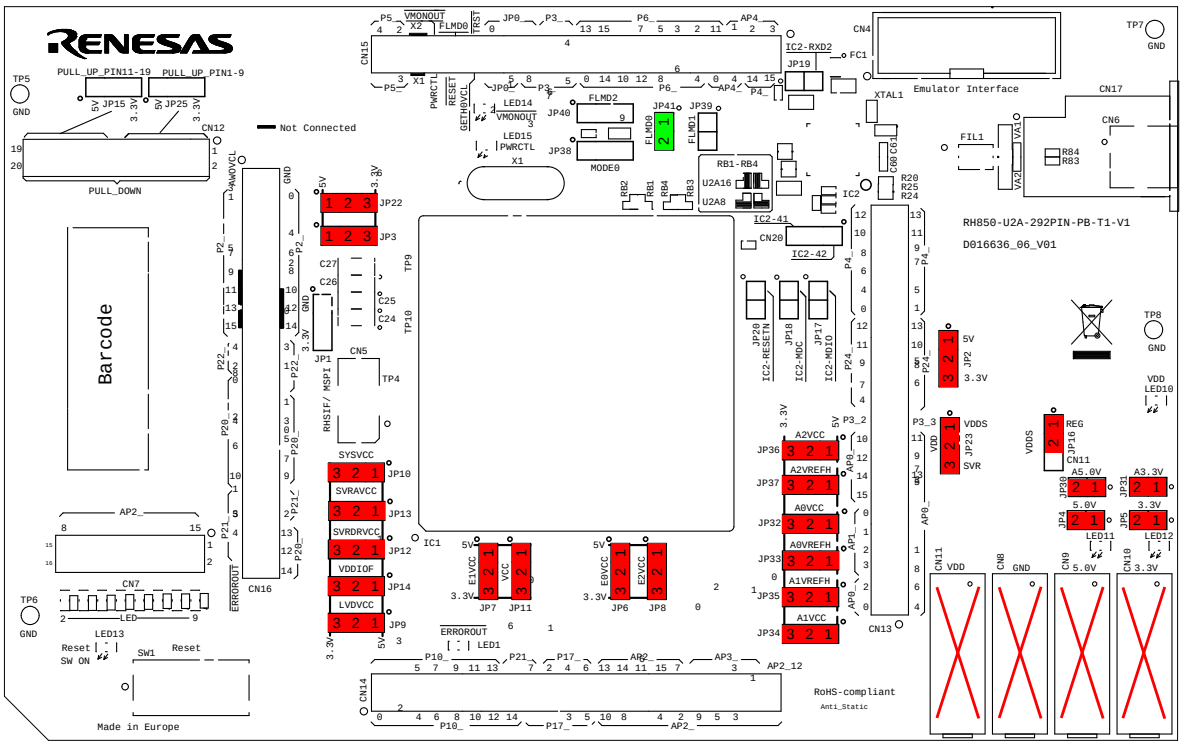


Figure 8.3 Main board operation without external power supply

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied, when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '2-3 ON' position, so that RESET is permanently asserted. Alternatively keep SW1 manually in' 2-1 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to section *6.2 RESET Switch*.

9.2 CAN0RX is Shared with FLASH Programmer Signal FLMD1

When using this product plugged into a motherboard where CAN0 is connected to the CAN-transceiver the FLASH programmer will not work.

This is because the CAN0RX function is shared with the FLMD1 function on the same device PIN.

Most CAN-transceiver are driving the RX line actively and the FLASH programmer then is not able to change signal level as required for flashing.

10. Mechanical Dimensions

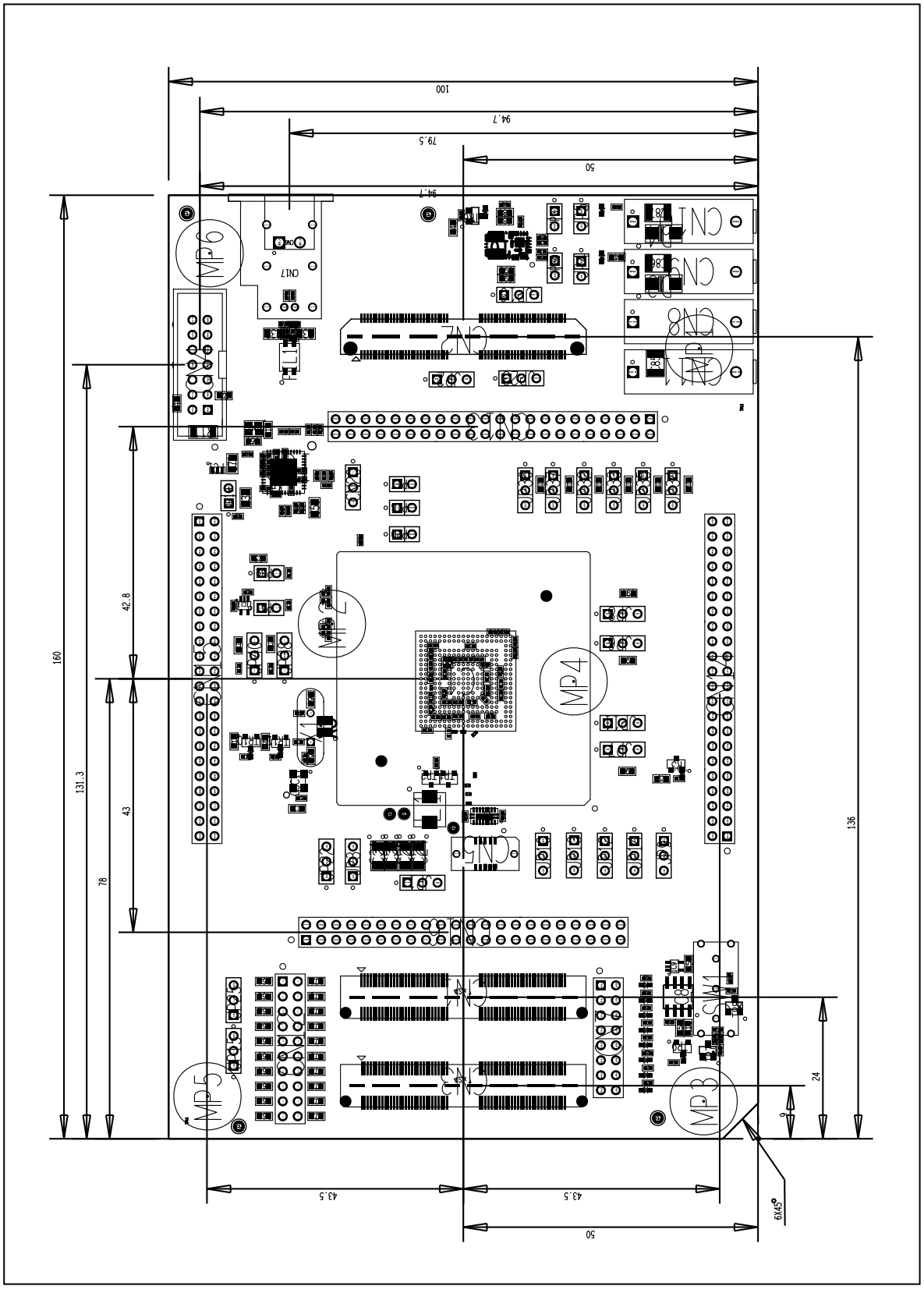


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Oscillators and resonators: OSC1, X3
- Capacitors: C60, C61, C97, C98
- Resistors: R2 – R4, R6, R15 – R18, R20, R21 – R23, R25, R143

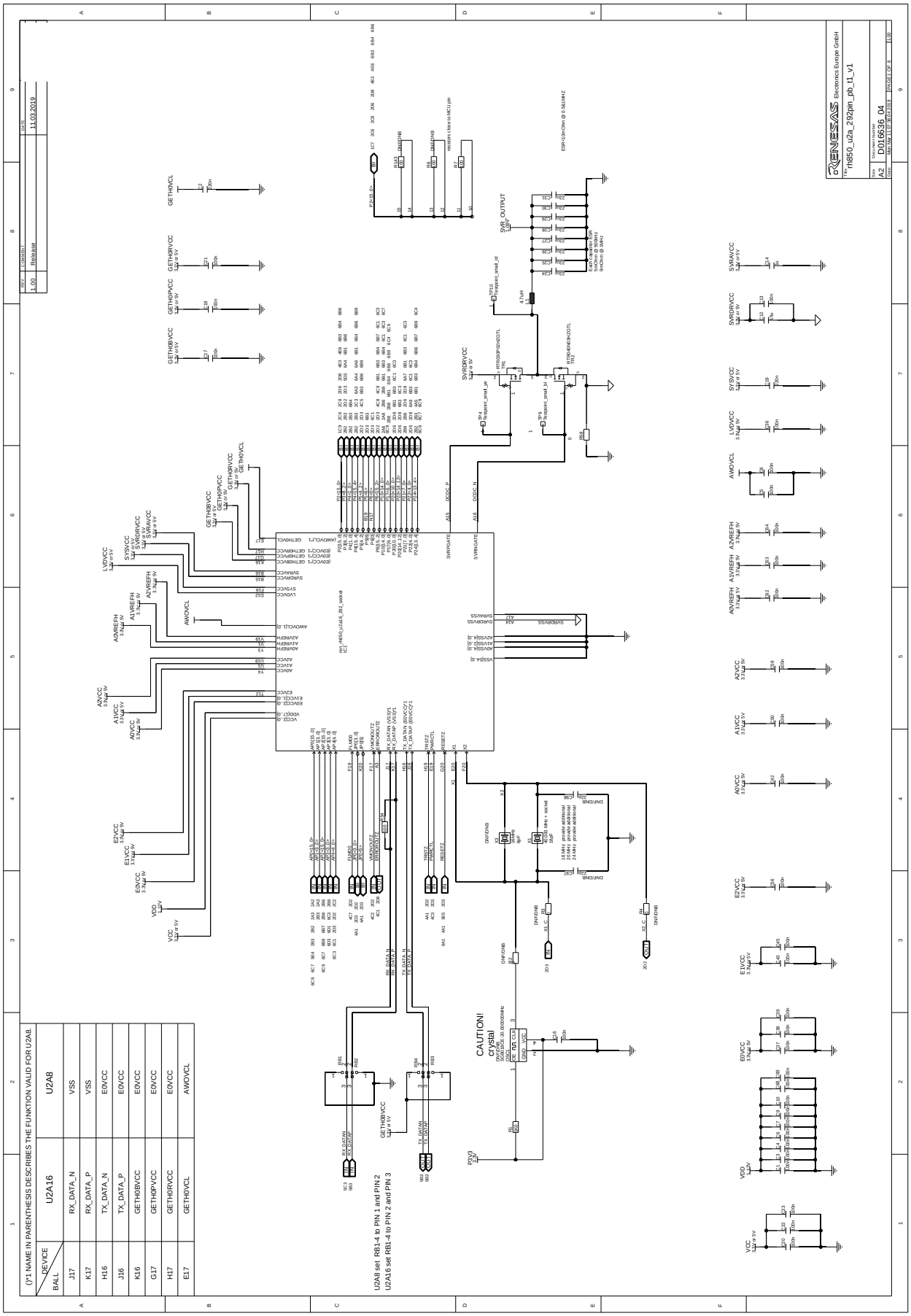
The above components are indicated with "DNF/DNB" in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

- 3 Hirschmann 4 mm power lab sockets, red for CN9 – CN11
- 1 Hirschmann 4 mm power lab sockets, black for CN8
- three resonators HC49 (16/20/24 MHz)
- 44 jumpers, 2.54 mm, black

The above components are indicated with "DO NOT FIT / TO DELIVER WITH THE BOARD" in the schematics.

11.1 Page 1


(*)1 NAME IN PARENTHESIS DESCRIBES THE FUNKTION VALID FOR U2A8.
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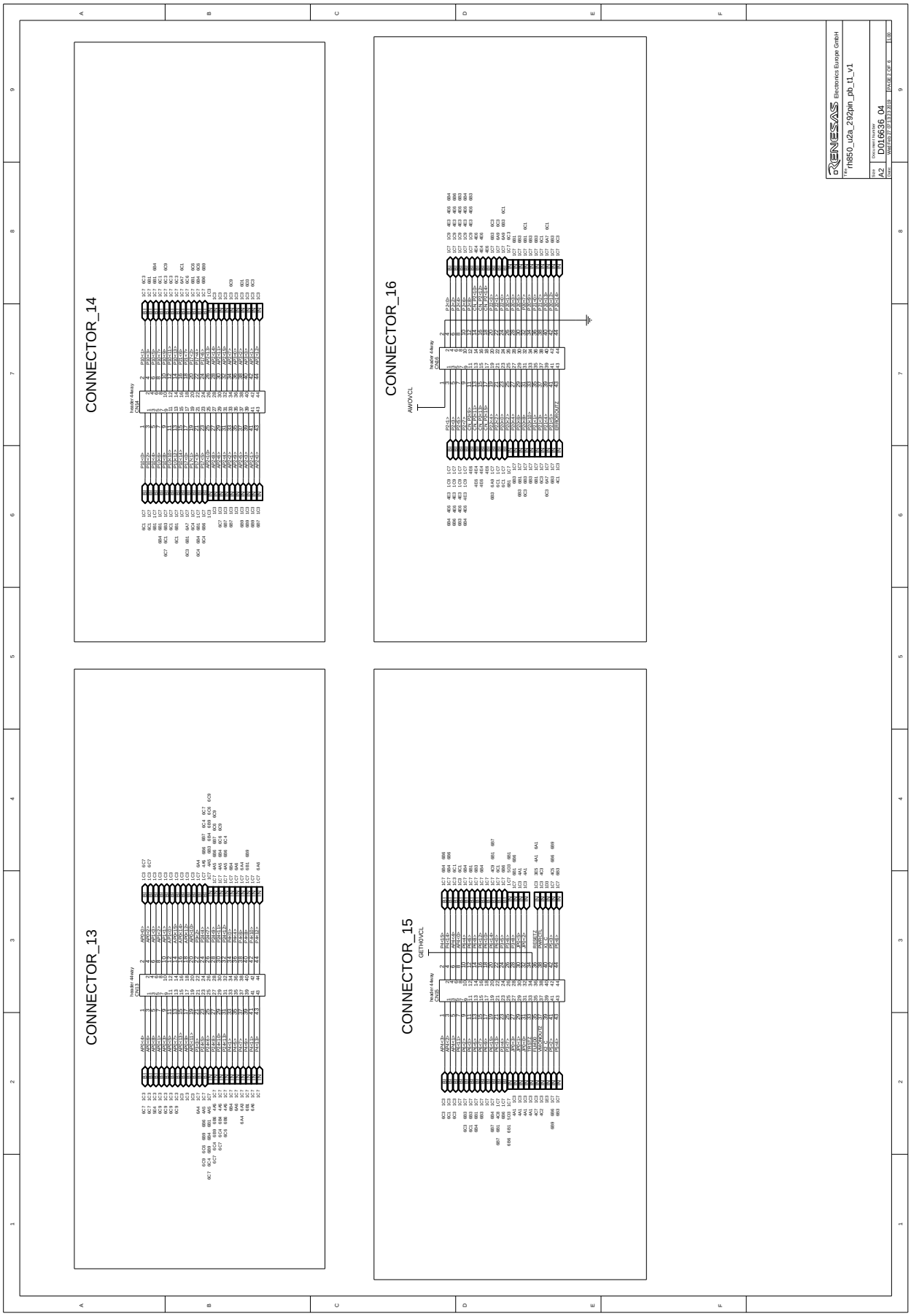
U2A16
U2A8
J17 RX_DATA_N VSS
K17 RX_DATA_P VSS
H16 TX_DATA_N E0VCC
J16 TX_DATA_P E0VCC
K16 GETH0BVCC E0VCC
G17 GETH0PVCC E0VCC
H17 GETH0RVCC E0VCC
E17 GETH0VCL AWOVCL
U2A8 set RB1-4 to PIN 1 and PIN 2
U2A16 set RB1-4 to PIN 2 and PIN 3
CAUTION!
crystal
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

11.2 Page 2


CONNECTOR_14
CONNECTOR_16
CONNECTOR_13
CONNECTOR_15
RENESAS Electronics Europe GmbH
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D0166636_04
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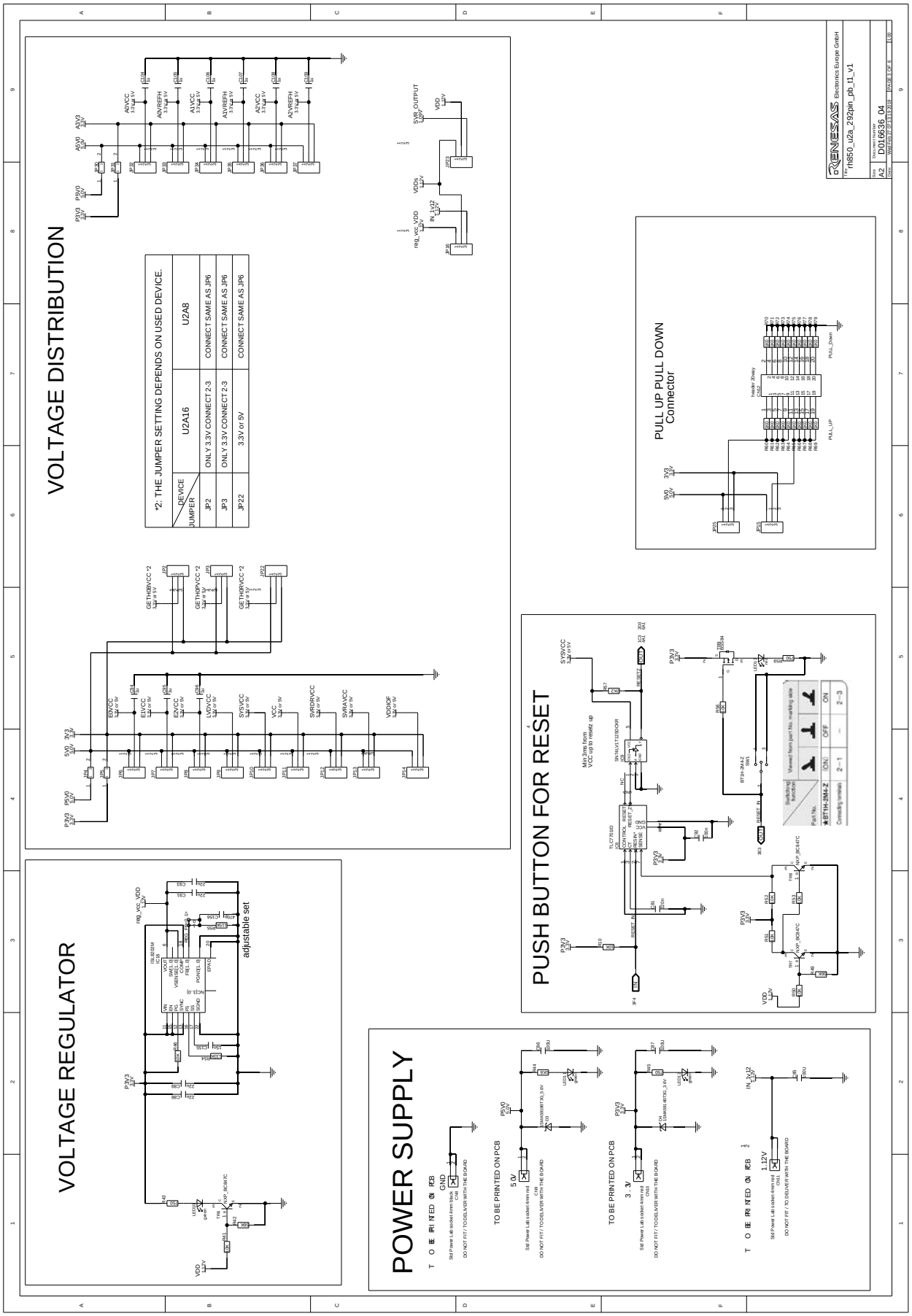
11.3 Page 3



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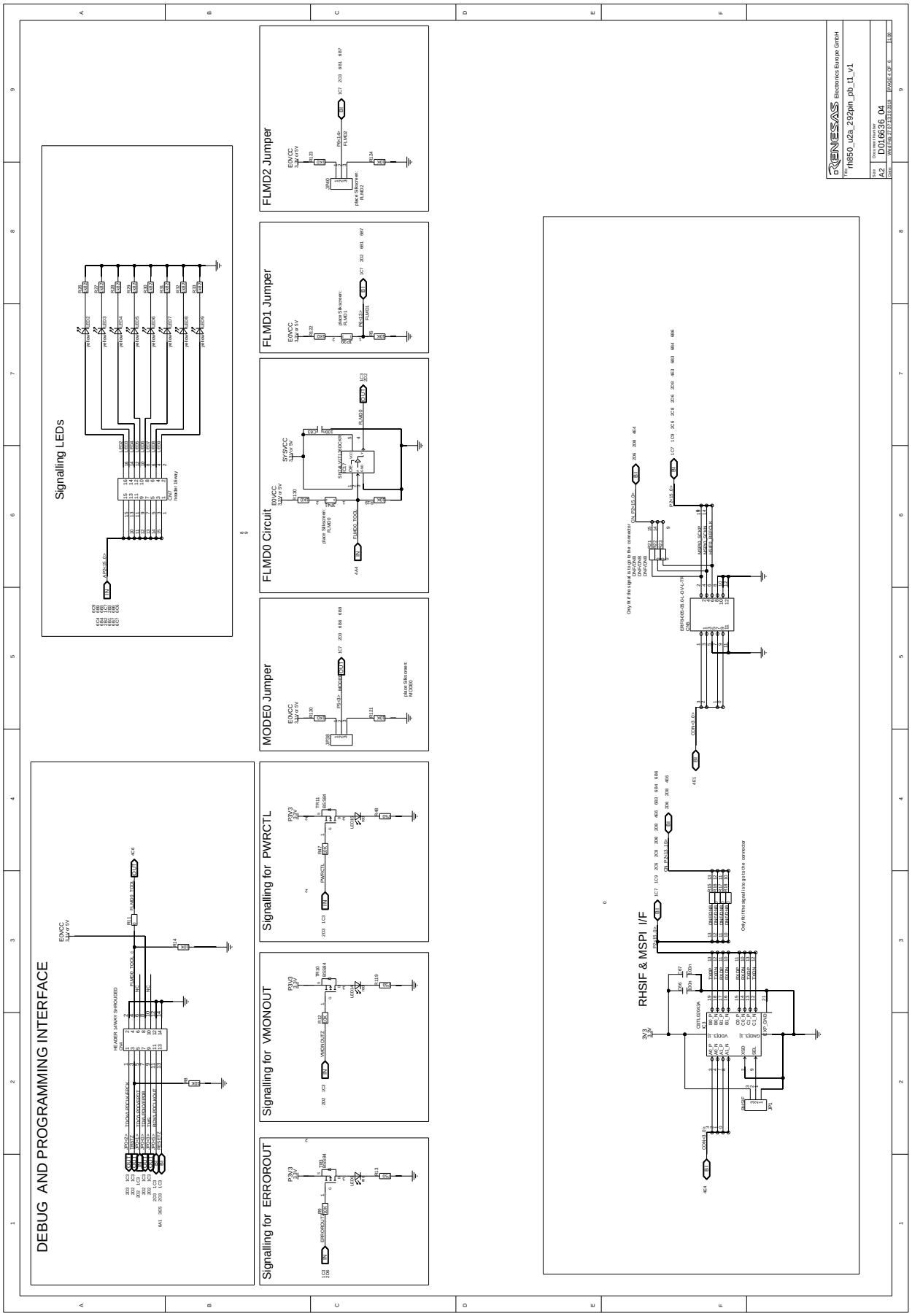
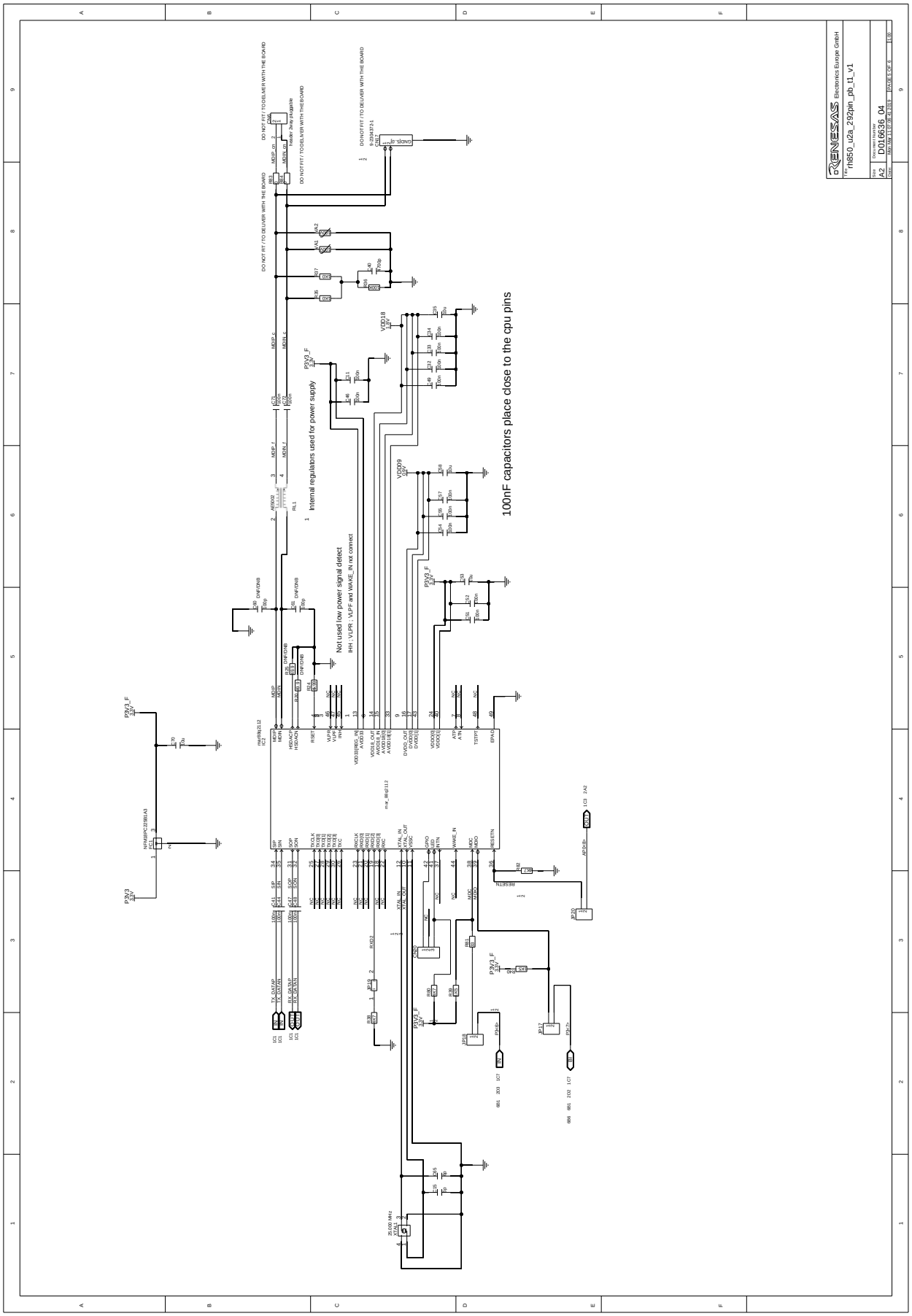
11.4 Page 4



11.5 Page 5


Internal regulators used for power suppy
Not used low power signal detect
100nF capacitors place close to the cpu pins
DO NOT FIT / TO DELIVER WITH THE BOARD
RENESAS Electronics Europe GmbH
rh850_u2a_292pin_pb_t1_v1
D0166636_04
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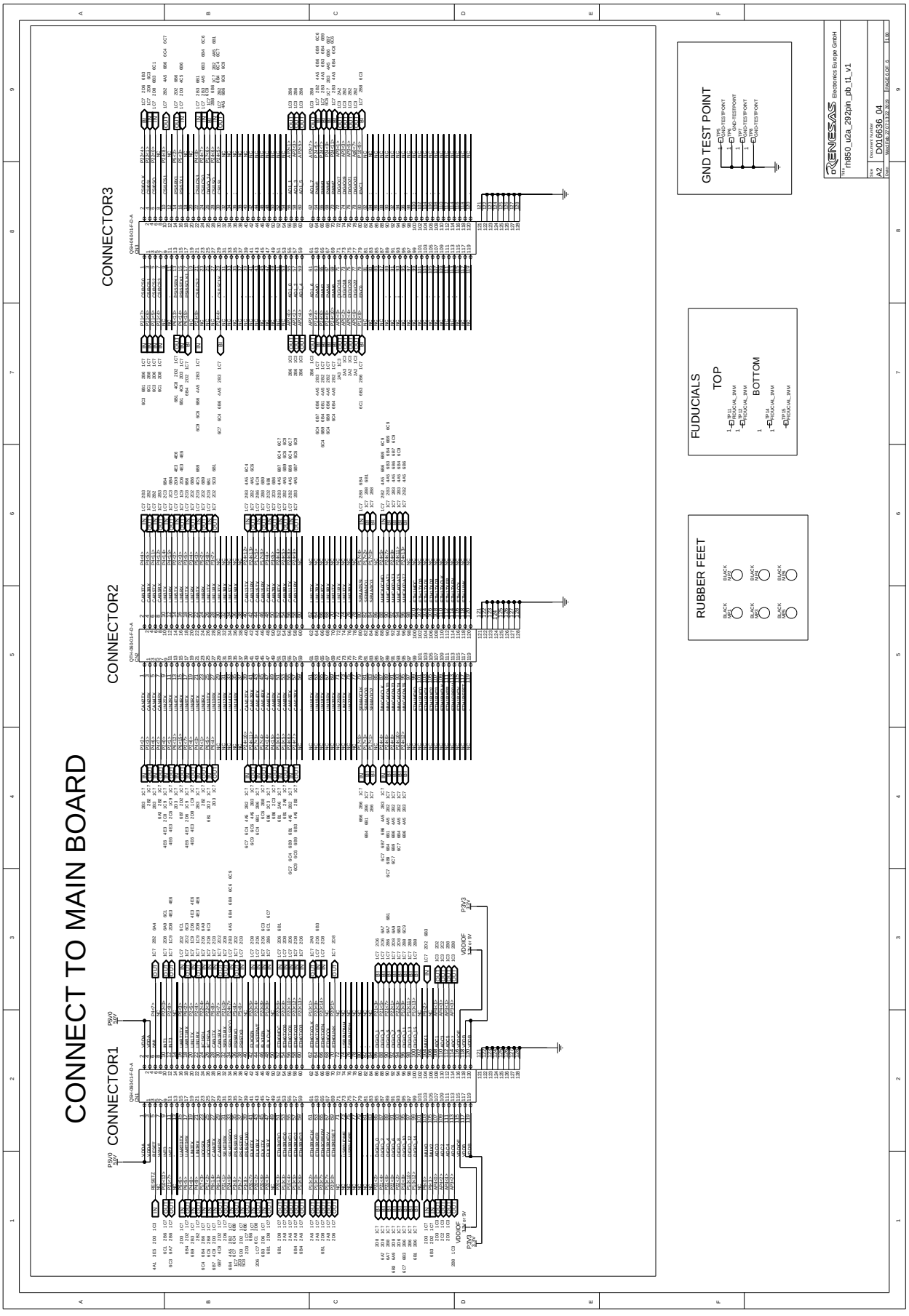
11.6 Page 6


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
GND TEST POINT
FUDUCIALS
TOP
BOTTOM
RUBBER FEET
RENESAS Electronics Europe GmbH
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D0166636_04
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		Description	
Rev.	**Date**	**Page**	**Summary**
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