Automotive & Embedded Info

Never Forget Basics Whether its Life or Anything Else ... Basics are Cores. While seeing a Tree how can we forget Seed...

SPI

SPI

What is SPI?

Serial peripheral interface. SPI is a 4 wire bus used communicate between different IC's on a PCB board. Single master communication protocol. Full duplex communication.

Lines/Signals in SPI: –

4 LINES. 1. MISO 2. MOSI 3. SCLK 4. SS.

Maximum and Standard Speed: –

Maximum speed: – 100 MHz

Standard speed: – —

Read and Write on SPI bus: –

The master transmit logic 0 for the desired chip over the chip selects line. A logic 0 is transmitted because chip select line is active low, meaning it's off state is logic 1; on is asserted with logic 0. If a waiting period is required (such as for A to D conversion), then the master must wait at least for that period of time before starting to issue the clock cycle.

During each SPI clock cycle, a full duplex data transmission occurs.

The master sends a bit on the MOSI line, the slave it read from the same line.

The slave sends a bit on the miso line, the master it read from the same line.

Transmission normally involves two shift register of some given word size, such as eight bits, one in a master and one in a slave, they are connected in a ring. Data is usually shifted out with the MSB bit first, while shifting a new LSB bit into the same register. After that register has been shifted out, the master and slave have exchange their register values. Then each device takes that value and does something with it, such as writing it to memory. If there is more data to exchange, the shift register are loaded with new data and the process repeats.

Modes of Operation in SPI: –

FOUR MODES. MODE 0, 1, 2 & 3.

S.NO.	MODE	CPHA	CPOL
1	0	0	0

2	1	0	1
3	2	1	0
4	3	1	1

At CPOL=0 the base value of the clock is zero.

For CPHA=0, data are captured on the clock's rising edge (low→high transition) and data is propagated on a falling edge (high→low clock transition).for CPHA=1, data are captured on the clock's falling edge and data is propagated on a rising edge.

At CPOL=1 the base value of the clock is one (inversion of CPOL=0).

For CPHA=0, data are captured on clock's falling edge and data is propagated on a rising edge. For CPHA=1, data are captured on clock's rising edge and data is propagated on a falling edge.

That is, CPHA=0 means sample on the leading (first) clock edge, while CPHA=1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. Note that with CPHA=0, the data must be stable for a half cycle before the first clock cycle.

Slave Daisy Chain Network in SPI: –

Yes. SPI bus are designed to be capable of being connect in daisy chain configuration, the first slave output is connected to second slave input etc. The SPI port of each slave is designed to send out during the second group of clock pulse an exact copy of what it received during first group of clock pulses. The whole chain act as a SPI communication shift registers; daisy chaining is often done with the shift register to provide a bank of

from the master, rather than a separate SS line for each slave.

Share this:

Twitter Facebook

Like

Be the first to like this.