

Debugger Basics - Training

[TRACE32 Online Help](#)

[TRACE32 Directory](#)

[TRACE32 Index](#)

[TRACE32 Training](#)



[Debugger Training](#)



[Debugger Basics - Training](#)

1

[System Concept](#)

5

 On-chip Debug Interface

6

 Debug Features

6

 TRACE32 Tools

7

 On-chip Debug Interface plus On-chip Trace Buffer

9

 On-chip Debug Interface plus Trace Port

11

 NEXUS Interface

12

[Starting a TRACE32 PowerView Instance](#)

13

 Basic TRACE32 PowerView Parameters

13

 Configuration File

13

 Standard Parameters

14

 Examples for Configuration Files

15

 Additional Parameters

19

 Application Properties (Windows only)

20

 Configuration via T32Start (Windows only)

21

 About TRACE32

22

 Version Information

22

 Prepare Full Information for a Support Email

23

[Establish your Debug Session](#)

24

[TRACE32 PowerView](#)

25

 TRACE32 PowerView Components

25

 Main Menu Bar and Accelerators

26

 Main Tool Bar

28

 Window Area

30

 Command Line

33

 Message Line

36

 Softkeys

37

 State Line

38

[Registers](#)

39

 Core Registers

39

Display the Core Registers	39
Colored Display of Changed Registers	40
Modify the Contents of a Core Register	41
Special Function Register	42
Display the Special Function Registers	42
Details about a Single Special Function Register	45
Modify a Special Function Register	46
The PER Definition File	47
Memory Display and Modification	48
The Data.dump Window	49
Display the Memory Contents	49
Modify the Memory Contents	54
Run-time Memory Access	55
Colored Display of Changed Memory Contents	65
The List Window	66
Displays the Source Listing Around the PC	66
Displays the Source Listing of a Selected Function	67
Breakpoints	69
Breakpoint Implementations	69
Software Breakpoints in RAM	69
Software Breakpoints in FLASH	71
Onchip Breakpoints in NOR Flash	72
Onchip Breakpoints on Read/Write Accesses	75
Onchip Breakpoints by Processor Architecture	76
ETM Breakpoints for ARM or Cortex-A/-R	88
Breakpoint Types	90
Program Breakpoints	91
Read/Write Breakpoints	93
Breakpoint Handling	95
Breakpoint Setting at Run-time	95
Real-time Breakpoints vs. Intrusive Breakpoints	96
Break.Set Dialog Box	98
The HLL Check Box - Function Name	99
The HLL Check Box - Program Line Number	102
The HLL Check Box - Variable	103
The HLL Check Box - HLL Expression	105
Implementations	108
Actions	109
Options	113
DATA Breakpoints	117
Advanced Breakpoints	121
TASK-aware Breakpoints	122

Intrusive TASK-aware Breakpoint	122
Real-time TASK-aware Breakpoint	125
COUNTer	126
Software Counter	126
On-chip Counter	129
CONDITION	130
CMD	138
memory/register/var	141
Display a List of all Set Breakpoints	146
Delete Breakpoints	147
Enable/Disable Breakpoints	147
Store Breakpoint Settings	148
Debugging	149
Debugging of Optimized Code	149
Basic Debug Control	152
Sample-based Profiling	164
Program Counter Sampling	164
Standard Procedure	165
Details	169
TASK Sampling	171

Debugger Basics - Training

Version 16-Apr-2019

System Concept

A single-core processor/multi-core chip can provide:

- An on-chip debug interface
- An on-chip debug interface plus an on-chip trace buffer
- An on-chip debug interface plus an off-chip trace port
- A NEXUS interface including an on-chip debug interface

Depending on the debug resources different debug features can be provided and different TRACE32 tools are offered.

The TRACE32 debugger allows you to test your embedded hardware and software by using the on-chip debug interface. The most common on-chip debug interface is JTAG.

A single on-chip debug interface can be used to debug all cores of a multi-core chip.

Debug Features

Depending on the processor architecture different debug features are available.

Debug features provided by all processor architectures:

- Read/write access to registers
- Read/write access to memories
- Start/stop of program execution

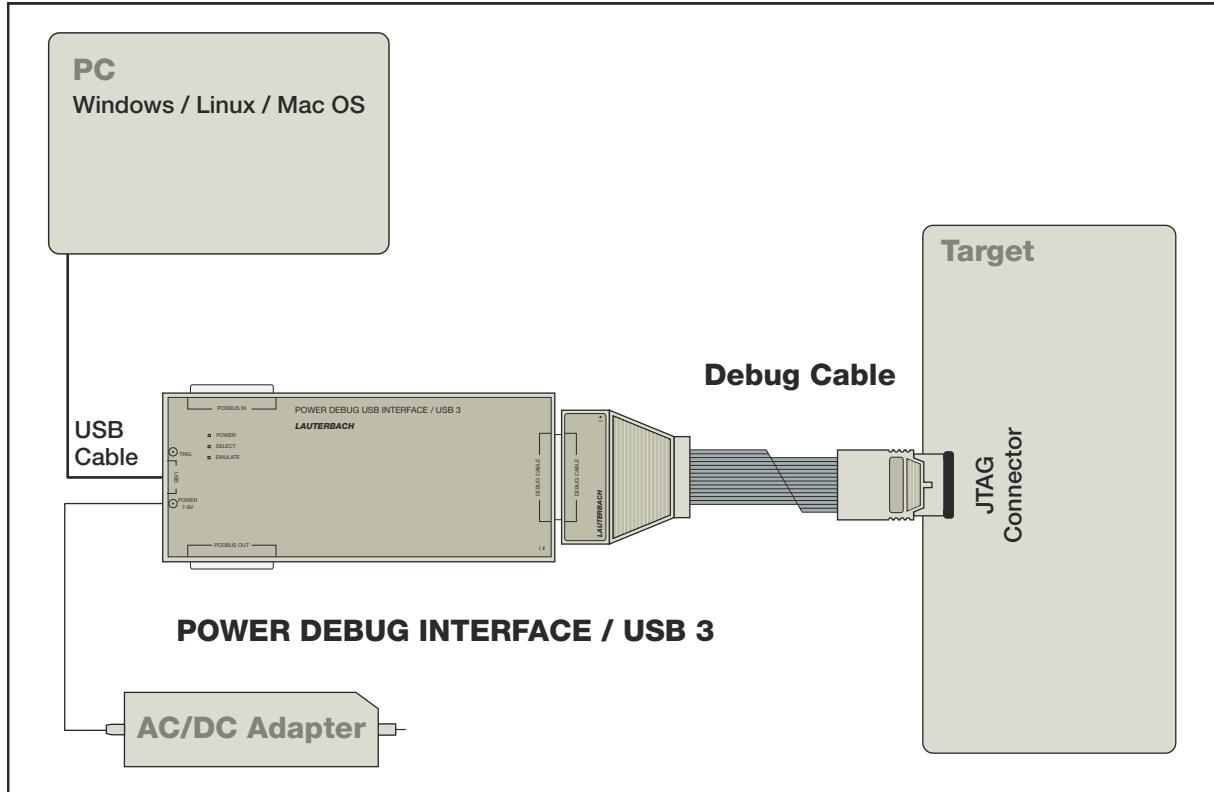
Debug features specific for a processor architecture:

- Number of on-chip breakpoints
- Read/write access to memory while the program execution is running
- Additional features as benchmark counters, triggers etc.

The TRACE32 debugger hardware always consists of:

- Universal debugger hardware
- Debug cable specific to the processor architecture

Debug Only Modules

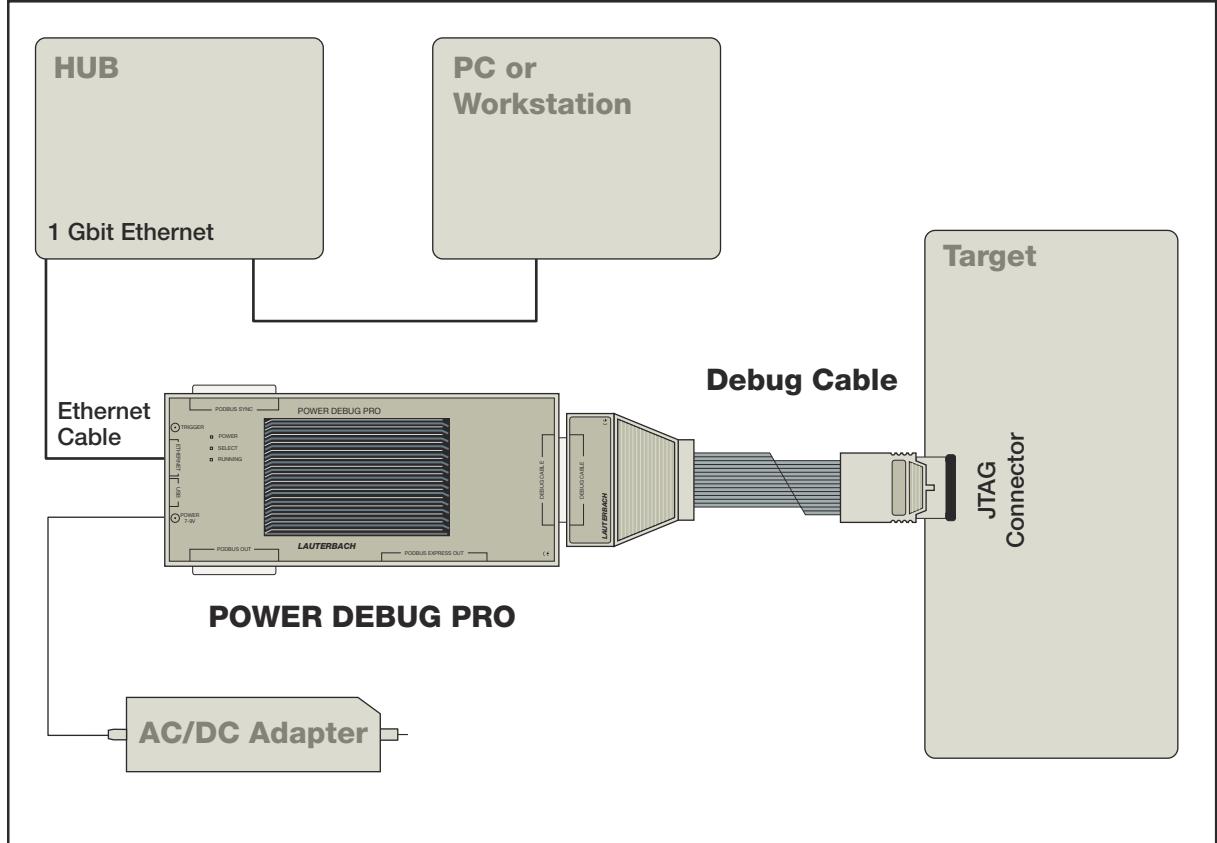


Current module:

- POWER DEBUG INTERFACE / USB 3

Deprecated module:

- POWER DEBUG INTERFACE / USB 2



Current module:

- POWER DEBUG PRO (USB 3 and 1 GBit Ethernet)

Deprecated modules:

- POWER DEBUG II (USB 2 and 1 GBit Ethernet)
- POWER DEBUG / ETHERNET (USB 2 and 100 MBit Ethernet)

On-chip Debug Interface plus On-chip Trace Buffer

A number of single-core processors/multi-core chips offer in addition to the on-chip debug interface an on-chip trace buffer.

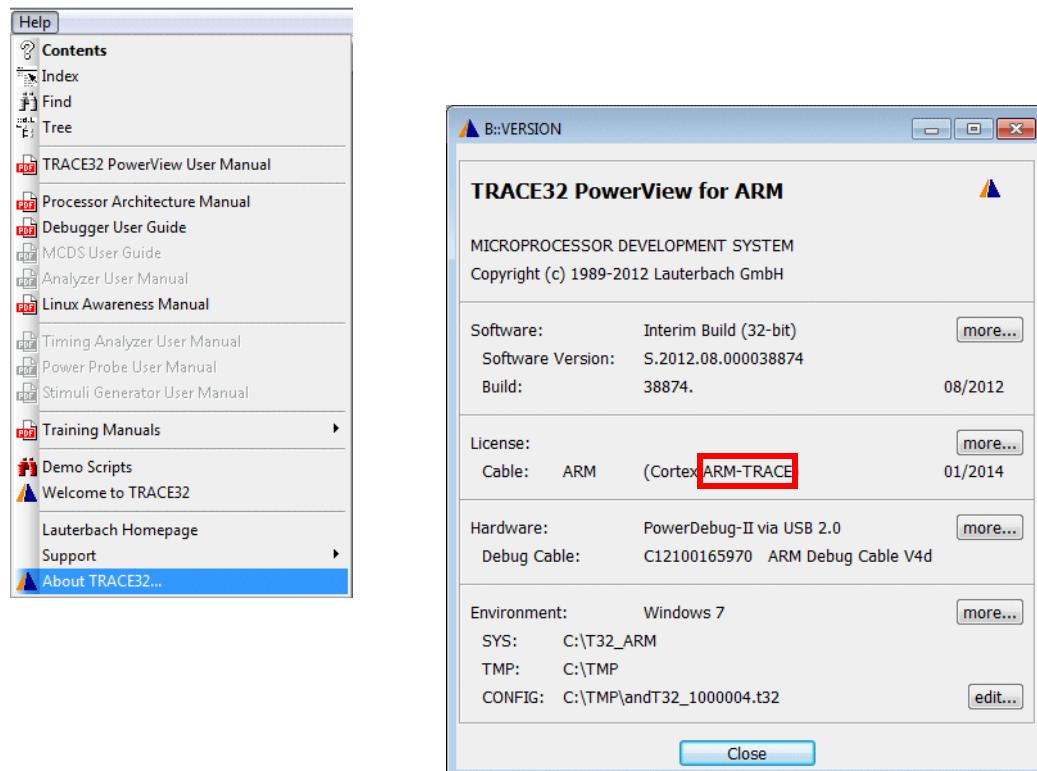
On-chip Trace Features

The on-chip trace buffer can store information:

- On the executed instructions.
- On task/process switches.
- On load/store operations if supported by the on-chip trace generation hardware.

In order to analyze and display the trace information the debug cable needs to provide a **Trace License**. The Trace Licenses use the following name convention:

- <core>-TRACE e.g. ARM-TRACE
- or <core>-MCDS) e.g. TriCore-MCDS



The display and the evaluation of the trace information is described in the following training manuals:

- “**ARM-ETM Training**” (training_arm_etm.pdf).
- “**Cortex-M Trace Training**” (training_cortexm_etm.pdf).
- “**AURIX Trace Training**” (training_aurix_trace.pdf).
- “**Hexagon-ETM Training**” (training_hexagon_etm.pdf).
- “**Nexus Training**” (training_nexus.pdf).

On-chip Debug Interface plus Trace Port

A number of single-core processors/multi-core chips offer in addition to the on-chip debug interface a so-called trace port. The most common trace port is the TPIU for the ARM/Cortex architecture.

Off-chip Trace Features

The trace port exports in real-time trace information:

- On the executed instructions.
- On task/process switches.
- On load/store operations if supported by the on-chip trace generation logic.

The display and the evaluation of the trace information is described in the following training manuals:

- [**“ARM-ETM Training”**](#) (training_arm_etm.pdf)
- [**“Cortex-M Trace Training”**](#) (training_cortexm_etm.pdf)
- [**“AURIX Trace Training”**](#) (training_aurix_trace.pdf)
- [**“Hexagon-ETM Training”**](#) (training_hexagon_etm.pdf)

NEXUS is a standardized interface for on-chip debugging and real-time trace especially for the automotive industry.

NEXUS Features

Debug features provided by all single-core processors/multi-core chips:

- Read/write access to the registers
- Read/write access to all memories
- Start/stop of program execution
- Read/write access to memory while the program execution is running

Debug features specific for single-core processor/multi-core chip:

- Number of on-chip breakpoints
- Benchmark counters, triggers etc.

Trace features provided by all single-core processors/multi-core chips:

- Information on the executed instructions.
- Information on task/process switches.

Trace features specific for the single-core processor/multi-core chip:

- Information on load/store operations if supported by the trace generation logic.

The display and the evaluation of the trace information is described in “[Nexus Training](#)” (training_nexus.pdf).

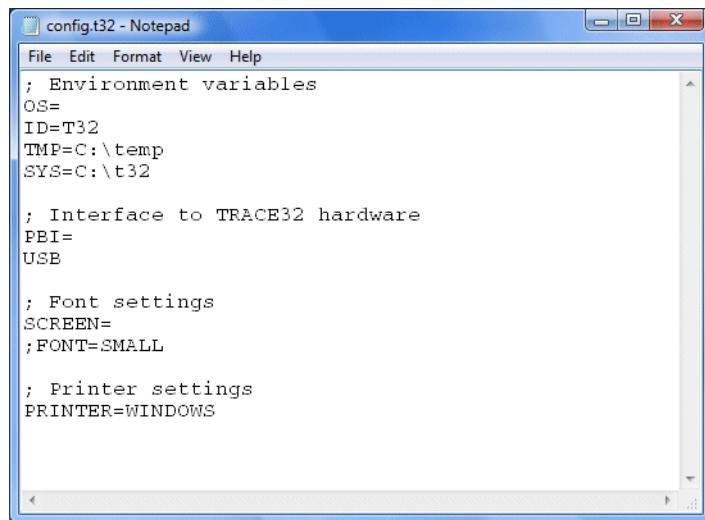
Basic TRACE32 PowerView Parameters

This chapter describes the basic parameters required to start a TRACE32 PowerView instance.

The parameters are defined in the configuration file. By default the configuration file is named **config.t32**. It is located in the TRACE32 system directory (parameter **SYS**).

Configuration File

Open the file **config.t32** from the system directory (default c :\T32\config.t32) with any ASCII editor.



A screenshot of a Windows Notepad window titled "config.t32 - Notepad". The window contains the following configuration file text:

```
config.t32 - Notepad
File Edit Format View Help
; Environment variables
OS=
ID=T32
TMP=C:\temp
SYS=C:\t32

; Interface to TRACE32 hardware
PBI=
USB

; Font settings
SCREEN=
;FONT=SMALL

; Printer settings
PRINTER=WINDOWS
```

The following rules apply to the configuration file:

- Parameters are defined paragraph by paragraph.
- The first line/headline defines the parameter type.
- Each parameter definition ends with an empty line.
- If no parameter is defined, the default parameter will be used.

Standard Parameters

Parameter	Syntax	Description
Host interface	PBI= <host_interface> PBI=ICD <host_interface>	Host interface type of TRACE32 tool hardware (USB or ethernet) Full parameter syntax which is not in use.
Environment variables	OS= ID=<identifier> TMP=<temp_directory> SYS=<system_directory> HELP=<help_directory>	(ID) Prefix for all files which are saved by the TRACE32 PowerView instance into the TMP directory (TMP) Temporary directory used by the TRACE32 PowerView instance (*) (SYS) System directory for all TRACE32 files (HELP) Directory for the TRACE32 help PDFs (**)
Printer definition	PRINTER=WINDOWS	All standard Windows printer can be used from TRACE32 PowerView
License file	LICENSE=<license_directory>	Directory for the TRACE32 license file (not required for new tools)



(*) In order to display source code information TRACE32 PowerView creates a copy of all loaded source files and saves them into the TMP directory.

(**) The TRACE32 online help is PDF-based.

Configuration File for USB

Single debugger hardware module connected via USB:

```
; Host interface
PBI=
USB

; Environment variables
OS=
ID=T32
TMP=C:\temp ; temporary directory for TRACE32
SYS=C:\t32   ; system directory for TRACE32
HELP=C:\t32\pdf ; help directory for TRACE32

; Printer settings
PRINTER=WINDOWS ; all standard windows printer can be
                 ; used from the TRACE32 user interface
```

Multiple debugger hardware modules connected via USB:

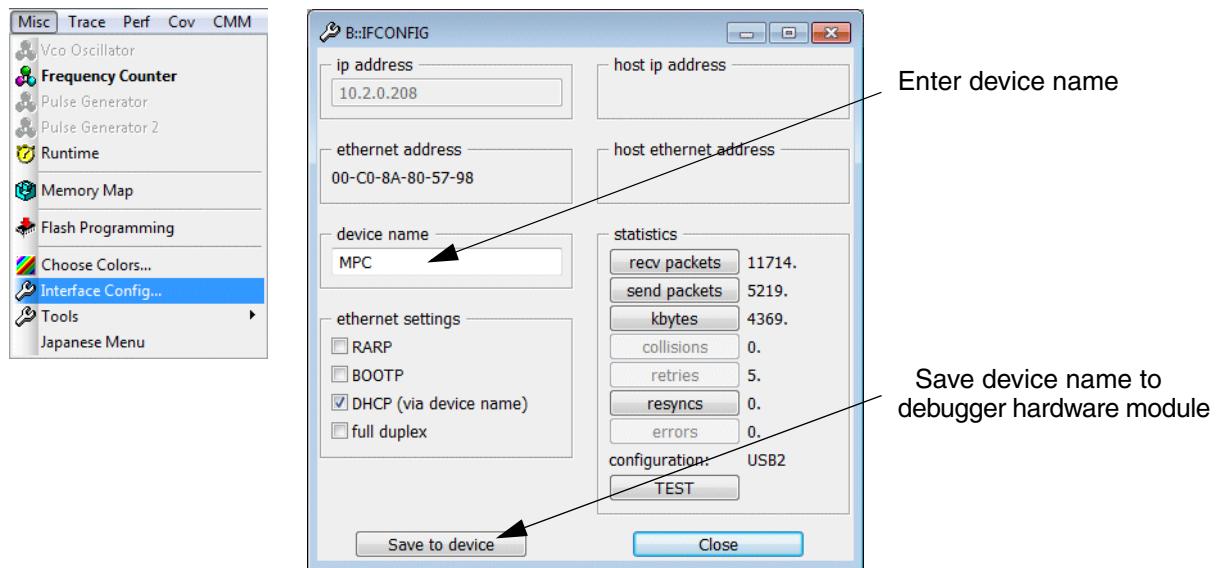
```
; Host interface
PBI=
USB
NODE=training1 ; NODE name of TRACE32

; Environment variables
OS=
ID=T32_training1
TMP=C:\temp ; temporary directory for TRACE32
SYS=C:\t32   ; system directory for TRACE32
HELP=C:\t32\pdf ; help directory for TRACE32

; Printer settings
PRINTER=WINDOWS ; all standard windows printer can be
                 ; used from TRACE32 PowerView
```

Use the IFCONFIG command to assign a device name (NODE=) to a debugger hardware module. The manufacturing default device name is the serial number of the debugger hardware module:

- e.g. E18110012345 for a debugger hardware module with ethernet interface, such as PowerDebug PRO.
- e.g. C18110045678 for a debugger hardware module with USB interface only, such as PowerDebug USB 3.



IFCONFIG

Dialog to assign USB device name

Please be aware that USB device names are case-sensitive

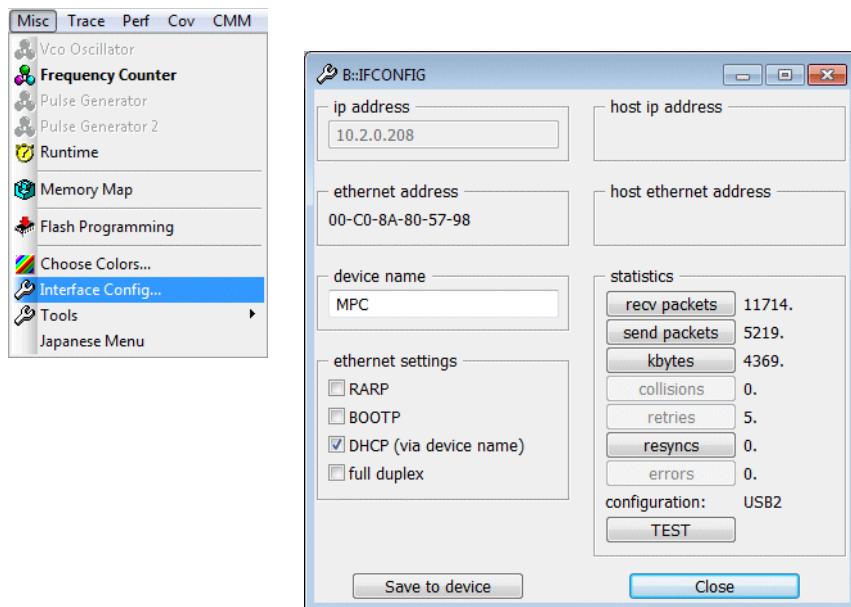
TRACE32 allows to communicate with a POWER DEBUG INTERFACE USB from a remote PC. For an example, see “[Example: Remote Control for POWER DEBUG INTERFACE / USB](#)” in TRACE32 Installation Guide, page 59 (installation.pdf).

```
; Host interface
PBI=
NET
NODE=training1

; Environment variables
OS=
ID=T32                                ; temp directory for TRACE32
SYS=C:\t32                               ; system directory for TRACE32
HELP=C:\t32\pdf                           ; help directory for TRACE32

; Printer settings
PRINTER=WINDOWS                         ; all standard windows printer can be
                                         ; used from the TRACE32 user interface
```

Ethernet Configuration and Operation Profile



IFCONFIG

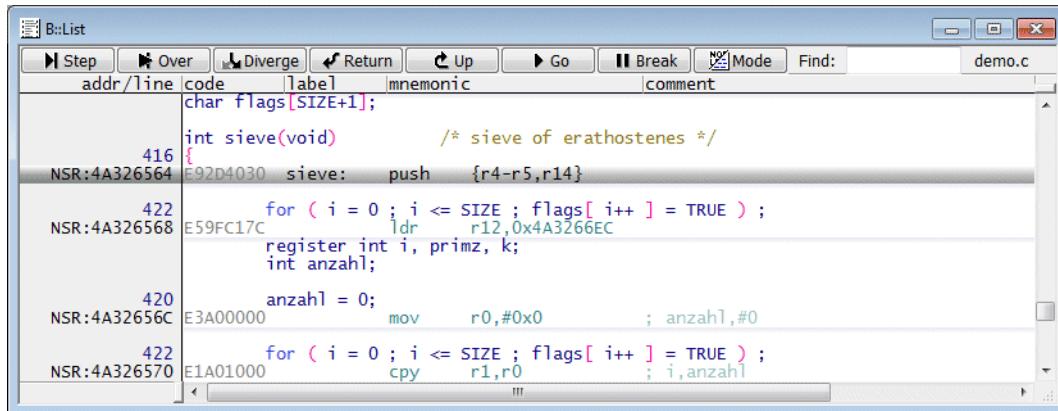
Dialog to display and change information for the Ethernet interface

Additional Parameters

Changing the font size can be helpful for a more comfortable display of TRACE32 windows.

```
; Screen settings
SCREEN=
FONT=SMALL ; Use small fonts
```

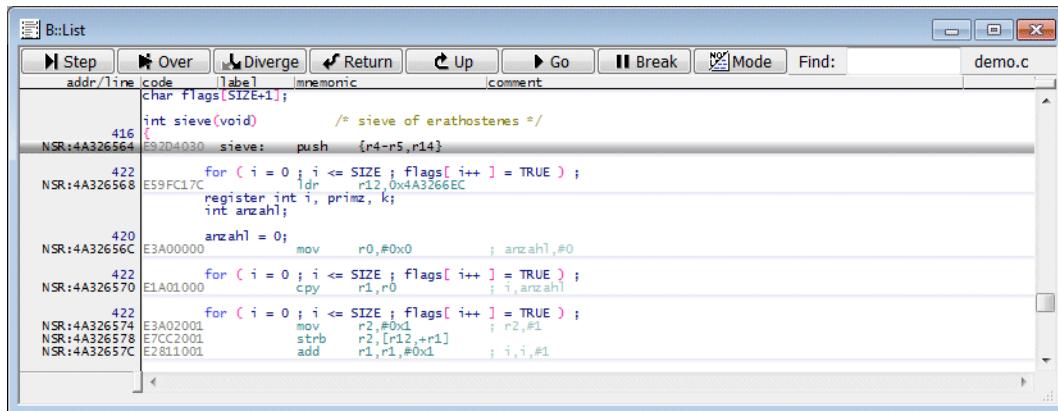
Display with normal font:



The screenshot shows the TRACE32 interface with the B::List window active. The window title is "B::List". The toolbar includes Step, Over, Diverge, Return, Up, Go, Break, Mode, and Find buttons. The status bar shows "demo.c". The list view displays assembly code for a sieve function. The font size is standard, making the code readable but potentially too large for some displays.

addr/line	code	label	mnemonic	comment
	char flags[SIZE+1];			
416 NSR:4A326564	E92D4030	sieve:	push {r4-r5,r14}	
422 NSR:4A326568	E59FC17C		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;	ldr r12,0x4A3266EC
			register int i, primz, k;	
			int anzahl;	
420 NSR:4A32656C	E3A00000		anzahl = 0;	mov r0,#0x0 ; anzahl,#0
422 NSR:4A326570	E1A01000		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;	cpy r1,r0 ; i,anzahl

Display with small font:

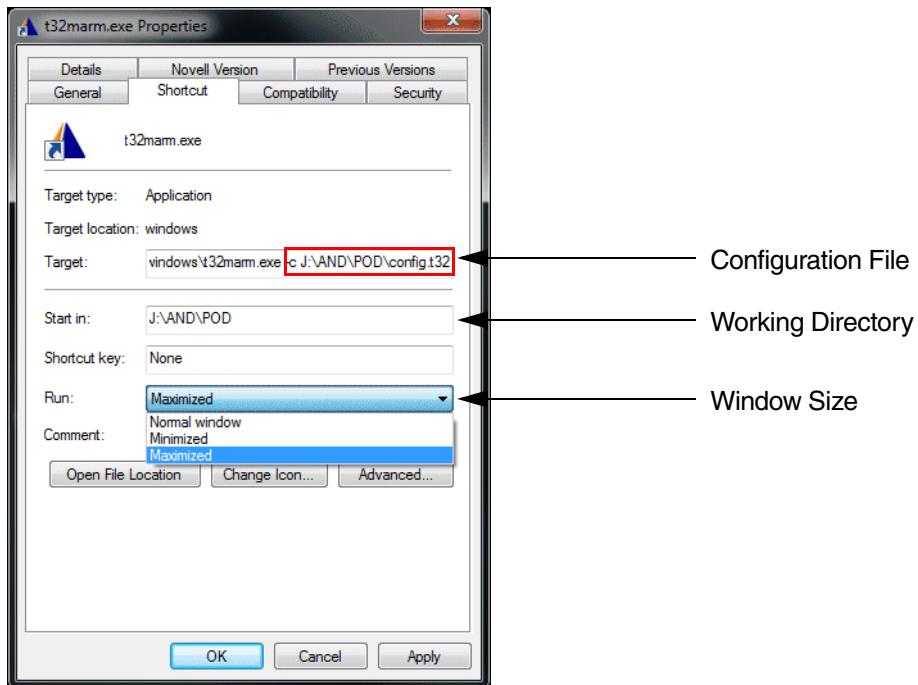


The screenshot shows the same TRACE32 interface and B::List window as the previous one, but with a smaller font size applied to the assembly code. The code is now much smaller and fits better within the window's vertical space, making it easier to view multiple lines of assembly at once.

addr/line	code	label	mnemonic	comment
	char flags[SIZE+1];			
416 NSR:4A326564	E92D4030	sieve:	push {r4-r5,r14}	
422 NSR:4A326568	E59FC17C		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;	ldr r12,0x4A3266EC
			register int i, primz, k;	
			int anzahl;	
420 NSR:4A32656C	E3A00000		anzahl = 0;	mov r0,#0x0 ; anzahl,#0
422 NSR:4A326570	E1A01000		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;	cpy r1,r0 ; i,anzahl
422 NSR:4A326574	E3A02001		for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;	mov r2,#0x1 ; r2,#1
NSR:4A326578	E7CC2001			strb r2,[r12,+r1]
NSR:4A32657C	E2811001			add r1,r1,#0x1 ; i,i,#1

Application Properties (Windows only)

The properties window allows you to configure some basic settings for the TRACE32 software.



Definition of the Configuration File

By default the configuration file **config.t32** in the TRACE32 system directory (parameter **SYS**) is used. The option **-c** allows you to define your own location and name for the configuration file.

```
C:\T32_ARM\bin\windows\t32marm.exe -c j:\and\config.t32
```

Definition of a Working Directory

After its start TRACE32 PowerView is using the specified working directory. It is recommended not to work in the system directory.

PWD

TRACE32 command to display the current working directory

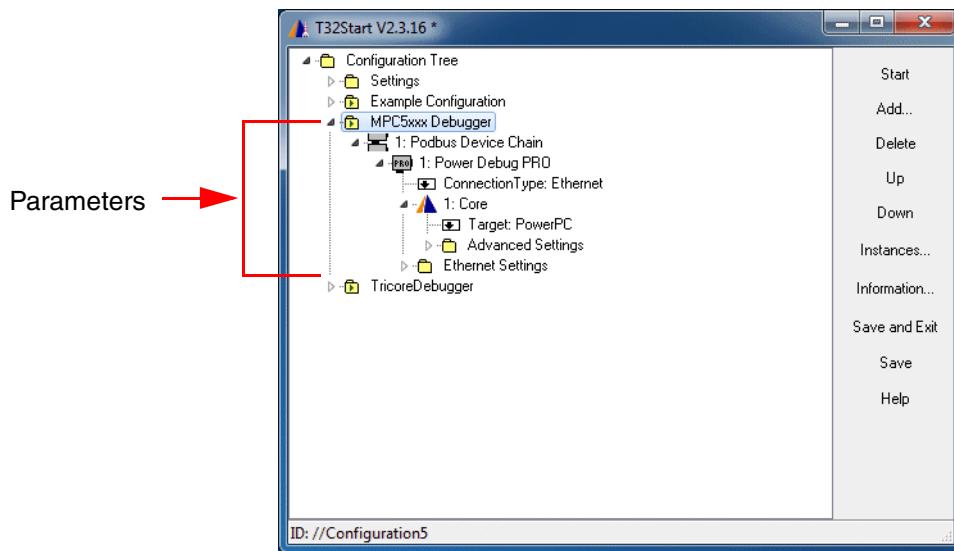
Definition of the Window Size for TRACE32 PowerView

You can choose between Normal window, Minimized and Maximized.

Configuration via T32Start (Windows only)

The basic parameters can also be set up in an intuitive way via **T32Start**.

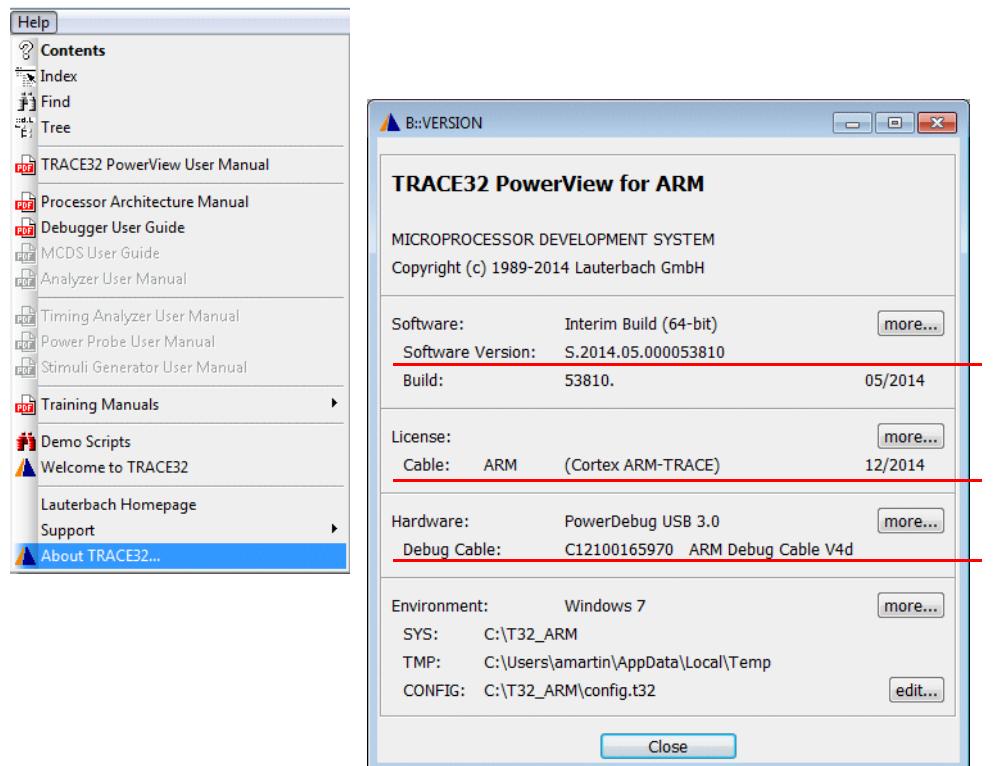
A detailed online help for **t32start.exe** is available via the **Help** button or in "**T32Start**" (app_t32start.pdf).



About TRACE32

If you want to contact your local Lauterbach support, it might be helpful to provide some basis information about your TRACE32 tool.

Version Information



The VERSION window informs you about:

1. The version of the TRACE32 software.
2. The debug licenses programmed into the debug cable and the expiration date of your software warranty respectively the expiration date of your software maintenance.
3. The serial number of the debug cable.

VERSION.view

Display the VERSION window.

VERSION.HARDWARE

Display more details about the TRACE32 hardware modules.

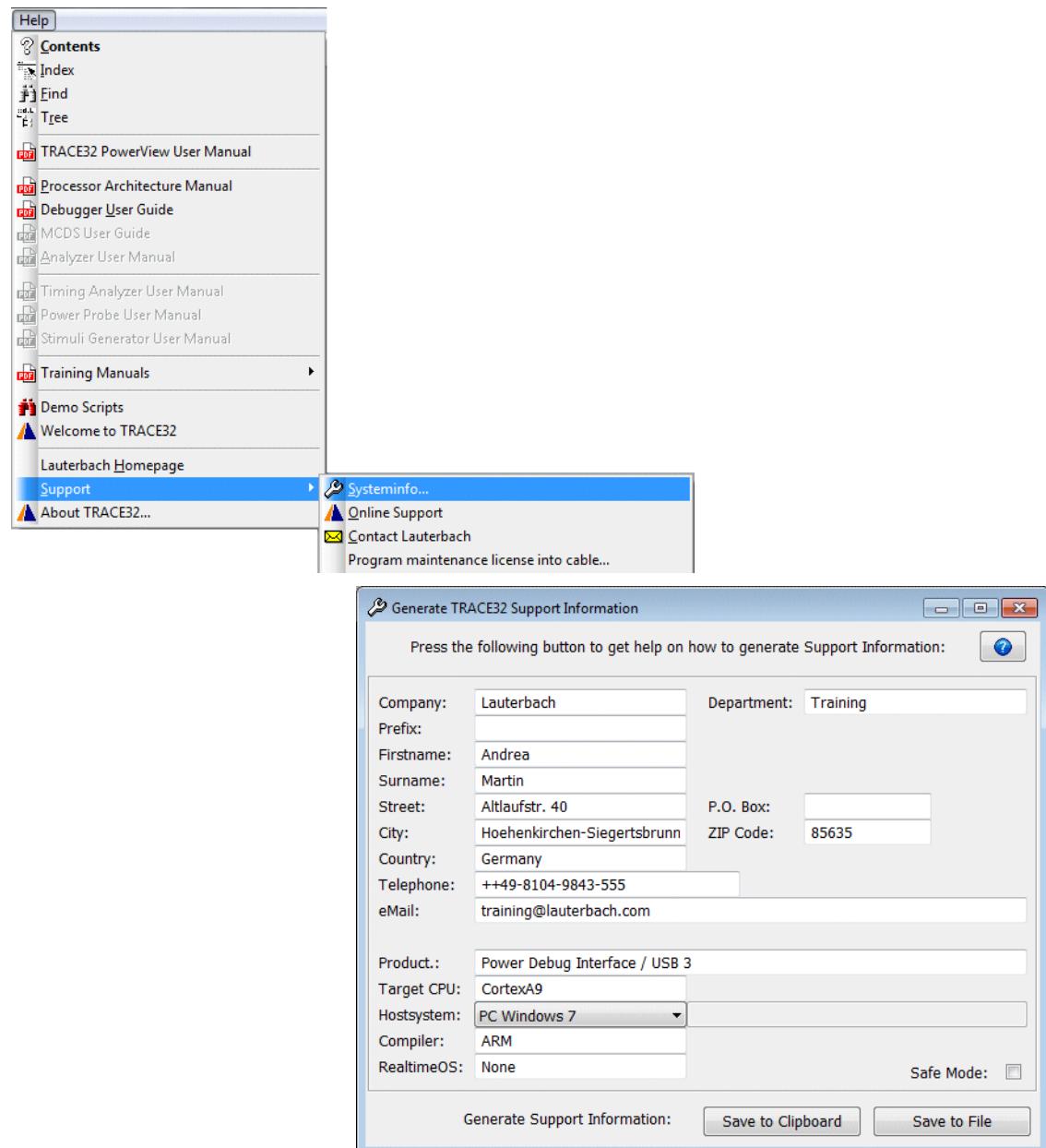
VERSION.SOFTWARE

Display more details about the TRACE32 software.

Prepare Full Information for a Support Email

Be sure to include detailed system information about your TRACE32 configuration.

1. To generate a system information report, choose **Help > Support > Systeminfo**.

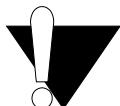
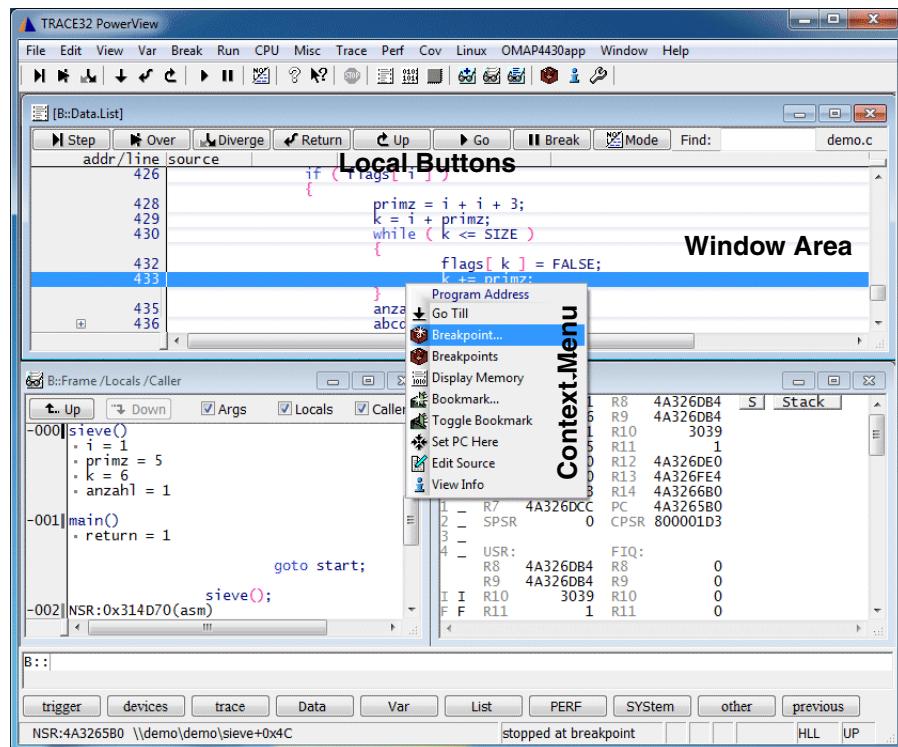


2. Preferred: click **Save to File**, and send the system information as an attachment to your e-mail.
3. Click **Save to Clipboard**, and then paste the system information into your e-mail.

Establish your Debug Session

Before you can start debugging, the debug environment has to be set up. An overview on the most common setups is given in “[Establish Your Debug Session](#)” (tutor_setup.pdf).

TRACE32 PowerView Components



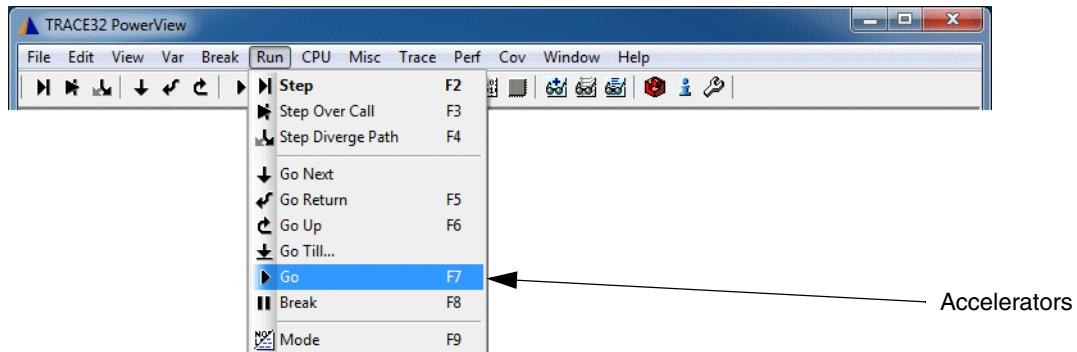
The structure of the menu bar and the tool bar are defined by the file **t32.men** which is located in the TRACE32 system directory.

TRACE32 allows you to modify the menu bar and the tool bar so they will better fit your requirements. Refer to "[“Training Menu”](#) (training_menu.pdf) for details.

Main Menu Bar and Accelerators

The main menu bar provides all important TRACE32 functions sorted by groups.

For often used commands accelerators are defined.



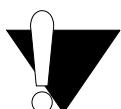
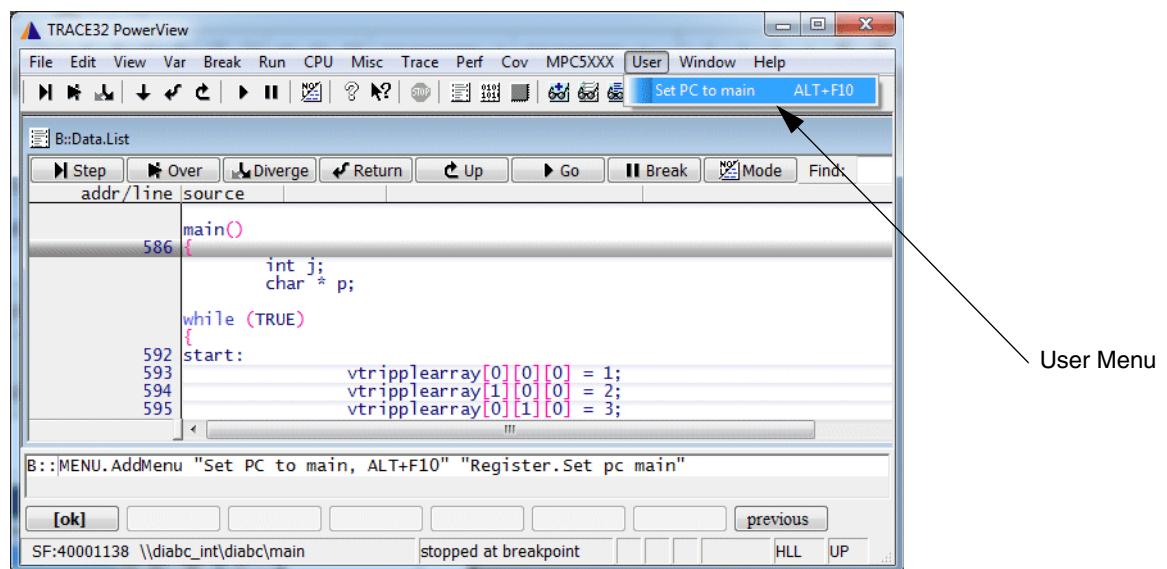
A user specific menu can be defined very easily:

MENU.AddMenu <name> <command> Add a user menu

MENU.RESET Reset menu to default

```
; user menu
MENU.AddMenu "Set PC to main" "Register.Set pc main"

; user menu with accelerator
MENU.AddMenu "Set PC to main, ALT+F10" "Register.Set pc main"
```



For more complex changes to the main menu bar refer to "[Training Menu](#)" (training_menu.pdf).

Videos about the menu programming can be found here:
http://www.lauterbach.com/tut_customization.html

Main Tool Bar

The main tool bar provides fast access to often used commands.

The user can add his own buttons very easily:

MENU.AddTool <tooltip_text> <tool_image> <command>

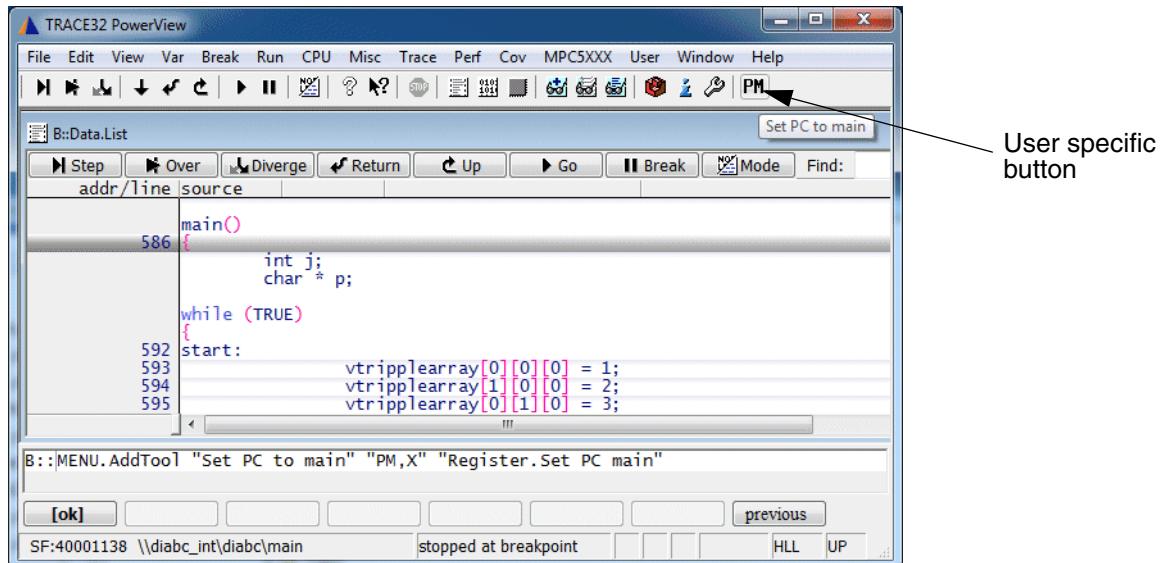
Add a button to the toolbar

MENU.RESet

Reset menu to default

```
; <tooltip text> here:      Set PC to main  
; <tool image> here:      button with capital letters PM in black  
; <command> here:        Register.Set PC main
```

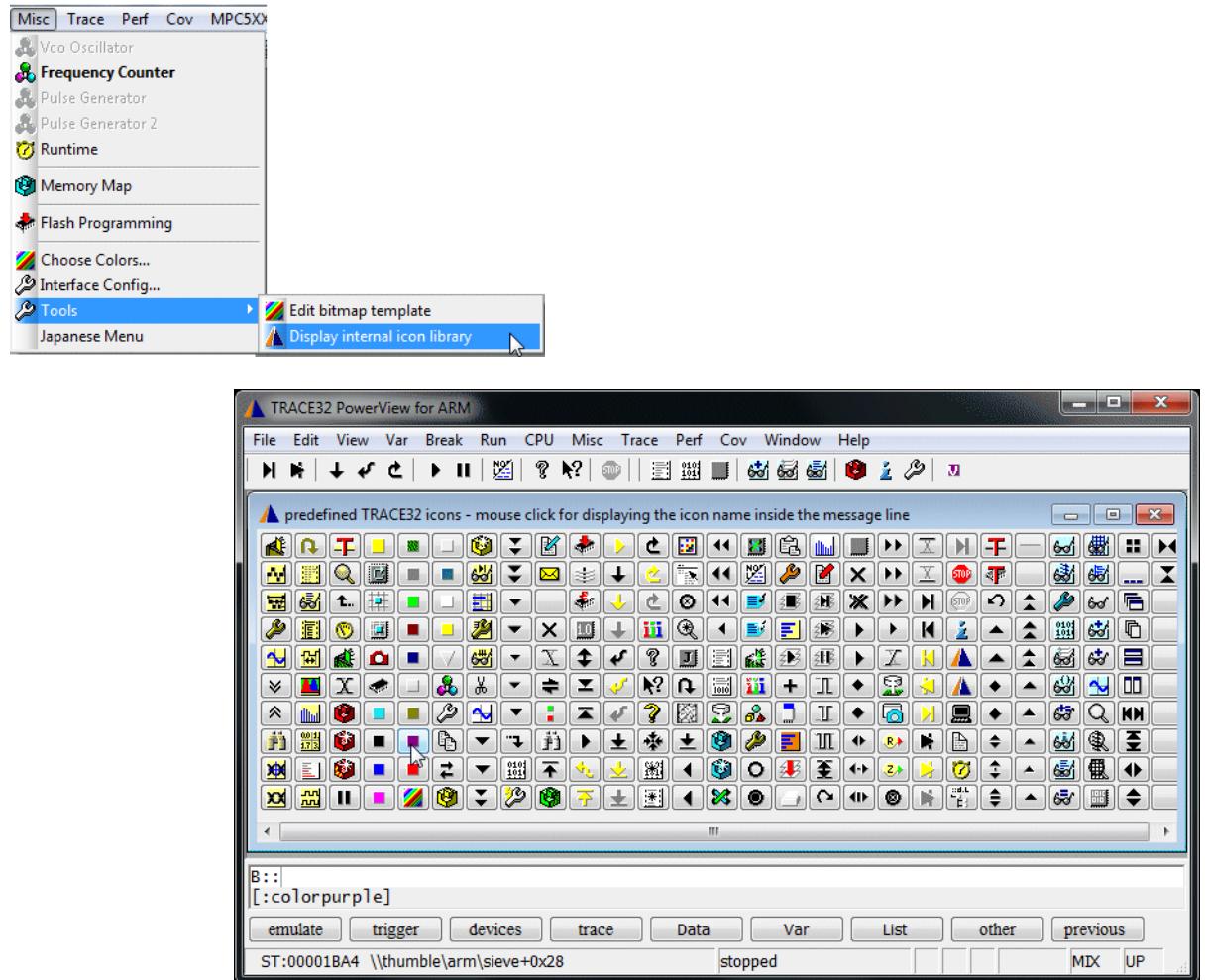
```
MENU.AddTool "Set PC to main" "PM,X" "Register.Set PC main"
```



Information on the <tool image> can be found in **Help -> Contents**

TRACE32 Documents -> IDE User Interface -> IDE Reference Guide -> MENU -> Programming Commands -> TOOLITEM.

All predefined TRACE32 icons can be inspected as follows:



Or by following TRACE32 command:

```
ChDir.DO ~~/demo/menu/internal_icons.cmm
```

The predefined icons can easily be used to create new icons.

```
; overprint the icon colorpurple with the character v in White color  
Menu.AddTool "Set PC to main" "v,W,colorpurple" "Register.Set PC main"
```

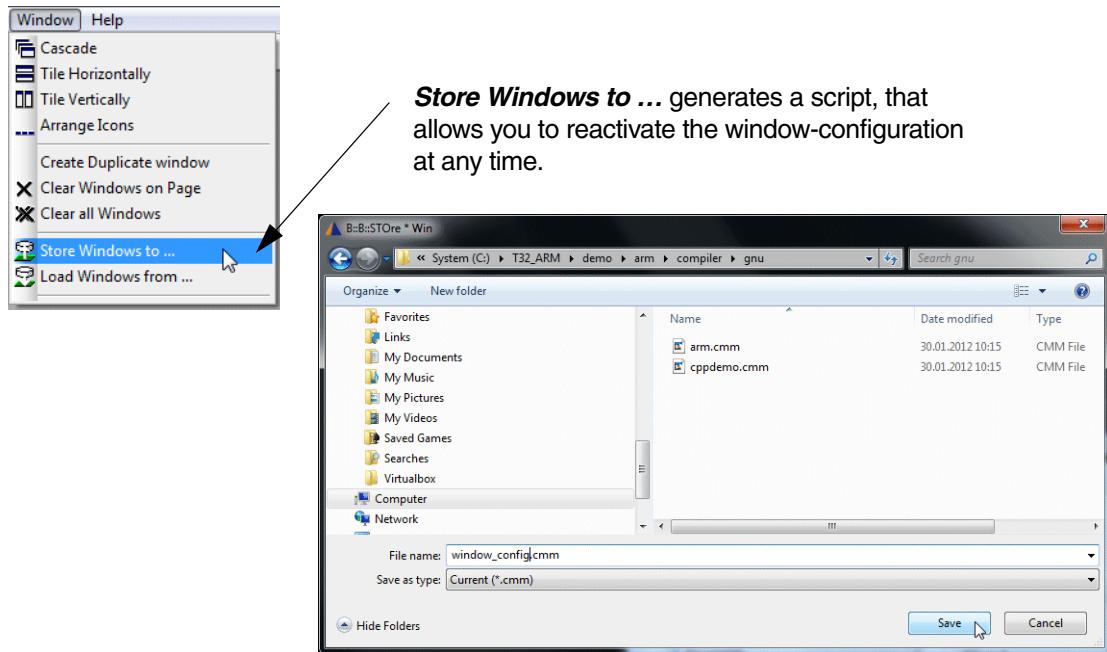


For more complex changes to the main tool bar refer to "["Training Menu"](#)" ([training_menu.pdf](#)).

Videos about the menu programming can be found here:
http://www.lauterbach.com/tut_customization.html

Save Page Layout

No information about the window layout is saved when you exit TRACE32 PowerView. To save the window layout use the **Store Windows to ...** command in the **Window** menu.



Script example:

```
// andT32_1000003 Sat Jul 21 16:59:55 2012

B:::

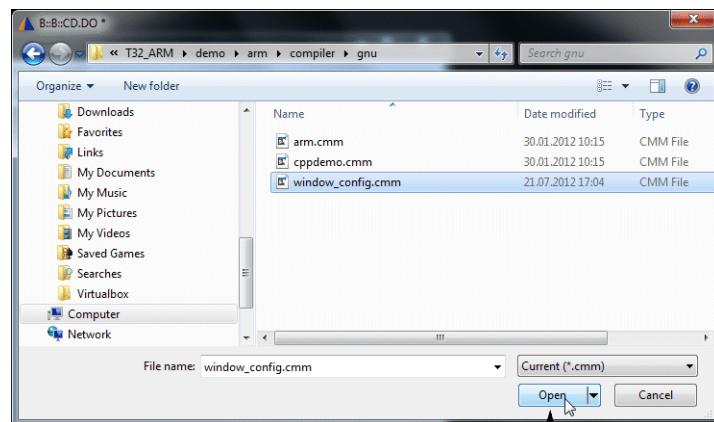
TOOLBAR ON
STATUSBAR ON
FRAMEPOS 68.0 5.2857 107. 45.
WINPAGE.RESET

WINCLEAR
WINPOS 0.0 0.0 80. 16. 15. 1. W000
WINTABS 10. 10. 25. 62.
List

WINPOS 0.0 21.643 80. 5. 25. 1. W001
WINTABS 13. 0. 0. 0. 0. 0. 0.
Break.List

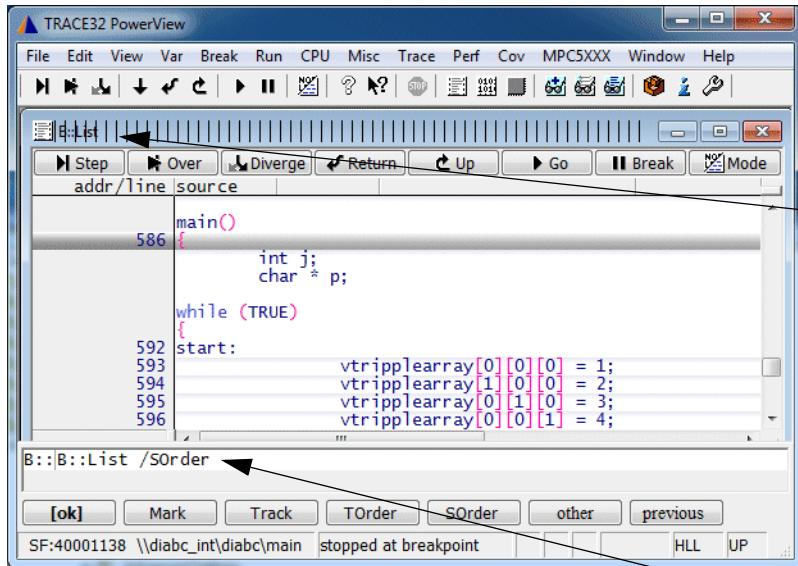
WINPAGE.SELECT P000

ENDDO
```



Run the script to reactivate the stored
window-configuration

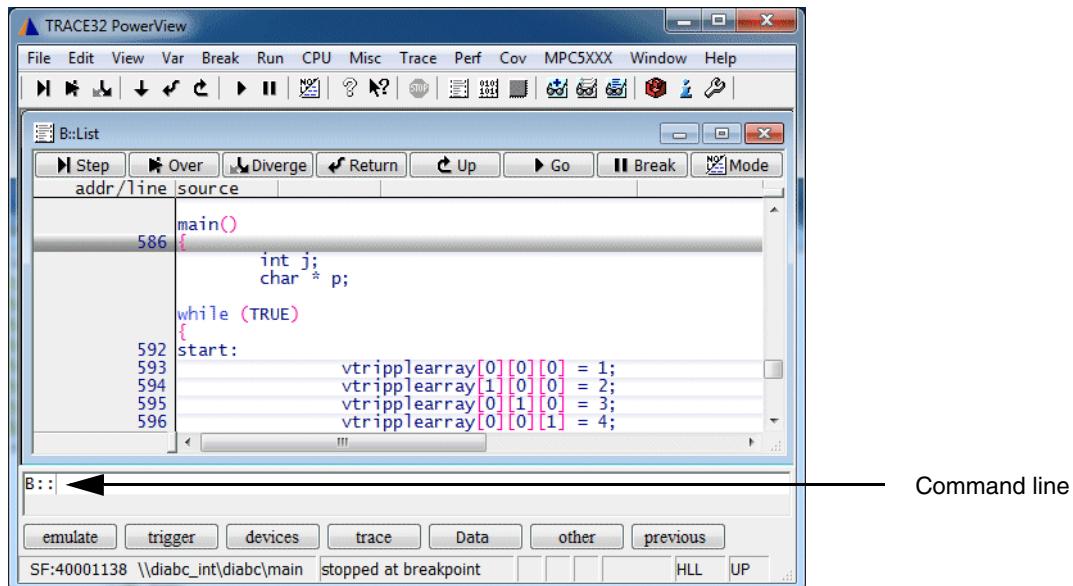
Modify Window



The window header displays the command which was executed to open the window

By clicking with the right mouse button to the window header, the command which was executed to open the window is re-displayed in the command line and can be modified there

Command Line

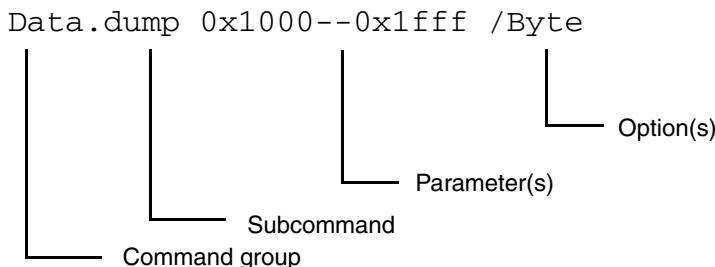


Command line

Command Structure

Device prompt: the default device prompt is **B::**. It stands for BDM which was the first on-chip debug interface supported by Lauterbach.

A TRACE32 command has the following structure:



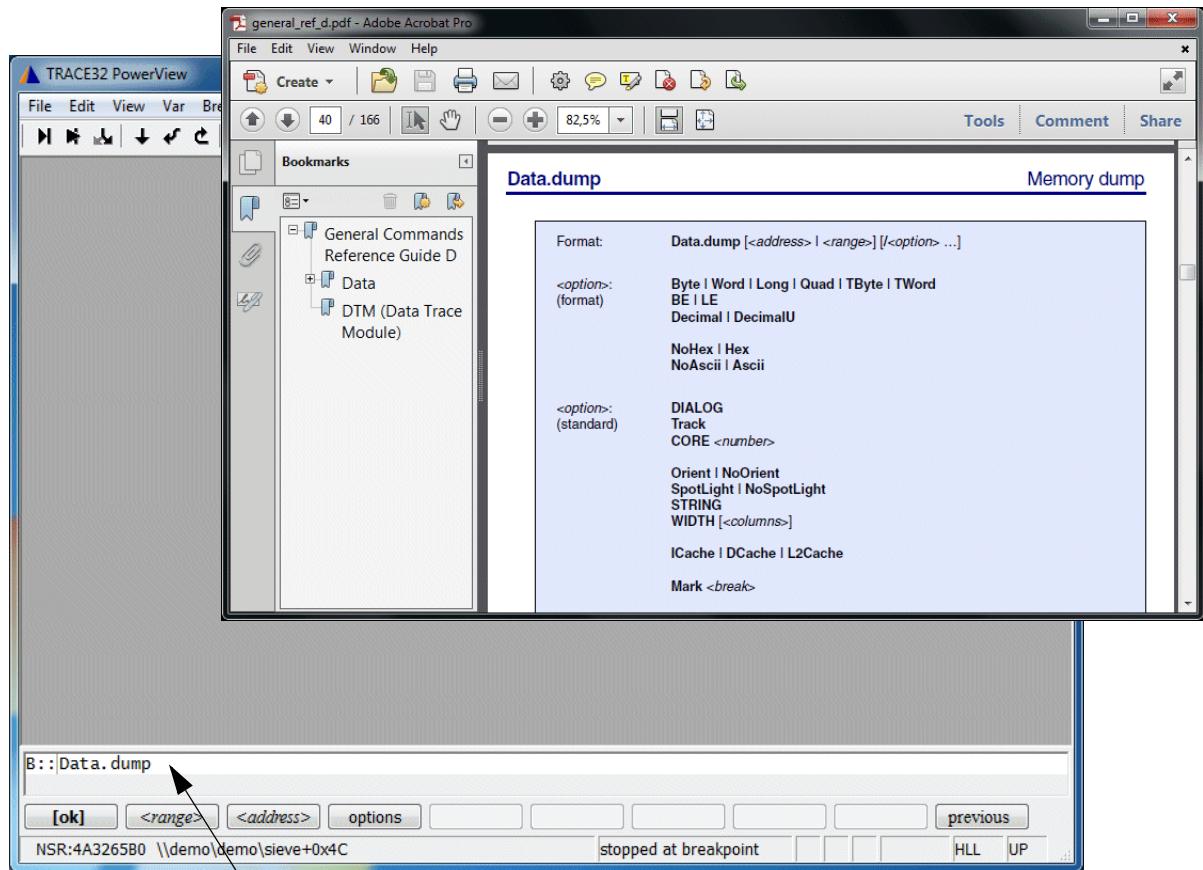
Command Examples

Data	Command group to display, modify ... memory
Data.dump	Displays a hex dump
Data.Set	Modify memory
Data.LOAD.auto	Loads code to the target memory

Break	Command group to set, list, delete ... breakpoints
Break.Set	Sets a breakpoint
Break.List	Lists all set breakpoint
Break.Delete	Deletes a breakpoint

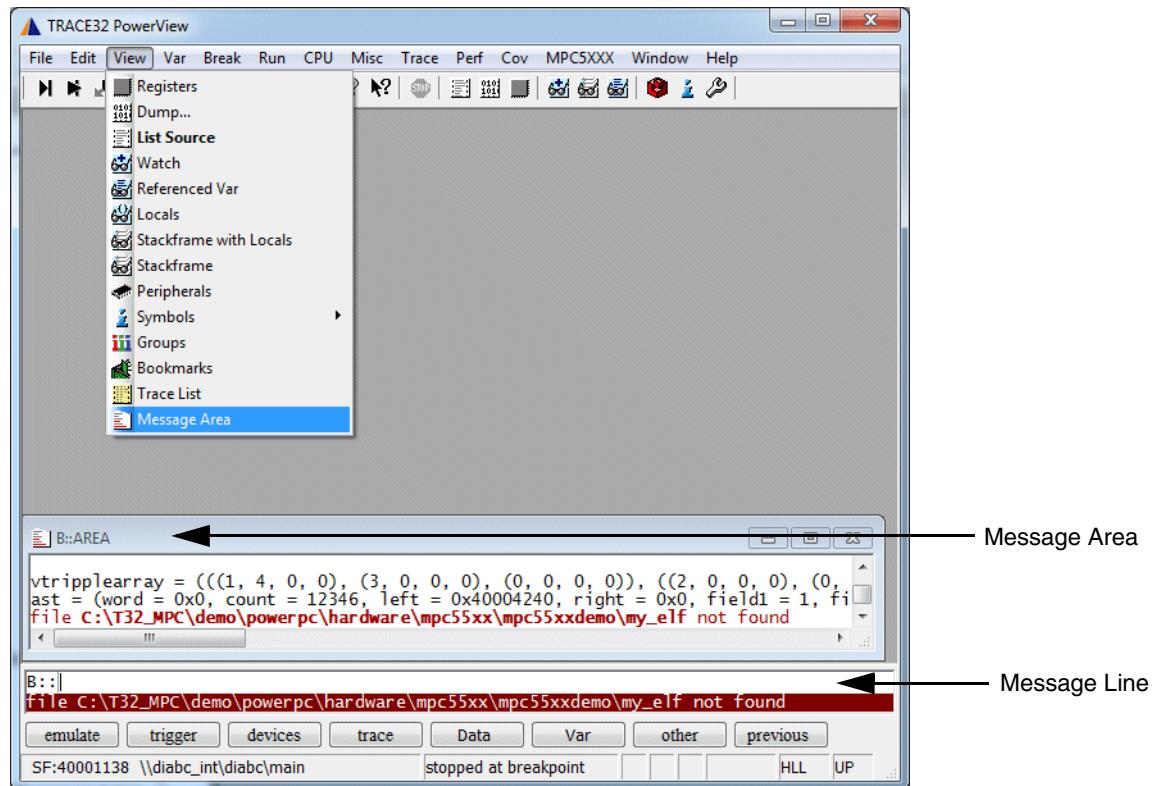
Each command can be abbreviated. The significant letters are always written in upper case letters.

Examples for the parameter syntax and the use of options will be presented throughout this training.



Enter the command to the command line.
Add one blank.
Push F1 to get the online help for the specified command.

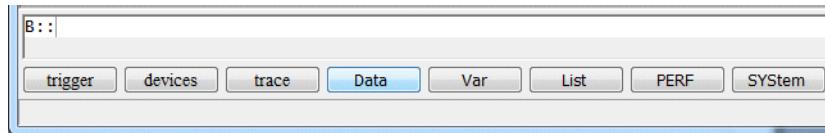
Message Line



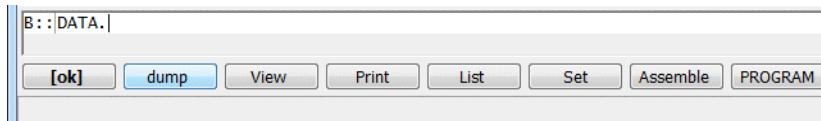
- **Message line** for system and error messages
- **Message Area window** for the display of the last system and error messages

The softkey line allows to enter a specific command step by step. Here an example:

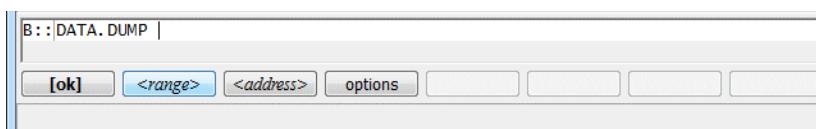
Select the command group, here **Data**.



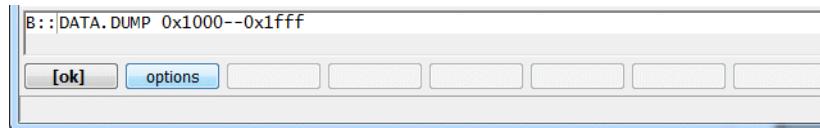
Select the subcommand, here **dump**.



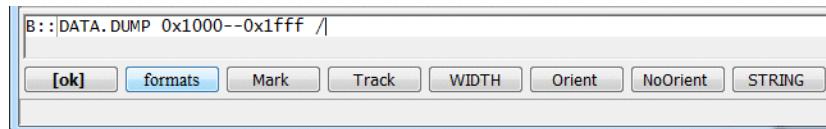
Angle brackets request an entry from the user,
here e.g. the entry of a <range> or an <address>.



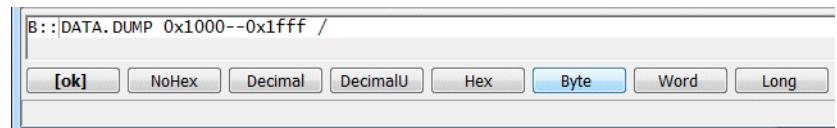
The display of the hex. dump can be adjusted to your needs by an option.



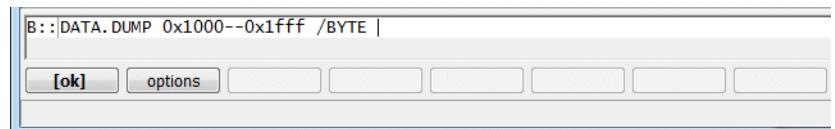
Select the option **formats** to get a list of all format options.



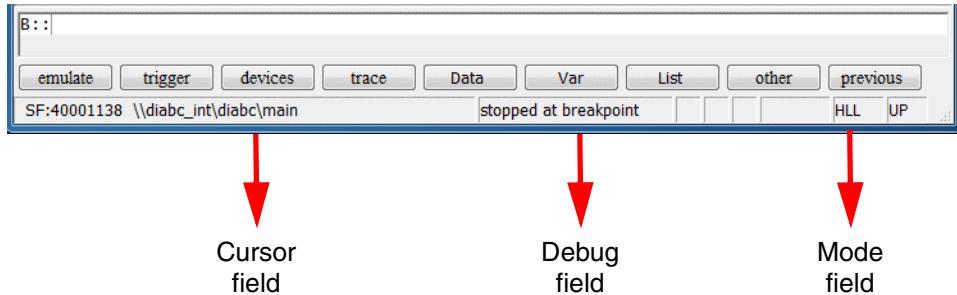
Select a format option, here **Byte**.



The command is complete now.



State Line



The **Cursor** field of the state line provides:

- Boot information (Booting ..., Initializing ... etc.).
- Information on the item selected by one of the TRACE32 PowerView cursors.

The **Debug** field of the state line provides:

- Information on the debug communication (system down, system ready etc.)
- Information on the state of the debugger (running, stopped, stopped at breakpoint etc.)

The **Mode** field of the state line indicates the debug mode. The debug mode defines how source code information is displayed.

- Asm = assembler code
- HLL = programming language code/high level language
- Mix = a mixture of both

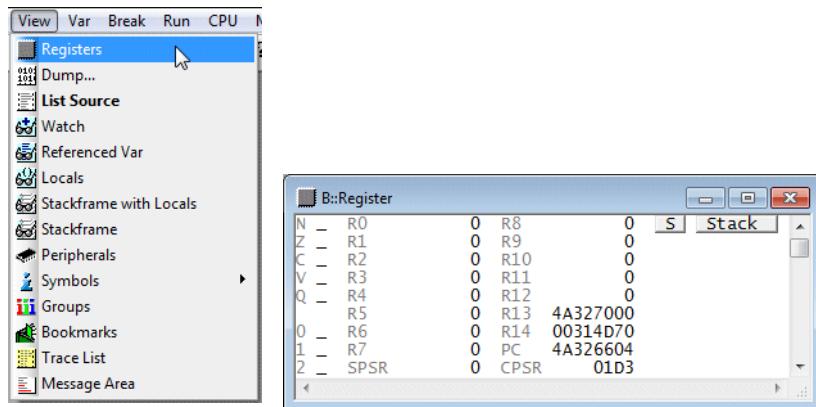
It also defines how single stepping is performed (assembler line-wise or programming language line-wise).



The debug mode can be changed by using the **Mode** pull-down.

Core Registers

Display the Core Registers

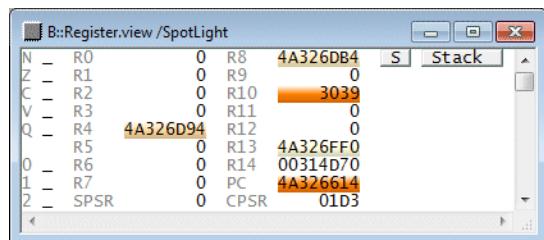


Register.view

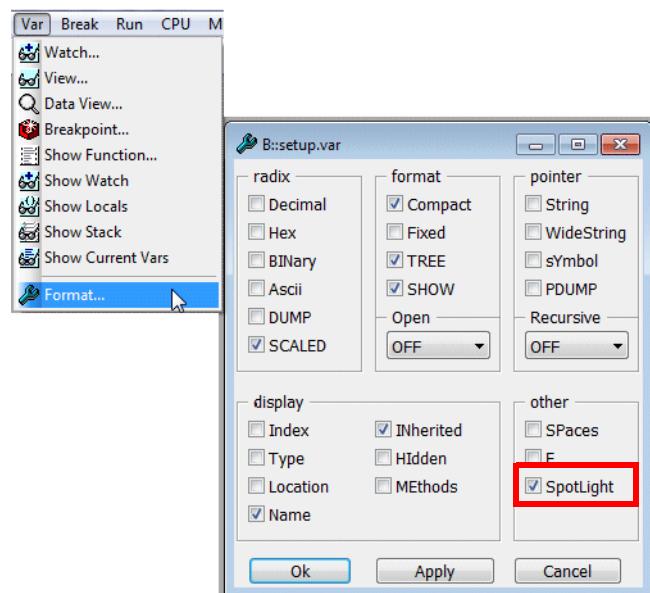
Colored Display of Changed Registers

The option /SpotLight advises TRACE32 PowerView to mark changes.

```
Register.view /SpotLight ; The registers changed by the last  
; step are marked in dark red.  
  
; The registers changed by the  
; step before the last step are  
; marked a little bit lighter.  
  
; This works up to a level of 4.
```



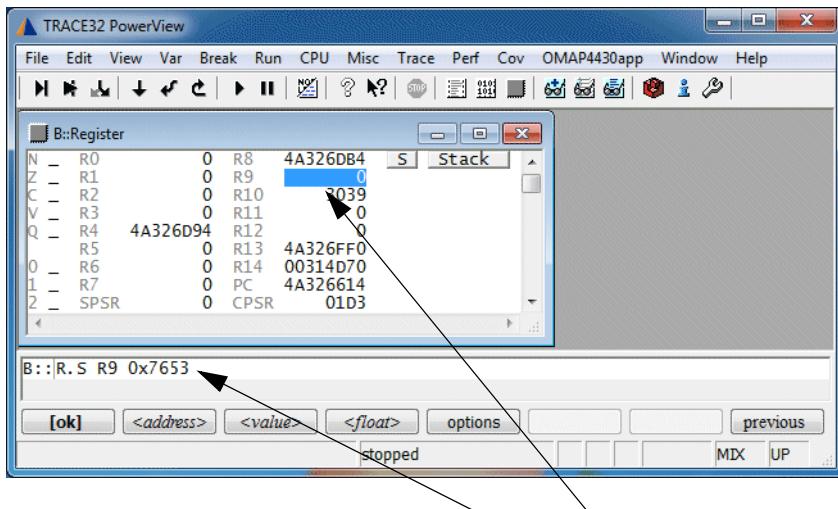
Establish /SpotLight as default setting



SETUP.Var %SpotLight

Establish the option SpotLight as default setting for
- all Variable windows
- Register window
- PERipheral window
- the HLL Stack Frame
- Data.dump window

Modify the Contents of a Core Register



By double clicking to the register contents
a **Register.Set** command is automatically displayed
in the command line.

Enter the new value and press return to modify the
register contents.

Register.Set <register> <value>

Modify register

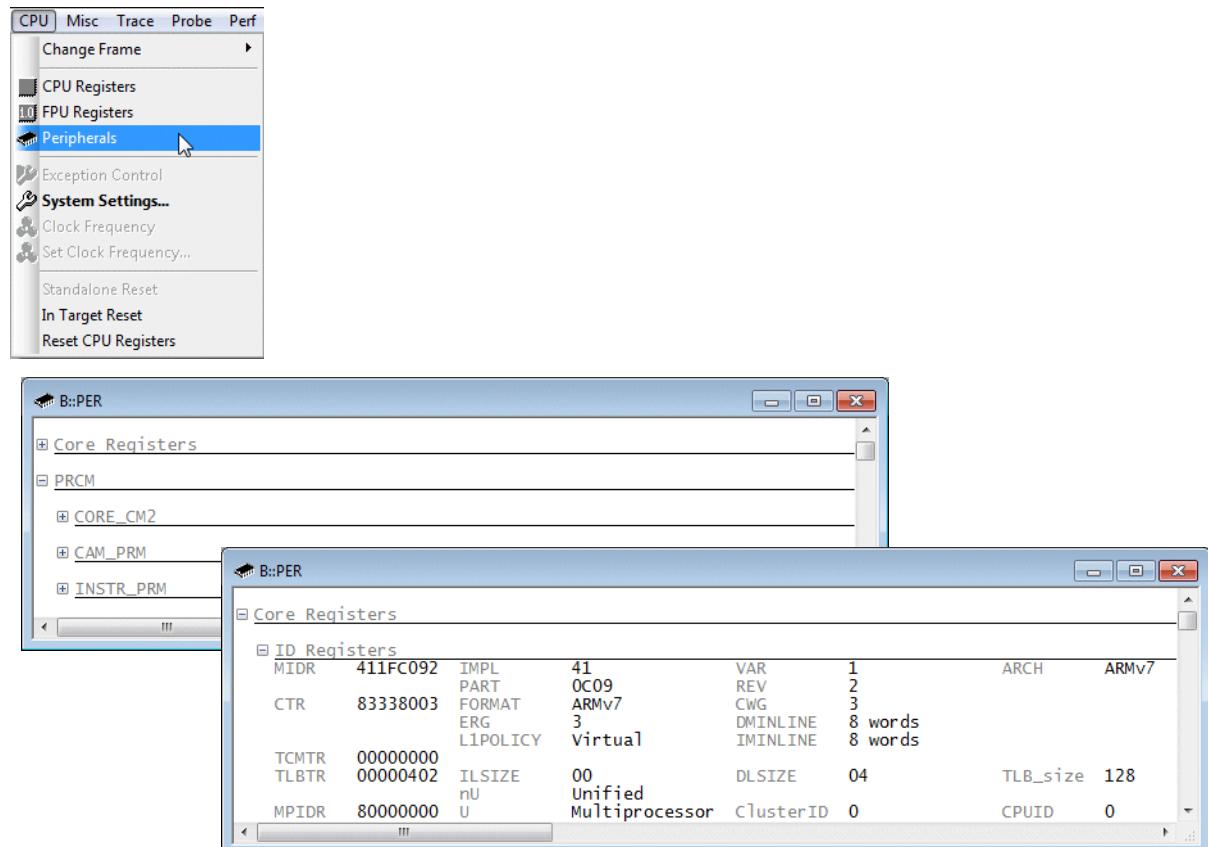
Special Function Register

Display the Special Function Registers

TRACE32 supports a free configurable window to display/manipulate configuration registers and the on-chip peripheral registers at a logical level. Predefined peripheral files are available for most standard processors/chips.

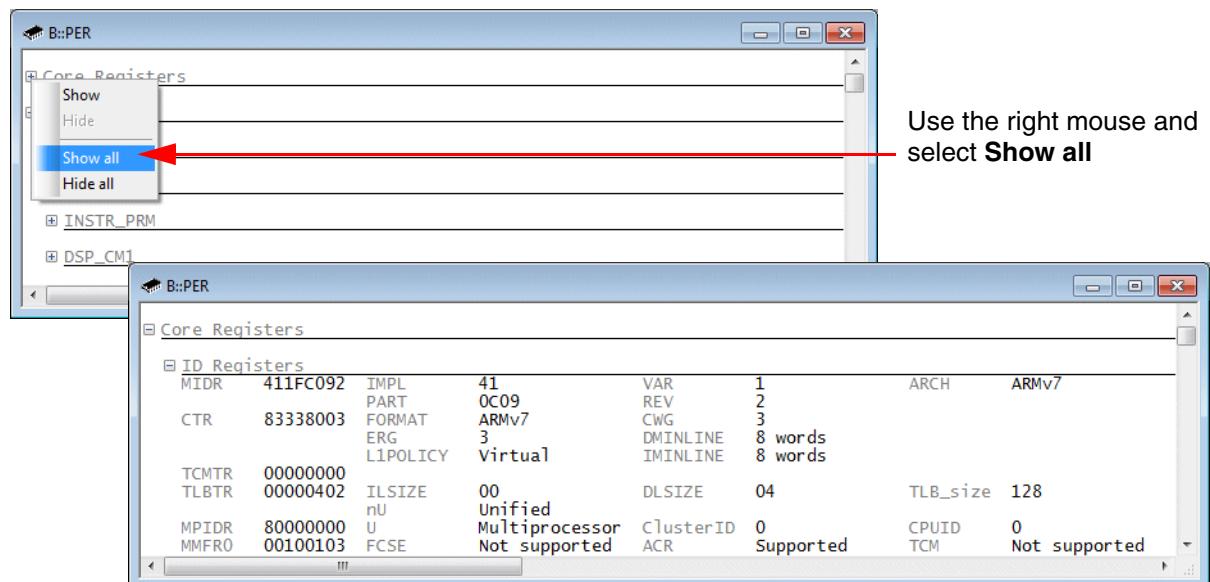
Tree Display

The individual configuration registers/on-chip peripherals are organized by TRACE32 PowerView in a tree structure. On demand, details about a selected register can be displayed.



Please be aware, that TRACE32 permanently updates all windows. The default update rate is 10 times per second.

Sometimes it might be useful to expand the tree structure from the start.



Commands:

PER.view <filename> [<tree_item>] Display the configuration registers/on-chip peripherals

```
; Display all functional units in expanded mode
; , advises TRACE32 PowerView to use the default peripheral file
; * stands for all <tree-items>
PER.View , "*"
```

```
; Display the functional unit "ID Registers" within "Core Registers"
; in expanded mode
PER.view , "Core Registers, ID Registers"
```

B::PER.view , "Core Registers, ID Registers"							
Core Registers							
ID Registers							
MIDR	411FC093	IMPL	41	VAR	1	ARCH	ARMv7
		PART	0C09	REV	3		
CTR	83338003	FORMAT	ARMv7	CWG	3		
		ERG	3	DMINLINE	8 words		
TCMTR	00000000	L1POLICY	Virtual	IMINLINE	8 words		
TLBTR	00000402	ILSIZE	00	DLSIZE	04	TLB_size	128
		nU	Unified				
MPIDR	80000000	U	Multiprocessor	ClusterID	0	CPUID	0
MMFR0	00100103	FCSE	Not supported	ACR	Supported	TCM	Not supported
		OSS	Not supported	CC_CPUA	Supported	PMSA	Not supported

```
; Display the functional unit "DMA_Channel_0" within "sDMA_Module,sDMA"
; in expanded mode
PER.view , "sDMA_Module,sDMA,DMA_Channel_0"
```

B::PER.view , "sDMA_Module,sDMA,DMA_Channel_0"							
sDMA_Module							
sDMA							
DMA4_CC DN1_0	000083E8	CURRENT_DESCRIPTOR_NBR			83E8		
DMA4_CC EN1_0	00550C3A	CURRENT_ELMNT_NBR			550C3A		
DMA4_CC FN1_0	0000F0C6	CURRENT_FRAME_NBR			F0C6		
DMA4_CCR1_0	0102A020	WRITE_PRIORITY			0	BUFFERING_DISABLE	0
		PREFETCH			0	SUPERVISOR	0
		BS			0	TRANSPARENT_COPY_ENABLE	1

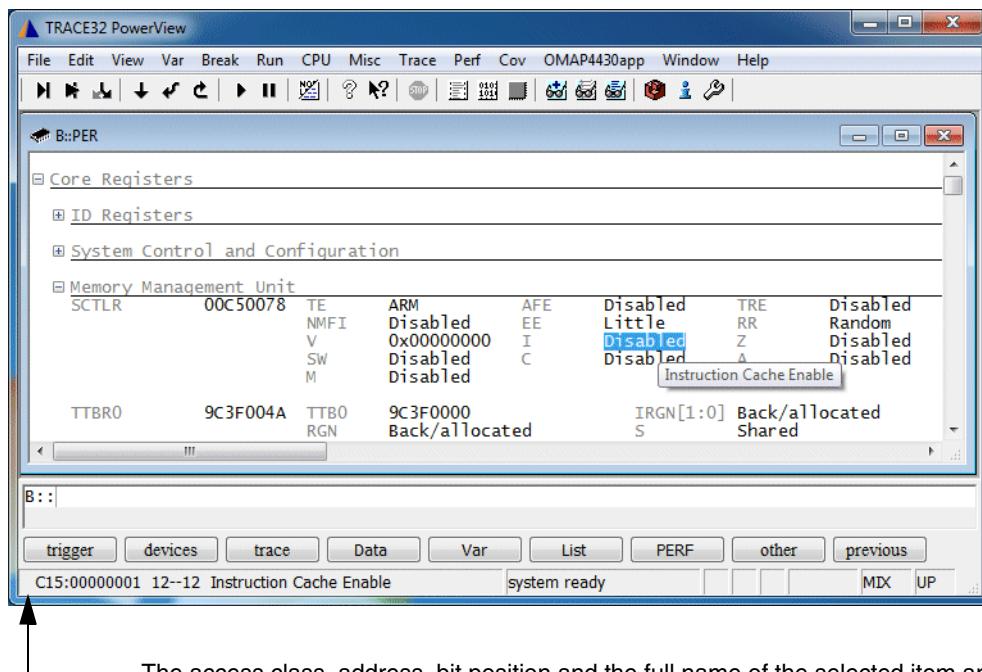
The following command sequence can be used to save the contents of all configuration registers/on-chip peripheral registers to a file.

```
; PRinTer.FileType ASCIIIE ; Select ASCII ENHANCED as output
                            ; format
                            ; (default output format)

PRinTer.FILE Per.lst ; Define Per.lst as output file

WinPrint.PER.view ; Save contents of all
                  ; configuration registers/on-chip
                  ; peripheral registers to the
                  ; specified file
```

Details about a Single Special Function Register

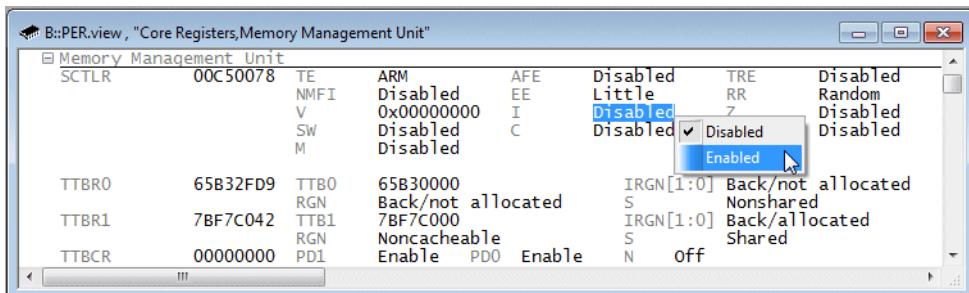


The access class, address, bit position and the full name of the selected item are displayed in the state line; the full name of the selected item is taken from the processor/chip manual.

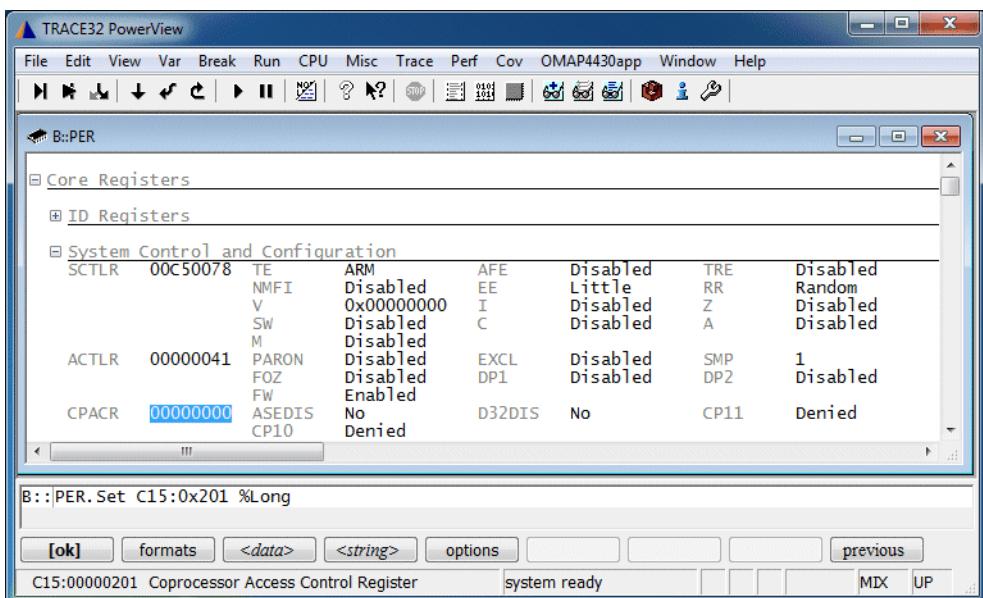
Modify a Special Function Register

You can modify the contents of a configuration/on-chip peripheral register:

- By pressing the right mouse button and selecting one of the predefined values from the pull-down menu.



- By a double-click to a numeric value. A **PER.Set** command to change the contents of the selected register is displayed in the command line. Enter the new value and confirm it with return.



PER.Set.simple <address>|<range> [%<format>] <value>

Modify configuration register/on-chip peripheral

Data.Set <address>|<range> [%<format>] <value>

Modify memory

Data.Set is equivalent to **PER.Set.simple** if the configuration register is memory mapped.

```
PER.Set.simple D:0xF87FFF10 %Long 0x00000b02
```

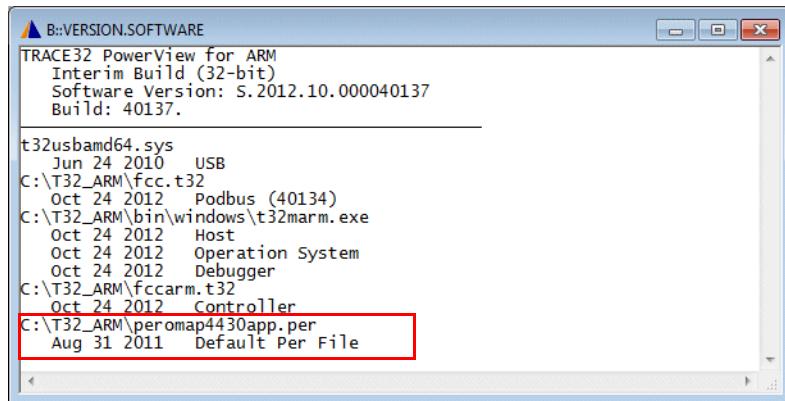
The PER Definition File

The layout of the PER window is described by a PER definition file.

The definition can be changed to fit to your requirements using the **PER** command group.

The path and the version of the actual PER definition file can be displayed by using:

VERSION.SOFTWARE



PER.view <filename>

Display the configuration registers/on-chip peripherals specified by
<filename>

```
PER.view C:\T32_ARM\percortexa9mpcore.per
```

Memory Display and Modification

This training section introduces the most often used methods to display and modify memory:

- The **Data.dump** command, that displays a hex dump of a memory area, and the **Data.Set** command that allows to modify the contents of a memory address.
- The **List** (former **Data.List**) command, that displays the memory contents as source code listing.

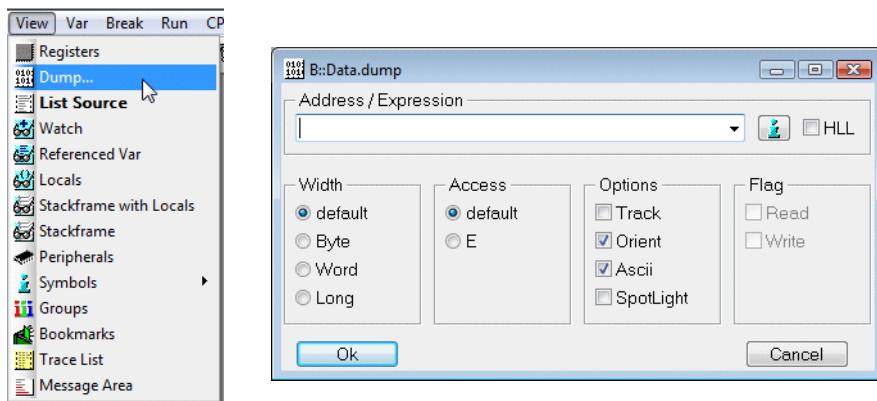
A so-called **access class** is always displayed together with a memory address. The following access classes are available for all processor architectures:

P:1000	Program address 0x1000
D:6814	Data address 0x6814

For additional access classes provided by your processor architecture refer to your “[Processor Architecture Manuals](#)”.

The Data.dump Window

Display the Memory Contents



Use an Address to Specify the Start Address for the Data.dump Window

The screenshot shows the TRACE32 interface. At the top, there is a configuration dialog for the 'Data.dump' window. The 'Address / Expression' field contains the value '0x6814' and is highlighted with a red box. Below this, there are sections for 'Width' (with 'default' selected), 'Access' (with 'default' selected), 'Options' (with 'Track' and 'Ascii' checked), and 'Flag' (with 'Read' checked). Buttons for 'Ok' and 'Cancel' are at the bottom left and right respectively. Below the configuration dialog is the main TRACE32 window titled 'B::Data.dump (0x6814) /DIALOG'. It displays memory dump data starting at address 0x6814. The data is presented in a grid with columns for address, bytes (0, 4, 8), and characters (C). The first few rows of data are as follows:

address	0	4	8	C
SD : 00006810	83421780	06004185	038255C0	A4404D68 83B82A0E8U25hM04
SD : 00006820	2C10F820	54018000	28506482	A5DD1248 55,885T2dP(H1288)
SD : 00006830	42010004	87354C60	08017201	2423DC18 55,885T2dP(H1288)
SD : 00006840	00000040	2C014624	42415055	0820A090 00NUS\$F5,1,UPqD88..5
SD : 00006850	6243200A	050402C0	18004142	410B0449 55,885T2dP(H1288)
SD : 00006860	02066040	500010F5	80800182	04B11560 0'85E1NPSS88,1,1E
SD : 00006870	982A2100	40000801	8512040D	10958806 55,885T2dP(H1288)
SD : 00006880	02254894	42830588	A0800324	C0484990 55,885T2dP(H1288)



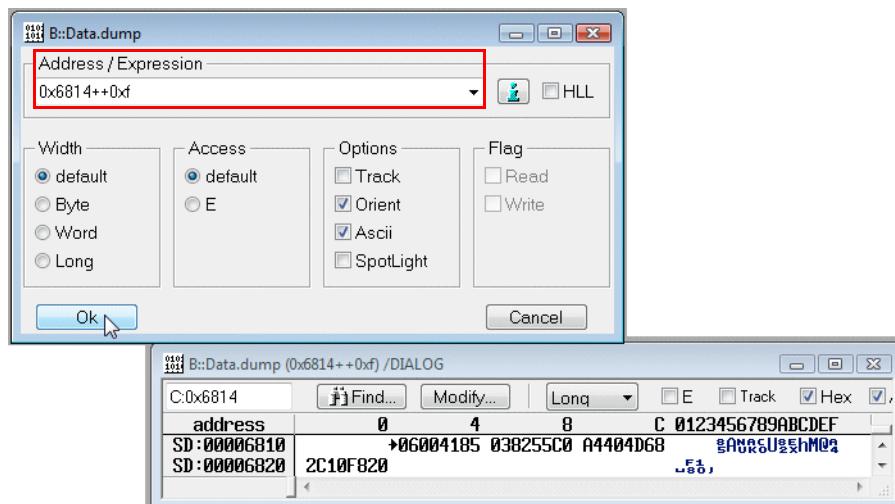
Please be aware, that TRACE32 permanently updates all windows. The default update rate is 10 times per second.

Use an Address Range to Specify the Addresses for the Data.dump Window

If you enter an address range, only data for the specified address range are displayed. This is useful if a memory area close to memory-mapped I/O registers should be displayed and you do not want TRACE32 PowerView to generate read cycles for the I/O registers.

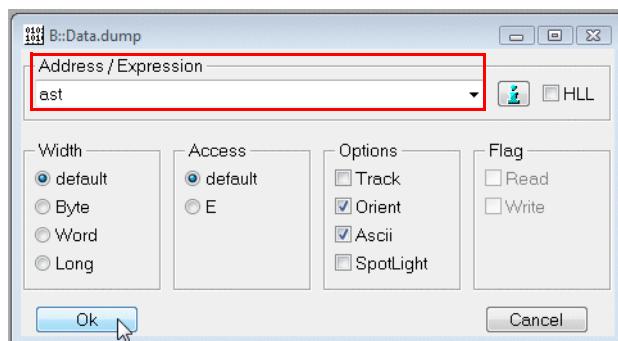
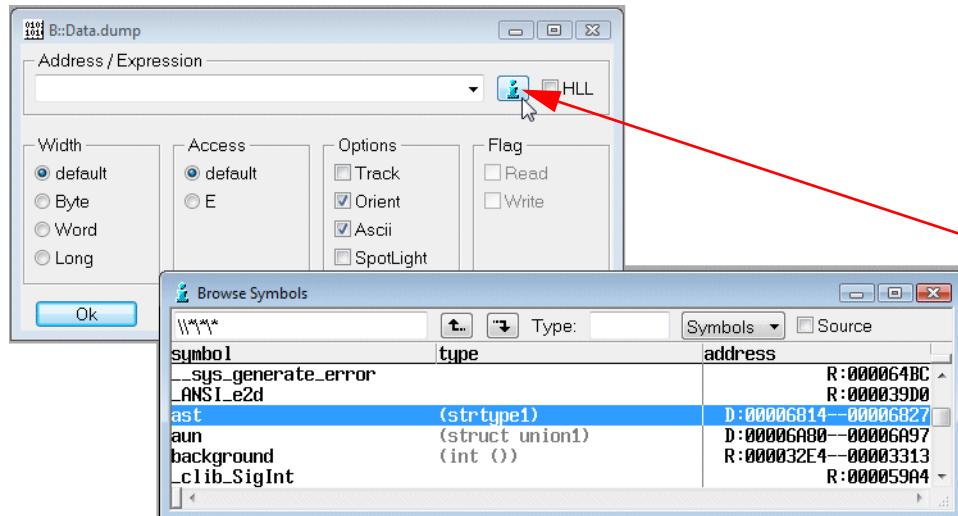
Conventions for address ranges:

- `<start_address>--<end_address>`
 - `<start_address>..<end_address>`
 - `<start_address>++<offset_in_byte>`
 - `<start_address>++<offset_in_word>` (for DSPs)



Use a Symbol to Specify the Start Address for the Data.dump Window

Use **i** to select any symbol name or label known to TRACE32 PowerView.



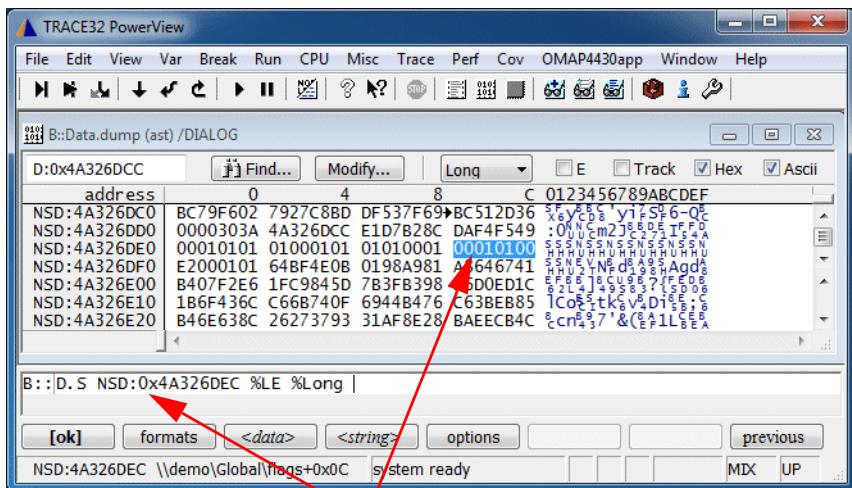
By default an oriented display
is used (line break at 2^X).

A small arrow indicates
the specified dump address.

B::Data.dump (ast) /DIALOG						
address	0	4	8	C	0123456789ABCDEF	
SD:00006810	83421780	06004185	038255C0	A4404D68	8342178006004185A4404D68	8342178006004185A4404D68
SD:00006820	2C10F820	54018080	28506482	A5DD1248	2C10F8205401808028506482A5DD1248	2C10F8205401808028506482A5DD1248
SD:00006830	42010A04	87354C60	00017201	2423DC18	42010A0487354C60000172012423DC18	42010A0487354C60000172012423DC18
SD:00006840	08000040	2C014624	42015055	0820A090	080000402C014624420150550820A090	080000402C014624420150550820A090
SD:00006850	6243200A	050402CD	18004142	410B0449	6243200A050402CD18004142410B0449	6243200A050402CD18004142410B0449
SD:00006860	02066040	500010F5	80800102	04B11560	02066040500010F58080010204B11560	02066040500010F58080010204B11560

```
Data.dump 0x6814 ; Display a hex dump starting at  
; address 0x6814  
  
Data.dump 0x6810--0x682f ; Display a hex dump of the  
; specified address range  
  
Data.dump 0x6810..0x682f ; Display a hex dump of the  
; specified address range  
  
Data.dump 0x6810++0x1f ; Display a hex dump of the  
; specified address range  
  
Data.dump ast ; Display a hex dump starting at  
; the address of the label ast  
  
Data.dump ast /Byte ; Display a hex dump starting at  
; the address of the label ast in  
; byte format
```

Modify the Memory Contents



By a left mouse double-click to the memory contents

a **Data.Set** command is automatically
displayed in the command line,
you can enter the new value and
confirm it with return.

Data.Set <address>|<range> [%<format>] <value> [/<option>]

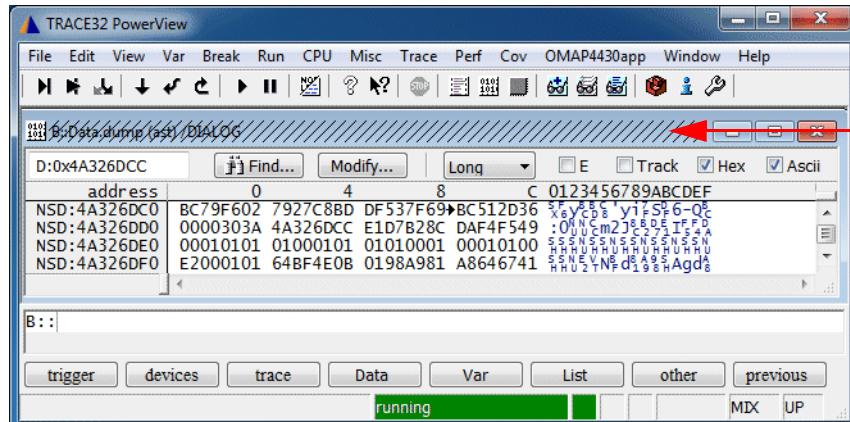
```
Data.Set 0x6814 0xaa ; Write 0xaa to the address
                      ; 0x6814

Data.Set 0x6814 %Long 0xaaaa ; Write 0xaaaa as a 32 bit value to
                             ; the address 0x6814, add the
                             ; leading zeros automatically

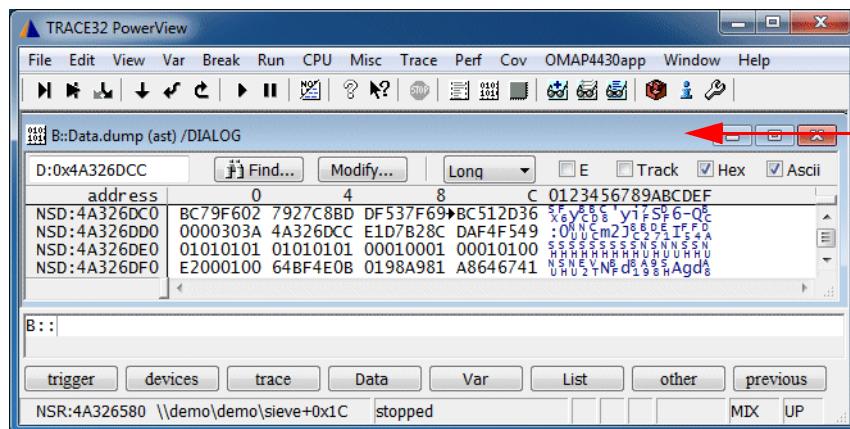
Data.Set 0x6814 %LE %Long 0xaaaa ; Write 0xaaaa as a 32 bit value to
                                   ; the address 0x6814, add the
                                   ; leading zeros automatically
                                   ; Use Little Endian mode
```

Run-time Memory Access

TRACE32 PowerView updates the displayed memory contents by default only if the core is stopped.



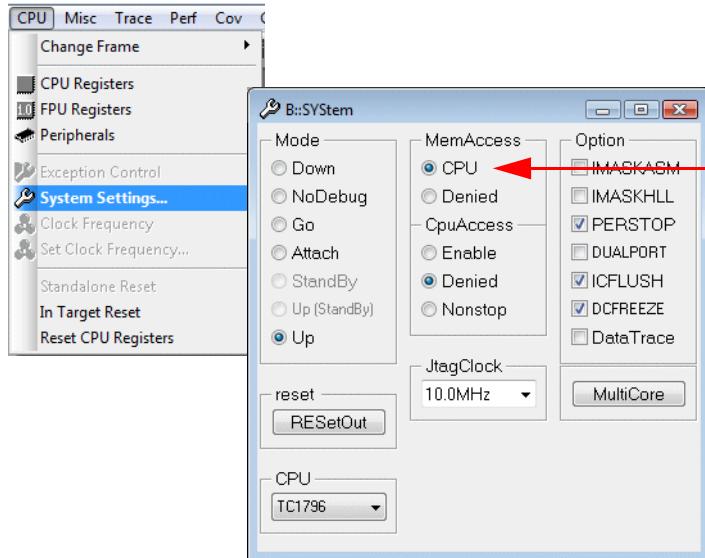
A hatched window frame indicates that the information display is frozen because the core is executing the program.



The plain window frame indicates that the information is updated, because the program execution is stopped.

Various cores allow a debugger to read and write physical memory (not cache) while the core is executing the program. The debugger has in most cases direct access to the processor/chip internal bus, so no extra load for the core is generated by this feature.

Open the **SYStem** window in order to check if your processor architecture allows a debugger to read/write memory while the core is executing the program:



MemAccess CPU/NEXUS/DAP indicates that the core allows the debugger to read/write the memory while the core is executing the program.

Please be aware that caches, MMUs, tightly-coupled memories and suchlike add conditions to the run-time memory access or at worst make its use impossible.

Restrictions

The following description is only a rough overview on the restrictions. Details about your core can be found in the [Processor Architecture Manual](#).

Cache

If run-time memory access for a cached memory location is enabled the debugger acts as follows:

- **Program execution is stopped**

The data is read via the cache respectively written via the cache.

- **Program execution is running**

Since the debugger has no access to the caches while the program execution is running, the data is read from physical memory. The physical memory contains the current data only if the cache is configured as write-through for the accessed memory location, otherwise out-dated data is read.

Since the debugger has no access to the cache while the program execution is running, the data is written to the physical memory. The new data has only an effect on the current program execution if the debugger can invalidate the cache entry for the accessed memory location. This useful feature is not available for most cores.

MMU

Debuggers have no access to the TLBs while the program execution is running. As a consequence run-time memory access can not be used, especially if the TLBs are dynamically changed by the program.

In the exceptional case of static TLBs, the TLBs can be scanned into the debugger. This scanned copy of the TLBs can be used by the debugger for the address translation while the program execution is running.

Tightly-coupled Memory

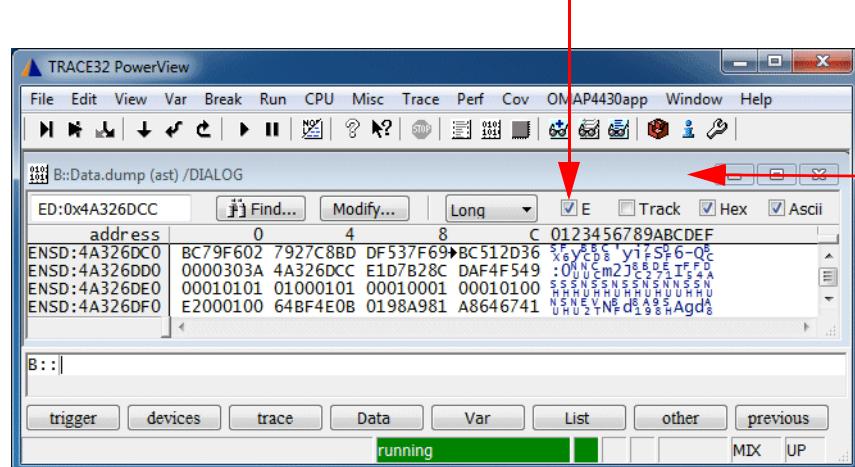
Tightly-coupled memory might not be accessible via the system memory bus.

Usage

The usage of the non-intrusive run-time memory access has to be configured explicitly. Two methods are provided:

- Configure the run-time memory access for a specific memory area.
- Configure run-time memory access for all windows that display memory contents (not available for all processor architectures).

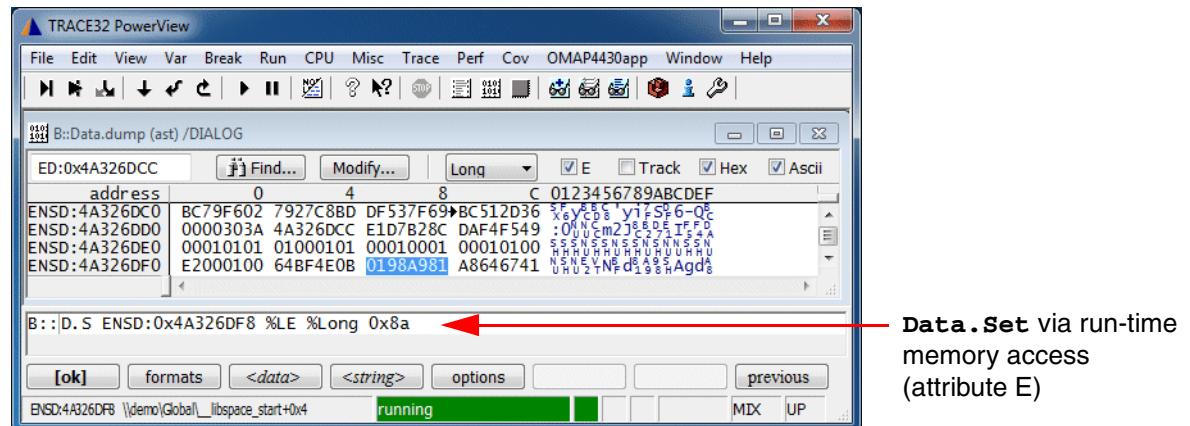
Configure the run-time memory access for a specific memory area:



If the **E** check box is enabled, the attribute E is added to the memory class:

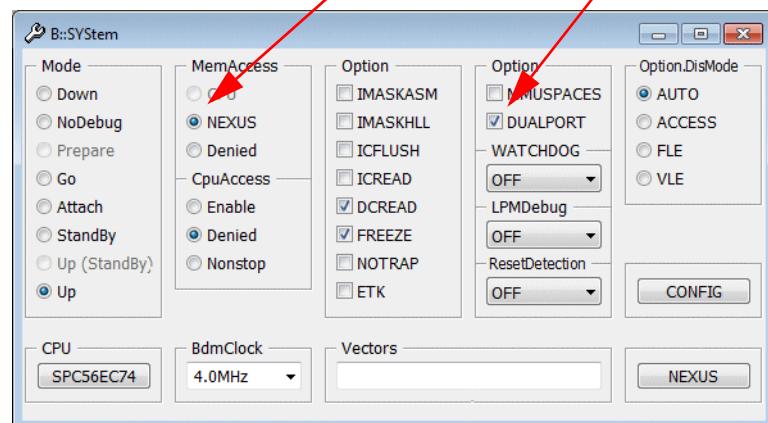
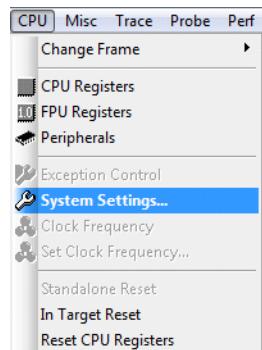
EP:1000	Program address 0x1000 with run-time memory access
ED:6814	Data address 0x6814 with run-time memory access

Write accesses to the memory work correspondingly:



```
SYSystem.MemAccess CPU ; Enable the non-intrusive  
; run-time memory access  
...  
Go ; Start program execution  
Data.dump E:0x6814 ; Display a hex dump starting at  
; address 0x6814 via run-time  
; memory access  
Data.Set E:0x6814 0xAA ; Write 0xAA to the address  
; 0x6814 via run-time memory  
; access
```

Configure the run-time memory access for all windows that display memory (not available for all cores):

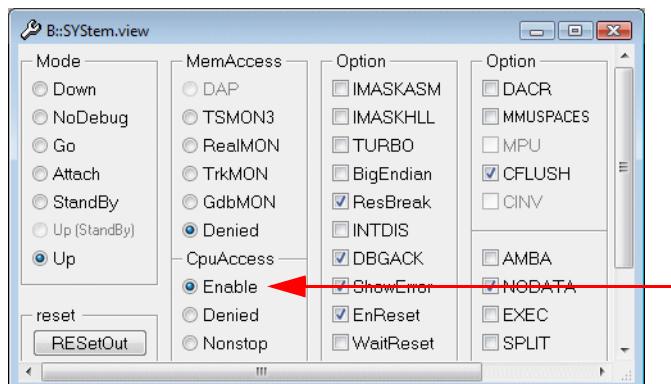


All windows that display memory have a plain window frame, because they are updated while the core is executing the program

Write access is possible for all memories while the core is executing the program

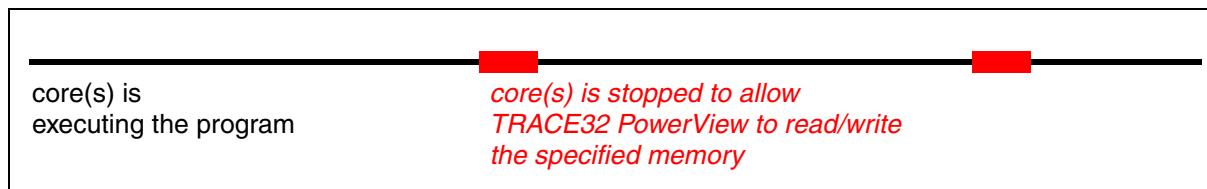
```
SYStem.MemAccess CPU ; Enable the non-intrusive  
                      ; run-time memory access  
  
SYStem.Option DUALPORT ON ; Activate the run-time memory  
                           ; access for all windows that  
                           ; display memory  
  
                           ; this SYStem.Option is only  
                           ; available for some processor  
                           ; architectures  
  
...  
  
Go ; Start program execution  
  
Data.dump 0x6814 ; Display a hex dump starting at  
                   ; address 0x6814 via run-time  
                   ; memory access  
  
Data.Set 0x6814 0xAA ; Write 0xAA to the address  
                     ; 0x6814 via run-time memory  
                     ; access
```

If your processor architecture doesn't allow a debugger to read or write memory while the core is executing the program, you can activate an intrusive run-time memory access if required.



CpuAccess Enable allows an intrusive run-time memory access

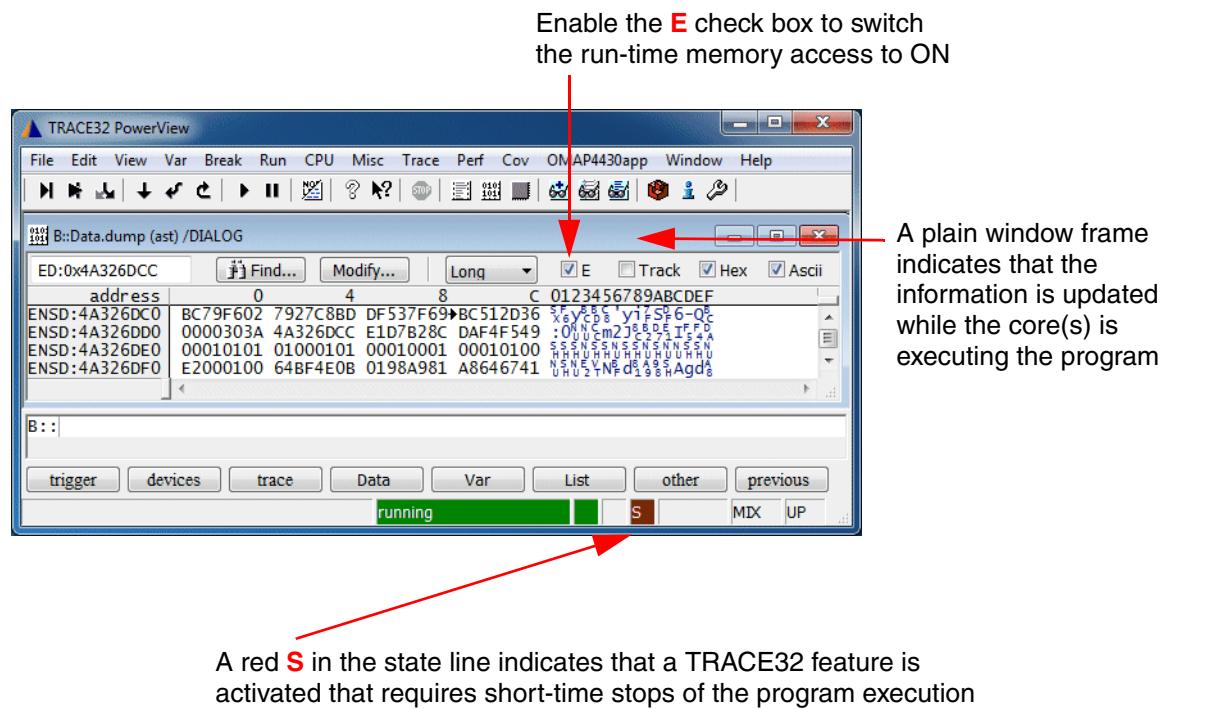
If an intrusive run-time memory access is activated, TRACE32 stops the program execution periodically to read/write the specified memory area. Each update takes at least **50 us**.



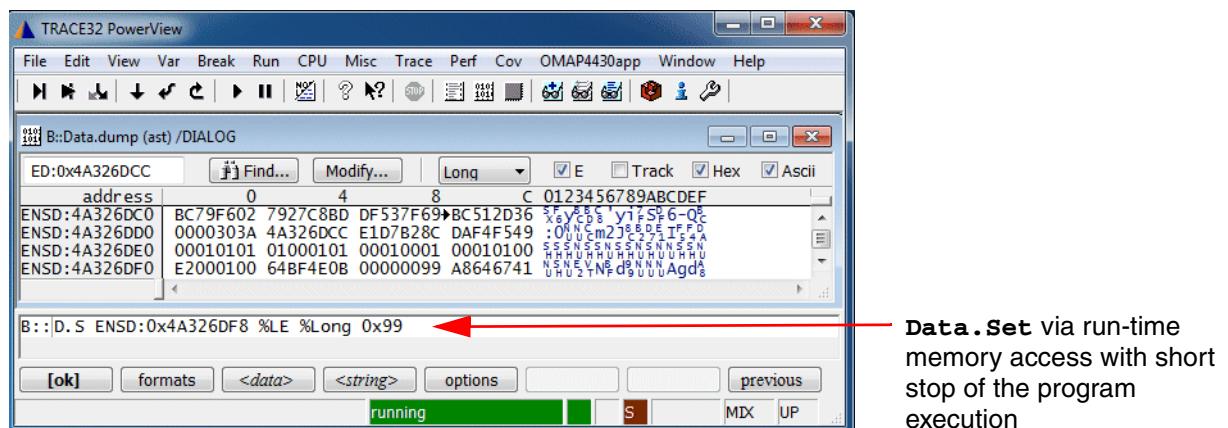
The time taken by a short stop depends on various factors:

- The time required by the debugger to start and stop the program execution on a processor/core (main factor).
- The number of cores that need to be stopped and restarted.
- Cache and MMU assessments that need to be performed to read the information of interest.
- The type of information that is read during the short stop.

An intrusive run-time memory access is only possible for a **specific memory area**.

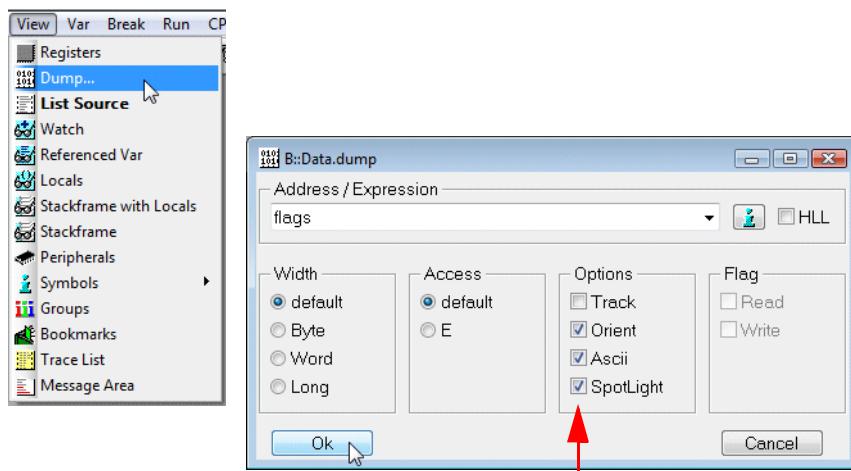


Write accesses to the memory work correspondingly:



```
SYStem.CpuAccess Enable ; Enable the intrusive  
; run-time memory access  
...  
Go ; Start program execution  
Data.dump E:0x6814 ; Display a hex dump starting at  
; address 0x6814 via an intrusive  
; run-time memory access  
Data.Set E:0x6814 0xAA ; Write 0xAA to the address  
; 0x6814 via an intrusive  
; run-time memory access
```

Colored Display of Changed Memory Contents



Enable the option **SpotLight** to mark the memory contents changed by the last 4 single steps in orange, older changes being lighter.

B::Data.dump (flags) /SpotLight /DIALOG							
address	0	1	2	3	4	5	6
SD:00007E78	16	A5	3D	90	01	00	01
							01
SD:00007E80	01	01	01	01	01	01	01
							01
SD:00007E88	01	01	01	01	01	01	01
							01
SD:00007E90	00	47	03	4A	50	C2	90
							A1
SD:00007E98	8A	01	01	85	33	15	99
							B2
SD:00007EA0	1A	00	10	4B	6C	12	0D
							02
SD:00007EA8	16	06	2D	31	52	48	81
							58

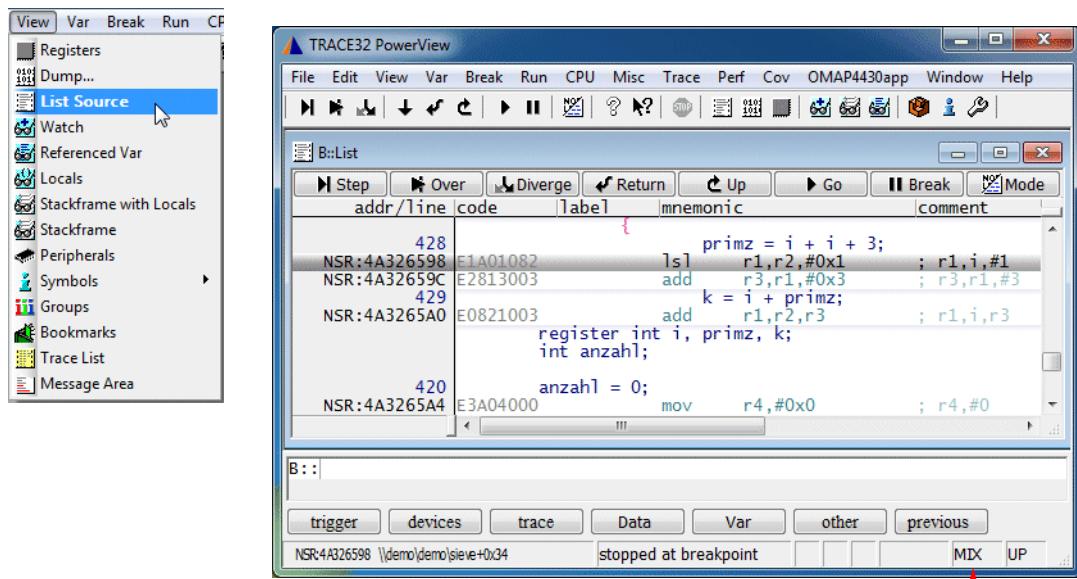
Data.dump flags /SpotLight

; Display a hex dump starting at
; the address of the label flags

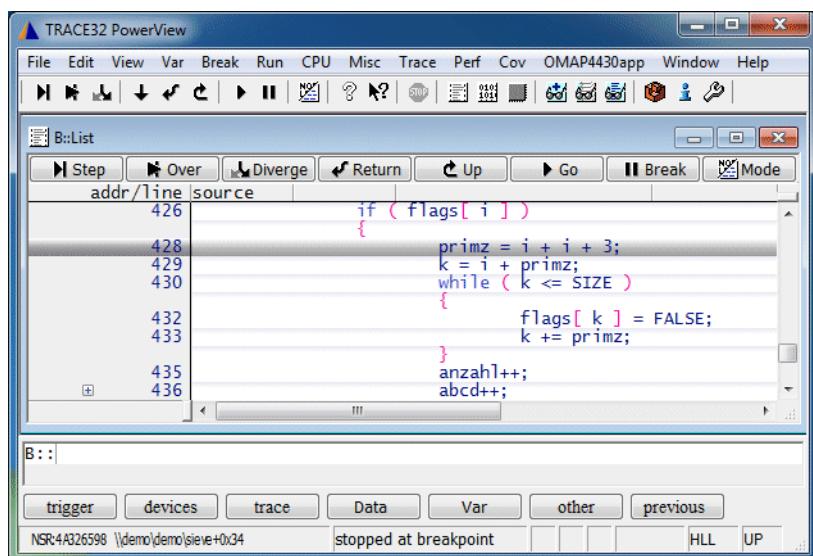
; Mark changes

The List Window

Displays the Source Listing Around the PC

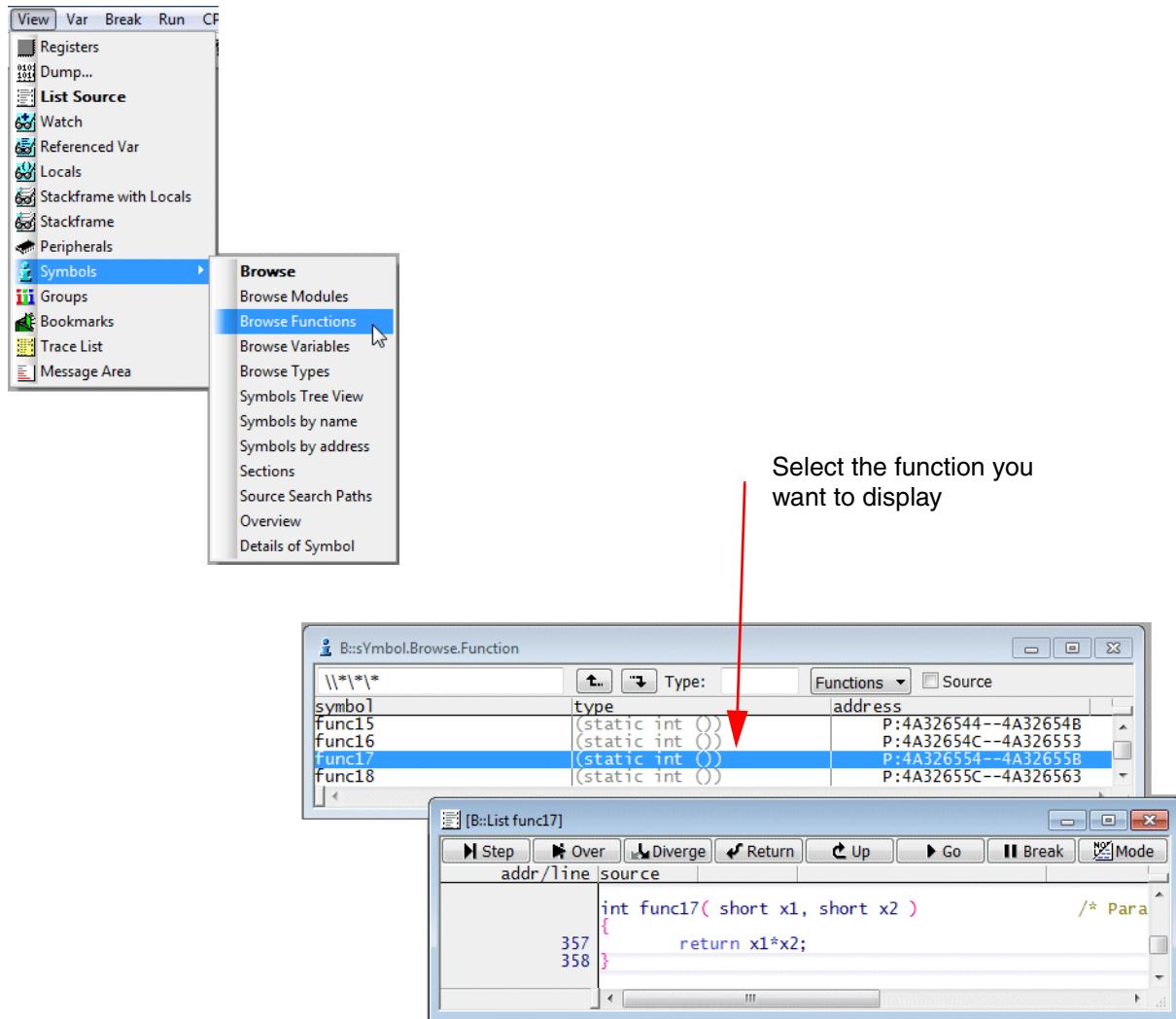


If MIX mode is selected for debugging, assembler and HLL information is displayed



If HLL mode is selected for debugging, only HLL information is displayed

Displays the Source Listing of a Selected Function



List [<address>] [/<option>]

Display source listing

Data.List [<address>] [/<option>]

Display source listing

```
List ; Display a source listing  
; around the PC  
  
List E: ; Display a source listing,  
; allow scrolling while the  
; program execution is running  
  
List * ; Open the symbol browser to  
; select a function for display  
  
List func17 ; Display a source listing of  
; func17
```

Breakpoints

Videos about the breakpoint handling can be found here:
http://www.lauterbach.com/tut_breakpoints.html

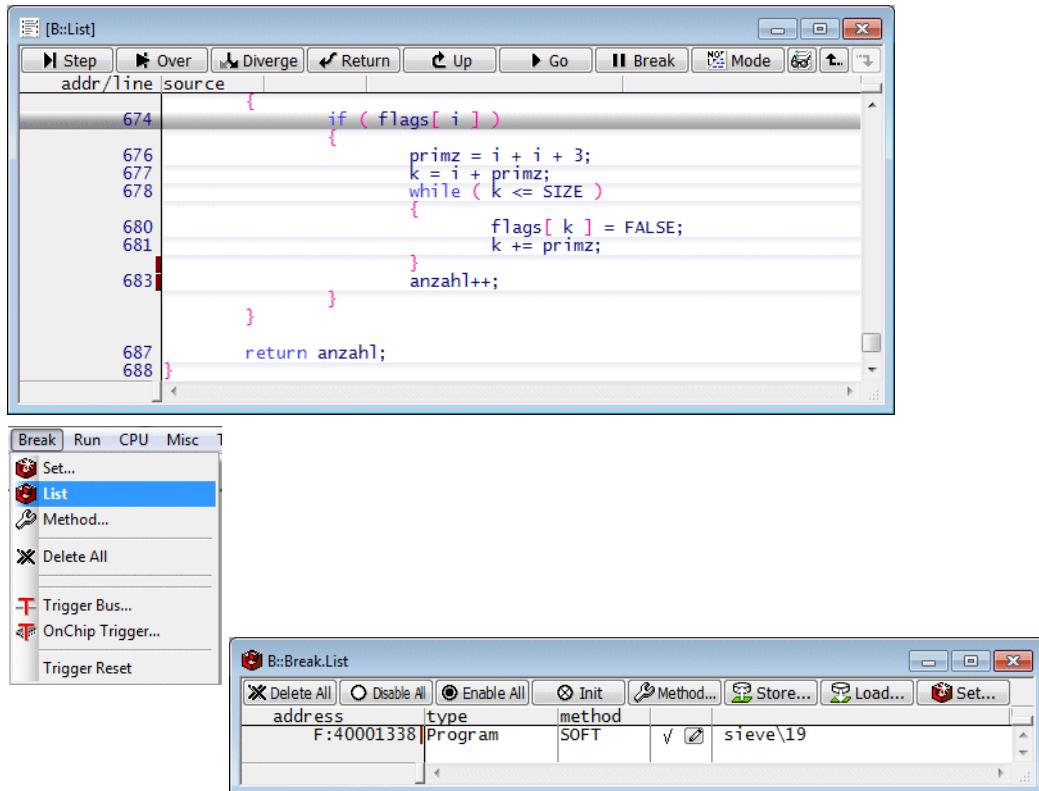
Breakpoint Implementations

A debugger has two methods to realize breakpoints: Software breakpoints and Onchip breakpoints.

Software Breakpoints in RAM

The default implementation for breakpoints on instructions is a Software breakpoint. If a Software breakpoint is set the original instruction at the breakpoint address is patched by a special instruction (usually TRAP) to stop the program and return the control to the debugger.

The number of software breakpoints is unlimited.



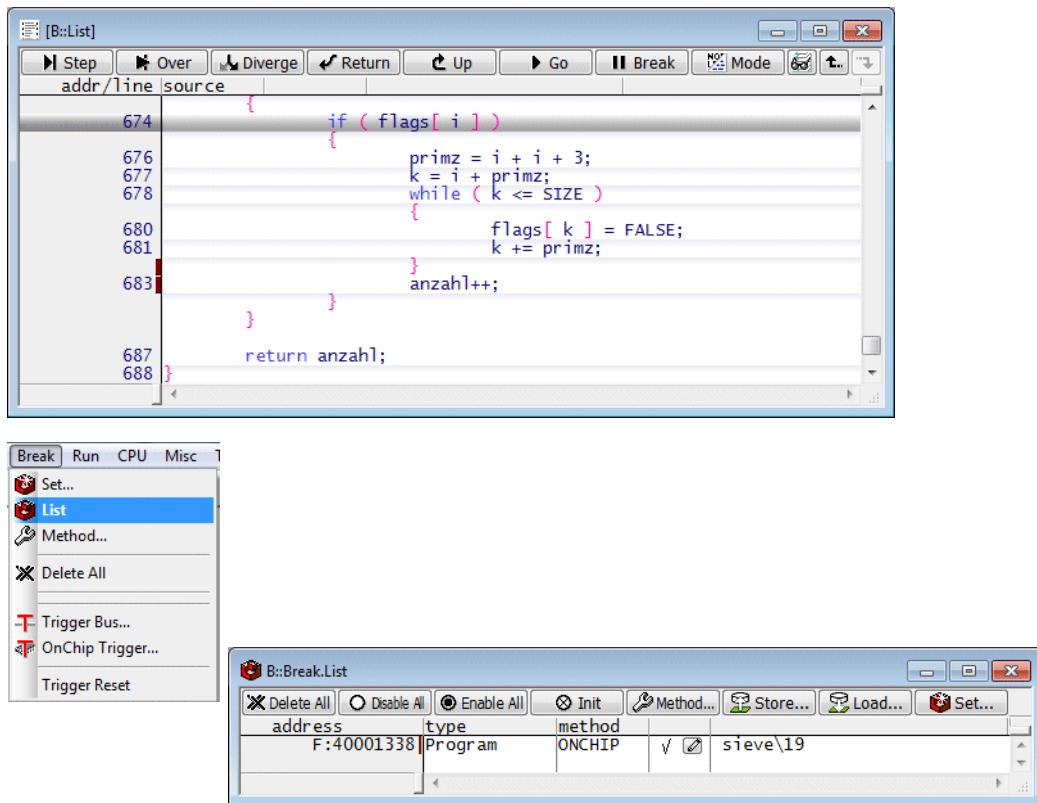
Breakpoints on instructions are called **Program** breakpoints by TRACE32 PowerView.

	Please be aware that TRACE32 PowerView always tries to set an Onchip breakpoint, when the setting of a Software Breakpoint fails.
---	---

TRACE32 allows to set Software breakpoints to FLASH. Please be aware that the affected FLASH sector has to be erased and programmed in order to patch the break instruction used by the Software breakpoint. This usually takes some time and reduces the number of FLASH erase cycles. For details refer to “[Software Breakpoints in FLASH](#)” (norflash.pdf).

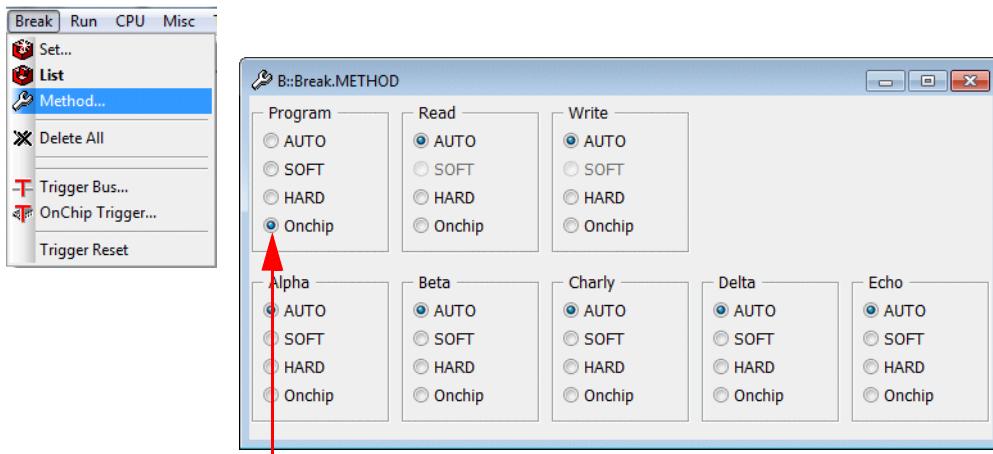
Onchip Breakpoints in NOR Flash

Most core(s) provide a small number of Onchip breakpoints in form of breakpoint registers. These Onchip breakpoints can be used to set breakpoints to instructions in read-only memory like onchip or NOR FLASH.



Since Software breakpoints are used by default for Program breakpoints, TRACE32 PowerView can be informed explicitly where to use Onchip breakpoints. Depending on your memory layout, the following methods are provided:

1. If the code is completely located in read-only memory, the default implementation for the Program breakpoints can be changed.



Change the implementation of Program breakpoints to **Onchip**

Break.METHOD Program Onchip

Advise TRACE32 PowerView to implement Program breakpoints always as Onchip breakpoints

2. If the code is located in RAM and onchip/NOR FLASH you can define code ranges where Onchip breakpoints are used.

MAP.BOnchip <range>

Advise TRACE32 PowerView to implement Program breakpoints as Onchip breakpoints within the defined address range

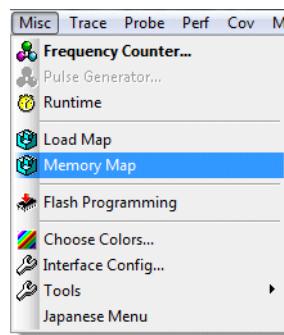
MAP.List

Check your settings

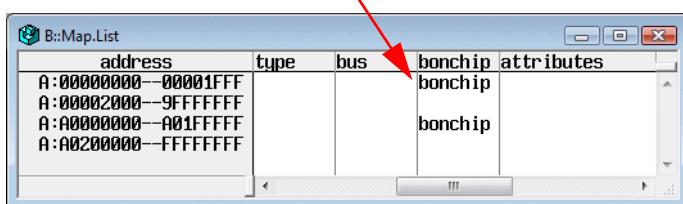
MAP.BOnchip 0x0++0x1FFF

MAP.BOnchip 0xA0000000++0x1FFFF

Check your settings as follows:



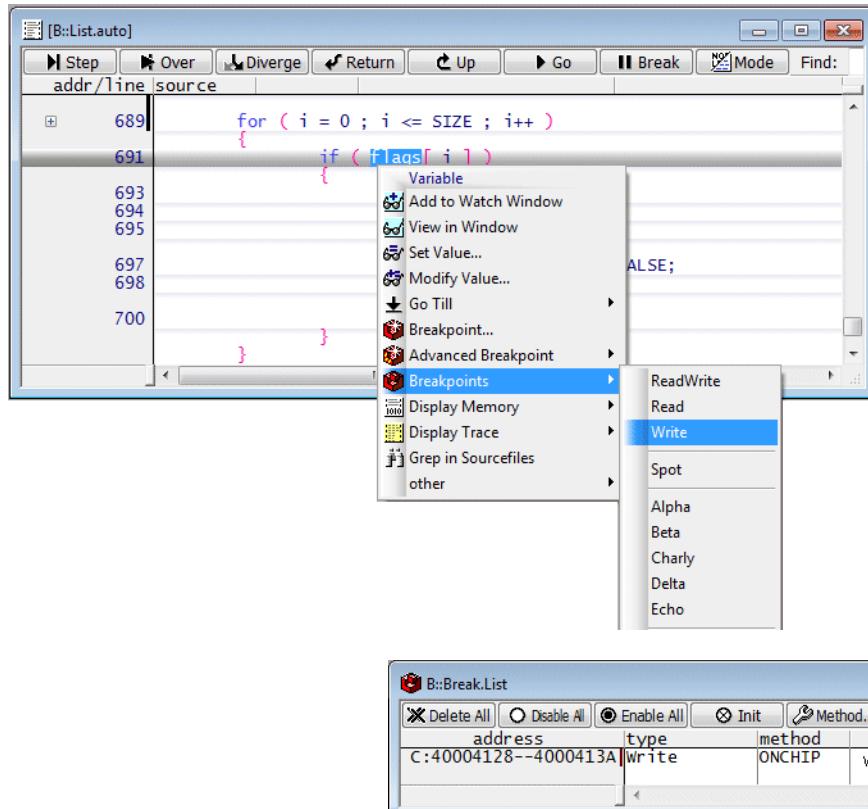
For the specified address ranges Program breakpoints are implemented as Onchip breakpoints. For all other memory areas Software breakpoints are used.



address	type	bus	bonchip	attributes
A:00000000--00001FFF			bonchip	
A:00002000--9FFFFFFF			bonchip	
A:A0000000--A01FFFFF			bonchip	
A:A0200000--FFFFFFFF			bonchip	

Onchip Breakpoints on Read/Write Accesses

Onchip breakpoints can be used to stop the core at a read or write access to a memory location.



The list on [page 1](#) gives an overview of the availability and the usage of the **Onchip breakpoints**. The following notations are used:

- **Onchip breakpoints:** Total amount of available Onchip breakpoints.
- **Program breakpoints:** Number of Onchip breakpoints that can be used to set Program breakpoints into onchip FLASH or NOR FLASH.
- **Read/Write breakpoints:** Number of Onchip breakpoints that stop the program when a read or write to a certain address happens.
- **Data value breakpoint:** Number of Onchip data breakpoints that stop the program when a specific data value is written to an address or when a specific data value is read from an address.

Single address

For some processor architectures Onchip breakpoints can only mark **single addresses** (e.g Cortex-A9).

Address ranges

Most processor architectures allow to mark **address ranges** with Onchip breakpoints. It is very common that one Onchip breakpoint marks the start address of the address range while the second Onchip breakpoint marks the end address (e.g. MPC57xx).

The command **TrOnchip.VarCONVert** allows to control how range breakpoints are set for scalars (int, float, double).

TrOnchip.VarCONVert ON	If a breakpoint is set to a scalar variable (int, float, double) the breakpoint is set to the start address of the variable. + Requires only one single address breakpoint. - Program will not stop on unintentional accesses to the variable's address space.
TrOnchip.VarCONVert OFF	If a breakpoint is set to a scalar variable (int, float, double) breakpoints are set to all memory addresses that store the variable value. + The program execution stops also on any unintentional accesses to the variable's address space. - Requires two onchip breakpoints since a range breakpoint is used.

The current setting can be inspected by using the command **TrOnchip.view**.

```
TrOnchip.VarCONvert ON  
Var.Break.Set vint /Write  
Data.View vint
```

breakpoint	address	data	value	symbol
W	SD:4000406C	00	'N'	\\\diabc\Global\vint
	SD:4000406D	00	'N'	\\\diabc\Global\vint+0x1
	SD:4000406E	00	'N'	\\\diabc\Global\vint+0x2
	SD:4000406F	00	'N'	\\\diabc\Global\vint+0x3

```
TrOnchip.VarCONvert OFF  
Var.Break.Set vint /Write  
Data.View vint
```

breakpoint	address	data	value	symbol
W	SD:4000406C	00	'N'	\\\diabc\Global\vint
W	SD:4000406D	00	'N'	\\\diabc\Global\vint+0x1
W	SD:4000406E	00	'N'	\\\diabc\Global\vint+0x2
W	SD:4000406F	00	'N'	\\\diabc\Global\vint+0x3
	SD:40004070	00	'N'	\\\diabc\Global\vlong

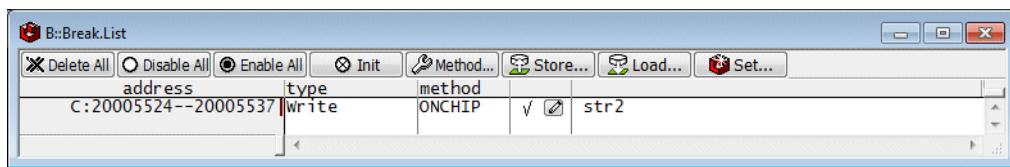
Bit masks

A number of processor architectures provide only **bit masks** or **fixed range sizes** to mark an address range with Onchip breakpoints. In this case the address range is always enlarged to the **smallest bit mask/next allowed range** that includes the address range.

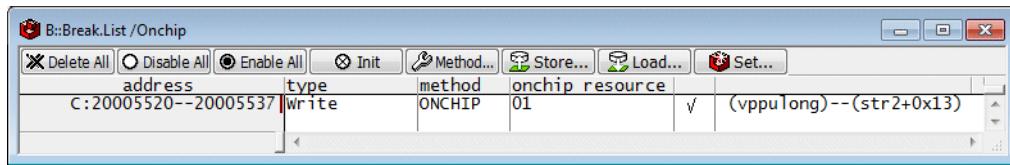
It is recommended to control which addresses are actually marked with breakpoints by using the **Break.List /Onchip** command:

Breakpoint setting:

```
Var.Break.Set str2  
Break.List
```



```
Break.List /Onchip
```



Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
68HC12 68HC12A	up to 2	up to 2 single address	up to 2 single address	1
68HC16	—	—	—	—
68k 6833x 6834x 68360	— — 1	— — 1	— — 1	— — —
78K0R	1	1 single address	1 single address	1
Andes	0 ... 8	up to 8	up to 8 range as bit mask	up to 8
APS	3 instruction	3 single address	—	—
ARM11	6 instruction 2 read/write	6 single address	2 single address	—
ARM7 ARM9 Janus	2 or (1 if software break-points are used)	up to 2 range as bit mask	up to 2 range as bit mask	2
ARP32	2 instruction 2 read/write	2 range as bit mask	up to 2 range as bit mask	up to 2
AVR32	6 instruction 2 read/write	6 range as bit mask	2 range as bit mask	2
AVR8	4	up to 4 range as bit mask	up to 2 range as bit mask	1
C166SV2	4	up to 4	up to 4 write up to 1 read	up to 4 write up to 1 read
ColdFire	4 instruction, 2 read/write	3 single address, 1 bit mask	2 single address or 2 ranges	2
Cortex-A5	3 instruction 2 read/write	3 single address	2 range as bit mask, break before make	—
Cortex-A7 Cortex-A9 Cortex-A15 Cortex-A17 Cortex-A32 Cortex-A35 Cortex-A53 Cortex-A57 Cortex-A72 Cortex-A73	6 instruction 4 read/write	6 single address	4 range as bit mask, break before make	—

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
Cortex-A8	6 instruction 2 read/write	6 range as bit mask	2 range as bit mask, break before make	—
Cortex-M0/M0+	1-2 by DW (Data Watchpoint unit) 1-4 by BU (Breakpoint Unit)	1-2 by DW range as bit mask 1-4 by BU single addr. only onchip flash only	1-2 by DW range as bit mask	—
Cortex-M1	1/2 by DW (Data Watchpoint unit) 2/4 by BPU (Breakpoint Unit)	1 or 2 by DW range as bit mask 2 or 4 (BPU) single addr. only onchip flash only	1 or 2 by DW range as bit mask	—
Cortex-M3	4 by DWT (Data Watchpoint and Trace unit) 6 by FPB (Flash Patch and Breakpoint unit)	4 by DWT break-after-make range as bit mask 6 by FPB single addr. only onchip flash only break-before-make	4 by DWT range as bit mask	1 needs two DWT comparators
Cortex-M4	1 or 4 by DWT (Data Watchpoint and Trace unit) 2 or 6 by FPB (Flash Patch and Breakpoint unit)	1 or 4 by DWT break-after-make range as bit mask 2 or 6 by FPB single addr. only onchip flash only break-before-make	1 or 4 by DWT range as bit mask	0 or 1 needs two DWT comparators
Cortex-M7	2 or 4 by DWT (Data Watchpoint and Trace unit) 4 or 8 by FPB (Flash Patch and Breakpoint unit)	2 or 4 by DWT break-after-make range as bit mask 4 or 8 by FPB single addr. only onchip flash only break-before-make	2 or 4 by DWT range as bit mask	1
Cortex-R4 Cortex-R5	2-8 instruction 1-8 read/write	2-8 range as bit mask	1-8 range as bit mask, break before make	—
Cortex-R7	6 instruction 4 read/write	6 single address	4 range as bit mask, break before make	—

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
eSi-RISC	up to 8 instruction up to 8 read/write	up to 8 single address	up to 8 single address or up to 4 ranges	—
eTPU	2	up to 2 single address	up to 2 read/write range as bitmask	2 (only with write breakpoints)
GTM (only MPC)	up to 4	up to 4	up to 4	2
H8S	2	up to 2	up to 2 range as bit mask	2
H8SX	4	up to 4	up to 4 range as bit mask	1
M32R	4 instruction 2 read/write	4 single address	2 single address or 2 ranges	2
MCORE	2	2 single address or 1 range as bit mask	2 range as bit mask	—
MCS12 MCS12C	up to 3	up to 3 single address	up to 3 single address	1
MCS8	2	up to 2 single address	up to 2 single address (reduced to 1 if com- bined with data)	1
MGT5100	1 instruction (No on-chip break- point, if software break- points are used) 1 read/write	1/0 single address	1 single address	—
MIPS32 MIPS64	up to 15 instruction up to 15 read/write	up to 15 range as bit mask	up to 15 range as bit mask	up to 15
MPC500 MPC800	4 instruction, 2 read/write	4 single address or 2 breakpoint ranges	2 single address or 1 breakpoint range	2
MPC5200	2 instruction (reduced to 1 if soft- ware breakpoints are used) 2 read/write	2/1 2 single address or 1 breakpoint range	2 2 single address or 1 breakpoint range	—
MPC55xx	4 instruction 2 read/write	4 single address or 2 breakpoint ranges	2 single address or 1 breakpoint range	—
MPC563x	4 instruction 2 read/write	4 single address or 2 breakpoint ranges	2 single address or 1 breakpoint range	2

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
MPC564x MPC567x	8 instruction 2 read/write	8 single address or 4 single address and 2 breakpoint ranges	2 single address or 1 breakpoint range	2
MPC57xx (e200z0)	4 instruction 2 read/write	4 single address or 2 breakpoint ranges	2 single address or 1 breakpoint range	—
MPC57xx (e200z2*, e200z4*, e200z7*)	8 instruction 4 read/write	8 single address or 4 single address and 2 breakpoint ranges	4 single address or 2 breakpoint range	2
MPC74xx MPC86xx	1 instruction (No on-chip breakpoint, if software breakpoints are used) 1 read/write	1/0 single address	1 single address	—
MPC8240 MPC8245 MPC825x MPC826x (PQ2)	1 instruction (No on-chip breakpoint, if software breakpoints are used)	1/0 single address	—	—
MPC8247 MPC8248 MPC827x MPC8280 (PQ27) MPC83xx (PQ2 Pro)	2 instruction (reduced to 1 if software breakpoints are used) 2 read/write	2/1 2 single address or 1 breakpoint range	2 2 single address or 1 breakpoint range	—
MPC85xx (PQ3)	2 instruction (reduced to 1 if software breakpoints are used) 2 read/write	2/1 2 single address or 1 breakpoint range	2 2 single address or 1 breakpoint range break before make	—
MSP430	2 ... 8	2 ... 8 ranges require 2 breakpoints	2 ... 8 ranges require 2 ... 4 breakpoints	2 ... 8
PPC401 PPC403	2 instruction, 2 read/write	2 single address or 2 ranges	2 single address or 2 ranges	—
PPC405 PPC44x	4 instruction, 2 read/write	4 single address or 2 address ranges	2 single address or 1 address range	2

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
PPC600	1 instruction (no on-chip break- point, if software break- points are used)	1/0 single address	—	—
PPC740 PPC750	1 instruction (No on-chip break- point, if software break- points are used) 1 read/write	1/0 single address	1 single address	—
PWR- ficient	2 instruction, 2 read/write	2 single address or 1 breakpoint range	2 single address or 1 breakpoint range	—
QORIQ	2 instruction, 2 read/write	2 single addr., or 1 large range, or 2 ranges up to 4 kB, or 1 single address and 1 range up to 4 kB	2 single addr., or 1 large range, or 2 ranges up to 4 kB, or 1 single address and 1 range up to 4 kB	—
RISC-V	up to 2^{32} for 32-bit RISC-V up to 2^{64} for 64-bit RISC-V	single address, range as bitmask (if supported)	single address, range as bitmask (if supported) break before make	—
RH850	12	12 range as bit mask	12 range as bit mask break before make	12
RX	8 instruction 4 read/write	8 range as bit mask	4 1 breakpoint range others range as bit mask	4
S12X S12Z	4	up to 4 single address or 2 address ranges	up to 4 single address or 2 address ranges	1
SH2A ST4A	10	up to 10	up to 10 range as bit mask	2
SH3	2	up to 2	up to 2 range as bit mask	—
SH4 ST40	6	up to 6	up to 6 range as bit mask	2
SH7047 SH7144/45	1	up to 1	up to 1	—
SH7058	12	up to 12	up to 12 range as bit mask	up to 12

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
STM8	2	0	up to 2	up to 2
Super10	up to 8	up to 8	up to 8	8
TriCore (AUDO-MAX, AURIX)	up to 8	up to 8 single address or up to 4 ranges	up to 8 single address or up to 4 ranges	—
TriCore (up to AUDO-FG)	up to 4 instruction up to 4 read/write	up to 4 single address or up to 2 ranges	up to 4 single address or up to 2 ranges	—
V850E1	2 4 or 8 instruction (onchip flash only)	4 or 8 single address 2 single address or 1 range	2 single address or 1 range	2
V850E2	4 8 instruction (onchip flash only)	8 single address 4 range as bit mask	4 range as bit mask	4
x86/x64	4	4 single address	4 Write or Read/Write single address or ranges of 2, 4 or 8 bytes (aligned)	—
XC2000/XE16x	4	up to 4	up to 4 write up to 1 read	up to 4 write up to 1 read
XC800	4	up to 4 up to 1 range (2 single needed)	up to 1 single address read or address range up to 1 single address write or address range	—
XSCALE	2 instruction/ 2 read/write	2 single address	2 single address or 1 range as bit mask	—

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoints	Data Value Breakpoints
APEX	4	4 single address	—	—
Blackfin	6 instruction 2 read/write	6 single address or 3 ranges	2 single address or 1 range	—
CEVA-X	4 instruction 4 read/write	4 single address	4 single address or range	2
DSP56K 56k/56300/56 800 56100	2 1	2 1	2 1	—
DSP 56300 56800E	2	up to 2 single address	up to 1 single address	—
MMDSP	2 instruction 1 read/write	2 single address	1 single address	1
OAK TeakLite TeakLite II Teak	3 instruction 1 read/write	3 single address	1 single address or range as bit mask	1
StarCore	12	up to 12 single address or up to 6 ranges	up to 6 single address or up to 3 ranges	1
STN8810 STN8815 STN8820	2	up to 2	up to 2	1
STRED	4 instruction 1 read/write	4 single address	1 range as bit mask break before make ReadWrite only	—
TeakLite III	2 instruction 1 read/write	2 single address	2 single address or 1 range	1
TMS320 C28x	2	2 single address	—	—
TMS320 C54x	2	2 single address	—	—
TMS320 C55x	4	up to 4 single address	up to 3 data, 1 breakpoint range and 2 bit masks	up to 3
TMS320 C62x	1	1 single address	—	—

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoints	Data Value Breakpoints
TMS320 C64x	up to 4	up to 4 single address	—	—
TMS320 C67x	1	1 single address	—	—
ZSP400	—	—	—	—
ZSP500	4	up to 4 single address	up to 1 range as bit mask	1

Softcores

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
MicroBlaze	0 ... 4 instruction 0 ... 4 read/write	0 ... 4 range as bit mask	0 ... 4 range as bit mask	—
NIOS2	0/4/8 (configurable)	up to 4	up to 4 single address or 2 ranges	up to 4

Configurable Cores

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
ARC 600/700	0/2/4/8	up to 0/2/4/8 range as bit mask	up to 0/2/4/8 range as bit mask	up to 0/1/2/4 only writes, only in "full" mode
ARC-EM				range as bit mask
ARC tangent-A4	0/2/4/8	up to 0/2/4/8 range requires 2 breakpoints	up to 0/2/4/8 write only range requires 2 breakpoints	up to 0/1/2/4 only writes, only in "full" mode
ARC tangent-A5				range requires 2 breakpoints
Beyond BA22	up to 8	up to 8 range requires 2 breakpoints	up to 8 range requires 2 breakpoints	up to 8 range requires 2 breakpoints

Family	Onchip Breakpoints	Program Breakpoints	Read/Write Breakpoint	Data Value Breakpoints
Diamond Cores	2	up to 2 range as bit mask	up to 2 range as bit mask	2
M8051EW	0, 1, 2 or 4	up to 4	up to 4 single addresses for read or write range requires 2 breakpoints or 2 single address read/write, max 1 read/write range	same as read/write breakpoints

ETM breakpoints extend the number of available breakpoints. Some Onchip breakpoints offered by ARM and Cortex-A/R cores provide restricted functionality. ETM breakpoints can help you to overcome some of these restrictions.

ETM breakpoints always show a break-after-make behavior with a rather large delay. Thus, use ETM breakpoints only if necessary.

	Program Breakpoints	Read/Write Breakpoints	Data Value Breakpoints
ARM7 ARM9	Onchip breakpoints: up to 2, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: up to 2, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip Breakpoint: up to 2, but address range only as bit mask ETM breakpoints: up to 2 data value breakpoints for exact address ranges
ARM11	Onchip breakpoints: 6, but only single addresses ETM breakpoints: up to 2 exact address ranges possible	Onchip breakpoints: 2, but only single addresses ETM breakpoints: up to 2 exact address ranges possible	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: up to 2 data value breakpoints for exact address ranges
Cortex-A5	Onchip breakpoints: 3, but only single addresses ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: 2, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: up to 2 data value breakpoints for exact address ranges
Cortex-A7 Cortex-R7	Onchip breakpoints: 6, but only single addresses ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: 4, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: up to 2 data value breakpoints for exact address ranges
Cortex-A8	Onchip breakpoints: 6, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: 2, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: up to 2 data value breakpoints for exact address ranges

	Program Breakpoints	Read/Write Breakpoints	Data Value Breakpoints
Cortex-R4 Cortex-R5	Onchip breakpoints: 2..8, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: 1..8, but address range only as bit mask ETM breakpoints: up to 2 exact address ranges	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: up to 2 data value breakpoints for exact address ranges
Cortex-A9 Cortex-A15 Cortex-A17	Onchip breakpoints: 6, but only single addresses ETM breakpoints: 2 exact address ranges	Onchip breakpoints: 4, but address range only as bit mask ETM breakpoints: —	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: —
Cortex-A32 Cortex-A35 Cortex-A53 Cortex-A57 Cortex-A72 Cortex-A73	Onchip breakpoints: 6, but only single addresses ETM breakpoints: 2 exact address ranges <small>(more on request)</small>	Onchip breakpoints: 4, but address range only as bit mask ETM breakpoints: —	Onchip breakpoints: no data value breakpoints possible ETM breakpoints: —

No ETM breakpoints are available for the Cortex-M family.

Please refer to the description of the **ETM.StoppingBreakPoints** command, if you want to use the ETM breakpoints.

Breakpoint Types

TRACE32 PowerView provides the following breakpoint types for standard debugging.

Breakpoint Types	Possible Implementations
Program	Software (Default) Onchip
Read, Write, ReadWrite	Onchip (Default)

Program Breakpoints

Set a Program breakpoint by a left mouse double-click to the instruction

```
[B::List]
Step Over Diverge Return Up Go Break Mode
addr/line source
674 { if ( flags[ i ] )
676     primz = i + i + 3;
677     k = i + primz;
678     while ( k <= SIZE )
680     {
681         flags[ k ] = FALSE;
682         k += primz;
683     }
684     anzahl++;
685 }
686 return anzahl;
687 }
```

The **red program breakpoint indicator** marks all code lines for which a Program breakpoint is set.

The program stops before the instruction marked by the breakpoint is executed (break before make).

Disable the Program breakpoint by a left mouse double-click to the red program breakpoint indicator.
The program breakpoint indicator becomes grey.

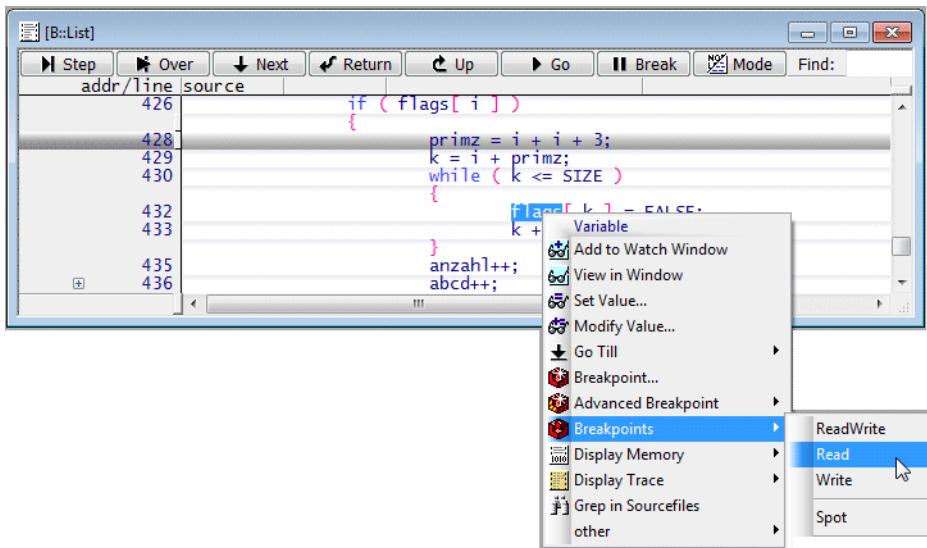
```
[B::List]
Step Over Next Return Up Go Break Mode
addr/line code Label mnemonic comment
426 { if ( flags[ i ] )
NSR:4A326590 E7DC1002 ldrb r1,[r12,+r2]
NSR:4A326594 E3510000 cmp r1,#0x0 ; r1,#0
NSR:4A326598 0A000016 beq 0xA3265F8
428 {
NSR:4A32659C E1A01082 lsl r1,r2,#0x1 ; r1,i,#1
NSR:4A3265A0 E2813003 add r3,r1,#0x3 ; r3,r1,#3
429 NSR:4A3265A4 E0821003 add r1,r2,r3 ; r1,i,primz
register int i, primz, k;
int anzahl;
```

Break.Set <address> /Program [/DISABLE]

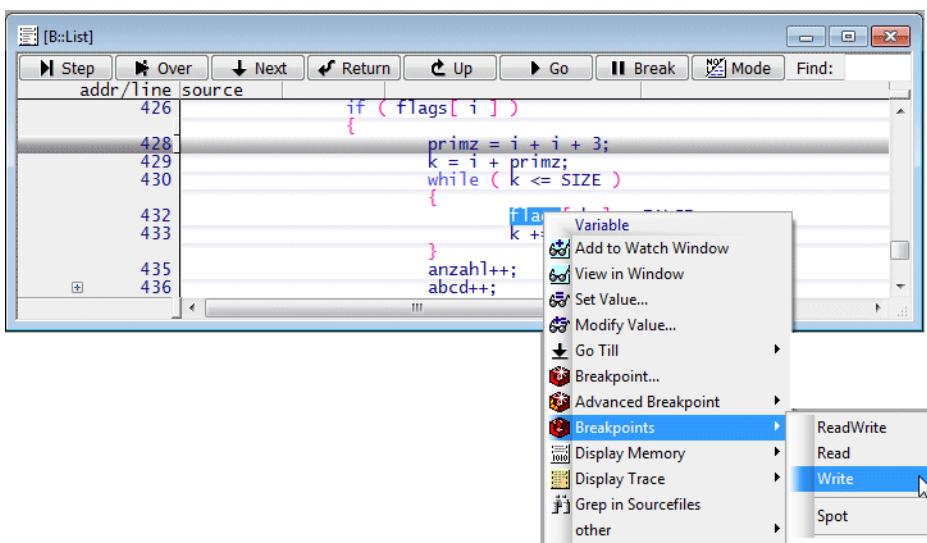
Set a Program breakpoint to the specified address.
The Program breakpoint can be disabled if required.

```
Break.Set 0xA34f /Program ; set a Program breakpoint to  
; address 0xA34f  
  
Break.Set func1 /Program ; set a Program breakpoint to the  
; entry of func1  
; (first address of function func1)  
  
Break.Set func1+0x1c /Program ; set a Program breakpoint to the  
; instruction at address  
; func1 plus 28 bytes  
; (assuming that byte is the  
; smallest addressable unit)  
  
Break.Set func11\7 ; set a Program breakpoint to the  
; 7th line of code of the function  
; func11  
; (line in compiled program)  
  
Break.Set func17 /Program /DISable ; set a Program breakpoint to the  
; entry of func17  
; disable Program breakpoint  
  
Break.List ; list all breakpoints
```

Read/Write Breakpoints

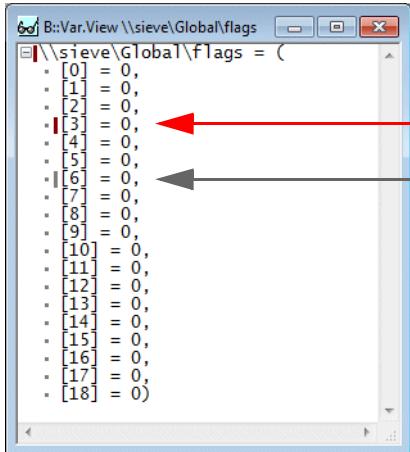


Core stops at
a read access
to the variable



Core stops at
a write access
to the variable

On most core(s) the program stops after the read or write access (break after make).



If an HLL variable is displayed, a small **red breakpoint indicator** marks an active Read/Write breakpoint.

A small **grey breakpoint indicator** marks a disabled Read/Write breakpoint.

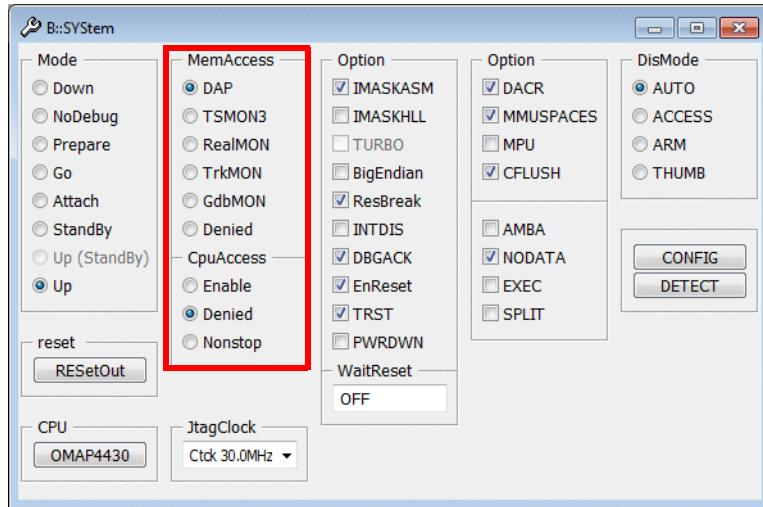
```
Break.Set <address> | <range> /Read | /Write | /ReadWrite [/DISable]
```

; allow HLL expression to specify breakpoint

```
Var.Break.Set <hll_expression> /Read | /Write | /ReadWrite [/DISable]
```

```
Break.Set 0xB56 /Read  
Break.Set ast /Write  
Break.Set vpchar+5 /ReadWrite /DISable  
Var.Break.Set flags /Write  
Var.Break.Set flags[3] /Read  
Var.Break.Set ast->count /ReadWrite /DISable  
Break.List
```

Breakpoint Setting at Run-time



Software breakpoints

- If **MemAccess** CPU/NEXUS/DAP is enabled, Software breakpoints can be set while the core(s) is executing the program. Please be aware that this is not possible if an instruction cache and an MMU is used.
- If **CpuAccess** is enabled, Software breakpoints can be set while the core(s) is executing the program. If the breakpoint is set via CpuAccess the real-time behavior is influenced.
- If **MemAccess** and **CpuAccess** is Denied Software breakpoints can only be set when the program execution is stopped.

The behavior of **Onchip breakpoints** is core dependent. E.g. on all ARM/Cortex cores Onchip breakpoints can be set while the program execution is running.

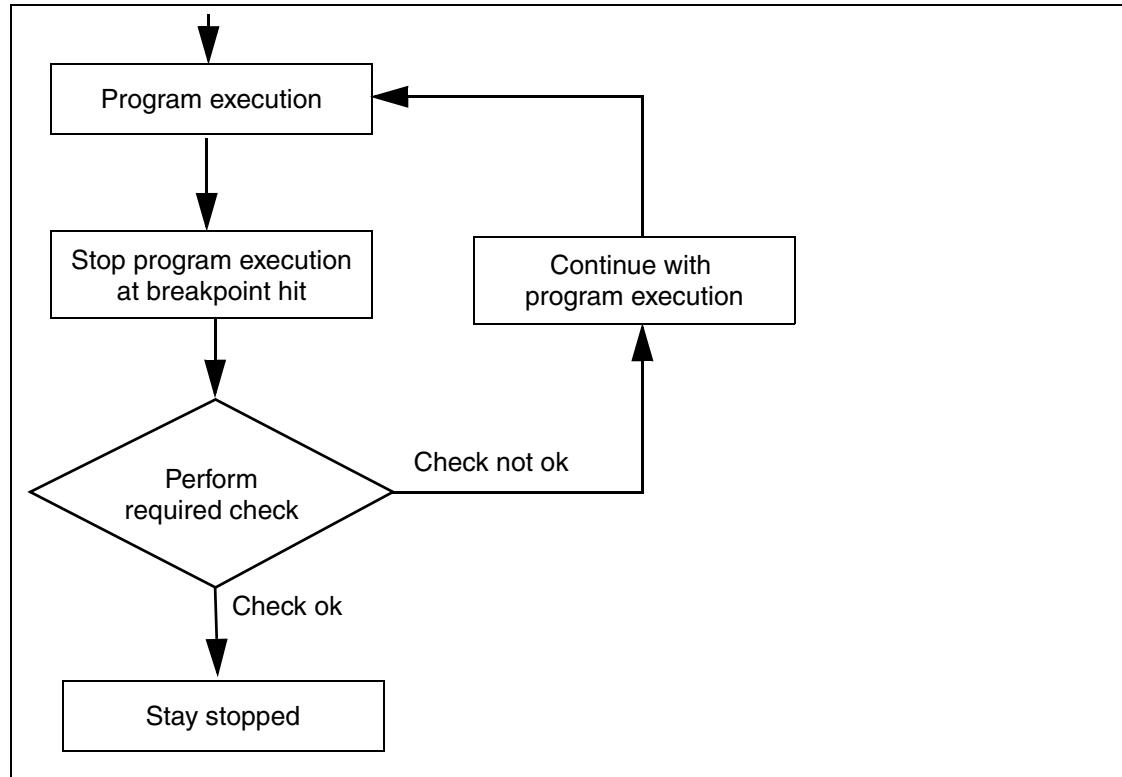
Real-time Breakpoints vs. Intrusive Breakpoints

TRACE32 PowerView offers in addition to the basic breakpoints (Program/Read/Write) also complex breakpoints. Whenever possible these breakpoints are implemented as real-time breakpoints.

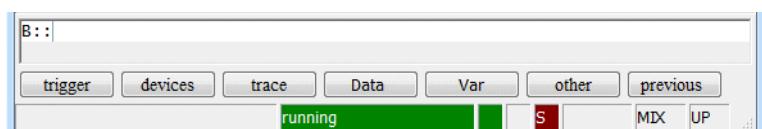
Real-time breakpoints do not disturb the real-time program execution on the core(s), but they require a complex on-chip break logic.

If the on-chip break logic of a core does not provide the required features or if Software breakpoints are used, TRACE32 has to implement an intrusive breakpoint.

Intrusive breakpoint perform as follows:



Each stop to perform the check suspends the program execution for at least 1 ms. For details refer to "["StopAndGo Mode"](#)" (glossary.pdf)



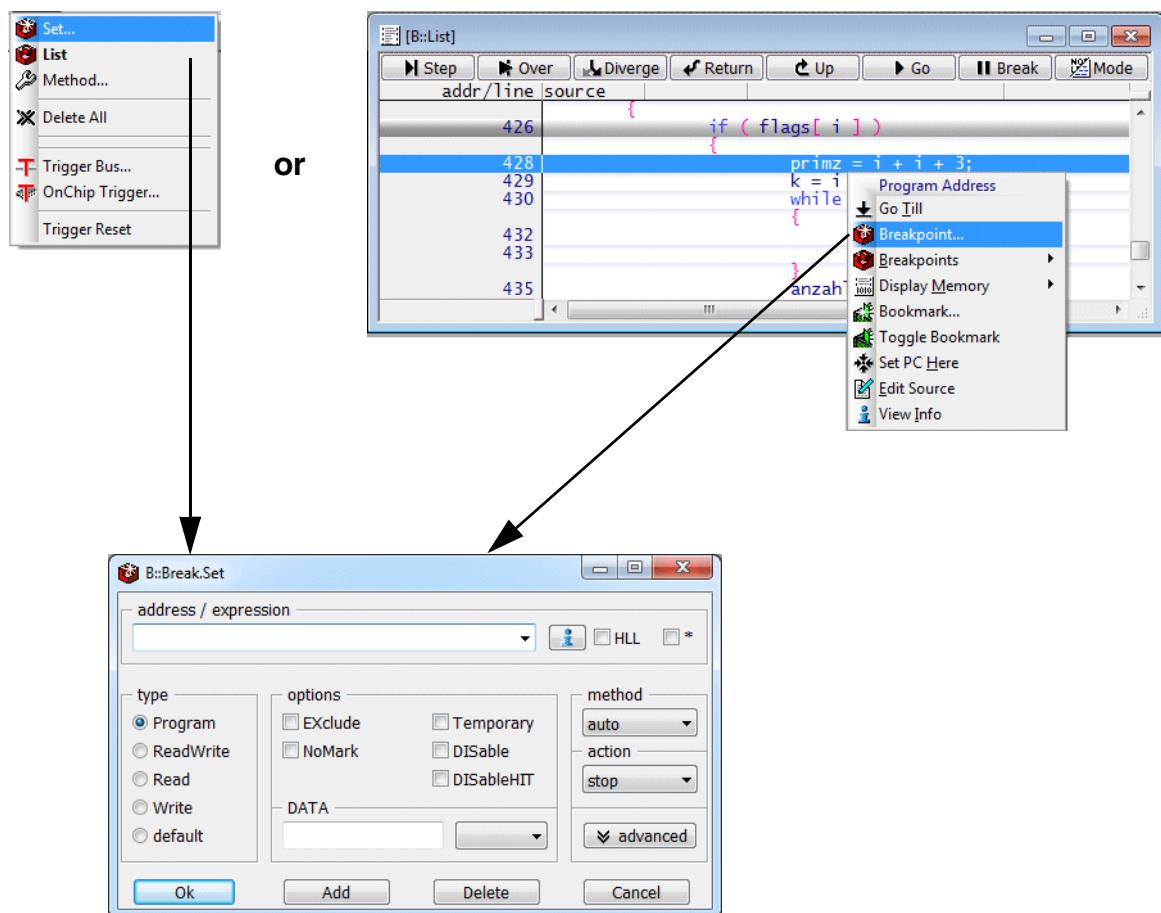
The (short-time) display of a red S in the state line indicates that an intrusive breakpoint was hit.

Intrusive breakpoints are marked with a special breakpoint indicator:



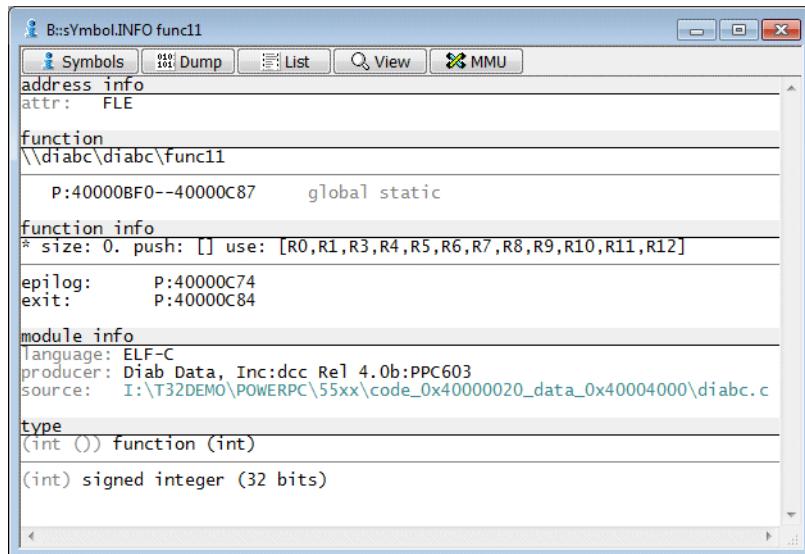
Break.Set Dialog Box

There are two standard ways to open a **Break.Set** dialog.



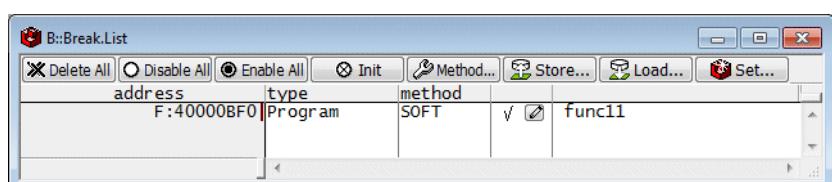
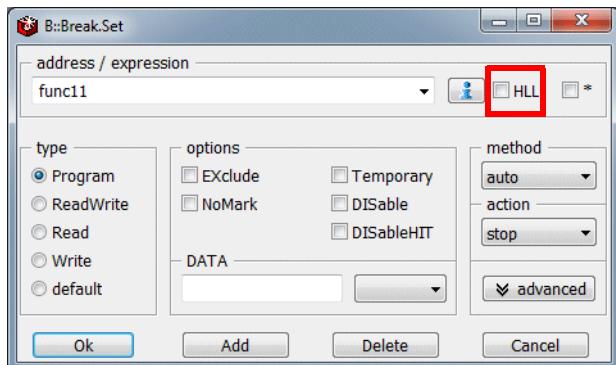
The HLL Check Box - Function Name

```
sYmbol.INFO func11 ; display symbol information  
; for function func11
```



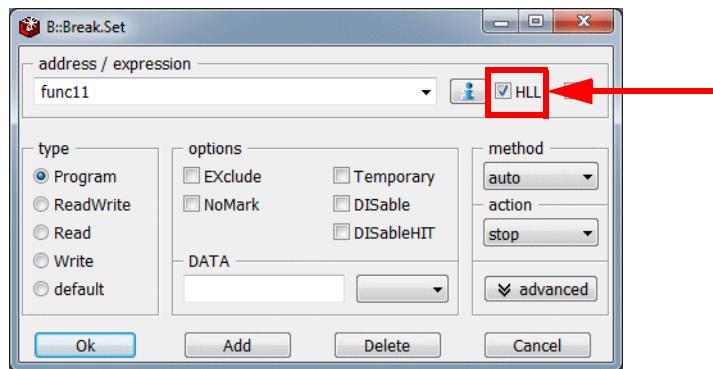
Function Name/HLL Check Box OFF

Program breakpoint is set to the function entry (first address of the function).



Break.Set func11

- If the on-chip break logic supports ranges for Program breakpoints, a Program breakpoint implemented as Onchip is set to the full address range covered by the function.
- If the on-chip break logic provides only bitmasks to realizes breakpoints on instruction ranges, a Program breakpoint implemented as Onchip is set by using the smallest bitmask that covers the complete address range of the function.
- otherwise this breakpoint is rejected with an error message.

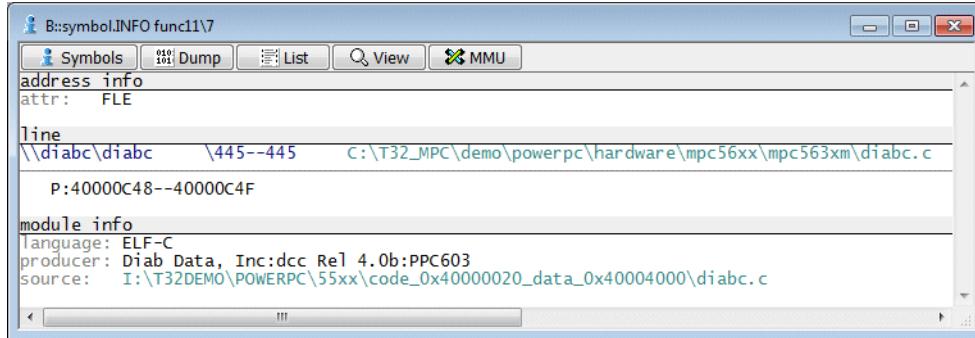


B::Break.List			
address	type	method	
F:40000BF0--40000C87	Program	ONCHIP	✓ <input type="checkbox"/> func11

```
Var.Break.Set func11
```

The HLL Check Box - Program Line Number

```
sYmbol.INFO func11\7 ; display debug information  
; for 7th program line in  
; function func11
```



Program Line Number/HLL Check Box OFF

Program breakpoint is set to the first assembler instruction generated for the program line number.

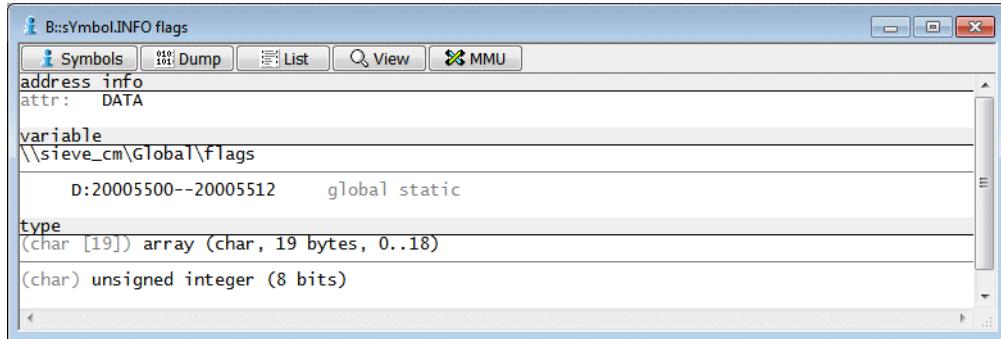
The B::Break.Set dialog shows a search field with 'func11\7' and an unchecked 'HLL' checkbox highlighted with a red box. The B::Break.List table shows a single entry for address F:40000C48, type Program, method SOFT, and condition func11\7.

address	type	method
F:40000C48	Program	SOFT

```
Break.Set func11\7
```

The HLL Check Box - Variable

```
sYmbol.INFO flags ; display symbol information  
; for variable flags
```



Variable/HLL Check Box OFF

Selected breakpoint (ReadWrite/Read/Write) is set to the start address of the variable.

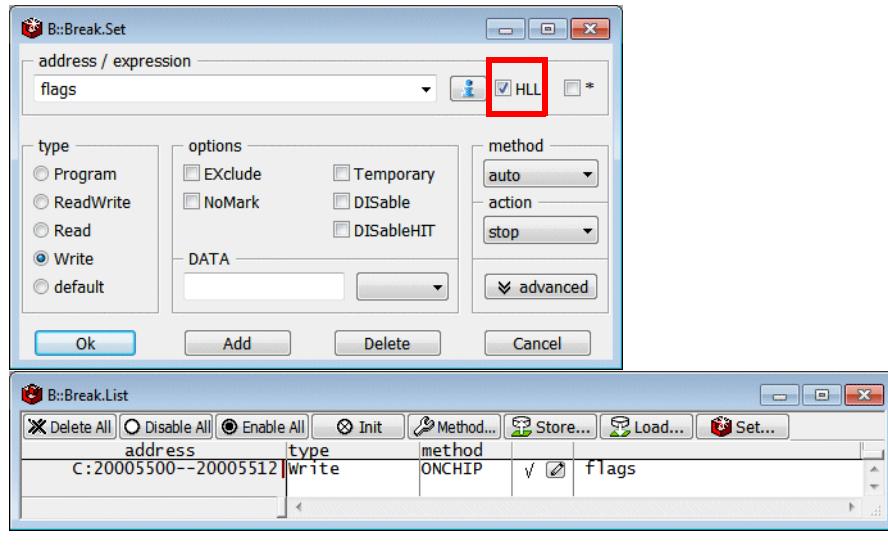
B::Break.Set
address / expression: flags
type: Write
options: EXclude, NoMark, DATA
method: auto, action: stop
Buttons: Ok, Add, Delete, Cancel

B::Break.List
address: C:20005500, type: Write, method: ONCHIP, flags

```
Break.Set flags
```

Variable/HLL Check Box ON

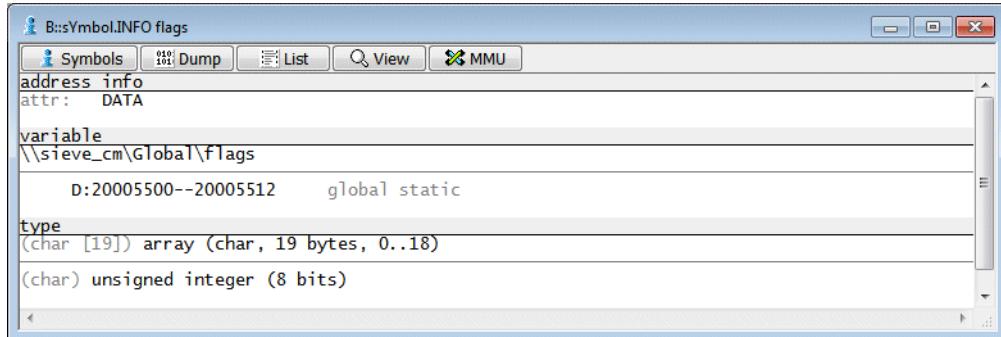
- If the on-chip break logic supports ranges for Read/Write breakpoints, the specified breakpoint is set to the complete address range covered by the variable.
- If the on-chip break logic provides only bitmasks to realizes Read/Write breakpoints on address ranges, the specified breakpoint is set by using the smallest bitmask that covers the address range used by the variable.



```
Var.Break.Set flags
```

The HLL Check Box - HLL Expression

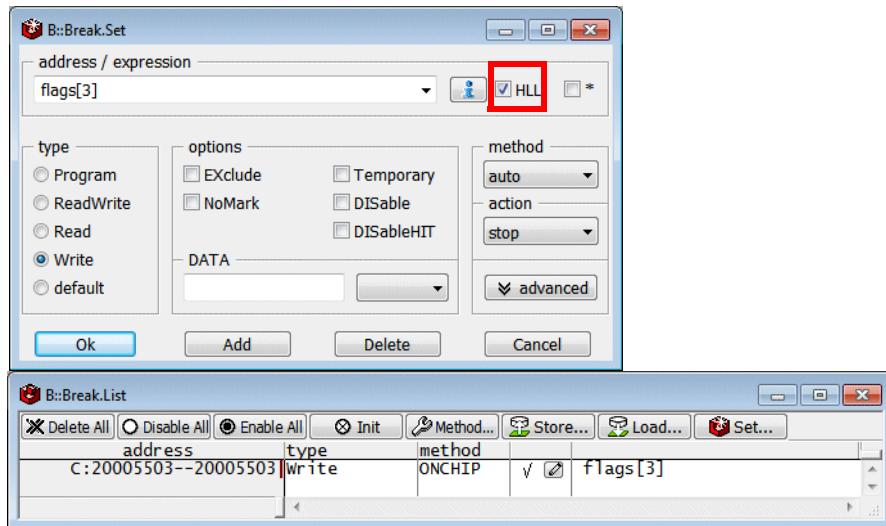
```
sYmbol.INFO flags ; display symbol information  
; for variable flags
```



Variable/HLL Check Box Must Be ON

If you want to use an HLL expression to specify the address range for a Read/Write breakpoint, the HLL check box has to be checked.

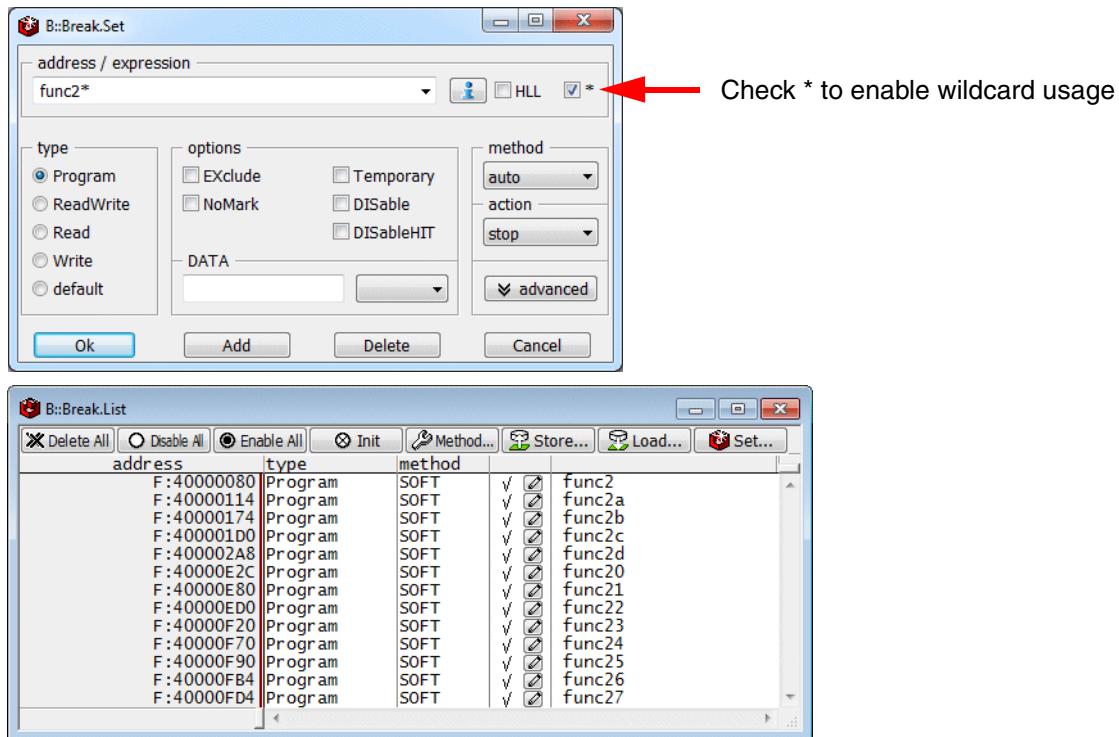
- If the on-chip break logic supports ranges for Read/Write breakpoints, the specified breakpoint is set to the complete address range covered by the HLL expression.
- If the on-chip break logic provides only bitmasks to realizes Read/Write breakpoints on address ranges, the specified breakpoint is set by using the smallest bitmask that covers the address range used by the HLL expression.



```
Var.Break.Set flags[3]
```

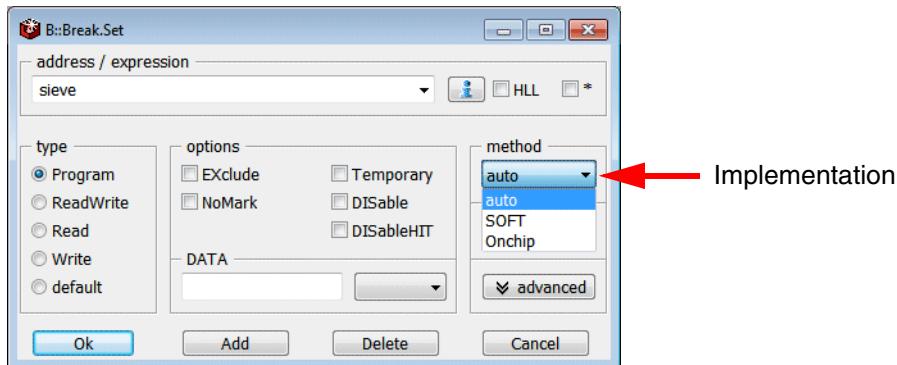
Allow Wildcards in address/expression

Set Program breakpoints the all function that match the defined name pattern.

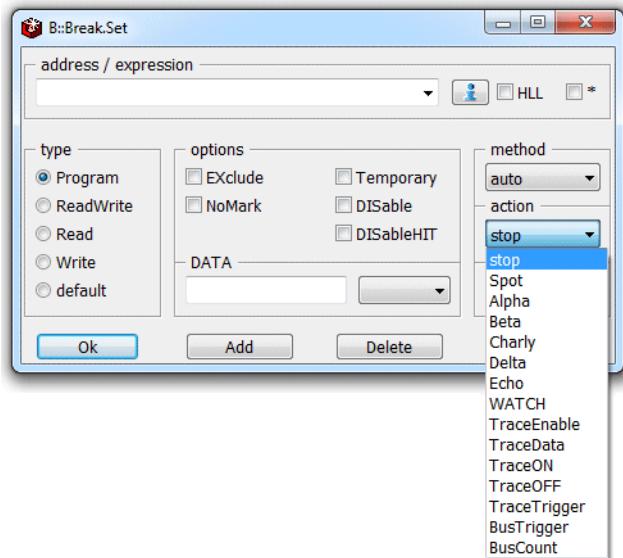


Requires sufficient resources if Onchip breakpoints are used.

```
Break.SetPattern func2*
```



Implementation	
auto	Use breakpoint implementation as predefined in TRACE32 PowerView.
SOFT	Implement breakpoint as Software breakpoint.
Onchip	Implement breakpoint as Onchip breakpoint.



By default the program execution is stopped when a breakpoint is hit (action **stop**). TRACE32 PowerView provides the following additional reactions on a breakpoint hit:

Action (debugger)	
Spot	The program execution is stopped shortly at a breakpoint hit to update the screen. As soon as the screen is updated, the program execution continues.
Alpha	Set an Alpha breakpoint.
Beta	Set a Beta breakpoint.
Charly	Set a Charly breakpoint.
Delta	Set a Delta breakpoint.
Echo	Set an Echo breakpoint.
WATCH	Trigger the debug pin at the specified event (not available for all processor architectures).

Alpha, Beta, Charly, Delta and Echo breakpoint are only used in very special cases. For this reason no description is given in the general part of the training material.

Action (on-chip or off-chip trace)	
TraceEnable	Advise on-chip trace logic to generate trace information on the specified event.
TraceON	Advise on-chip trace logic to start with the generation of trace information at the specified event.
TraceOFF	Advise on-chip trace logic to stop with the generation of trace information at the specified event.
TraceTrigger	Advise on-chip trace logic to generate a trigger at the specified event. TRACE32 PowerView stops the recording of trace information when a trigger is detected.

A detailed description for the Actions (on-chip and off-chip trace) can be found in the following manuals:

- “[ARM-ETM Training](#)” (training_arm_etm.pdf).
- “[Cortex-M Trace Training](#)” (training_cortexm_etm.pdf).
- “[AURIX Trace Training](#)” (training_aurix_trace.pdf).
- “[Hexagon-ETM Training](#)” (training_hexagon_etm.pdf).
- “[Nexus Training](#)” (training_nexus.pdf).

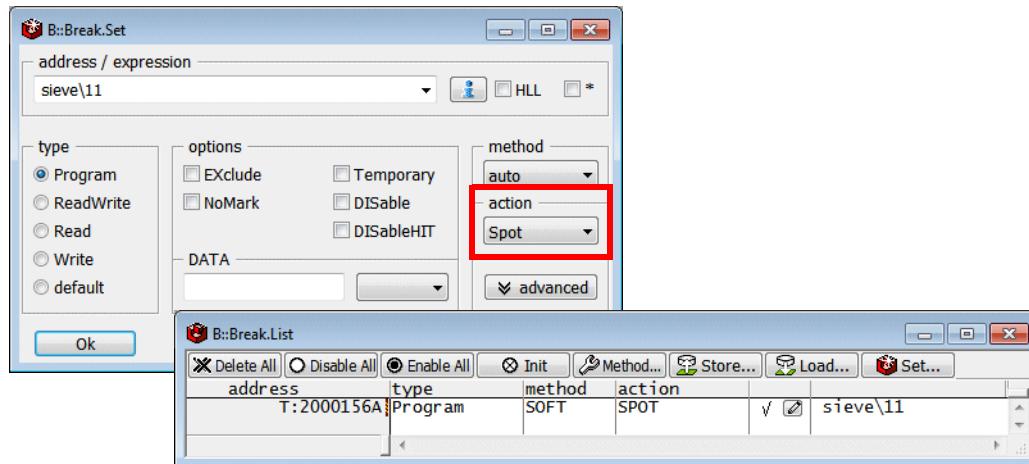
or with the description of the **Break.Set** command.

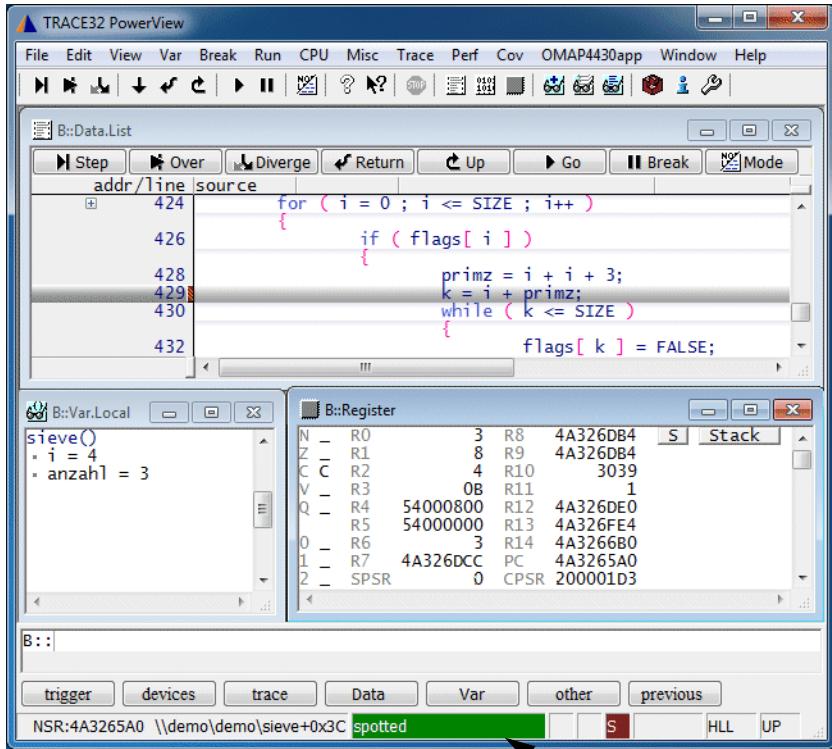
Example for the Action Spot

The information displayed within TRACE32 PowerView is by default only updated, when the core(s) stops the program execution.

The action Spot can be used to turn a breakpoint into a watchpoint. The core stops the program execution at the watchpoint, updates the screen and restarts the program execution automatically. Each stop takes **50 ... 100 ms** depending on the speed of the debug interface and the amount of information displayed on the screen.

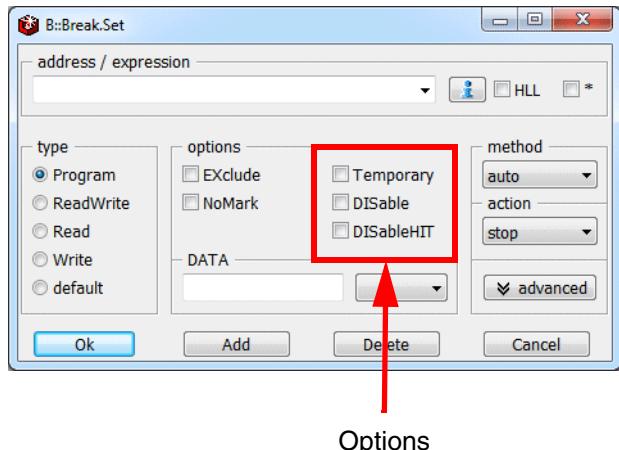
Example: Update the screen whenever the program executes the instruction sieve\11.





```
Break.Set sieve\11 /Spot
```

Options



Options

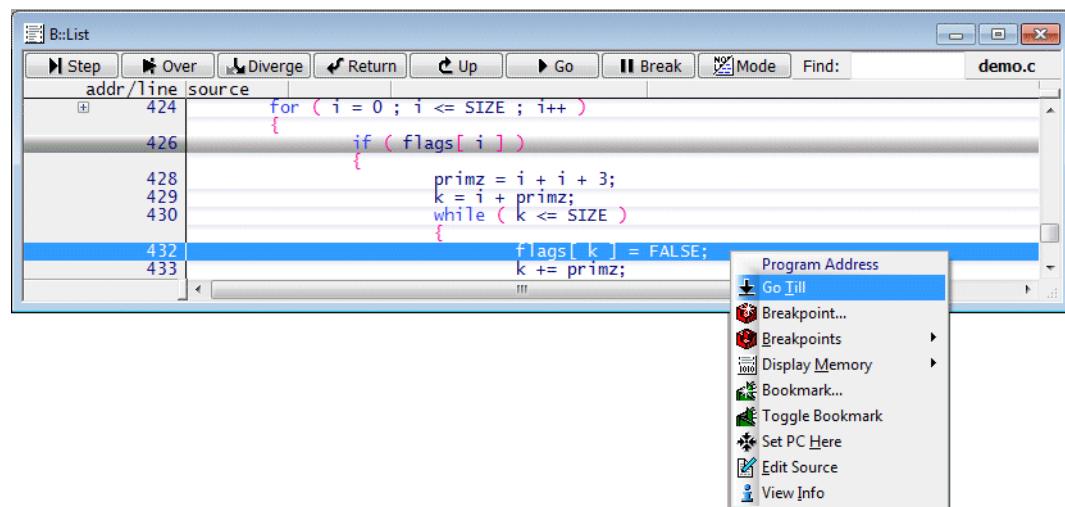
Temporary	OFF: Set a permanent breakpoint (default). ON: Set a temporary breakpoint. All temporary breakpoints are deleted the next time the core(s) stops the program execution.
DISable	OFF: Breakpoint is enabled (default). ON: Set breakpoint, but disabled.
DISableHIT	ON: Disable the breakpoint after the breakpoint was hit.

Example for the Option Temporary

Temporary breakpoints are usually not set via the Break.Set dialog, but they are often used while debugging.

Examples:

- **Go Till**

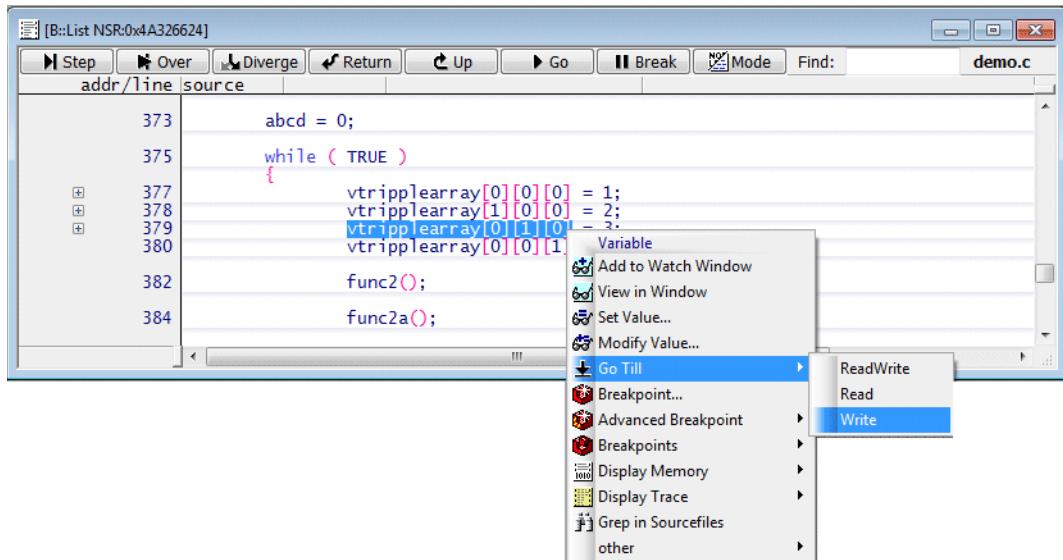


Go <address> [<address> ...]

```
; set a temporary Program breakpoint to
; the entry of the function func4
; and start the program execution
Go func4

; set a temporary Program breakpoints to
; the entries of the functions func4, func8 and func9
; and start the program execution
Go func4 func8 func9
```

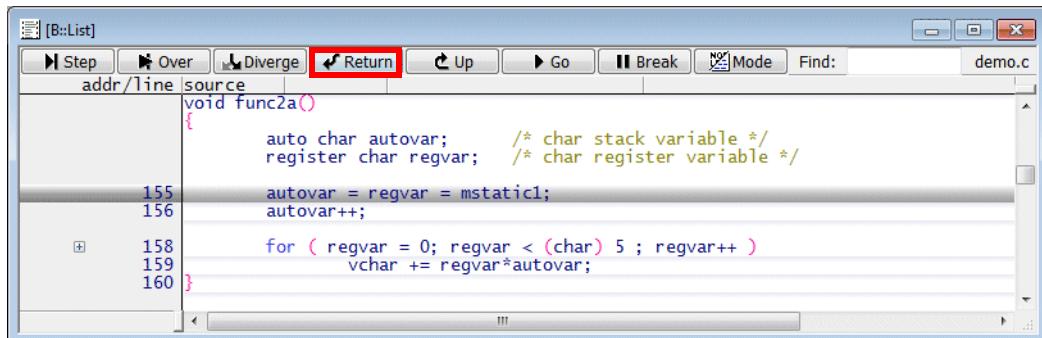
- Go Till -> Write



Var.Go <hl_expression> [/Write]

```
; set a temporary write breakpoint to the variable
; vtripplearray[0][1][0] and start the program execution
Var.Go vtripplearray[0][1][0] /Write
```

- **Go.Return and similar commands**



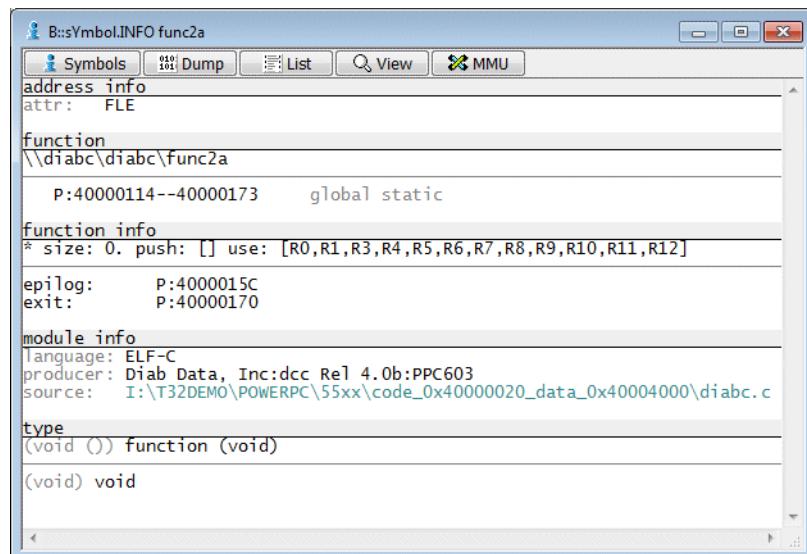
Go.Return

```

; first Go.Return
; set a temporary breakpoint to the start of the function epilogue
; and start the program execution
Go.Return
; stopping at the function epilog first has the advantage that the
; local variables are still valid at this point.

; second Go.Return
; set a temporary breakpoint to the function return
; and start the program execution
Go.Return

```



DATA Breakpoints

The DATA field offers the possibility to combine a Read/Write breakpoint with a specific data value.

- DATA breakpoints are implemented as real-time breakpoints if the core supports **Data Value Breakpoints** (for details on your core refer to “[Onchip Breakpoints by Processor Architecture](#)”, page 76).

TRACE32 PowerView indicates a real-time breakpoints by a full red bar.



TRACE32 PowerView allows inverted data values if this is supported by the on-chip break logic.

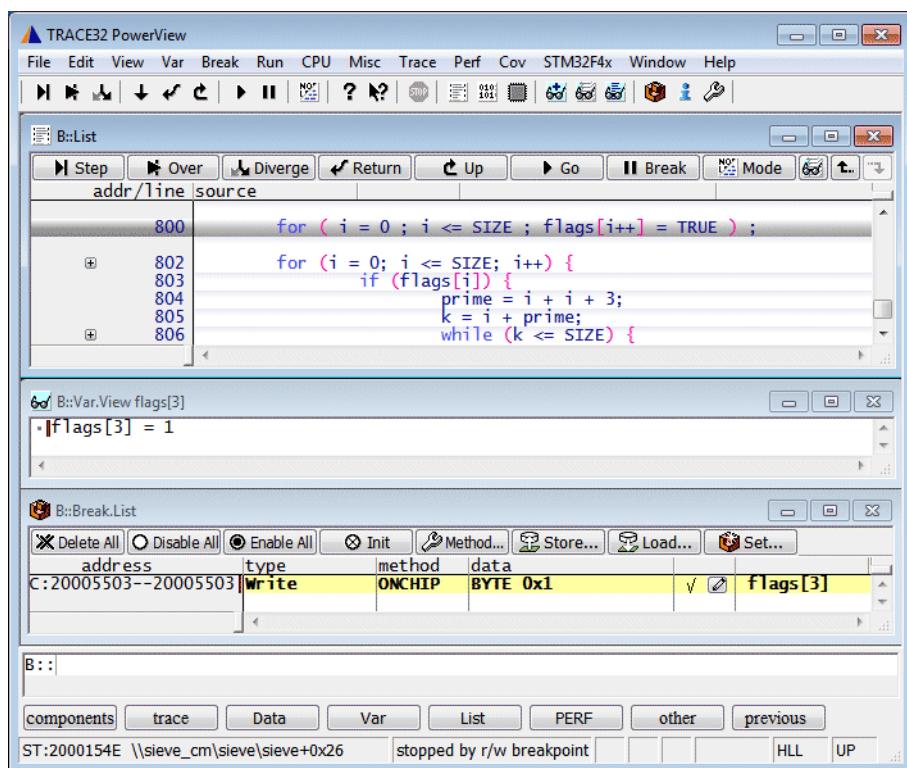
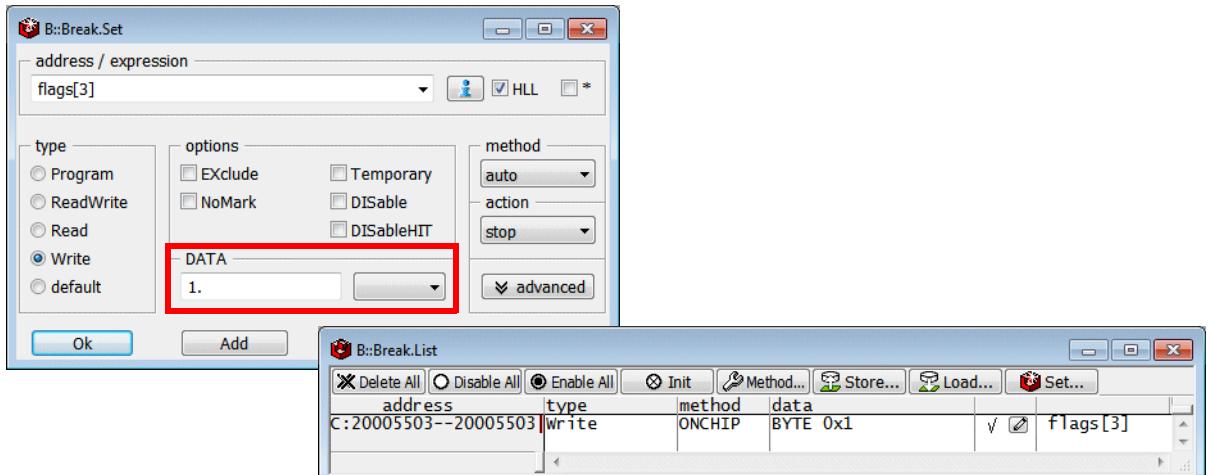
- DATA breakpoints are implemented as intrusive breakpoints if the core does not support Data Value Breakpoints. For details on the intrusive DATA breakpoints refer to the description of the [Break.Set](#) command.

TRACE32 PowerView indicates an intrusive breakpoint by a hatched red bar.



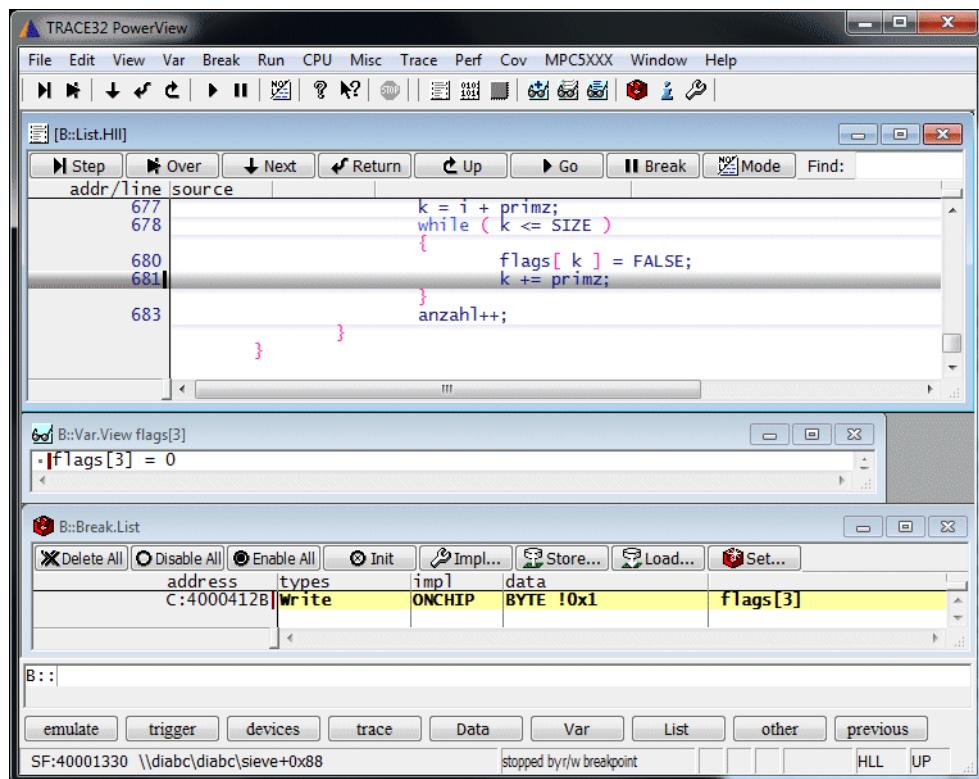
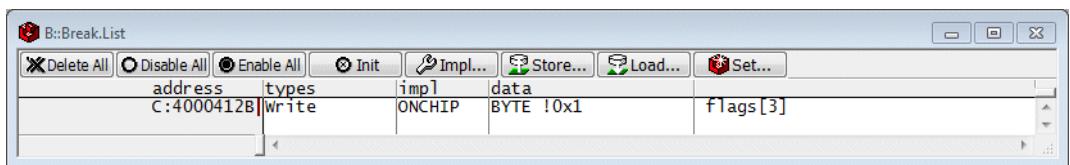
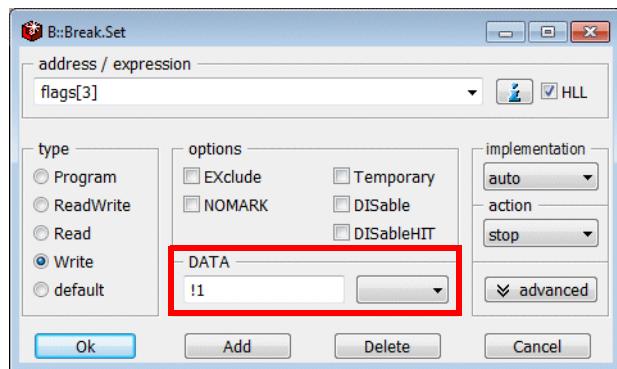
TRACE32 PowerView allows inverted data values for intrusive DATA breakpoints.

Example: Stop the program execution if a 1 is written to flags[3].



```
Var.Break.Set flags[3] /Write /DATA.auto 1.
```

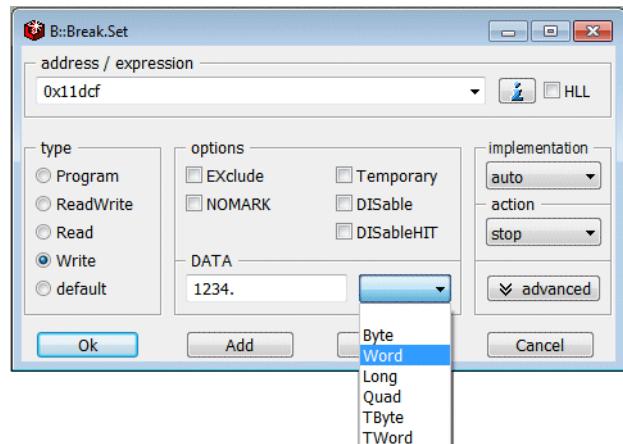
Example: Stop the program execution if another value than 1 is written to flag[3].



```
Var.Break.Set flags[3] /Write /DATA.auto !1.
```

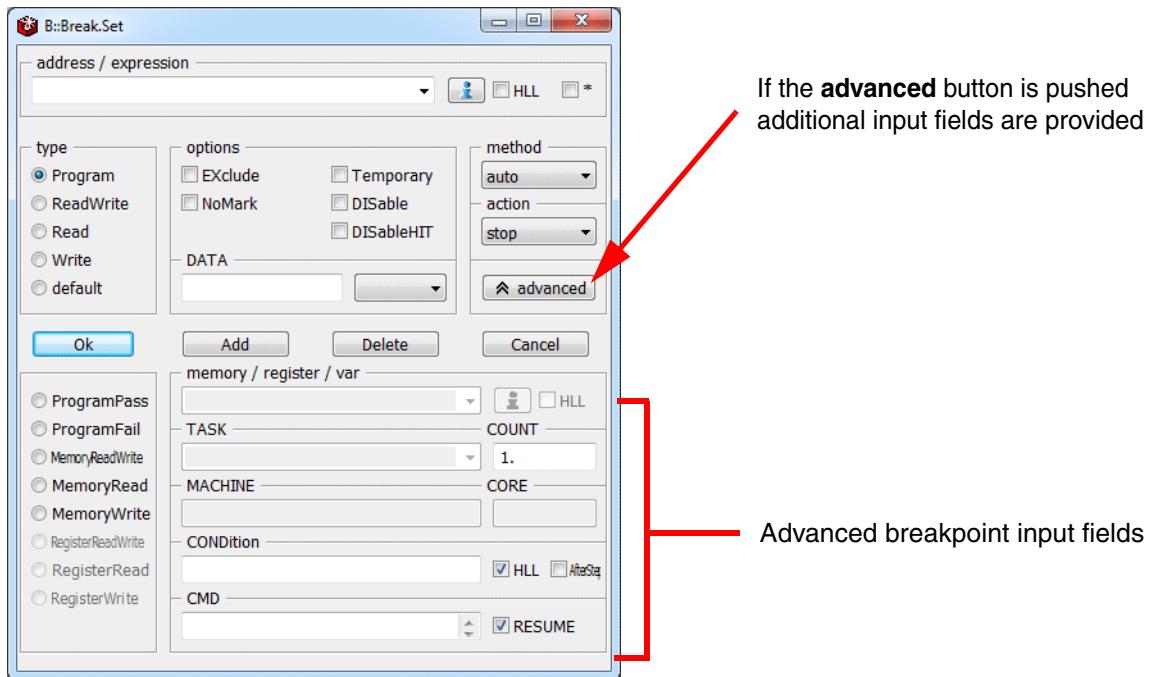
If an HLL expression is used TRACE32 PowerView gets the information if the data is written via a byte, word or long access from the symbol information.

If an address or symbol is used the user has to specify the access width, so that the correct number of bits is compared.



```
Break.Set 0x11dcf /Write /DATA.Word 1234.
```

Advanced Breakpoints



If the **advanced** button is pushed
additional input fields are provided

Advanced breakpoint input fields

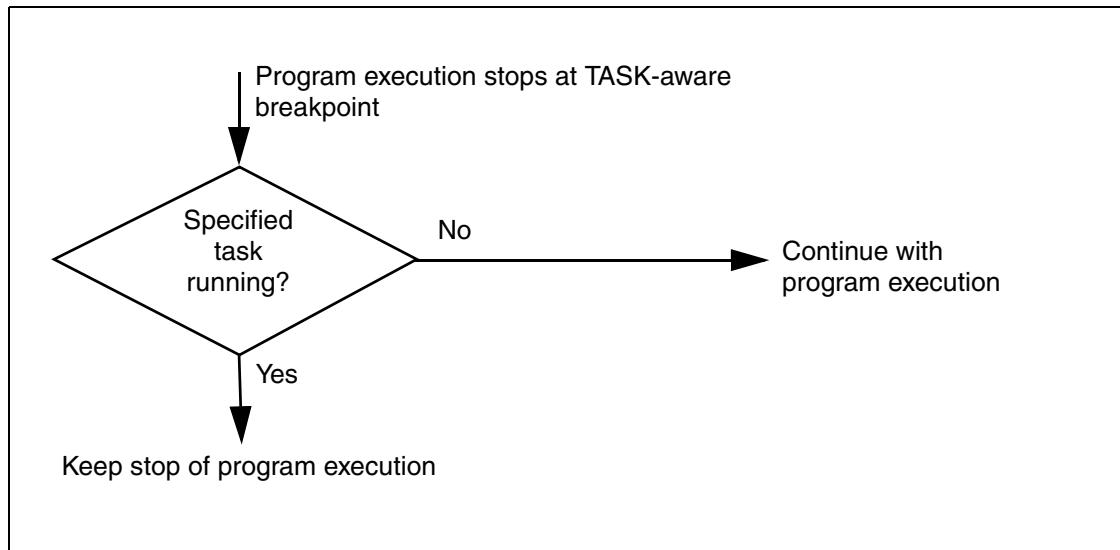
TASK-aware Breakpoints

If OS-aware debugging is configured (refer to “[OS-aware Debugging](#)” in TRACE32 Glossary, page 26 (glossary.pdf)), TASK-aware breakpoints allow to stop the program execution at a breakpoint if the specified task/process is running.

TASK-aware breakpoints are implemented on most cores as intrusive breakpoints. A few cores support real-time TASK-aware breakpoints (e.g. ARM/Cortex). For details on the real-time TASK-aware breakpoints refer to the description of the **Break.Set** command.

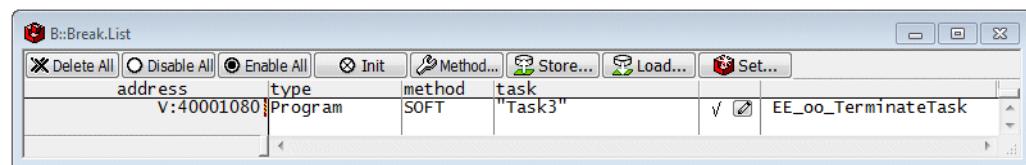
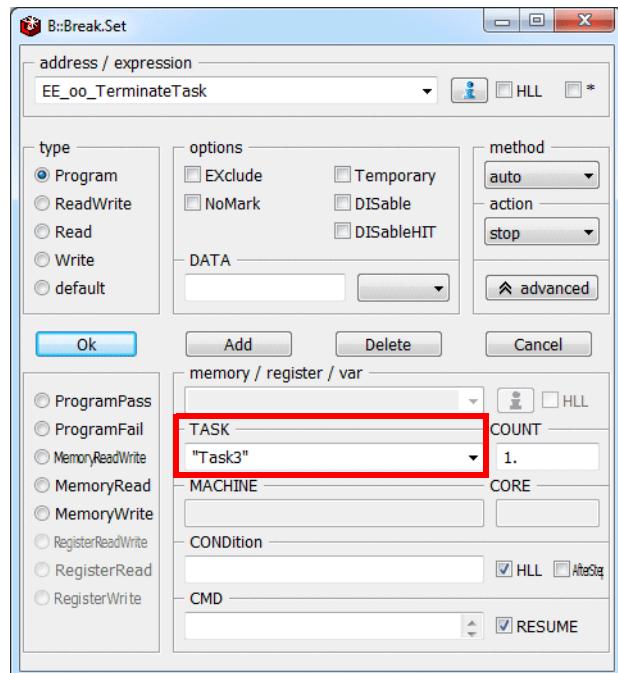
Intrusive TASK-aware Breakpoint

Processing:



Each stop at the TASK-aware breakpoint takes at least 1.ms. This is why the red S is displayed in the TRACE32 PowerView state line whenever the breakpoint is hit.

Example: Stop the program execution at the entry to the function EE_oo_TerminateTask only if the task/process "Task3" is running.



```
Break.Set EE_oo_TerminateTask /Program /TASK "Task3"
```

TRACE32 PowerView

File Edit View Var Break Run CPU Misc Trace Probe Perf Cov MPC5XXX EE_cpu_0 Window Help

B:List.auto

Step	Over	Diverge	Return	Up	Go	Break	Mode	Find
addr/line	code	label	mnemonic	comment				
62	StatusType EE_oo_TerminateTask(void)							
SV:40001080	182106F0 EE_oo_Te..:e_stwu	r1,-0x10(r1) ; r1,-16(r1)						
SV:40001084	0080 se_mflr	r0						
	register EE_FREG np_flags;							
65	EE_ORTI_set_service_in(EE_SERVICETRACE_TERMINATETASK);							
SV:40001086	1C8D8080 e_add16i	r4,r13,-0x7F80 ; r4,r13,-32640						
	...	E_OS_RESOURCE if the task still occupy resources						
		E_OS_CALLLEVEL if called at interrupt level						

B:Break.List

X Delete All	O Disable All	Enable All	Init	Method...	Store...	Load...	Set...	
ress	type	method	task					
V:40001080	Program	SOFT	"(other)"	<input checked="" type="checkbox"/> EE_oo_TerminateTask				

B::

components trace Data Var List PERF SYStem other previous

running S MIX UP

The red S indicates that an intrusive breakpoint is used

TRACE32 PowerView

File Edit View Var Break Run CPU Misc Trace Probe Perf Cov MPC5XXX EE_cpu_0 Window Help

B:List.auto

Step	Over	Diverge	Return	Up	Go	Break	Mode	Find
addr/line	code	label	mnemonic	comment				
62	StatusType EE_oo_TerminateTask(void)							
SV:40001080	182106F0 EE_oo_Te..:e_stwu	r1,-0x10(r1) ; r1,-16(r1)						
SV:40001084	0080 se_mflr	r0						
	register EE_FREG np_flags;							
65	EE_ORTI_set_service_in(EE_SERVICETRACE_TERMINATETASK);							
SV:40001086	1C8D8080 e_add16i	r4,r13,-0x7F80 ; r4,r13,-32640						
	...	E_OS_RESOURCE if the task still occupy resources						
		E_OS_CALLLEVEL if called at interrupt level						

B:Break.List

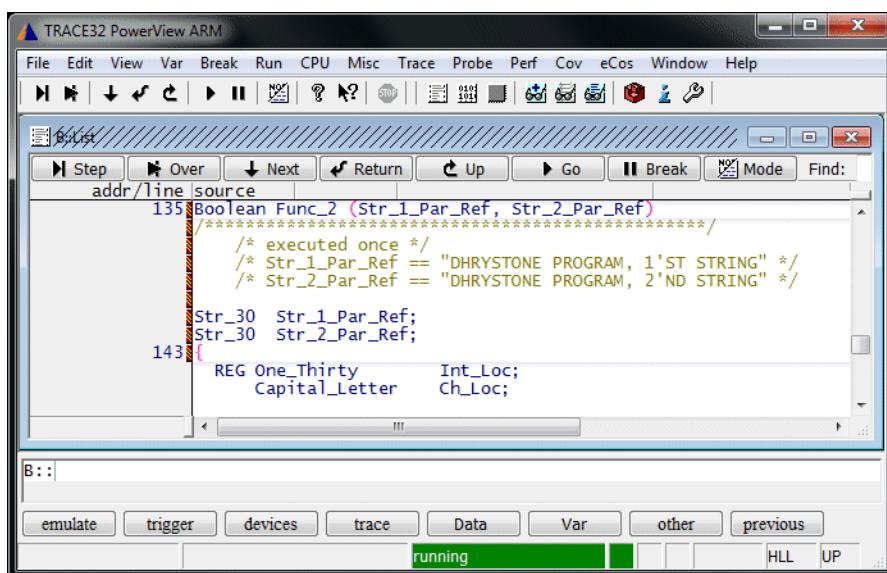
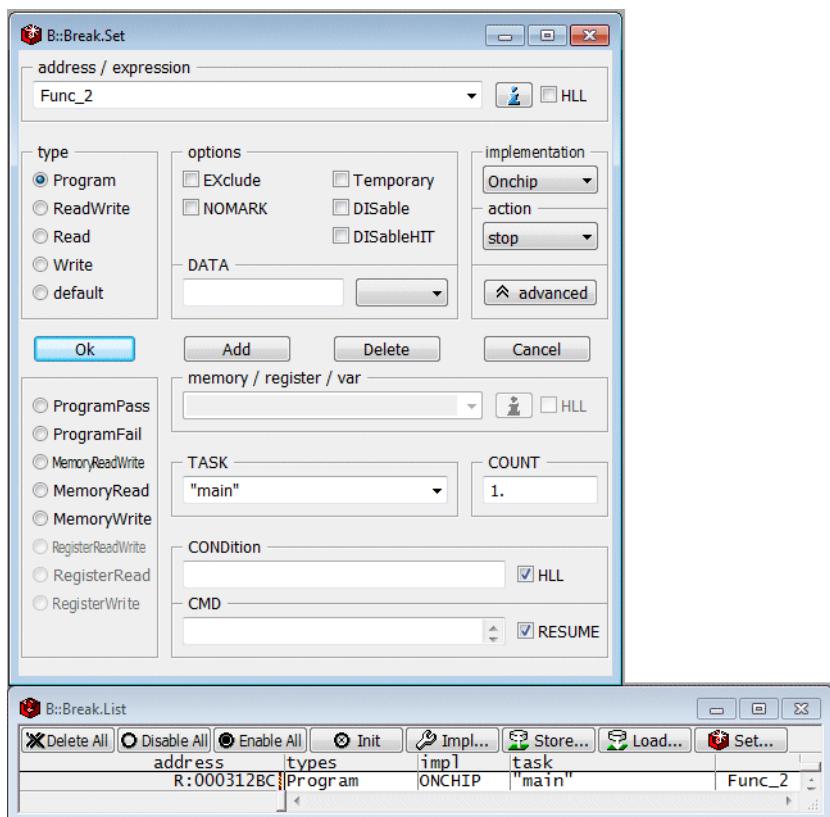
X Delete All	O Disable All	Enable All	Init	Method...	Store...	Load...	Set...	
ress	type	method	task					
V:40001080	Program	SOFT	"(other)"	<input checked="" type="checkbox"/> EE_oo_TerminateTask				

B::

components trace Data Var List PERF SYStem other previous

SV:40001080 \ppcie_terminatE (other) stopped at breakpoint MIX UP

Example for ARM9: Stop the program execution at the entry to the function Func_2 only if the taskF "main" is running (Onchip breakpoint).

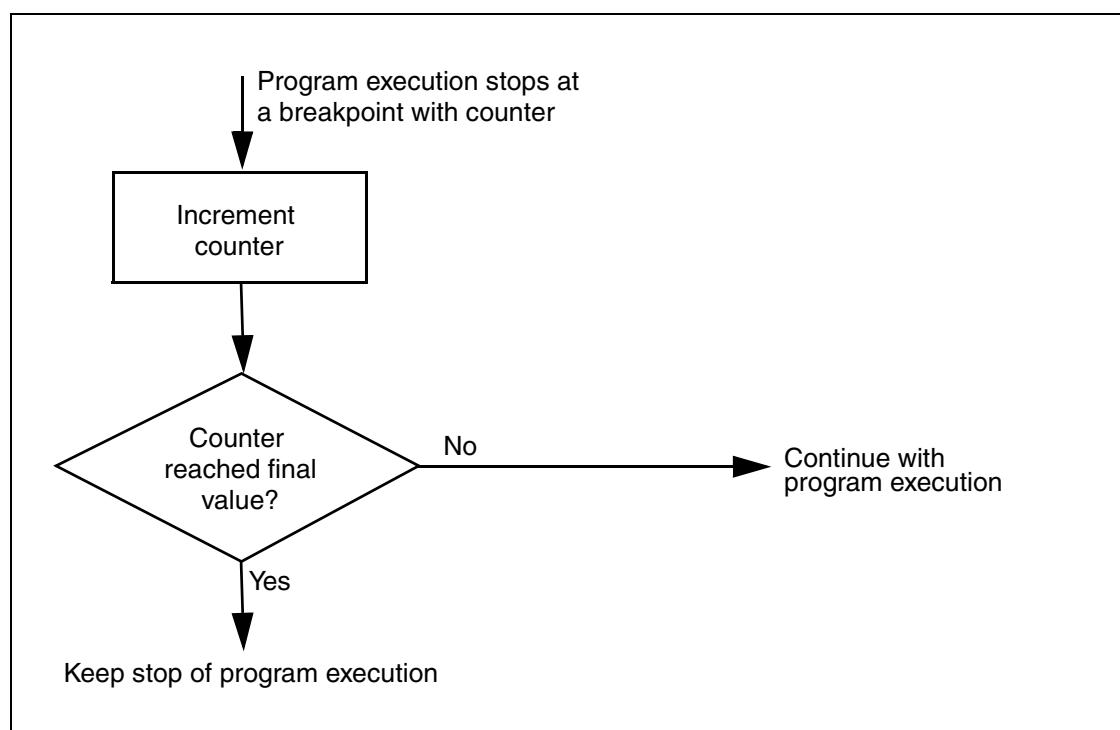


Counters allow to stop the program execution on the *n th* hit of a breakpoint.

Software Counter

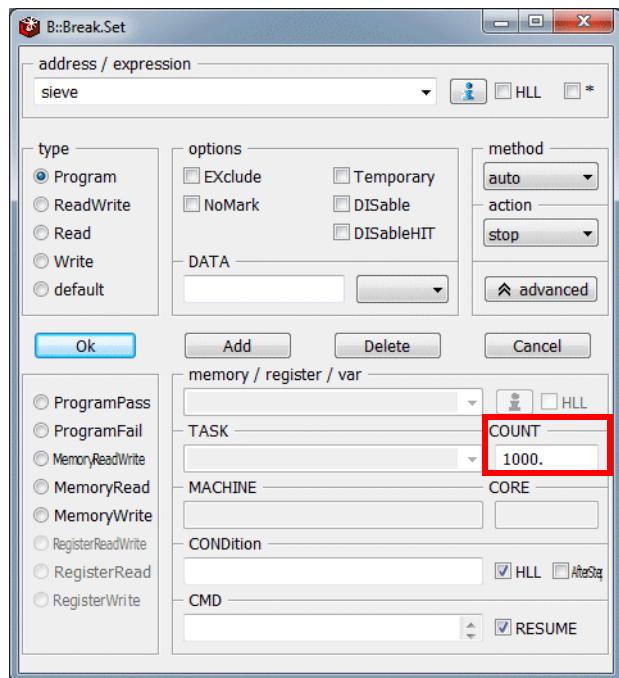
If the on-chip break logic of the core does not provide counters or if a Software breakpoint is used, counters are implemented as software counters.

Processing:



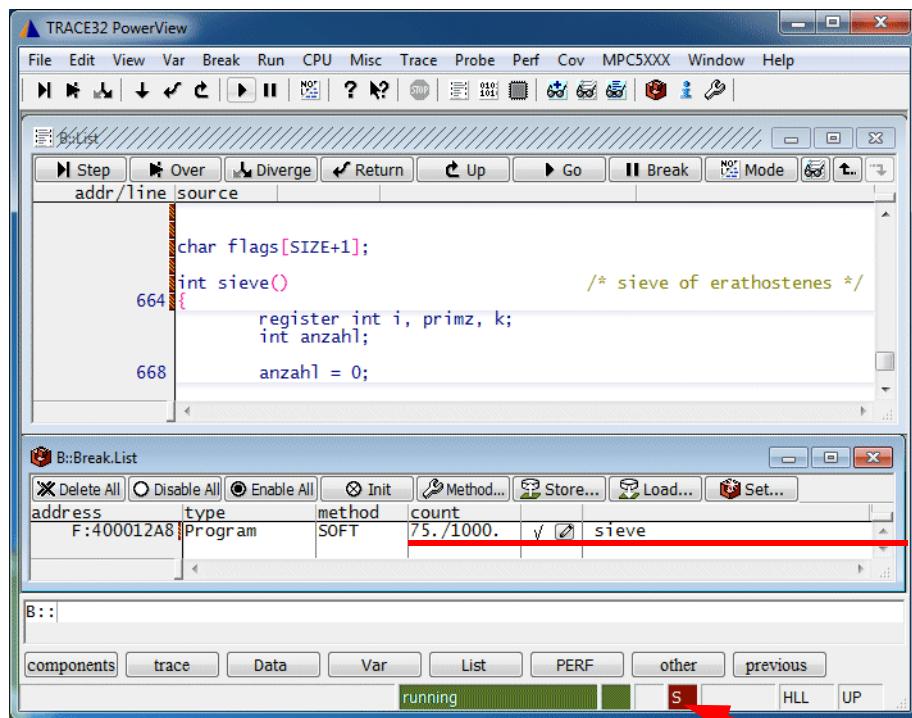
Each stop at a Counter breakpoint takes at least 1.ms. This is why the red S is displayed in the TRACE32 PowerView state line whenever the breakpoint is hit.

Example: Stop the program execution after the function sieve was entered 1000. times.



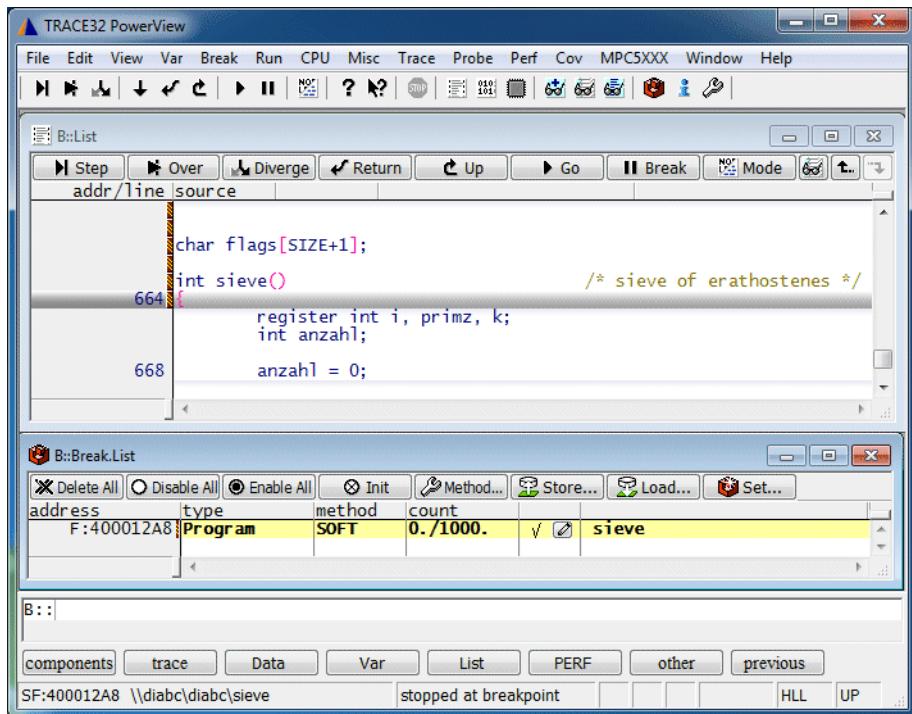
B::Break.List					
address	type	method	count		
F:400012A8	Program	SOFT	0./1000.	✓	<input checked="" type="checkbox"/>
					sieve

```
Break.Set sieve /COUNT 1000.
```



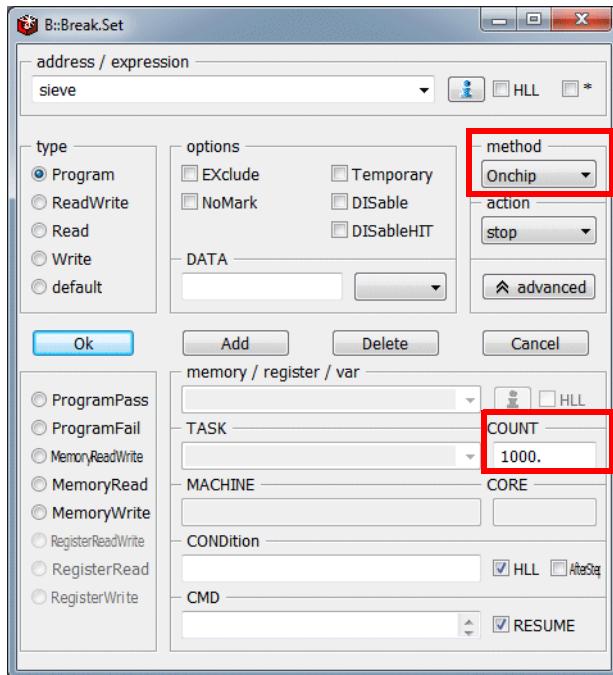
The current counter value is displayed in the **Break.List** window

The red S indicates an intrusive breakpoint



The on-chip break logic of some cores e.g. MPC55xx provides counters. They are used together with Onchip breakpoints.

Example: Stop the program execution after the function sieve was entered 1000. times.



B::Break.List					
address	type	method	count	store	load
F:400012A8	Program	ONCHIP	0./1000.	✓	✗
				sieve	

```
Break.Set sieve /COUNT 1000. /Onchip
```

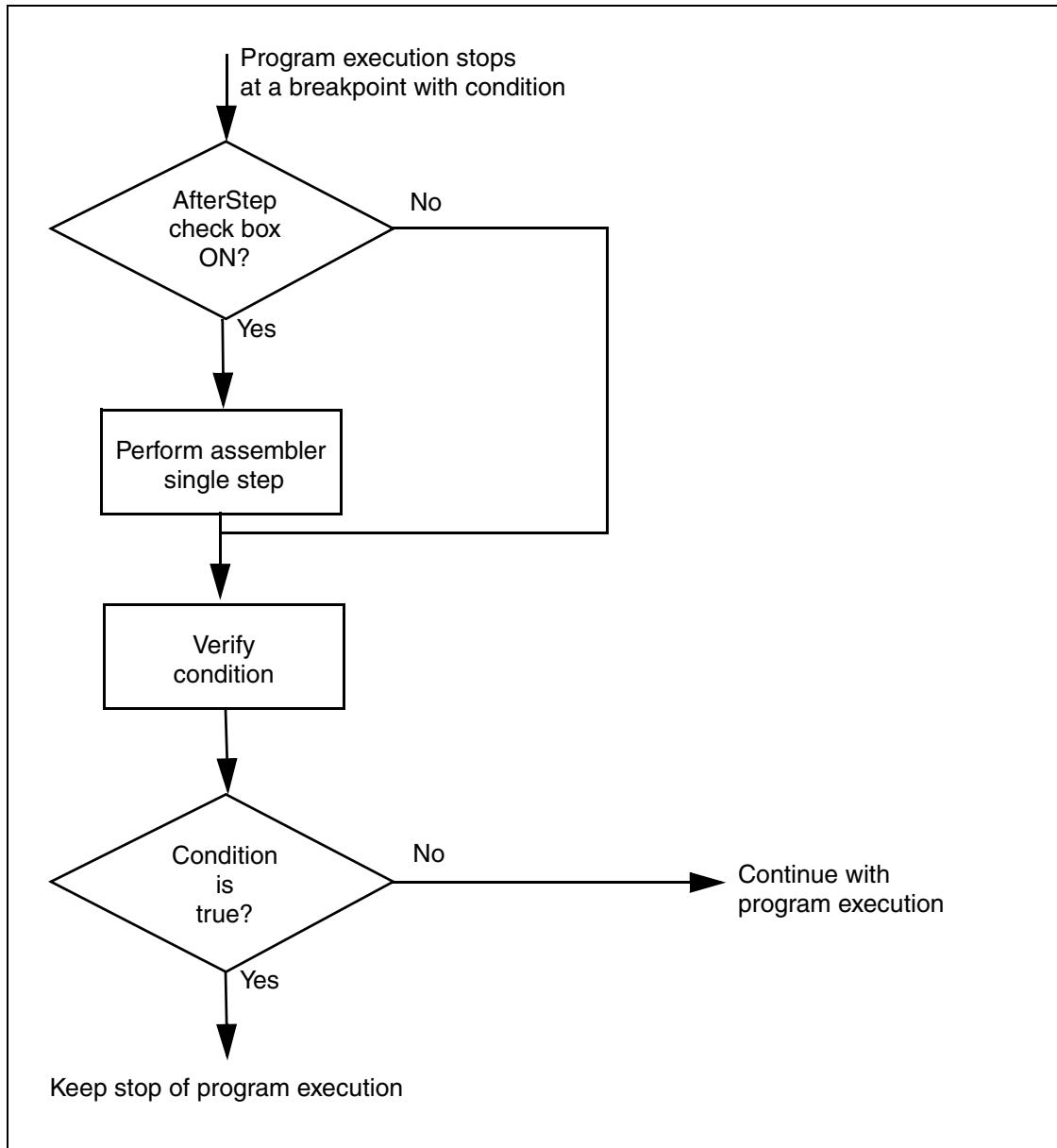
The counters run completely in real-time. No current counter value can be displayed while the program execution is running. As soon as the counter reached its final value, the program execution is stopped.

CONDition

The program execution is stopped at the breakpoint only if the specified condition is true.

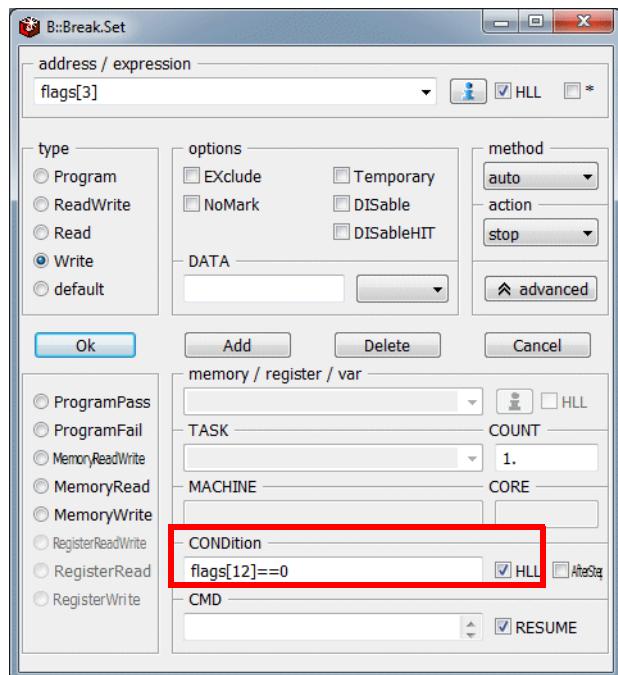
CONDition breakpoints are always intrusive.

Processing:

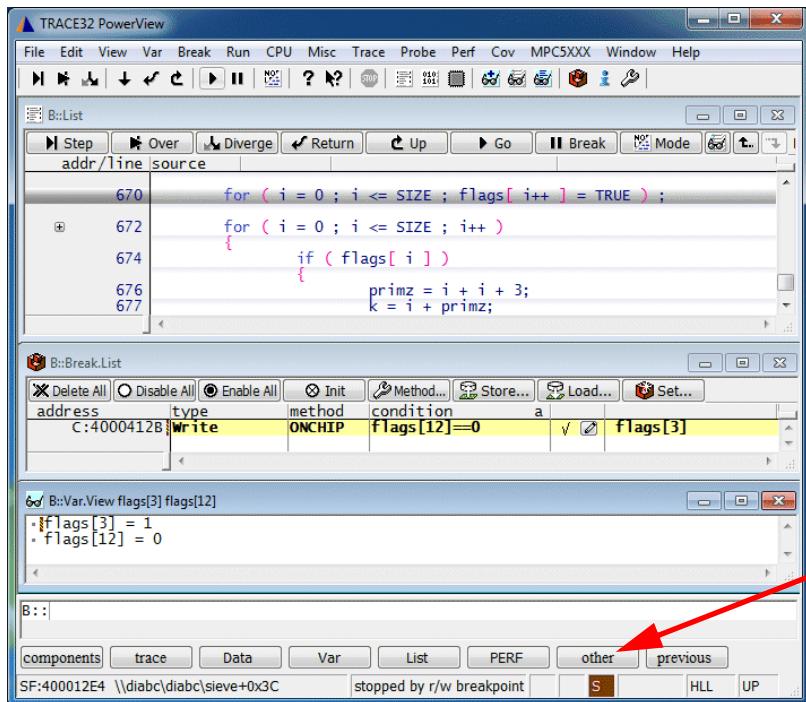


Each stop at a CONDition breakpoint takes at least 1.ms. This is why the red S is displayed in the TRACE32 PowerView state line whenever the breakpoint is hit.

Example: Stop the program execution on a write to flags[3] only if flags[12] is equal to 0 when the breakpoint is hit.



B::Break.List					
<input type="checkbox"/> Delete All	<input type="checkbox"/> Disable All	<input checked="" type="checkbox"/> Enable All	<input type="checkbox"/> Init	<input type="checkbox"/> Method...	<input type="checkbox"/> Store...
address	type	method	condition	a	<input type="checkbox"/> Set...
C:4000412B	Write	ONCHIP	flags[12]==0	✓	<input type="checkbox"/> flags[3]



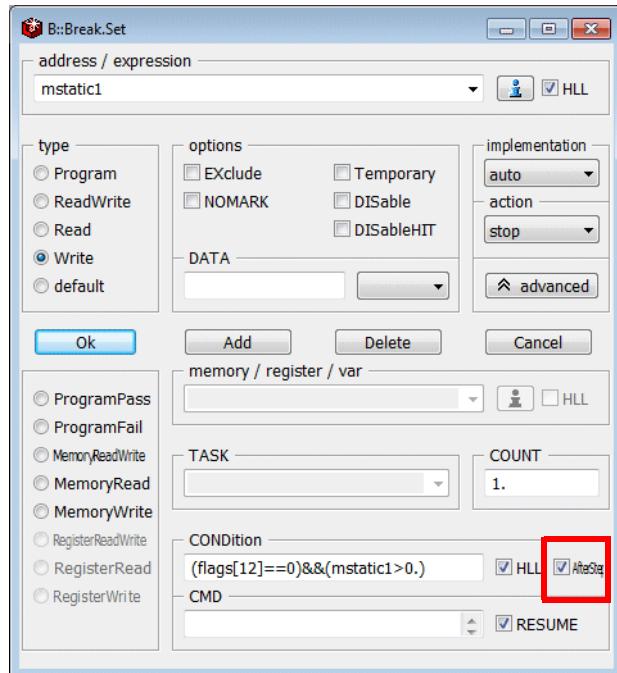
The red S indicates
an intrusive breakpoint

```
Var.Break.Set flags[3] /Write /VarCONDITION flags[12]==0
```

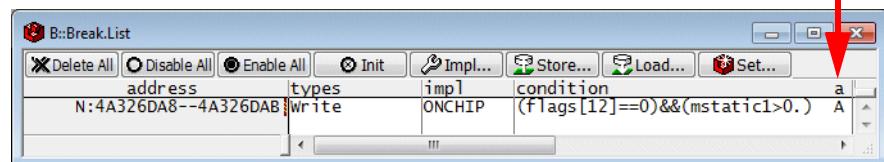
Example: “Break-before-make” Read/Write breakpoints only

Stop the program execution at a write access to the variable mstatic1 only if flags[12] is equal to 0 and mstatic1 is greater 0.

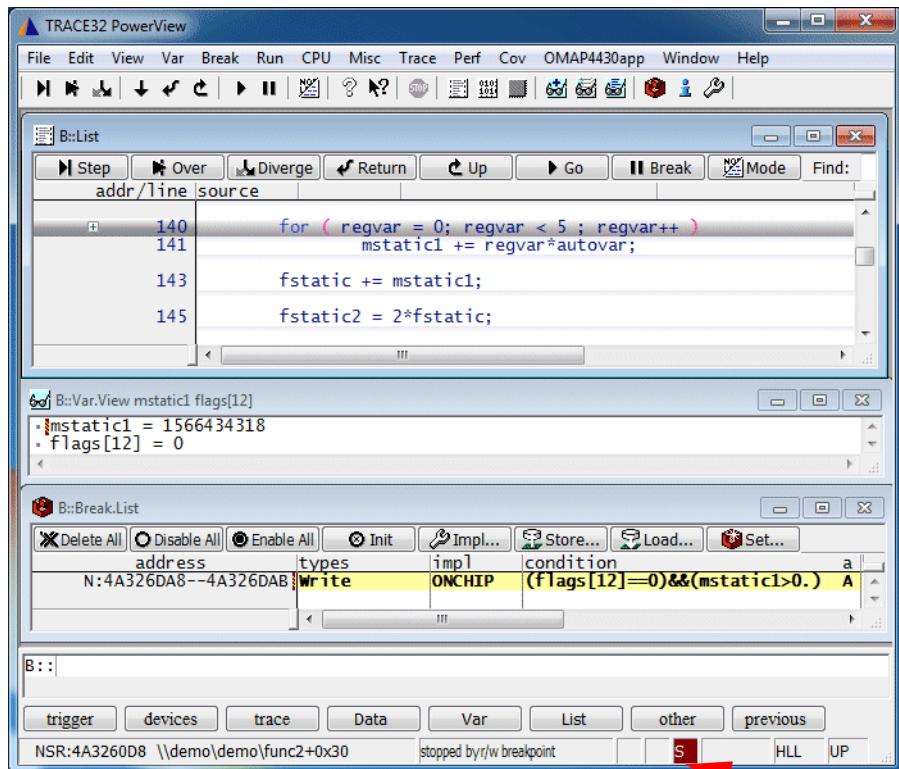
Perform an assembler single step because the processor architecture stops before the write access is performed.



AfterStep checked



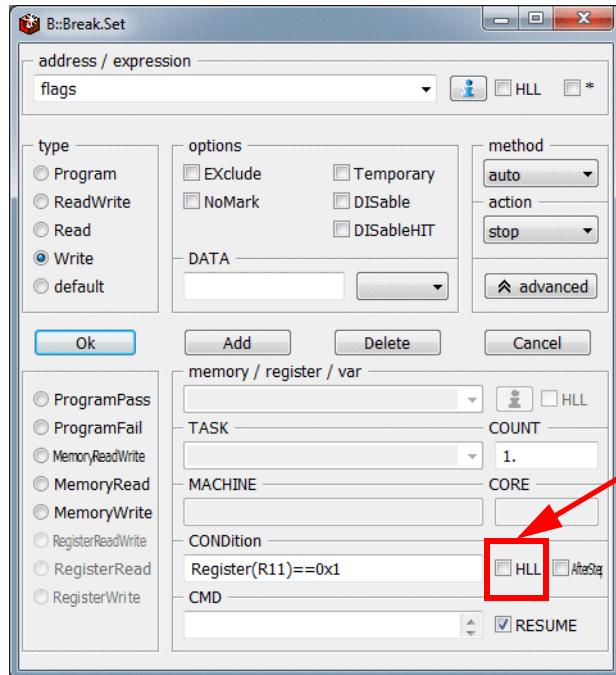
```
Var.Break.Set mstatic1 /Write /VarCondition (flags[12]==0)&&(mstatic1>0)
/AfterStep
```



The red S indicates an intrusive breakpoint

It is also possible to write register-based or memory-based conditions.

Examples: Stop the program executions on a write to the address flags if Register R11 is equal to 1.

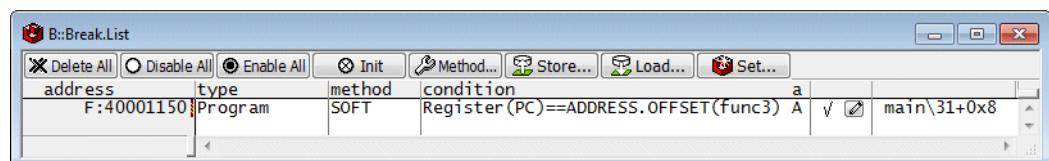
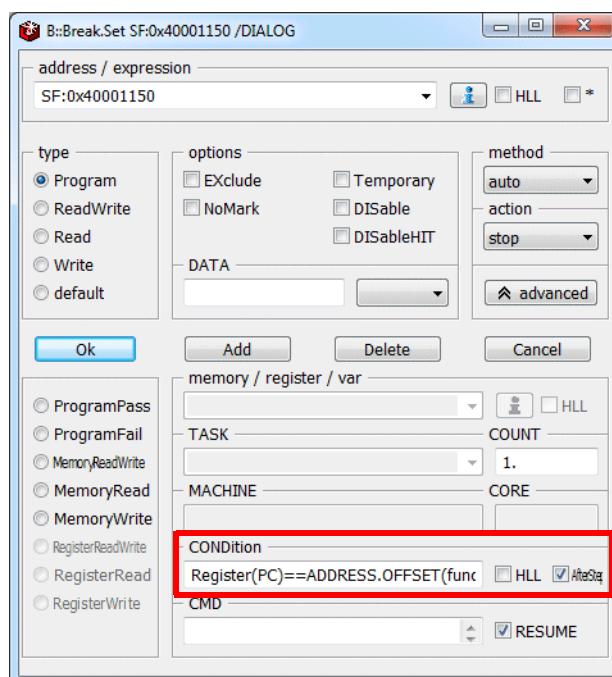
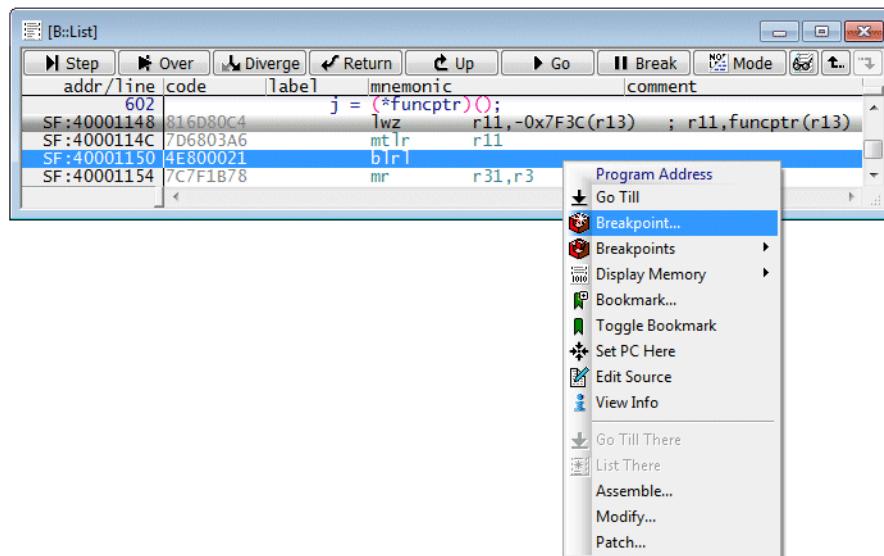


Switch HLL OFF ->
TRACE32 syntax can be used
to specify the condition

```
; stop the program execution at a write to the address flags if the
; register R11 is equal to 1
Break.Set flags /Write /CONDITION Register(R11)==0x1

; stop program execution at a write to the address flags if the long
; at address D:0x1000 is larger then 0x12345
Break.Set flags /Write /CONDITION Data.Long(D:0x1000)>0x12345
```

Example: Stop the program execution if an register-indirect call calls the function func3.



```
Break.Set main\31+0x8 /CONDITION Register(PC)==ADDRESS.OFFSET(func3)
/AfterStep
```

TRACE32 PowerView

File Edit View Var Break Run CPU Misc Trace Probe Perf Cov MPC5XXX Window Help

B::List

addr/line	code	label	mnemonic	comment
232				/* simple function */
SF:40000310 9421FFF8	func3:	stwu	r1,-0x8(r1)	; r1,-8(r1)
SF:40000314 7C0802A6		mflr	r0	
SF:40000318 900100C		stw	r0,0x0C(r1)	; r0,12(r1)
233	return 5;			
SF:4000031C 3860005		li	r3,0x5	; r3,5
234				
SF:40000320 8001000C		lwz	r0,0x0C(r1)	; r0,12(r1)
SF:40000324 7C0803A6		mtlr	r0	

B::Break.List

X Delete All	O Disable All	<input checked="" type="radio"/> Enable All	Init	Method...	Store...	Load...	Set...
address	type	method	condition	a			
F:40001150	Program	SOFT	Register(PC)==ADDRESS.OFFSET(func3)	A	<input checked="" type="checkbox"/>	main\31+0x8	

B::

components trace Data Var List PERF SYStem Step other previous

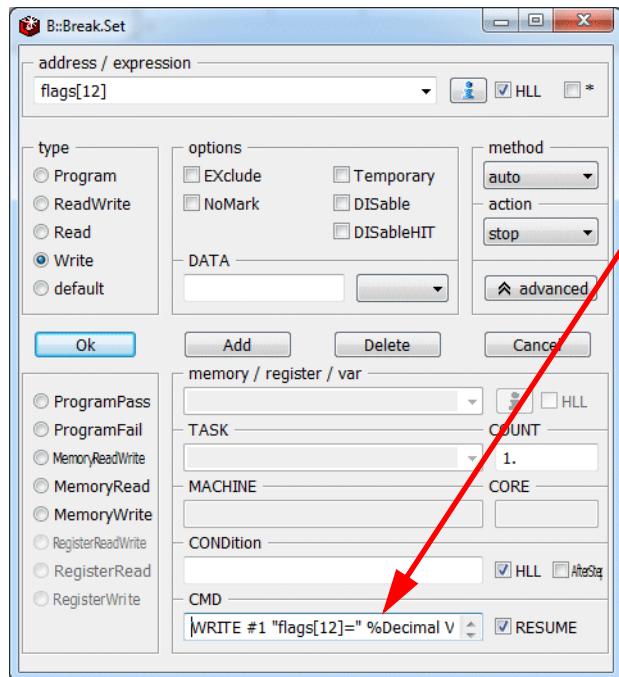
SF:40000310 \\diabc\\diabc\\func3 stopped at breakpoint MIX UP

The field CMD allows to specify one or more commands that are executed when the breakpoint is hit.

Example: Write the contents of flags[12] to a file whenever the write breakpoint at the variable flags[12] is hit.

```
OPEN #1 outflags.txt /Create
```

; open the file for writing



The specified command(s) is executed whenever the breakpoint is hit. With RESUME ON the program execution will continue after the execution of the command(s) is finished.

B::Break.List						
<input type="checkbox"/> Delete All	<input type="checkbox"/> Disable All	<input checked="" type="checkbox"/> Enable All	<input type="checkbox"/> Init	<input type="checkbox"/> Method...	<input type="checkbox"/> Store...	<input type="checkbox"/> Load...
address	type	method	cmd			
C:40004134	Write	ONCHIP	\WRITE #1 "fFlags[12]" %Decimal Var.VALUE(fFlags[12])	r	/	<input checked="" type="checkbox"/> fFlags[12]

The **cmd** field in the Break.List window informs the user which command(s) is associated with the breakpoint. R indicates that RESUME is ON.

```
Var.Break.Set flags[12] /Write /CMD "\WRITE #1 ""flags[12]" %Decimal  
Var.VALUE(flags[12])" /RESUME
```



It is recommended to set RESUME to OFF, if CMD

- starts a PRACTICE script with the command DO
- commands are used that open processing windows like Trace.STATistic.Func, Trace.Chart.sYmbol or CTS.List

because the program execution is restarted before these commands are completed.

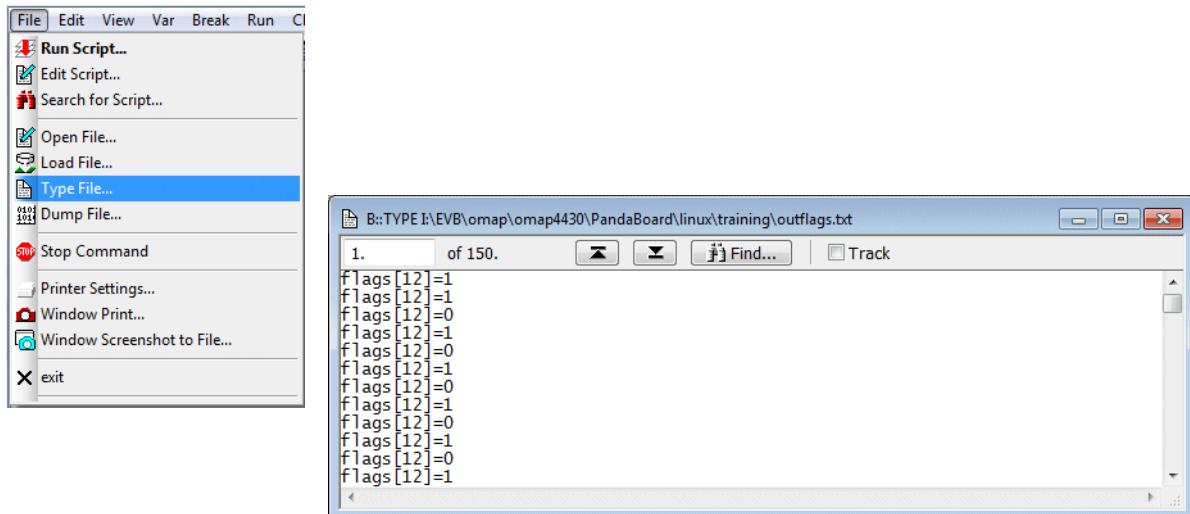
The screenshot shows the TRACE32 PowerView interface. The main window displays assembly code for a file named 'diabc.c'. The code includes instructions like stbx, addi, b, li, cmpwi, and bgt. A red arrow points to the status bar at the bottom of the window, which shows the message 'stopped by r/w breakpoint'.

The state of the debugger toggles between running and stopped

```
close #1
```

; close the file when you are done

Display the result:



The on-chip break logic of some cores allows to combine data accesses and instructions to form a complex breakpoint (e.g. ARM or PowerArchitecture).

Preconditions

- Harvard architecture.
- The on-chip break logic supports a logical AND between Program and Read/Write breakpoints.

Advantageous

- Program breakpoints on address ranges are possible.
- Read/Write breakpoints on address ranges are possible.

Example: Stop the program execution when the function sieve writes a 1 to variable flags[3]. (If your core does not support this feature, the **radio buttons** (MemoryWrite, MemoryRead etc.) are grey.)

The screenshot shows the **B::Break.Set** dialog box. The address / expression field contains **sieve**. The type field has **MemoryWrite** selected. The options section includes checkboxes for EXclude, NOMARK, Temporary, DISable, and DISableHIT. The implementation dropdown is set to **auto** and the action dropdown is set to **stop**. The memory / register / var field contains **flags[3]**. The TASK dropdown is empty, and the COUNT field contains **1.**. The condition and CMD fields are empty. A red box highlights the **MemoryWrite** radio button in the type section. A green box highlights the **flags[3]** field in the memory section. A blue box highlights the **1.** in the COUNT field. A dashed blue arrow points from the COUNT field to the text "Define the data value for the MemoryWrite accesses". A red arrow points from the **MemoryWrite** radio button to the text "Select MemoryWrite". A green arrow points from the **flags[3]** field to the text "Define the address (range) for the MemoryWrite accesses". A red arrow points from the **1.** in the COUNT field to the text "Define the address (range) of the instructions here".

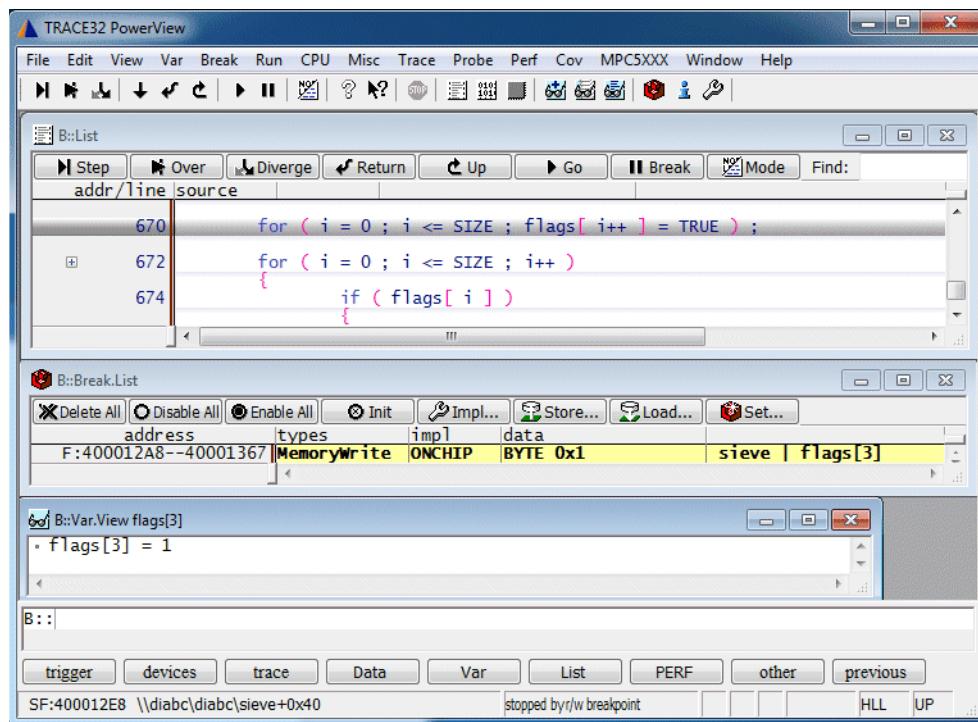
1. Define the address (range) of the instructions here

2. Select MemoryWrite

3. Define the address (range) for the MemoryWrite accesses

4. Define the data value for the MemoryWrite accesses

```
Var.Break.Set sieve /VarWrite flags[3] /DATA.auto 1.
```



Exclude

(Advanced users only, not available on all cores)

The breakpoint is inverted.

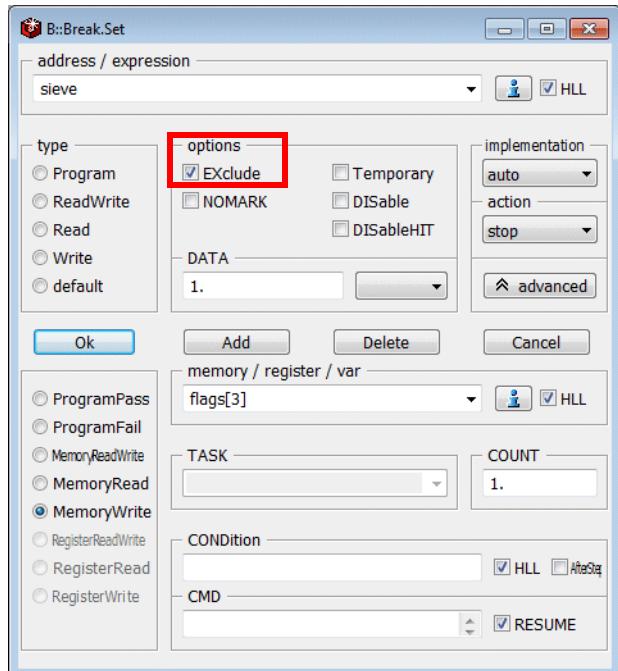
- by the inverting logic of the on-chip break logic
- by setting the specified breakpoint type to the following 2 address ranges
0x0--(start_of_breakpoint_range-1)
(end_of_breakpoint_range+1)--end_of_memory

The EXclude option applies only to Onchip breakpoints.

If the on-chip breakpoint logic does not provide an inverting logic, the core has to provide the facility to set the specified breakpoint type on 2 address ranges.

Example for the Option EXclude

Stop the program execution when code outside of the function sieve writes 1 to the variable flags[3].



B::Break.List						
<input type="button" value="Delete All"/>	<input type="button" value="Disable All"/>	<input type="button" value="Enable All"/>	<input type="button" value="Init"/>	<input type="button" value="Impl..."/>	<input type="button" value="Store..."/>	<input type="button" value="Load..."/>
address	types	impl	options	data		
F:400012A8--40001367	MemoryWrite	ONCHIP	EXclude	BYTE 0x1	sieve	flags[3]

```
Var.Break.Set sieve /VarWrite flags[3] /DATA.auto 1. /EXclude
```

```

[B::List]
Step Over Diverge Return Up Go Break Mode Find:
breakpoint addr/line source
649         j = func25();
651         p = func26();
653         for (j = 0; j < 10; j++)
654         {
655             sieve();
656         }
658 }

char flags[SIZE+1];
int sieve() /* sieve of er */
{
    register int i, primz, k;
    int anzahl;
    anzahl = 0;
    for (i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE)
    {
        for (i = 0 ; i <= SIZE ; i++)
    }
}

```

The function sieve is marked with **Exclude memoryWrite** breakpoints

The following command allows to check how the option EXclude is implemented.

`Break.List /Onchip`

Inverting logic of on-chip break logic:

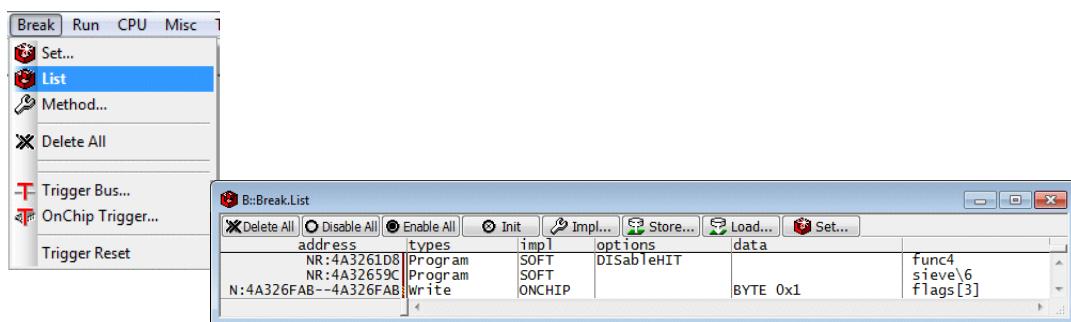
B::Break.List /Onchip					
<input checked="" type="checkbox"/> Delete All	<input type="radio"/> Disable All	<input checked="" type="radio"/> Enable All	<input checked="" type="checkbox"/> Init	<input checked="" type="checkbox"/> Impl...	<input checked="" type="checkbox"/> Store...
address	types	impl	options	data	onchip resource
R:00001800--00001BFF	Memorywrite	ONCHIP	Exclude	BYTE 0x1	(func23+0x4)--(main\26+0x23) f1ags[3]

Two address range breakpoints:

B::Break.List /Onchip					
<input checked="" type="checkbox"/> Delete All	<input type="radio"/> Disable All	<input checked="" type="radio"/> Enable All	<input checked="" type="checkbox"/> Init	<input checked="" type="checkbox"/> Impl...	<input checked="" type="checkbox"/> Store...
address	types	impl	options	data	onchip resource
C:00000000--700013E9	Memorywrite	ONCHIP		BYTE 0x1	C:0x0--0x700013E9 f1ags[3]
C:70001450--FFFFFFFFFF	Memorywrite	ONCHIP		BYTE 0x1	C:0x70001450--0xFFFFFFFF f1ags[3]

If your TRACE32 PowerView does not accept the option EXclude, delete all other Onchip breakpoints, to make sure that enough resources are available.

Display a List of all Set Breakpoints

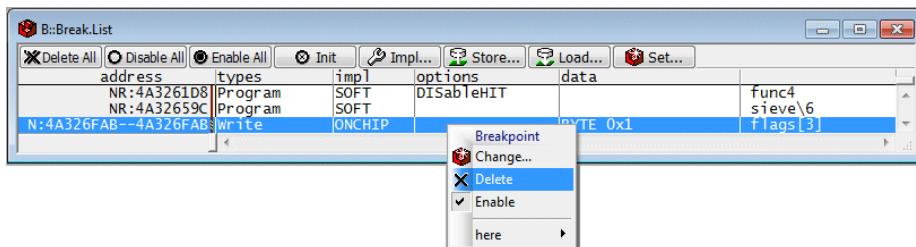


address	Address of the breakpoint
types	Type of the breakpoint
impl	Implementation of the breakpoint or disabled
action	Action selected for the breakpoint (if not stop)
options	Option defined for the breakpoint
data	Data value that has to be read/written to stop the program execution by the breakpoint
count	Current value/final value of the counter that is combined with a breakpoint
condition A (AfterStep)	Condition that has to be true to stop the program execution by the breakpoint A ON: Perform an assembler single step before condition is evaluated
cmd (command) R (resume)	Commands that are executed after the breakpoint hit R ON: continue the program execution after the specified commands were executed
task	Name of the task for a task-aware breakpoint
	Symbolic address of the breakpoint

Break.List [/<option>]

List all breakpoints

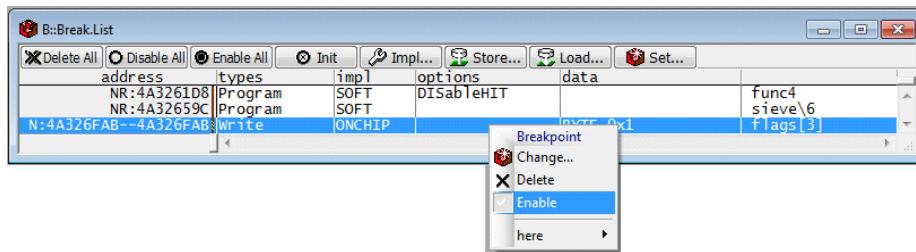
Delete Breakpoints



Break.Delete <address>|<address_range> [/<type>] [/<implem.>] [/<option>] Delete breakpoint

Var.Break.Delete <hl_expression> [/<type>] [/<implem.>] [/<option>] Delete HLL breakpoint

Enable/Disable Breakpoints



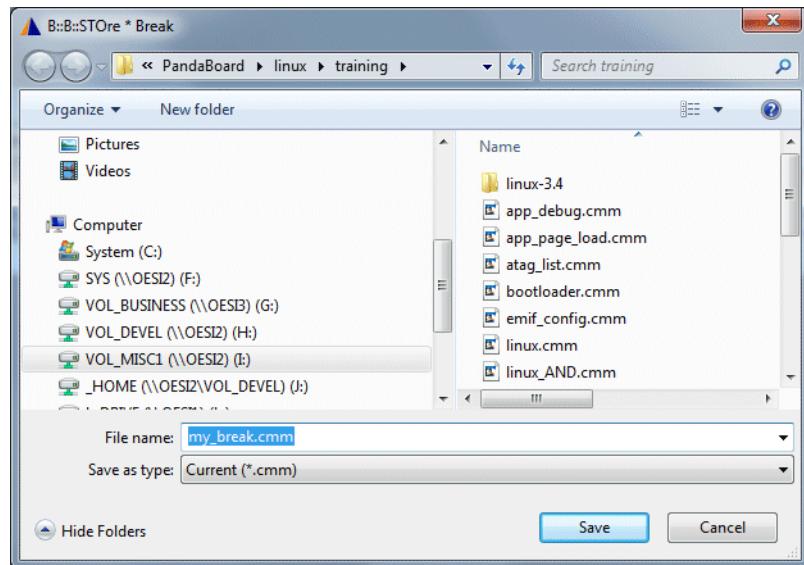
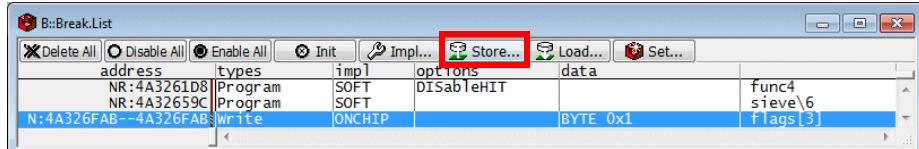
Break.ENABLE <address>|<address_range> [/<option>]

Enable breakpoint

Break.DISABLE <address>|<address_range> [/<option>]

Disable breakpoint

Store Breakpoint Settings



```
// AndT32 Fri Jul 04 13:17:41 2003

B:::

BREAK.RESET
B.S    func4 /P /DISABLEHIT
B.S    sieve /P
V.B.S \\\diabp555\Global\flags[3]; /W /DATA.BYTE 0x1;

ENDDO
```

STOre <filename> Break

Generate a script for breakpoint settings

Debugging of Optimized Code

A video tutorial about debugging optimized code can be found here:

http://www.lauterbach.com/tut_optimized.html

HLL mode and MIX mode debugging is simple, if the compiler generates a continuous block of assembler code for each HLL code line.

If compiler optimization flags are turned on, it is highly likely that two or more detached blocks of assembler code are generated for individual HLL code lines. This makes debugging laboriously.

TRACE32 PowerView displays a drill-down button, whenever two or more detached blocks of assembler code are generated for an HLL code line.

```
B:List.HII
Step Over Next Return Up Go Break Mode Find: diabc.c
addr/line source
664 char flags[SIZE+1];
int sieve()
{
    register int i, primz, k;
    int anzahl;
    anzahl = 0;
    for ( i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE ) ;
    for ( i = 0 ; i <= SIZE ; i++ )
    {
        if ( flags[ i ] )
    }
```

Drill-down button

The following background information is fundamental if you want to debug optimized code:

- In HLL debug mode, the HLL code lines are displayed as written in the compiled program (source line order).
- In MIX debug mode, the target code is disassembled and the HLL code lines are displayed together with their assembler code blocks (target line order). This means if two or more detached blocks of assembler code are generated for an HLL code line, this HLL code line is displayed more than once in a MIX mode source listing.

The expansion of the drill-down button shows how many detached blocks of assembler code are generated for the HLL line (e.g. two in the example below).

List.HLL

Display source listing, display HLL code lines only.

List.Mix /Track

Display source listing, display disassembled code and the assigned HLL code lines.

The blue cursor in the MIX mode display follows the cursor movement of the HLL mode display (Track option).

addr/line	source
	char flags[SIZE+1];
664 [int sieve() /* sieve of erathostenes */
	register int i, primz, k;
	int anzahl;
668	anzahl = 0;
670	for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;
672 L	for (i = 0 ; i <= SIZE ; i++)
672	for (i = 0 ; i <= SIZE ; i++)
674	if (flags[i])

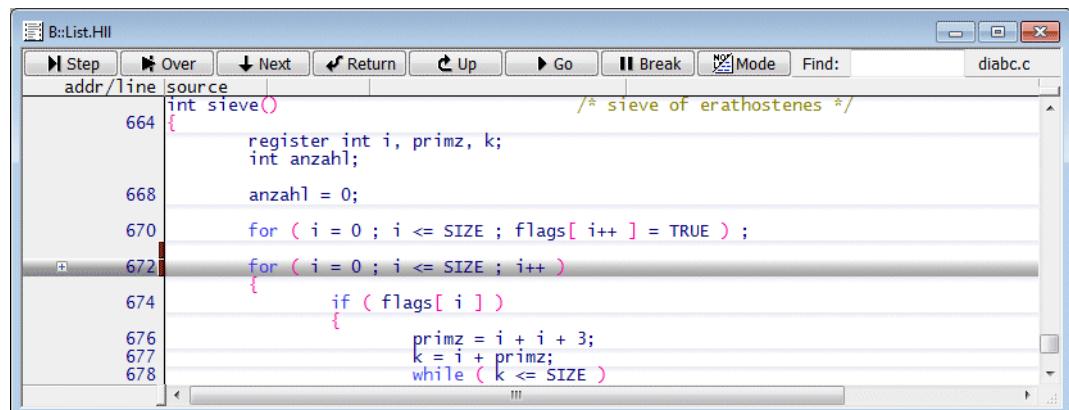
addr/line	code	label	mnemonic	comment
672	SF:400012EC	.L514:	li	r31,0x0 ; i,0
	SF:400012F0	.L522:	cmpwi	r31,0x12 ; i,18
	SF:400012F4	41810050	bgt	0x40001344 ; .L517 (-)
674	SF:400012F8	3D804000	lis	r12,0x4000 ; r12,16384
	SF:400012FC	398C4128	addi	r12,r12,0x4128 ; r12,r12,16680
	SF:40001300	7D8CF8AE	lbzx	r12,r12,r31 ; r12,r12,i
	SF:40001304	2C0C0000	cmpwi	r12,0x0 ; r12,0
	SF:40001308	41820034	beq	0x4000133C ; .L521 (-)
676	SF:4000130C	7D9FFA14	add	r12,r31,r31 ; r12,i,i
	SF:40001310	3BCC0003	addi	r30,r12,0x3 ; primz,r12,3
677	SF:40001314	7FBFF214	add	r29,r31,r30 ; k,i,primz
678	SF:40001318	2C100012	cmpwi	r29,0x12 ; k,18
	SF:4000131C	4181001C	bgt	0x40001338 ; .L519 (-)
680	SF:40001320	3D804000	lis	r12,0x4000 ; r12,16384
	SF:40001324	398C4128	addi	r12,r12,0x4128 ; r12,r12,16680
	SF:40001328	39600000	li	r11,0x0 ; r11,0
	SF:4000132C	7D6CE9AE	stbx	r11,r12,r29 ; r11,r12,k
681	SF:40001330	7FBDF214	k += primz;	
	SF:40001334	4BFFF4E4	add	r29,r29,r30 ; k,k,primz
683	SF:40001338	3B9C0001	b	0x40001318 ; .L520
			}	
684	SF:4000133C	.L519:	addi	r28,r28,0x1 ; anzahl,anzahl,1
	SF:40001340	3BFF0001	for (i = 0 ; i <= SIZE ; i++)	
		.L521:	addi	r31,r31,0x1 ; i,i,1
			b	0x400012F0 ; .L522

To keep track when debugging optimized code, it is recommended to work with an HLL mode and a MIX mode display of the source listing in parallel.

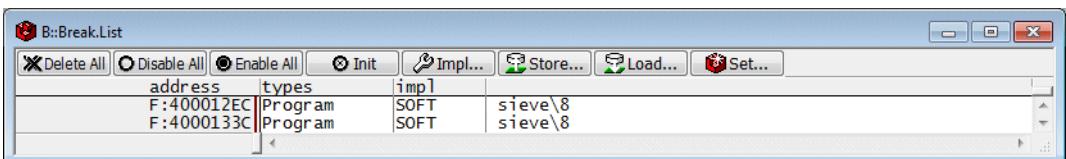
```
List.Hll  
List.Mix
```

Please be aware of the following:

If a Program breakpoint is set to an HLL code line for which two or more detached blocks of assembler code are generated, a Program breakpoint is set to the start address of each assembler block.



The screenshot shows the B::List.HLL window with the title bar "B::List.HLL". The window contains a toolbar with buttons for Step, Over, Next, Return, Up, Go, Break, Mode, and Find. The "Mode" button is currently set to "diabc.c". The main area displays assembly code for a function named "sieve". The code includes comments like /* sieve of erathostenes */ and various assembly instructions and labels. The assembly code is generated from C code, showing how multiple C loops are translated into separate assembly blocks.

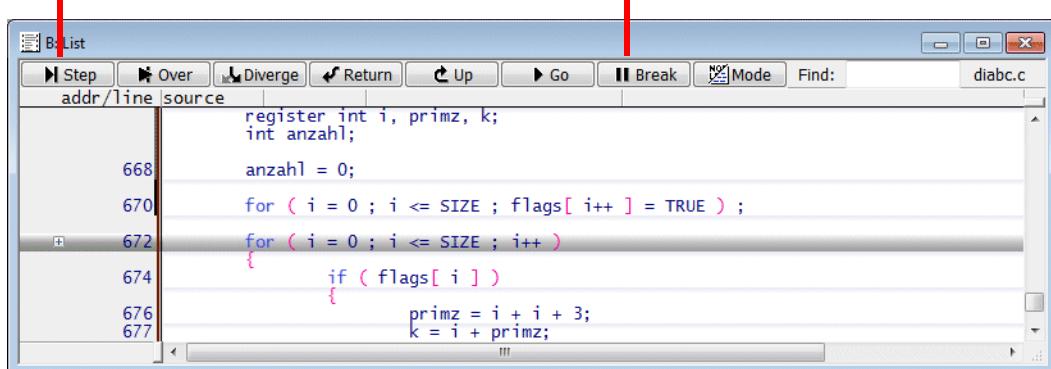


The screenshot shows the B::Break.List window with the title bar "B::Break.List". The window contains a toolbar with buttons for Delete All, Disable All, Enable All, Init, Implement..., Store..., Load..., and Set... The main area is a table with columns: address, types, impl, and file. It lists two breakpoints: one at address F:400012EC and another at F:4000133C, both of type Program and soft implementation, pointing to the file "sieve\8".

address	types	impl	file
F:400012EC	Program	SOFT	sieve\8
F:4000133C	Program	SOFT	sieve\8

Basic Debug Control

There are local buttons in the **List** window for all basic debug commands



Step	Single stepping (command: Step)
Over	Step over call (command Step.Over).
Diverge	Exit loops or fast forward to not yet stepped code lines. Step.Over is performed repeatedly.

More details on Step.Diverge

TRACE32 maintains a list of all assembler/HLL lines which were already reached by a Step. These reached lines are marked with a slim grey line in the List window.

```
int sieve() /* sieve of erathostenes */
{
    register int i, primz, k;
    int anzahl;

    /line so
    in
    anzahl = 0;
    { or ( i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE ) ;
    or ( i = 0 ; i <= SIZE ; i++ )
        if ( flags[ i ] )
    {
```

The following command allows you to get more details:

```
List.auto /DIVERGE
```

[B::List /DIVERGE]

s	state	i	addr/line	source
h stop			664	int sieve() /* sieve of erathostenes
h done			668	{ register int i, primz, k;
h done			670	int anzahl;
h done	[672	for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;
hit	672			for (i = 0 ; i <= SIZE ; i++)
				{ if (flags[i])
				{
			676	primz = i + i + 3;
			677	k = i + primz;
			678	while (k <= SIZE)
			680	{
			681	flags[k] = FALSE;
			682	k += primz;
			683	anzahl++;
				}
target			687	return anzahl;
			688	}

Drag this handle to see the DIVERGE details

[B::List /DIVERGE]

s	state	i	addr/line	code	label	mnemonic	comment
a stop			602	j = (*funcptr)();			
a stop			SF:40001148	lzw r11,-0x7F3C(r13)	r11	funcptr(r	
a done			SF:4000114C	mtlr r11			
a done	i		SF:40001150	birl			
a stop			SF:40001154	mr r31,r3		; j,r3	
a done			604	j = func5((int) j, (char) 2, (long) 3);			
a done			SF:40001158	mr r3,r31		; r3,j	
a done			SF:4000115C	li r4,0x2		; r4,2	
a done			SF:40001160	li r5,0x3		; r5,3	
a done			SF:40001164	b1 0x400003A0		; func5	
stop			SF:40001168	mr r31,r3		; j,r3	

Column layout

s	Step type performed on this line a: Step on assembler level was started from this code line h: Step on HLL level was started from this code line
state	done: code line was reached by a Step and a Step was started from this code line. hit: code line was reached by a Step. target: code line is a possible destination of an already started Step, but was not reached yet (mostly caused by conditional branches). stop: program execution stopped at code line.
i	indirect branch taken (return instructions are not marked).

Example 1: Diverge through function sieve.

1. Run program execution until entry to function sieve.

stop indicates that the program execution was stopped at this code line

```
char flags[SIZE+1];  
int sieve()  
{  
    register int i, primz, k;  
    int anzahl = 0;  
    for ( i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE ) ;  
    for ( i = 0 ; i <= SIZE ; i++ )  
        if ( flags[ i ] )  
            {  
                primz = i + i + 3;  
                k = i + primz;  
                while ( k <= SIZE )  
                    {  
                        flags[ k++ ] = TRUE;  
                        k = k + 2;  
                    }  
            }  
    }
```

2. Start a Step.Diverge command.

h indicates that a Step command in HLL mode was started in this line

hit indicates that this code line was reached by Step command

```
char flags[SIZE+1];  
int sieve()  
{  
    register int i, primz, k;  
    int anzahl = 0;  
    for ( i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE ) ;  
    for ( i = 0 ; i <= SIZE ; i++ )  
        if ( flags[ i ] )  
            {  
                primz = i + i + 3;  
                k = i + primz;  
                while ( k <= SIZE )  
                    {  
                        flags[ k++ ] = TRUE;  
                        k = k + 2;  
                    }  
            }  
    }
```

3. Continue with Step.Diverge.



s state	i	addr/line	source
h stop		664	char flags[SIZE+1];
h done		668	int sieve() /* sieve of eratho
hit		670	register int i, primz, k;
		672	int anzahl;
		674	anzahl = 0;
		676	for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;
		677	for (i = 0 ; i <= SIZE ; i++)
		678	{ if (flags[i])
		676	primz = i + i + 3;
		677	k = i + primz;
		678	while (k <= SIZE)
			{

done indicates that the code line was reached by a Step command and that a Step command was started from this code line

The drill-down button indicates that two or more detached blocks of assembler code are generated for an HLL code line

```

B::List / DIVERGE
Step Over Diverge Return Up Go Break Mode Find: sieve
s state i addr/line source
h stop 664 char flags[SIZE+1];
int sieve() /* sieve of erathos
register int i, primz, k;
int anzahl;
anzahl = 0;
for ( i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE ) ;
for ( i = 0 ; i <= SIZE ; i++ )
{
    if ( flags[ i ] )
        primz = i + i + 3;
    k = i + primz;
    while ( k <= SIZE )
}

```

4. Continue with Step.Diverge.

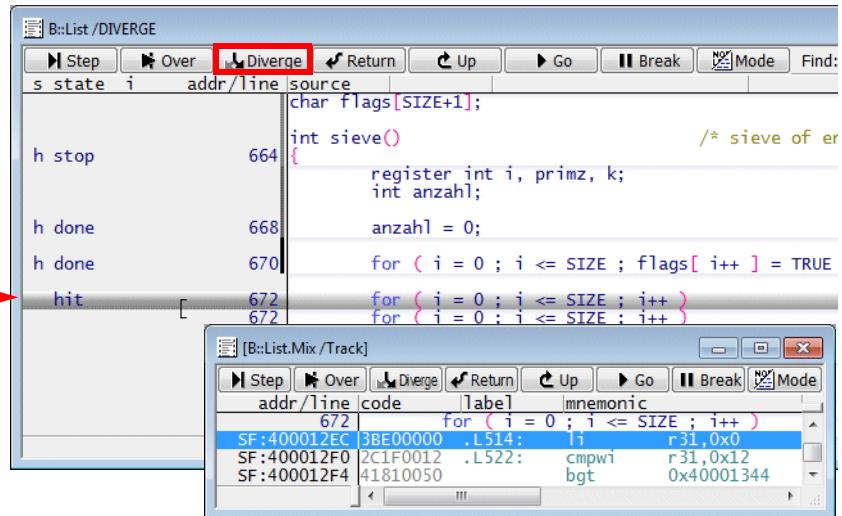
The drill-down tree is expanded and the HLL code line representing the reached block of assembler code is marked as hit

```

B::List / DIVERGE
Step Over Diverge Return Up Go Break Mode Find: sieve
s state i addr/line source
h stop 664 char flags[SIZE+1];
int sieve() /* sieve of erathos
register int i, primz, k;
int anzahl;
anzahl = 0;
for ( i = 0 ; i <= SIZE ; flags[ i++ ] = TRUE ) ;
for ( i = 0 ; i <= SIZE ; i++ )
{
    if ( flags[ i ] )
        primz = i + i + 3;
    k = i + primz;
    while ( k <= SIZE )
}

```

This HLL code line includes a conditional branch



char flags[SIZE+1];
int sieve()
{
 register int i, primz, k;
 int anzahl;

 anzahl = 0;

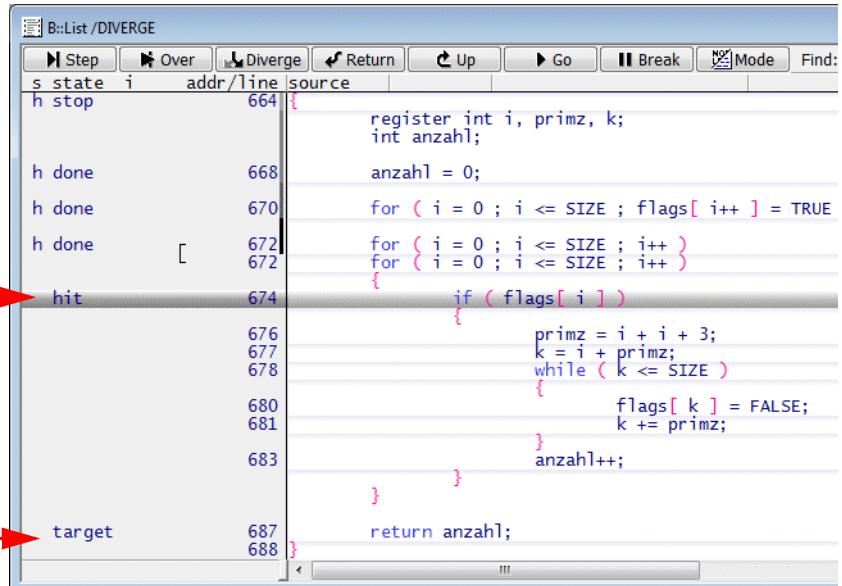
 for (i = 0 ; i <= SIZE ; flags[i++] = TRUE)
 for (j = 0 ; j <= SIZE ; j++)
 if (flags[j])
 primz = i + j + 3;
 k = i + primz;
 while (k <= SIZE)
 {
 flags[k] = FALSE;
 k += primz;
 }
 anzahl++;
}
return anzahl;

5. Continue with Step.Diverge.

The reached code line is marked as **hit**



The not-reached code line is marked as **target**



register int i, primz, k;
int anzahl;

anzahl = 0;

for (i = 0 ; i <= SIZE ; flags[i++] = TRUE)
 for (j = 0 ; j <= SIZE ; j++)
 if (flags[j])
 primz = i + j + 3;
 k = i + primz;
 while (k <= SIZE)
 {
 flags[k] = FALSE;
 k += primz;
 }
 anzahl++;

return anzahl;

6. Continue with Step.Diverge (several times).

All code lines are now either marked as **done**, **hit** or **target**

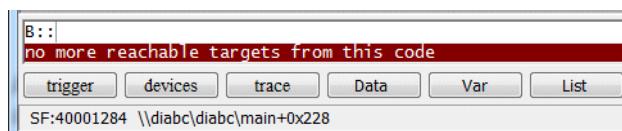
s state	i	addr/line	source
h stop		664	int sieve()
h done		668	register int i, primz, k;
h done		670	int anzahl;
h done target		672	anzahl = 0;
h done		672	for (i = 0 ; i <= SIZE ; flags[i++] =
h done		674	for (i = 0 ; i <= SIZE ; i++)
h done		676	{
h done		677	if (flags[i])
h done		678	{
h done hit		680	primz = i + i + 3;
target		681	k = i + primz;
target		683	while (k <= SIZE)
target		687	{
		688	flags[k] = FALSE;
			k += primz;
			}
			anzahl++;
			}
			return anzahl;

7. Continue with Step.Diverge.

A code line former marked as **target** changes to **hit** when it is reached

s state	i	addr/line	source
char flags[SIZE+1];			/* sieve of e
h stop		664	int sieve()
h done		668	register int i, primz, k;
h done		670	int anzahl;
h done target		672	anzahl = 0;
h done		672	for (i = 0 ; i <= SIZE ; flags[i++] = TRUE
h done		674	for (i = 0 ; i <= SIZE ; i++)
h done		676	{
h done		677	if (flags[i])
h done		678	{
h done		680	primz = i + i + 3;
h done		681	k = i + primz;
hit		683	while (k <= SIZE)
hit		683	{
target		687	flags[k] = FALSE;
target		688	k += primz;
			}
			anzahl++;
			}
			return anzahl;

When all reachable code lines are marked as **done**, the following message is displayed:



The **DIVERGE** marking is cleared when you use the **Go.direct** command without address or the **Break** command while the program execution is stopped.

Example 2: Exit a loop.

DIVERGE marking is done whenever you single step.

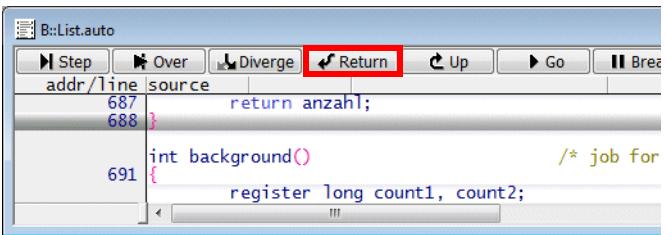
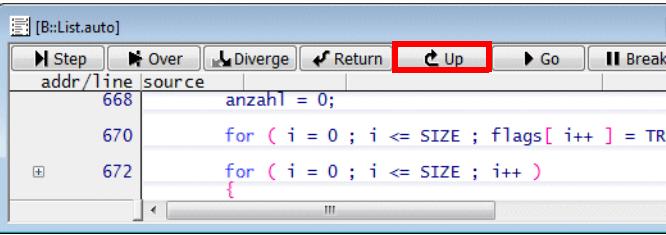
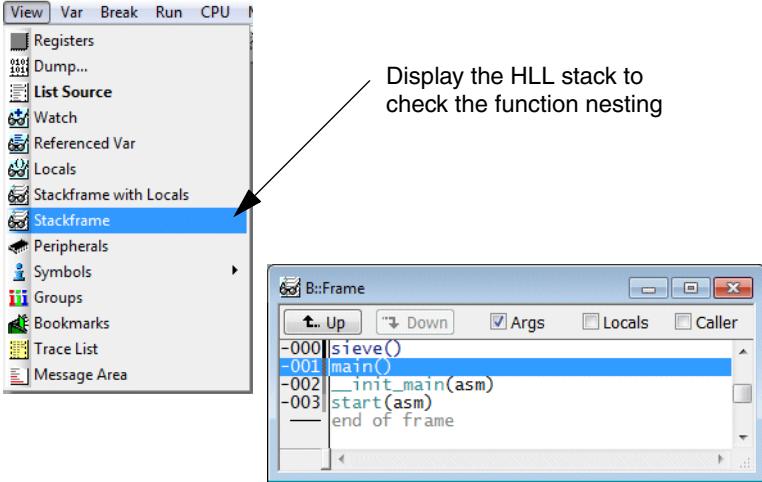
If all code lines of a loop are marked as **done/hit**, a Step.Diverge will exit the loop

B::List /DIVERGE

s	state	i	addr/line	source
				register int i, primz, k; int anzahl;
h done			668	anzahl = 0;
h done			670	for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;
h done target	[672	for (i = 0 ; i <= SIZE ; i++) for (i = 0 ; i <= SIZE ; i++)
h done			674	{ if (flags[i])
h done			676	primz = i + i + 3;
h done			677	k = i + primz;
h done			678	while (k <= SIZE)
h done hit			680	{ flags[k] = FALSE;
			681	k += primz;
target			683	} anzahl++;
target			687	}
			688	return anzahl;
			691	int background() /* job for background */
				register long count1, count2;

B::List /DIVERGE

s	state	i	addr/line	source
				char flags[SIZE+1];
				int sieve() /* sieve of erathostenes */
h stop			664	{ register int i, primz, k;
h done			668	int anzahl;
h done			670	anzahl = 0;
h done target	[672	for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;
h done			674	for (i = 0 ; i <= SIZE ; i++) for (i = 0 ; i <= SIZE ; i++)
h done			676	{ if (flags[i])
h done			677	primz = i + i + 3;
h done			678	k = i + primz;
h done			680	while (k <= SIZE)
h done			681	{ flags[k] = FALSE;
hit			683	k += primz;
target			687	} anzahl++;
			688	}
				return anzahl;

Return	<p>Return sets a temporary breakpoint to the last instruction of a function and then starts the program execution.</p> 
Up	<p>This command is used to return to the function that called the current function. For this a temporary breakpoint is set to the instruction directly after the function call. Afterwards the program execution is started.</p>  <p>Display the HLL stack to check the function nesting</p> 

Step [<count>]	Single step
Step.Change <expression>	Step until <expression> changes
Step.Till <condition>	Step until <condition> becomes true, <condition> written in TRACE32 syntax
Var.Step.Change <hll_expression>	Step until <hll_expression> changes
Var.Step.Till <hll_condition>	Step until <hll_condition> becomes true, <hll_condition> as allowed in used programming language

```
Step 10.

Step.Change Register(R11)

Step.Till Register(R11)>0xAA

Var.Step.Change flags[3]

Var.Step.Till flags[3]==1
```

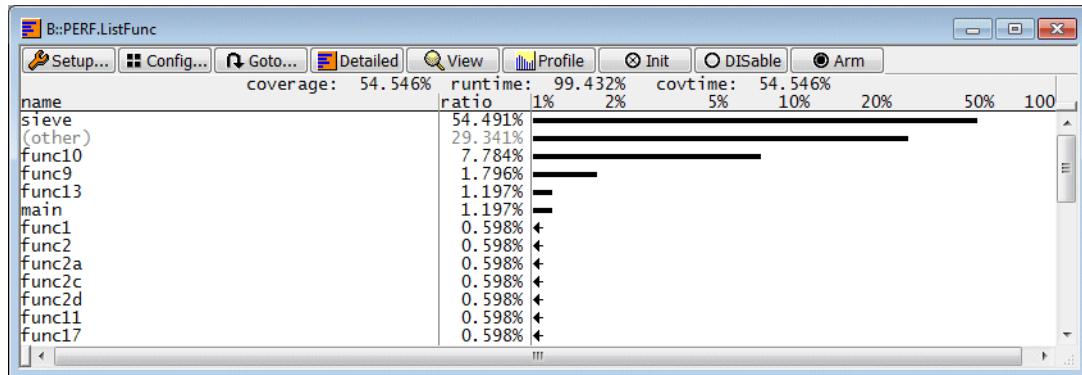
Step.Over

Step over call

Go [<address> <label>]	Start program execution
Go.Next	Set a temporary breakpoint to the next code line and start the program execution
Go.Return	Set a temporary breakpoint to the return instruction and start the program execution
Go.Up [<level> <address>]	Run program until it returns to the caller function

Program Counter Sampling

Task: get the percentage of time used by a high-level language function.



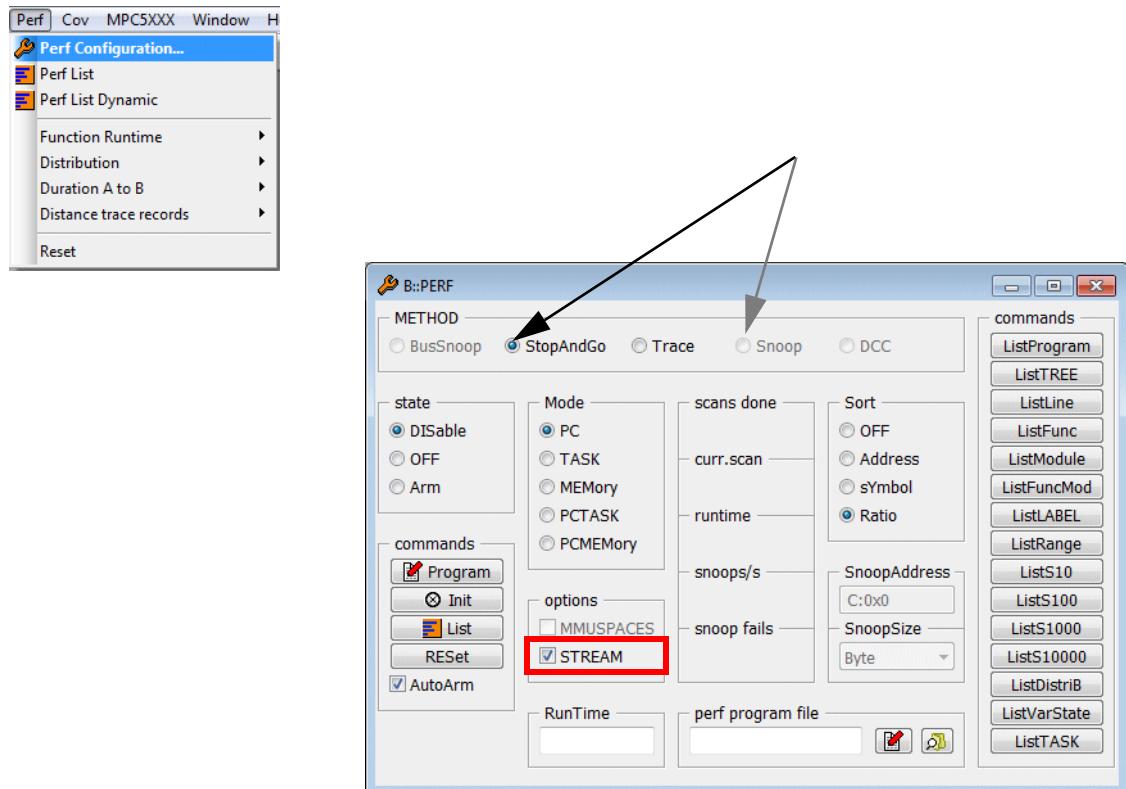
Measurement procedure: The Program Counter is sampled periodically. This is implemented in two ways.

- **Snoop:** Processor architecture allows to read the Program Counter while the program execution is running.
- **StopAndGo:** The program execution is stopped shortly in order to read the Program Counter.

Standard Procedure

Steps to be taken:

1. Open the PERF configuration window.



PERF.state

Display PERF configuration window

The PERF METHOD **Snoop** is automatically selected, if the processor architecture supports reading the Program Counter while the program execution is running.

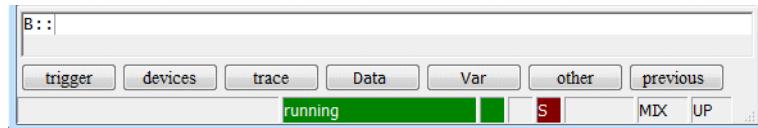
The default METHOD for all other processor architectures is **StopAndGo**.

Remarks on the StopAndGo method

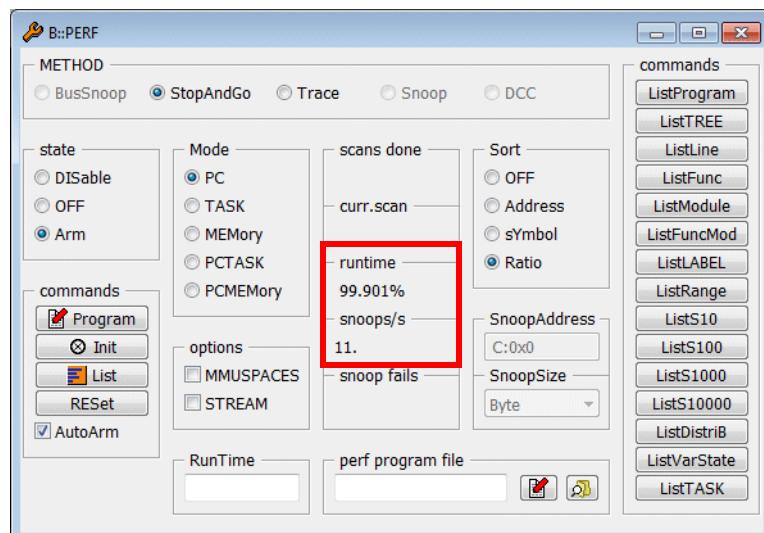
StopAnd Go means that the core is stopped periodically in order to get the actual Program Counter.

STREAM ON	The software running on the TRACE32 debug hardware initiates the periodic stops. This has the following advantages: <ul style="list-style-type: none">• Low intrusive (approx. 50. to 100.us)• More samples per second are possible
STREAM OFF	The software running on the host initiates the periodic stops. <ul style="list-style-type: none">• More intrusive (1 ms in a worst case scenario)• Less samples per second are possible

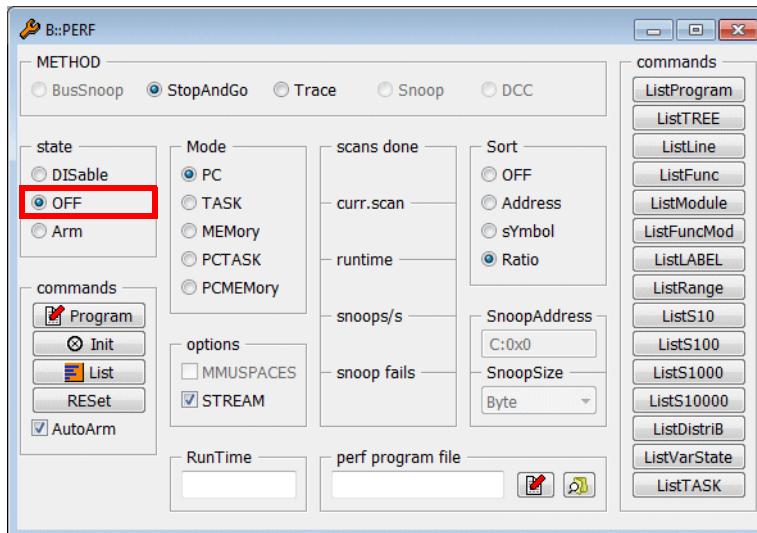
The display of a red **S** in the TRACE32 state line indicates that the program execution is periodically interrupted by the sample-based profiling.



TRACE32 tunes the sampling rate so that more than 99% of the run-time is retained for the actual program run (runtime). The smallest possible sampling rate is nevertheless 10 (snoops/s).



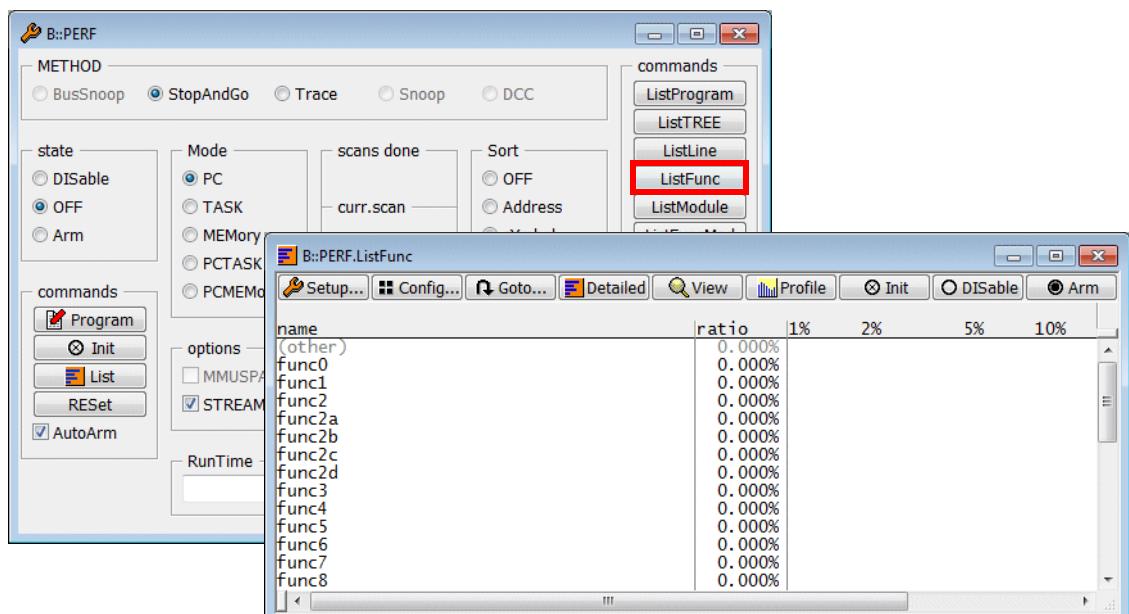
2. Enable the sample-based profiling by selecting the OFF state.



PERF.OFF

Enable the sample-based profiling

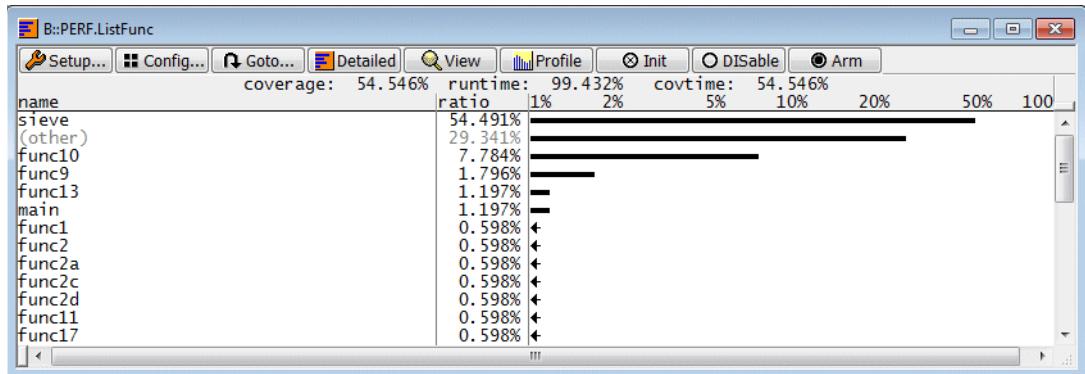
3. Open a result window by pushing the ListFunc button.



PERF.ListFunc

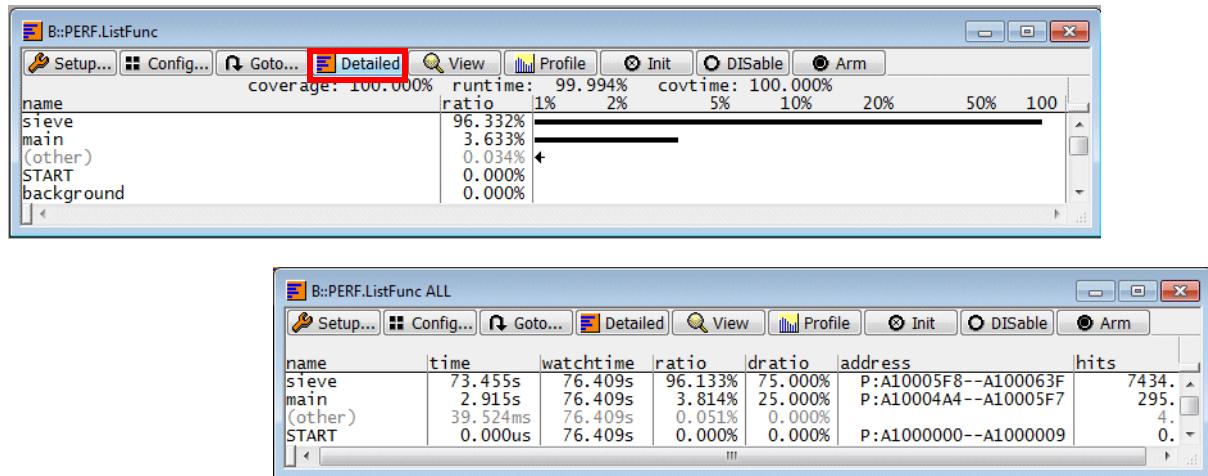
Open an HLL function profiling window

4. Start the program execution and the sampling.



In-depth Result

Push the Detailed button, to get more detailed information on the result.



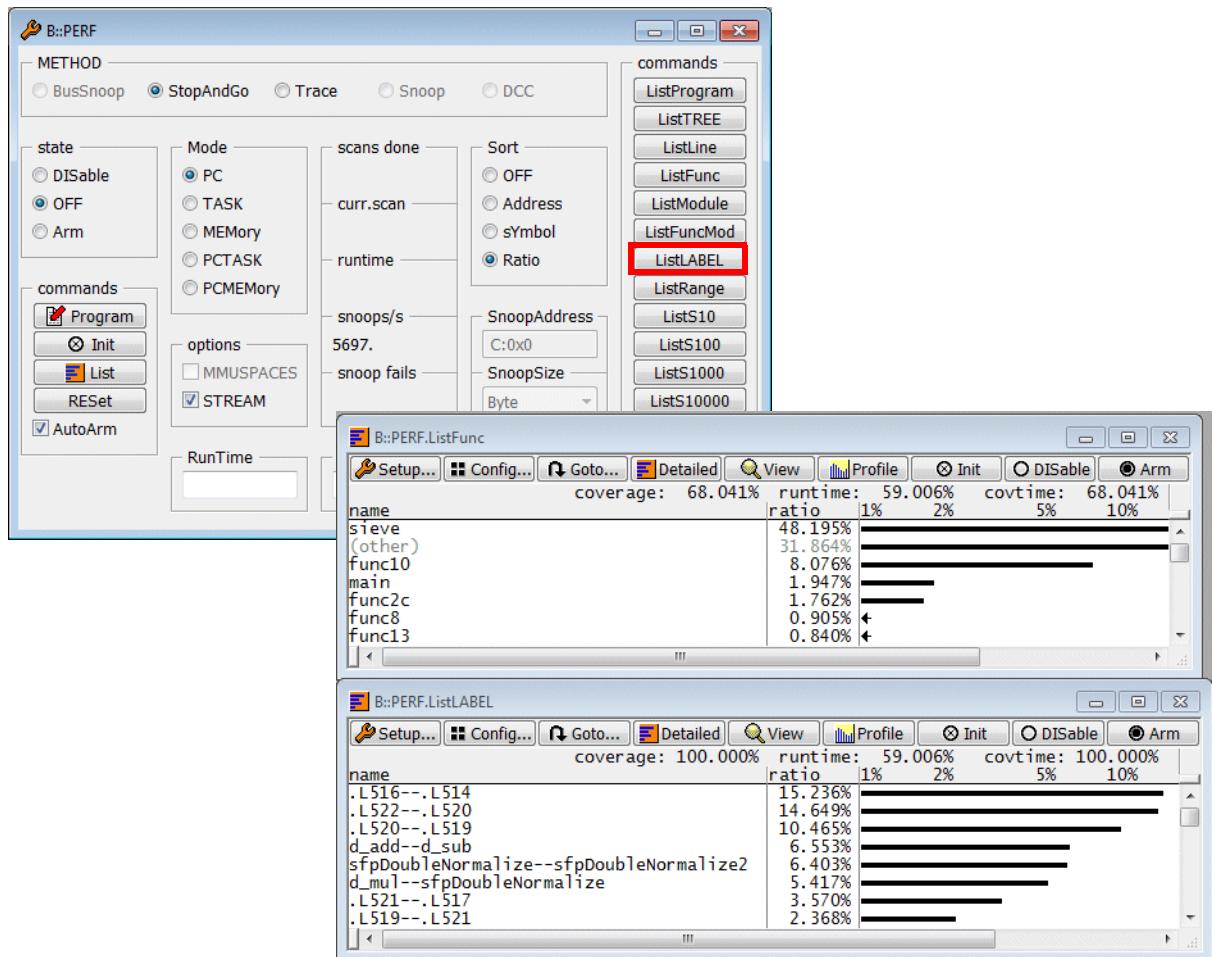
PERF.ListFunc ALL

Open a detailed HLL function profiling window

name	Function name
time	Time in function
watchtime	Time the function is observed
ratio	Ratio of time spent by the function in percent
dratio	Similar to Ratio , but only for the last second
address	Function's address range
hits	Number of samples taken for the function

(other)

TRACE32 assigns all samples that can not be assigned to a high-level language function to **(other)**. Especially if the ratio for (other) is quite high, it might be interesting what code is running there. In this case pushing the button **ListLABEL** is recommended.



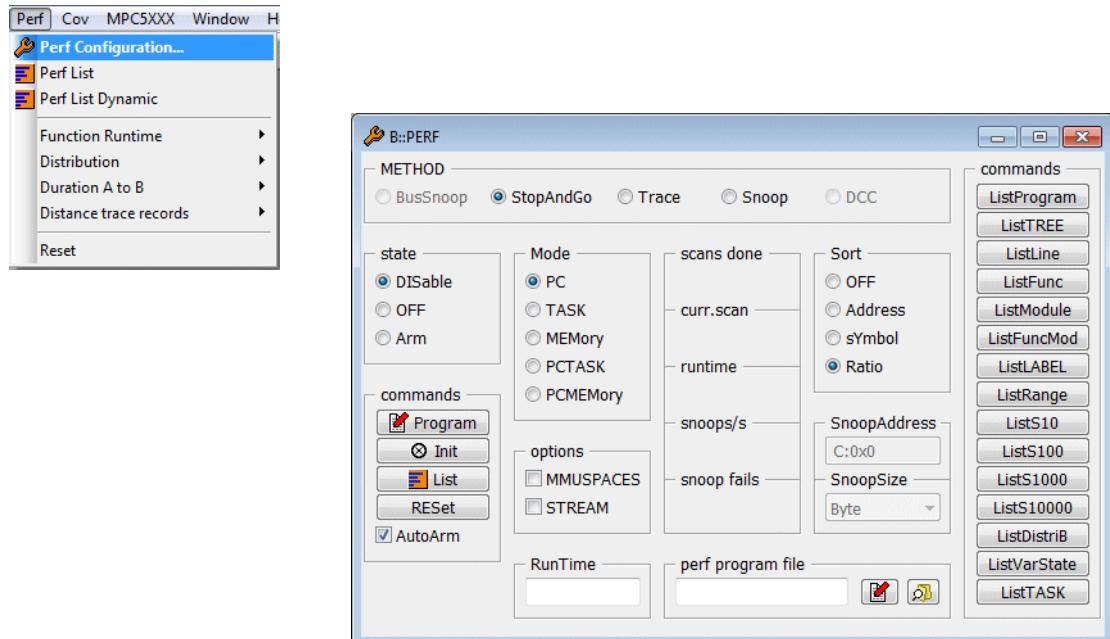
PERF.ListLABEL

Open a window for label-based profiling

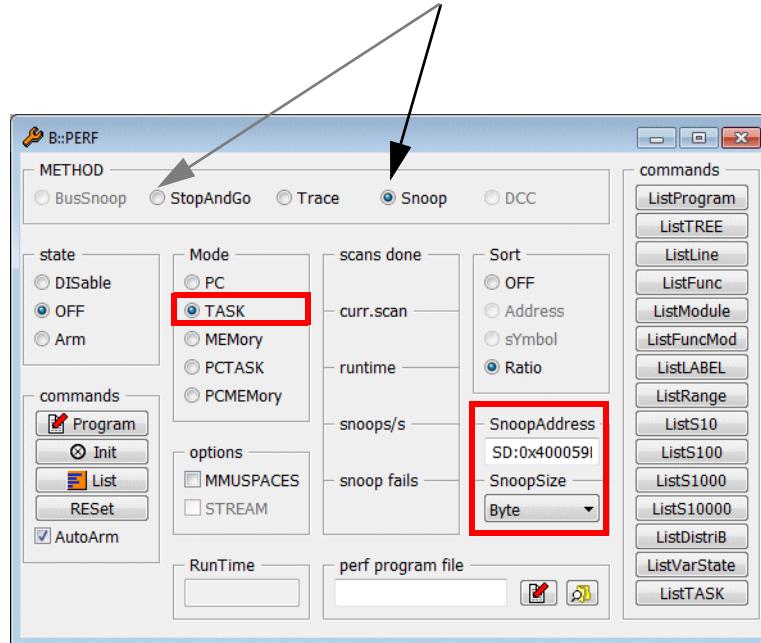
If OS-aware debugging is configured (refer to “[OS-aware Debugging](#)” in TRACE32 Glossary, page 26 (glossary.pdf)), TASK information can be sampled.

Steps to be taken:

1. Open the **PERF configuration window**.



2. Select Mode TASK.



Since every OS has a variable that contains the information which task/process is currently running, this variable has to be sampled while the program execution is running in order to perform TASK sampling.

TRACE32 fills the following fields when TASK mode is selected:

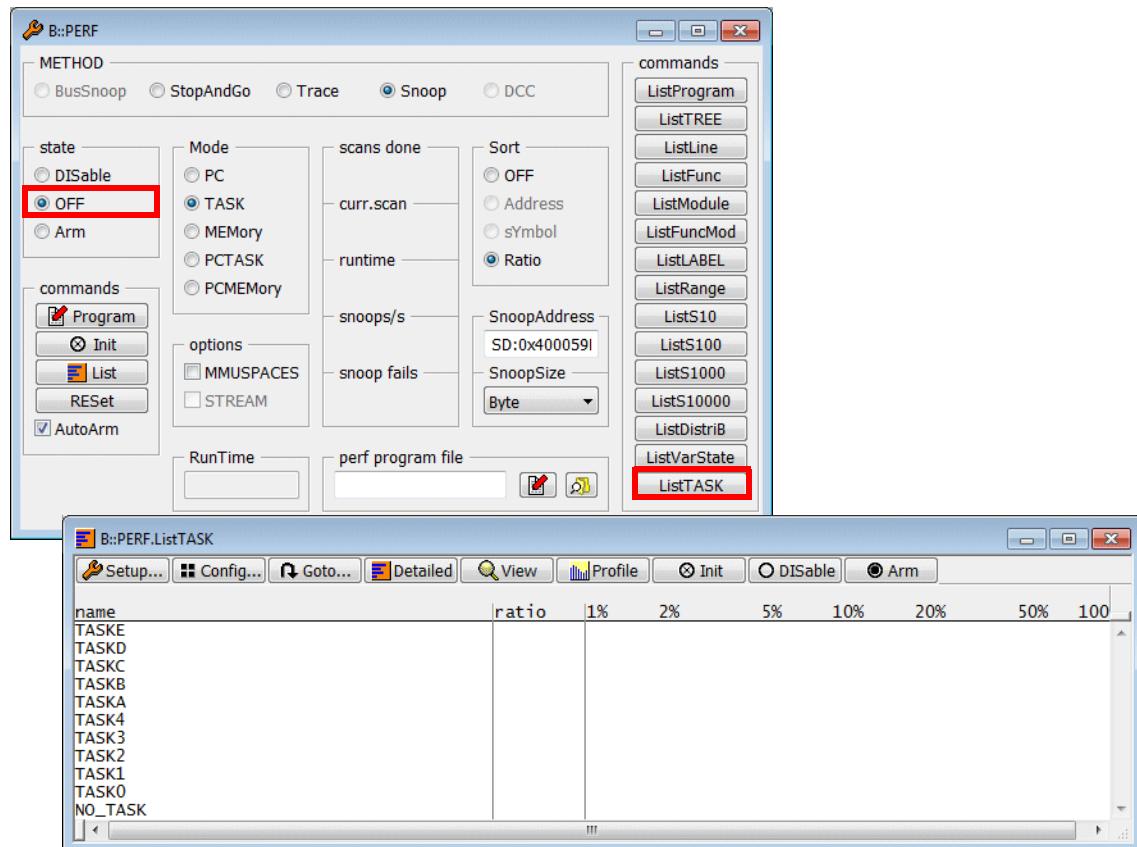
- the **SnoopAddress** field with the address of the variable.
- the **SnoopSize** field with the size of the variable.

The PERF METHOD **Snoop** is automatically selected, if the processor architecture supports reading physical memory while the program execution is running. For details refer to "["Run-time Memory Access"](#) (glossary.pdf)).

The default METHOD for all other processor architectures is **StopAndGo**.

PERF.Mode TASK

3. Enable sample-based profiling by switching to OFF state and open the result window by pushing the ListTask button.



PERF.OFF

Enable the sample-based profiling

PERF.ListTASK

4. Start the program execution and the sampling.

