Lab	Type	Tutorial
Unit : I – Fundamentals of Digital System		
1	A	Q-1 Perform the following. 1) $(32.15)_{10} = (\ )_2$ 2) $(11011.101)_2 = (\ )_{10}$ 3) $(378.93)_{10} = (\ )_8$ 4) $(4057.06)_8 = (\ )_{10}$ 5) $(2598.675)_{10} = (\ )_{16}$ 6) $(A0F9.0EB)_{16} = (\ )_{10}$ 7) $(110101.101010)_2 = (\ )_8$ 8) $(367.52)_8 = (\ )_2$ 9) $(01011111011.011111)_2 = (\ )_{16}$ 10) $(3A9E.B0D)_{16} = (\ )_2$ 11) $(756.603)_8 = (\ )_{16}$ 12) $(B9F.AE)_{16} = (\ )_8$ 13) $(-128)_{10} = (\ )_2$ 14) $(-1)_{10} = (\ )_2$
	B	Q-2 Given that $(4096)_{10} = (1000)_x$, Find the value of x.
	A	Q-3 Convert the decimal number 250.5 to base 3, base 4, base 7 & base 8.
	B	Q-4 Convert $(33.45)_{10}$ to binary. Result should be accurate to within $(0.01)_{10}$.
2	B	Q-1 Find the 10's complement of the following. 1) $(935)_{11}$ 2) $(6106)_{10}$
	B	Q-2 Add $(6E)_{16}$ and $(C5)_{16}$
	A	Q-3 Subtract $(45)_8$ from $(66)_8$
	A	Q-4 Perform the following subtraction using 2's complement method: $(11010)_2$ - $(10000)_2$
	B	Q-5 Convert $(1000\ 0110)_{BCD}$ to Decimal, Binary & Octal.
	A	Q-6 Convert the Gray code 1101 to Binary.
	A	Q-7 Find the XS-3 code of 37.
	A	Q-8 Add the following in BCD: 1) 108 + 789 2) 205.7 + 193.65
	B	Q-9 Subtract the following in BCD: 1) 86 – 24 2) 467.6 – 258.9
	B	Q-10 Add the following in XS-3: 1) 275 + 496 2) 89.6 + 273.7

Unit : II – Simplification of Logic function		
3	A	Q-1 Using laws of Boolean algebra, prove that AB + BC + A'C = AB + A'C
	A	Q-2 Show that: AB'C + B + BD' + ABD' + A'C = B + C
	B	Q-3 Show that (A+C) (A+D) (B+C) (B+D) = AB + CD
	A	Q-4 Simplify using Boolean algebra laws: F = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C
	A	Q-5 Reduce the expression using K-Map: F = $\sum_m$(0,2,3,4,5,6)
	B	Q-6 Reduce to simplest form using K-Map: F(A,B,C,D) = $\sum_m$ (0,1,2,5,8,9,10)
	A	Q-7 Reduce the Expression: F = $\prod_M$ (2,8,9,10,11,12,14)
	B	Q-8 Reduce the Expression: F = $\prod_M$ (0,1,3,4,5,6,7,13,15)
	A	Q-9 Minimize following Boolean function using K-Map: F = $\sum_m$(1,2,4,6,7,11,15)+d(0,3)
	B	Q-10 Simplify following Boolean function using K-Map: F(W,X,Y,Z) = $\sum_m$(1,3,5,8,9,11,15)+d(2,13)
	B	Q-11 Reduce the expression in SOP and POS form using K-Map: F(A,B,C,D) = $\sum_m$(1,5,6,12,13,14)+d(2,4)
4	A	Q-1 Simplify the following Boolean function by means of Tabulation method: F (A,B,C,D) = $\sum_m$(1,2,3,5,6,7,8,9,12,13,15)
	B	Q-2 Simplify the following Boolean function by means of Tabulation method: F (A,B,C,D) = $\sum_m$(0,1,3,7,8,9,11,15)
	A	Q-3 Using D as MEV, reduce Y =A'B'C'D' + A'B'CD' + AB'C'D' + AB'C'D + AB'CD + AB'CD'
	A	Q-4 Simplify the following Boolean function using VEM. F = AB'CD + A'BC'D + AB'CD' + A'B'C'D
	B	Q-5 Simplify following Boolean function using VEM. F = A'B'C'D + A'BC'D' + A'BC'D + AB'C'D' + AB'CD' + AB'CD + ABCD'
	A	Q-6 Using E as the MEV, reduce F = A'B'C'D'E + A'B'C'DE + A'BCD'E' + A'BCD'E + AB'C'D'E' + AB'C'D'E + AB'C'D + A'BCDE'
	B	Q-7 Using C & D as MEVs, reduce Y = A'B'C'D' + A'B'C'D + A'B'CD' + A'BCD + ABCD + AB'CD

Unit : III – Combinational Digital Circuits		
5	A	Q-1 Minimize the logic function X = A (B'+C') (A+D). Also realize the reduced function using NOR gates only.
	B	Q-2 Simplify using Boolean laws and draw the logic diagram for the given expression. F = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C
	A	Q-3 Reduce the expression F = ∑m (0,2,3,4,5,6) using K-map and implement using NAND gates only.
	A	Q-4 Implement following Boolean function using 8 : 1 multiplexer. Y (A,B,C,D) = ∑m (15,7,4,6,8,9,12,14)
	B	Q-5 Implement following Boolean function using 8 : 1 multiplexer. F (A,B,C,D) = ∑m (2,3,5,7,8,9,12,13,14,15)
	A	Q-6 Implement following Boolean function using 4 : 1 multiplexer. F (A,B,C) = ∑m (1,3,5,6)
	B	Q-7 Implement following Boolean function using 4 : 1 multiplexer. F (A,B,C) = ∑m (1,2,4,7)
Unit : IV – Sequential Digital Circuits		
6	A	Q-1 Design 3-bit ripple up-counter using negative edge JK Flip-flops. Also draw waveform.
	B	Q-2 Design 4-bit ripple up-counter using negative edge JK Flip-flops.
	B	Q-3 Design Modulo-8 counter using T Flip-flops.
	A	Q-4 Design Mod-10 (Decade) Counter using T Flip-flops.
7	A	Q-1 Design a counter to generate the repetitive sequence 0, 3, 5, 7, 4 using D Flip-flop.
	B	Q-2 Design a counter to generate the repetitive sequence 0, 1, 2, 4, 3, 6 using T Flip-flop.
	A	Q-3 Design 3-bit synchronous up counter using T Flip-flop.
	B	Q-4 Design a synchronous BCD counter with JK Flip-flop.