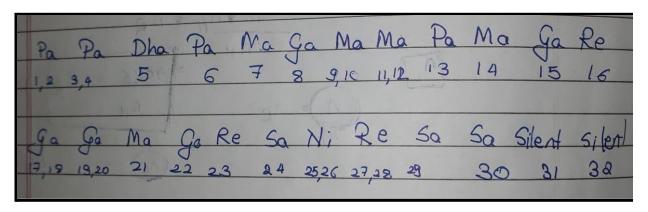
# **Experiment 6: Music Synthesizer**

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### Overview of the experiment:

In this experiment, we played music using the notes which were introduced in the class. The notes are given in a particular sequence like in music. We were needed to use FSM to automate such that notes will be played one after another in the given sequence and for a particular duration.

This is the table that was needed to follow



In this, each count corresponds to 0.25 seconds.

We also needed to make a clock(clock\_music) with a frequency of 4 Hz(1/0.25s) from the master clock of 50MHz.

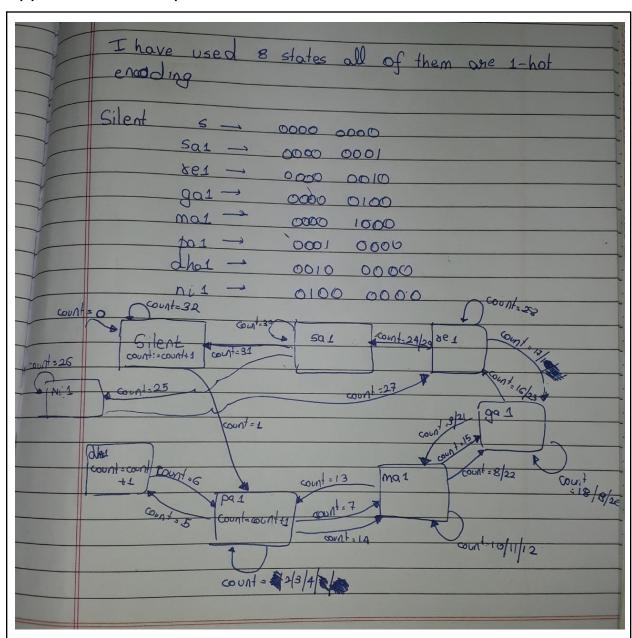
All the state transition and everything will happen at the rising edge of clock music These distinct notes will be the states of the FSM. There will be an initial state(reset) which is the silent state.

At reset, the count will be 0, thereafter, at the first rising edge of the clock music, the count is incremented to 1 and the note Pa, will be played, for the second rising edge the count value gets incremented to 2, however, the corresponding note is again 'Pa'. At the fifth rising edge of the clock music, when the count is incremented to 5, the note 'Dha' should be played..and this will be continued.

## State Table:-

| Count | Present State | Next state |
|-------|---------------|------------|
| 1     | Pa            | Pa         |
| 2     | Pa            | Pa         |
| 3     | Pa            | Pa         |
| 4     | Pa            | Dha        |
| 5     | Dha           | Pa         |
| 6     | Pa            | Ма         |
| 7     | Ма            | Ga         |
| 8     | Ga            | Ма         |
| 9     | Ма            | Ма         |
| 10    | Ма            | Ма         |
| 11    | Ма            | Ма         |
| 12    | Ма            | Pa         |
| 13    | Pa            | Ма         |
| 14    | Ма            | Ga         |
| 15    | Ga            | Re         |
| 16    | Re            | Ga         |
| 17    | Ga            | Ga         |
| 18    | Ga            | Ga         |
| 19    | Ga            | Ga         |
| 20    | Ga            | Ма         |
| 21    | Ма            | Ga         |
| 22    | Ga            | Re         |
| 23    | Re            | Sa         |
| 24    | Sa            | Ni         |
| 25    | Ni            | Ni         |
| 26    | Ni            | Re         |
| 27    | Re            | Re         |
| 28    | Re            | Sa         |
| 29    | Sa            | Sa         |
| 30    | Sa            | Silent     |
| 31    | Silent        | Silent     |
| 32    | Silent        | Reset      |
|       |               |            |

### Approach to the experiment:



## Design document and VHDL code if relevant:

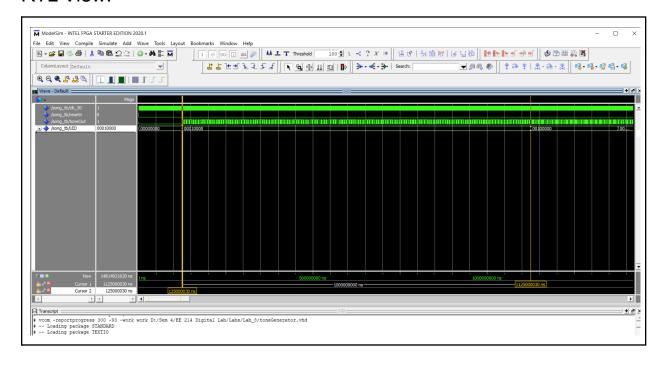
```
architecture fsm of music is
-- Fill all the states
type state type is (Silent,sa,re,ga,ma,pa,dha,ni);
signal y_present : state_type:=Silent;
signal count
                 : integer
signal clock_music
                        : std_logic:='0';
constant s:std logic vector(7 downto 0):=(others=>'0');
constant sa1 : std logic vector(7 downto 0):=(0=>'1', others=>'0');
constant re1 : std logic vector(7 downto 0):=(1=>'1', others=>'0');
constant ga1 : std logic vector(7 downto 0):=(2=>'1', others=>'0');
constant ma1 : std_logic_vector(7 downto 0):=(3=>'1', others=>'0');
constant pa1 : std logic vector(7 downto 0):=(4=>'1', others=>'0');
constant dha1: std logic vector(7 downto 0):=(5=>'1', others=>'0');
constant ni1 : std logic vector(7 downto 0):=(6=>'1', others=>'0');
signal switch
                        : std logic vector(7 downto 0):=s;
component toneGenerator is
port (toneOut : out std logic; --this pin will give your notes output
clk: in std logic;
LED: out std logic vector(7 downto 0):
switch: in std logic vector(7 downto 0));
end component;
begin
        process(clk 50,resetn,y present,count,clock music)
                                                                 -- Fill sensitivity list
        variable y_next_var : state_type := Silent;
        variable n count : integer := 0;
        variable timecounter: integer range 0 to 1E8 := 0;
                                         : std_logic:='0';
        variable clk c
        begin
                y_next_var := y_present;
                n_count := count;
                case y_present is
                        when Silent=>
                                 switch<=s:
                                 if(count = 0) then
                                         y next var:=pa;
                                         n count := count + 1;
                                 elsif(count = 31) then
                                         y_next_var:=Silent;
                                         n count:=count+1;
                                 elsif(count = 32) then
                                         y_next_var:=pa;
                                         n count:=1;
                                 else
                                         y_next_var:=pa;
```

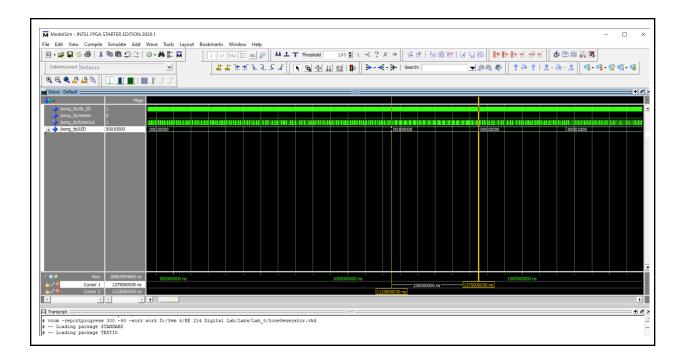
```
n_count:=1;
        end if;
WHEN sa => --if the machine in Sa state
        switch<=sa1;
        if((count = 24)) then
                y_next_var:=ni;
                n_count := count + 1;
        elsif(count=29) then
                y_next_var:= sa;
                n_count := count + 1;
        elsif(count = 30) then
                y_next_var:=Silent;
                n_count := count + 1;
        else
                y_next_var:=sa;
                n_count:=count+1;
        end if;
WHEN re =>
        switch<=re1;
        if(count = 16) then
                y_next_var:=ga;
                n_count := count + 1;
        elsif((count = 23) or (count = 28)) then
                y_next_Var:=sa;
                n_count := count + 1;
        elsif(count = 27) then
                y_next_var:=re;
                n_count := count + 1;
        end if;
WHEN ga =>
        switch<=ga1;
        if(count = 8) then
                y_next_var:=ma;
                n count := count + 1;
        elsif((count = 15) or (count = 22))then
                y_next_Var:=re;
                n count := count + 1;
        elsif((count = 17) \text{ or } (count = 18) \text{ or } (count = 19)) \text{ then}
                y_next_var:=ga;
                n_count := count + 1;
        elsif(count = 20) then
                y_next_var:=ma;
                n_count:=count+1;
        end if;
        WHEN ma =>
```

```
switch<=ma1;
                if((count = 7) \text{ or } (count = 14) \text{ or } (count = 21)) \text{ then}
                         y_next_var:=ga;
                         n_count := count + 1;
                elsif((count = 9) or (count = 10) or (count = 11))then
                         y_next_Var:=ma;
                         n_count := count + 1;
                elsif((count = 12)) then
                         y_next_var:=pa;
                         n_count := count + 1;
                end if;
                WHEN pa =>
                switch<=pa1;
                if((count = 1) or (count = 2) or (count = 3)) then
                         y_next_var:=pa;
                         n_count := count + 1;
                elsif((count = 4))then
                         y_next_Var:=dha;
                         n_count := count + 1;
                elsif((count = 6) or (count = 13)) then
                         y_next_var:=ma;
                         n count := count + 1;
                end if;
                WHEN dha =>
                switch<=dha1;
                if((count = 5)) then
                        y_next_var:=pa;
                         n_count := count + 1;
                end if;
                WHEN ni =>
                switch<=ni1;
                if((count = 25)) then
                         y_next_var:=ni;
                         n_count := count + 1;
                elsif((count = 26))then
                         y_next_Var:=re;
                         n_count := count + 1;
                end if;
        WHEN others =>
                                 y_next_var:=Silent;
                                 n count:=0;
END CASE;
if (clk_50 = '1' and clk_50' event) then
        if (resetn = '0') then
                if timecounter = 6250000 then -- The cycles in which clk is 1 or 0
```

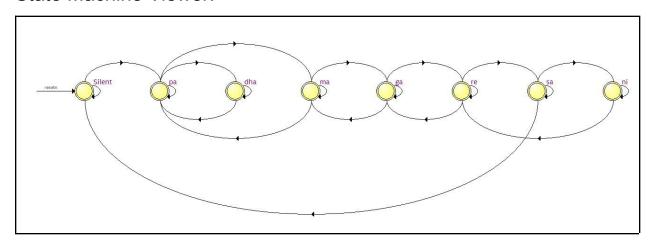
```
timecounter := 1;
                                                                                     -- When it reaches
max count i.e. 25x10<sup>6</sup> (half a second) it will be 0 again
                                           clk_c := not clk_c;
                                                                            -- this variable will toggle
                                  else
                                           timecounter := timecounter + 1; -- Counter will be incremented
till it reaches max count
                                  end if;
                          elsif resetn = '1' then
                                  timecounter := 1;
                                  clk c := '0';
                         end if;
                 end if:
                 clock_music <= clk_c;
                 if(resetn = '1') then
                         y_present<= Silent;</pre>
                          count<=0;
                          elsif(clock_music = '1' and clock_music' event) then
                                  y_present<=y_next_var;</pre>
                                  count <=n count;
                 end if;
        end process;
        : toneGenerator port map(toneOut=>toneOut,clk=>clk_50,LED=>LED,switch=>switch);
end fsm;
```

#### RTL View:





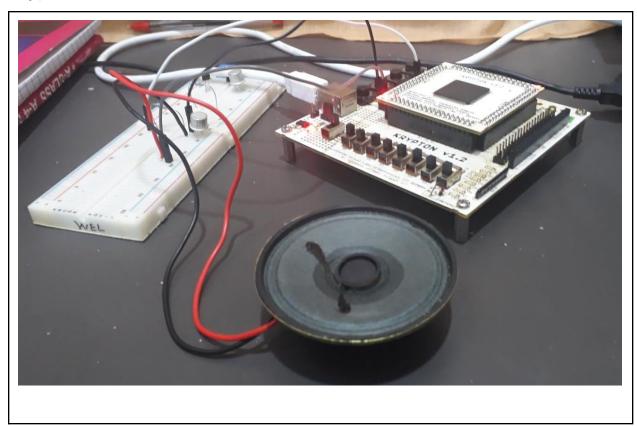
### State Machine Viewer:-



## Gate-level Simulation:



# Krypton board\*:



## Observations\*:

Video can be seen here