

# EE 618 Course Project

## Report

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1.1

## Second - stage design -

CMPB is implemented using two emitters (like  $R_1$  &  $R_2$ )  
 (say  $R_3$  &  $R_4$ )

The gain of the second stage is

$$g_{m10} (r_{o10} \parallel r_{o12} \parallel r_{o14} \parallel r_{o16} \parallel R_3)$$

where  $r_{o16}$  is the output resistance of  $I_{B3}$ .

Target second stage gain = 5. Assuming  $R_3$  is very large,

$$\Rightarrow g_{m10} \left( \frac{1}{d_p I_{10} + d_n I_{12} + d_p I_{14} + d_n I_{16}} \right) = 5 \quad (\because g_{ds} = d I)$$

Now, by KCL,  $I_{10} + I_{14} = I_{12} + I_{16}$ .

$$\text{So } \frac{g_{m10}}{(d_p + d_n)(I_{10} + I_{14})} = 5$$

from simulation,  $\Delta p \approx 0.8$  &  $\Delta n \approx 0.376$

choose  $I_{D0} + I_{D4} = 0.8 \mu A$

Then, previous eq<sup>n</sup> gives  $g_{m10} = 5.29 \times 10^{-3} \text{ A/V}^2$

$$\Rightarrow \sqrt{\frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_{10}} = 5.292 \times 10^{-3}$$

$$\Rightarrow I_{D0} \left( \frac{W}{L} \right)_{10} = 0.22 \quad (\text{Assuming } \mu_p C_{ox} = 63 \times 10^{-6})$$

Also,  $|V_{GS1}|_{10} = |V_{GS7_2}| = 0.1$

$$\Rightarrow \sqrt{\frac{2 I_{D0}}{\mu_p C_{ox} \left( \frac{W}{L} \right)_{10}}} = 0.1$$

$$\Rightarrow \frac{I_{D0}}{\left( \frac{W}{L} \right)_{10}} = 3.15 \times 10^{-7}$$

So, we get,  $I_{D0} = 264.6 \mu A \Rightarrow I_{D4} = 635.4 \mu A$

$$\& \left( \frac{W}{L} \right)_{10} = 840.$$

choose  $L_{10} = 0.15 \mu m \Rightarrow W_{10} = 126 \mu m$

Now, choose  $V_{GS7_{12}} = 0.1$  &  $I_{D2} = 450 \mu A$

$$\Rightarrow \left( \frac{W}{L} \right)_{12} = 618 \quad (\mu_n C_{ox} = 145.6 \times 10^{-6})$$

so,  $L_{12} = 0.15 \mu m, W_{12} = 92.7 \mu m$

Now, the output common mode should be 0.75 V

&  $I_{D4} = 635.4 \mu A$ .  $V_{Thp} = 0.294$  from simulation

$$\Rightarrow \frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_{14} (1.5 - 0.75 - 0.294)^2 = 635.4 \times 10^{-6}$$

$$\Rightarrow \left( \frac{W}{L} \right)_{14} = 97$$

$$\Rightarrow L_{14} = 0.15 \mu m, W_{14} = 14.55 \mu m$$

Transistors M<sub>3</sub>, M<sub>9</sub>, M<sub>11</sub>, M<sub>13</sub> have similar sizes.

for M<sub>16</sub>, we can adjust the size based on the current-mirror-diode-connected transistor to get  $I_{16} = 450 \times 10^{-6} A$

### First-stage design -

First, allocate a  $N_{GST}$  of 0.1 each for M<sub>5</sub>-M<sub>8</sub> & 0.2 each for M<sub>1</sub>-M<sub>4</sub> & the transistor corresponding to  $I_B$ .

$$\text{Gain} = A_V = \frac{g_m, r_{o3}^2 g_m, (g_m r_{o5} r_{o7}) || R_1)}{g_m r_{o1} r_{o3} + (g_m r_{o5} r_{o7}) || R_1)}$$

assuming  $R_1 \gg g_m r_{o5} r_{o7}$  & that  $g_m r_{o1} r_{o3} \approx g_m r_{o5} r_{o7}$ , we get

$$A_V \approx \frac{g_m, g_m r_{o5} r_{o7}}{2}$$

$$\text{Target } A_V \approx 800 \text{ V/V}$$

$$\Rightarrow g_m, g_m r_{o5} r_{o7} = 1600$$

Also, choose  $I_{B1} = 0.9 \text{ mA}$

$$\text{Now, for M1-M4, } \mu_n C_{ox} \left( \frac{W}{L} \right)_{1-4} (0.2)^2 = 0.45 \times 10^{-3}$$

$$\Rightarrow \left( \frac{W}{L} \right)_{1-4} \approx 77$$

likewise,  $\left( \frac{W}{L} \right)_{5-8} \approx 721$  (current through them is  $0.45 \text{ mA}$  too)

let  $L_{1-4} = 0.4 \mu\text{m} \Rightarrow W_{1-4} = 30.8 \mu\text{m}$   
 $L_{5-8} = 0.4 \mu\text{m} \Rightarrow W_{5-8} = 288.4 \mu\text{m}$

Now, for  $I_{B1}, |N_{GST}| = 0.1 \Rightarrow \left( \frac{W}{L} \right)_{B1} = 154$   
 $\& I_{B1} = 0.9 \text{ mA}$

choose  $L_{B1} = 0.4 \mu\text{m} \Rightarrow W_{B1} = 61.6 \mu\text{m}$

Also,  $R1 = R2 = R3 = R4 = 4 \text{ M}\Omega$

### Bias voltages -

$$V_{B_3} - V_{T_n} = 0.1 \quad (V_{GST1,2} = 0.1) \\ \Rightarrow V_{B_3} = 0.1 + V_{T_n} \\ \Rightarrow \boxed{V_{B_3} = 0.46 \text{ V}}$$

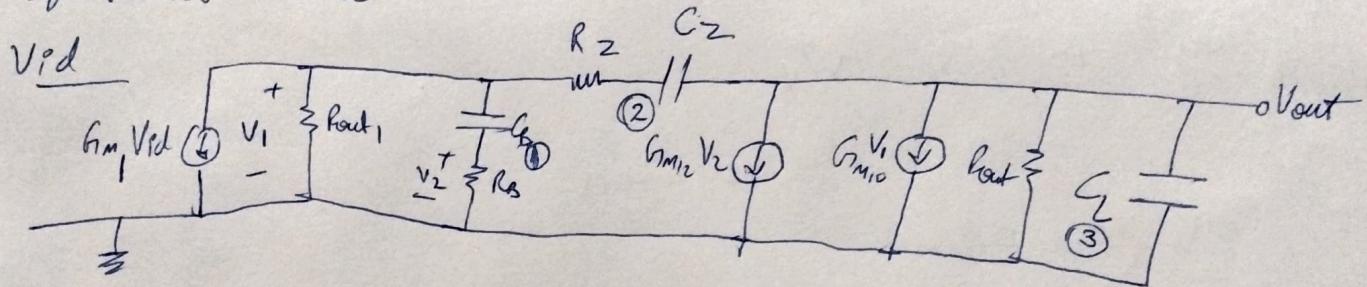
Now,  $V_{B_{1, \text{min}}} = 0.2 + 0.2 + 0.2 + V_{T_n} = 0.86 \text{ V}$

$$V_{B_{2, \text{max}}} = 1.5 - 0.1 - 0.1 - V_{T_P} \approx 1 \text{ V}$$

So, choose  $\boxed{V_{B_2} = 1 \text{ V} \text{ & } V_{B_1} = 1.1 \text{ V}}$

### Frequency Compensation -

Equivalent Model -



$$C_1 \equiv C_B, \quad C_2 \equiv C_2, \quad C_3 \equiv C_L$$

Here,  $R_{\text{out},1}$  is o/p resistance of first stage,  $R_{\text{out}}^1$  is o/p resistance of second stage &  $G_{m1}R_{\text{out},1}$  is gain of first stage.

Ignoring transistor parameter capacitances.

Now,

$$\gamma_1^0 = (R_B + R_{\text{out},1})C_B$$

$$\gamma_2^0 = (R_2 + R_{\text{out},1} + R_{\text{out}}^1 + G_{m1,10}R_{\text{out},1}R_{\text{out}}^1)C_2$$

$$\gamma_3^0 = R_{\text{out}}^1 C_L = \gamma_3^1$$

$$\gamma_2^1 = (R_2 + R_{\text{out},1} \parallel R_B + R_{\text{out}}^1 + (G_{m1,10} + G_{m1,12})(R_{\text{out},1} \parallel R_B)R_{\text{out}}^1)C_2$$

$$\gamma_3^2 = \left( \frac{R_2 + R_{\text{out},1}}{1 + G_{m1,10}R_{\text{out},1}} \parallel R_{\text{out}}^1 \right) C_L$$

Now, generally,

$$R_B \approx R_2 < R_{out} < R_{out},$$

$$\& C_B \approx C_2 < C_L \quad \& G_{m10} \approx G_{m12}$$

So,  $\gamma_1^0 \approx R_{out}, C_B$

$$\gamma_2^0 \approx G_{m10} R_{out}, R_{out} < C_2$$

$$\gamma_3^0 = \gamma_3' = R_{out} C_L$$

$$\gamma_2' \approx (G_{m10} + G_{m12}) R_B R_{out} C_2$$

$$\& \gamma_3^2 \approx \frac{C_L}{G_{m10}}$$

So, denominator of transfer function is

$$s^3 + (\gamma_1^0 + \gamma_2^0 + \gamma_3^0)s^2 + (\gamma_1^0 \gamma_2' + \gamma_1^0 \gamma_3' + \gamma_2^0 \gamma_3^2)s + (\gamma_1^0 \gamma_2' \gamma_3^2)$$

where roots are  $\frac{1}{P_1}, \frac{1}{P_2} \& \frac{1}{P_3}$

Let  $P_1 \ll P_2 \ll P_3$

Then,  $\left| \frac{1}{P_1} + \frac{1}{P_2} + \frac{1}{P_3} \right| \approx \left| \frac{1}{P_1} \right| = \gamma_1^0 + \gamma_2^0 + \gamma_3^0$

$$\Rightarrow |P_1| = (\gamma_1^0 + \gamma_2^0 + \gamma_3^0)^{-1}$$

4  $\left| \frac{1}{P_1 P_2} + \frac{1}{P_2 P_3} + \frac{1}{P_3 P_1} \right| \approx \frac{1}{|P_1 P_2|} = \gamma_1^0 \gamma_2' + \gamma_1^0 \gamma_3' + \gamma_2^0 \gamma_3^2$

$$\Rightarrow |P_2| = \frac{\gamma_1^0 + \gamma_2^0 + \gamma_3^0}{\gamma_1^0 \gamma_2' + \gamma_1^0 \gamma_3' + \gamma_2^0 \gamma_3^2}$$

4  $\frac{1}{|P_1 P_2 P_3|} = \gamma_1^0 \gamma_2^0 \gamma_3^0$

$$\Rightarrow |P_3| = \frac{\gamma_1^0 \gamma_2' + \gamma_1^0 \gamma_3' + \gamma_2^0 \gamma_3^2}{\gamma_1^0 \gamma_2^0 \gamma_3^0}$$

Substituting ~~&~~  $\chi$ 's in the expression, we get

$$P_1 \approx \frac{1}{G_{m10} R_{out} R_{out}, C_2} = 2\pi f_{3dB}$$

$$\& P_2 = \frac{G_{m10} C_2}{(G_{m10} + G_{m2}) R_B C_2 + C_L (C_B + C_2)}$$

&  $P_3$  can be ignored as it's far away

Now, zeros -

for  $V_{out} = 0$ . Then no current will flow through  $R_{out}$  &  $C_2$ .

$$\Rightarrow V_1 = (G_{12} V_2 + G_{10} V_1) \left( R_2 + \frac{1}{sC_2} \right)$$

$$\& V_2 = \frac{R_B}{R_B + \frac{1}{sC_B}} V_1$$

$$\Rightarrow I = \left( \frac{s G_{12} R_B C_B}{1 + s R_B C_B} + G_{10} \right) \left( R_2 + \frac{1}{sC_2} \right)$$

$$\Rightarrow s^2 \left( R_B C_B C_2 (G_{m10} + G_{m12}) R_2 \right) \\ + s (R_B C_B (G_{m10} + G_{m12}) + G_{m10} R_2 C_2) + G_{m10} = 0$$

$$\text{Now, coeff. of } s^2 \approx 10^3 \times 10^{-15} \times 10^{-15} \times 10^{-3} \times 10^3 \approx 10^{-27}$$

$$\text{coeff. of } s \approx 10^3 \times 10^{-15} \times 10^{-3} \approx 10^{-15}$$

~~$\text{coeff. of const.}$~~   $\approx 10^{-3}$

So, coeff. of  $s^2$  can be ignored.

$$\text{So, } |\omega_z| = \frac{G_{m10}}{R_B C_B (G_{m10} + G_{m12}) + G_{m10} R_2 C_2}$$

the other zeros will be far ~~away~~ away.

Now, place  $P_2 = \omega_2$

$$\Rightarrow \frac{G_{m10} C_2}{(G_{m10} + G_{m12}) R_B C_B C_2 + C_2 (C_B + C_2)} = \frac{G_{m10}}{R_B C_B (G_{m10} + G_{m12}) + G_{m10} C_2 C_2}$$

$$\Rightarrow C_L (C_B + C_2) = G_{m10} R_2 C_2^2$$

Now, for  $f_{UGF} = 1.2 \text{ GHz}$  & dc gain = 70 dB,

$$\xrightarrow{-20 \text{ dB/dec slope}} -20 = \frac{70 - 0}{\log \left( \frac{P_1}{1.2 \times 2\pi \times 10^9} \right)}$$

$$\Rightarrow P_1 = 2.384 \text{ mW rad s}^{-1}$$

$$\text{So, } \frac{1}{G_{m10} R_{\text{out}} R_{\text{out}} C_2} = P_1 = 2.384 \times 10^6$$

$$\Rightarrow C_2 = \frac{1}{(G_{m10} R_{\text{out}}) 2.384 \times 10^6 \times R_{\text{out}}}$$

↑  
 ~~$R_1 \parallel g_{m3} r_{o3} r_{o1} \parallel g_{m4} r_{o5} r_{o2}$~~

gain of 2<sup>nd</sup> stage = 5

$$\begin{aligned} & R_1 \parallel g_{m3} r_{o3} r_{o1} \parallel g_{m4} r_{o5} r_{o2} \\ & \approx \frac{g_{m3} r_{o3} r_{o1}}{g_{m4} r_{o5} r_{o2}} \\ & \approx 251.85 \text{ k}\Omega \end{aligned}$$

for  $P_2 = \omega_2$ ,

$$C_L (C_B + C_2) = G_{m10} R_2 C_2^2$$

putting  $C_L = 0.15 \mu\text{F}$ ,  $C_2 = 0.33 \mu\text{F}$  &  $g_{m10} \approx 5.21 \times 10^{-3} \text{ A}^{-1}$ , we get

$$C_B + 0.33 \times 10^{-12} = 5.21 \times 10^{-15} R_2$$

$$\text{choose } C_B \approx 0.05 \mu\text{F} \Rightarrow R_2 = 249.7 \text{ k}\Omega$$

for  $R_B$ , a decent value of  $10 \text{ k}\Omega$  works

1.2

## Iterations

### Main Pseudo A-B Amplifier

First we targeted DC gain and later moved on to frequency Compensation |u GF | Slew Rate

The value of  $R_2, C_2, R_b, C_b$  were very flexible since it affected our DC gain very less.  
So the 1<sup>st</sup> target was to satisfy DC gain.

In our 1<sup>st</sup> iteration, we achieved DC gain [79dB] but slew Rate was about 66 v/us and setting time was beyond required condition [159 ns].

The values of Main Telescopic weren't changed much since DC gain was achieved.

We tried then changing the values of  $C_2, R_2, C_b, R_b$  & the current passing through AB amplifier & output stage.

Theoretical	Simulation
$C_2 \approx 0.33 \text{ pF}$	$C_2 \approx 50 \text{ fF}$
$C_b \approx 0.05 \text{ pF}$	$C_b = 100 \text{ pF}$
$R_2 = 248.7 \Omega$	$R_2 = \cancel{4} \text{ k}\Omega$
$R_b = 10 \text{ k}\Omega$	$R_b = 100$

$C_2, R_2$  were sensitive due to miller effect while  $R_b, C_b$  were not that much for the simulations that we ran.

We tried to keep all capacitors as small as possible to get higher slew rate.

The  $M_9 M_{10}$   $w/L$  was also decreased to decrease  $g_m \rightarrow$  To decrease miller effect.  
It went from  $90/0.15 \rightarrow 30/0.15$ . [In final iteration]

Initially we used ideal voltage & current sources but after creating them through diode connected & current mirror, they weren't exact &  $V_{b3}$  was changing at higher frequency due to loading

This changed our values a lot, so again we had to tweak  $w/L$  of transistors. The voltage swing had to be resolved 1<sup>st</sup>.

We took  $C_2 = \cancel{1}$  in 2<sup>nd</sup> iteration to be 1 pF

Our UGF increased from 1.001 GHz to 1.09 GHz  
Phase margin from  $108^\circ$  to  $72.28^\circ$

Slew Rate was ↑ a lot from 3.66 V/us to 37.2 V/us.  
 $w/L$  of  $M_9$  decreased from  $90/0.15 \rightarrow 75/0.15$

### 3<sup>rd</sup> Iteration

The value of  $\zeta$  was further reduced from 1 pF to 0.55 pF &  $C_b$  from loop to 0.06 pF  
 $w/l$  of  $M^9$  decreased from  $75/6.15 \rightarrow 30/6.15$   
 $R_z$  value decreased ~~from 370~~  $\rightarrow 370$

UGF  $\uparrow$  to 1.21 GHz  
 Phase margin  $\downarrow$  to ~~59~~ 59

Slew Rate  $\uparrow$  to 406 V/us.

Settling Time = 3.79 ns.

$V_{b1}$ ,  $V_{b2}$ ,  $V_{b3}$  values were tweaked. The w was ~~made~~ changed to achieve high accuracy between ideal & practical

### Final Iteration

Phase Margin went to  $60.82^\circ$

UGF  $\uparrow$  to 1.24 GHz

Settling Time  $\rightarrow$  3.9 ns

Slew Rate  $\rightarrow$  ~~403~~ 403 V/us.

# 1 Iterations of Pseudo Class AB Amplifier

## 1.a Target Specifications

	Iteration1	Iteration2	Iteration3	Final Iteration
DC gain(dB)	79.2	79.64	76.8	76.24
Phase margin	108.95°	72.28°	58.53°	60.69°
UGF(Ghz)	1.001	1.09	1.21	1.24
Slew Rate(V/uS)	66.61	37.2	406	403.41
1% Settling time(ns)	159	-	3.79	3.90

## 1.b Values of parameters

	Iteration1	Iteration2	Iteration3	Final Iteration
$R_b$	100Ω	100Ω	10kΩ	10kΩ
$C_b$	100pF	100pF	0.06pF	0.06pF
$R_z$	4kΩ	4kΩ	370Ω	370Ω
$C_z$	50pF	1pF	0.55pF	0.55pF
$(\frac{W}{L})_{M_9}$	90/0.15	75/0.15	30/0.15	30/0.15



## 1.4

Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	30.8	0.4
M2	30.8	0.4
M3	30.8	0.4
M4	30.8	0.4
M5	180.25	0.25
M6	180.25	0.25
M7	180.25	0.25
M8	180.25	0.25
M9	30	0.15
M10	30	0.15
M11	10	0.15
M12	10	0.15
M13	5	0.15
M14	5	0.15

Table: Sizes of transistors in Main Amplifier

## Auxiliary circuit design -

2.1

First stage -

Gain of first stage =  $g_m R_i$

When  $\Delta V_{in} = \sqrt{\frac{2I_B}{\mu_n C_{ox}(\frac{W}{L})_{1,2}}}$ , the current gets steered to just one side

Eq 4.114 in Chapter 4 of Razavi

We choose  $\Delta V_{in} = 20mV$  &  $I_B = 200\mu A$

From simulation, we found  $\mu_n C_{ox} = 1.538 \times 10^{-3}$

$$\Rightarrow \left(\frac{W}{L}\right)_{1,2} \approx 650$$

$$\Rightarrow \boxed{L_{1,2} = 0.2\mu m \text{ & } W_{1,2} = 130\mu m}$$

To let  $V_{DD} - I_B R_i$  reach 0, choose  $R_i = 7.5 k\Omega$

## Second stage

To let MP1-2 & MN1-2 be in subthreshold,

$$\text{choose } V_{Bp} = V_{DD} - V_{Thp} \cong 1.5 - 0.3 = 1.2 \text{ V}$$

$$\& V_{BN} = V_{Thn} = 0.36 \text{ V}$$

To deliver a peak current of 1mA,

$$\frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_p (V_{DD} - V_{Thp}) = 10^{-3} \quad (\text{when gate dropt} \downarrow \text{from } V_{DD})$$

$$= 1 \left( \frac{W}{L} \right)_p = 4.67 \quad (\mu_p C_{ox} = 3.07 \times 10^{-4} \text{ from simulations})$$

Why,  $\left( \frac{W}{L} \right)_N = 1.13$

$$\text{choose } L_p = L_N = 0.25 \mu\text{m}$$

$$\& W_p = 1.17 \mu\text{m} \& W_N = 0.28 \mu\text{m}$$

From  the paper,

$$\omega_{P_2} = \frac{1}{R_1(C_{P_1} + C_B)} \gg \frac{1}{R_2 C_B} = \omega_{P_1}$$

$$= 1 \frac{R_2 C_B}{R_1(C_{P_1} + C_B)} \gg 1$$

$$C_{P_1} + C_B \approx fF, \text{ choose } C_B = 2pF$$

$$R_1 = 2.5 k\Omega, \text{ choose } R_B = 10 k\Omega.$$

2.2

I IterationAuxiliary Circuit

→ After completing design of Pseudo Class AB Amplifiers we designed Auxiliary Circuit. We decided to tune only Auxiliary Circuit, since disturbing Pseudo Class AB would change all previous Parameters/Target Specifications.

Here we first make the outer AB amplifier to be close to subthreshold region. We also need to take care that voltage swing =  $\pm 1.3V$ . Simultaneously we need to check this after changing any Parameter.

In. 1<sup>st</sup> Iteration

$$V_{bp} = 1.2V \quad ] \text{To keep just in Sub threshold}$$

$$V_{bn} = 0.378V \quad \text{MP1 \& MN1}$$

DC Gain (Entire OTA) = 76.35

Phase margin ~~50~~ = 50.82

UGIF = 1.24 GHz

Slew Rate = 405 V/μs.

It was notable to give high current, due to which slew rate didn't increase much.

Again when DC gain + Voltage swing was satisfied the frequency component mainly depend upon  $C_b$ ,  $I_{out}$  sources.

(W) Parameter was ↑ a lot to give high current at the output.

The disadvantage was that now our Load

Capacitances also ↑. There was trade-off between Slew Rate

& The Current in main branch was also ↑.

The DC Gain was ↓ = 66 dB

Phase got ↓ = 49.36

UGIF ↑ = 2.56 GHz

Slew Rate Got ↑ = 997 V/μs.

we need to now make DC gain  $> 70 \text{ dB}$  & Phase Margin  $> 60$

The voltages were decreased at  $V_{bp}$  &  $V_{bn}$   
 $\& \gamma_b \downarrow$ .

To satisfy Voltage swing ( $w/L$ ) of MSBP  $\downarrow$ .  
 This lead to decrease in ~~load~~  $\&$  Capacitor load significantly.

The DC gain  $\uparrow = 72.38 \text{ dB}$

Phase margin  $= 26.44^\circ$   
 was still at

$$UGF = 2.61 \text{ GHz}$$

The slew rate  $\uparrow$  further about  $1050 \text{ V/us}$ .

The ideal voltages were removed & diode-connected MOSFET were added.

When  $R_b \uparrow \rightarrow$  The phase margin was lowered and  
 the slew rate  $\downarrow$  & when  $R_b$  was too low, slew rate  $\downarrow$   
 When  $C_b \downarrow \rightarrow$  UGF  $\uparrow$  Phase margin was  $\uparrow$  &  
 slew rate  $\downarrow$

We now have to play with  $C_b$   $R_b$  to achieve most optimum one.

Current wasn't changed much since it would disturb everything

$R_b$  is much more sensitive than  $C_b$

Let  $R_b = 1.6k \rightarrow$  Slew Rate  $900 \text{ V/us}$

$C_b = 16p \rightarrow$  Phase Margin  $\rightarrow 31.21^\circ$

DC Gain  $= 72.38 \text{ dB}$

$$UGF = 2.505 \text{ GHz}$$

Further changes didn't satisfied slew rate / Phase margin  $\downarrow$ .

# 1 Iterations of Auxiliary circuit

## 1.a Target Specifications

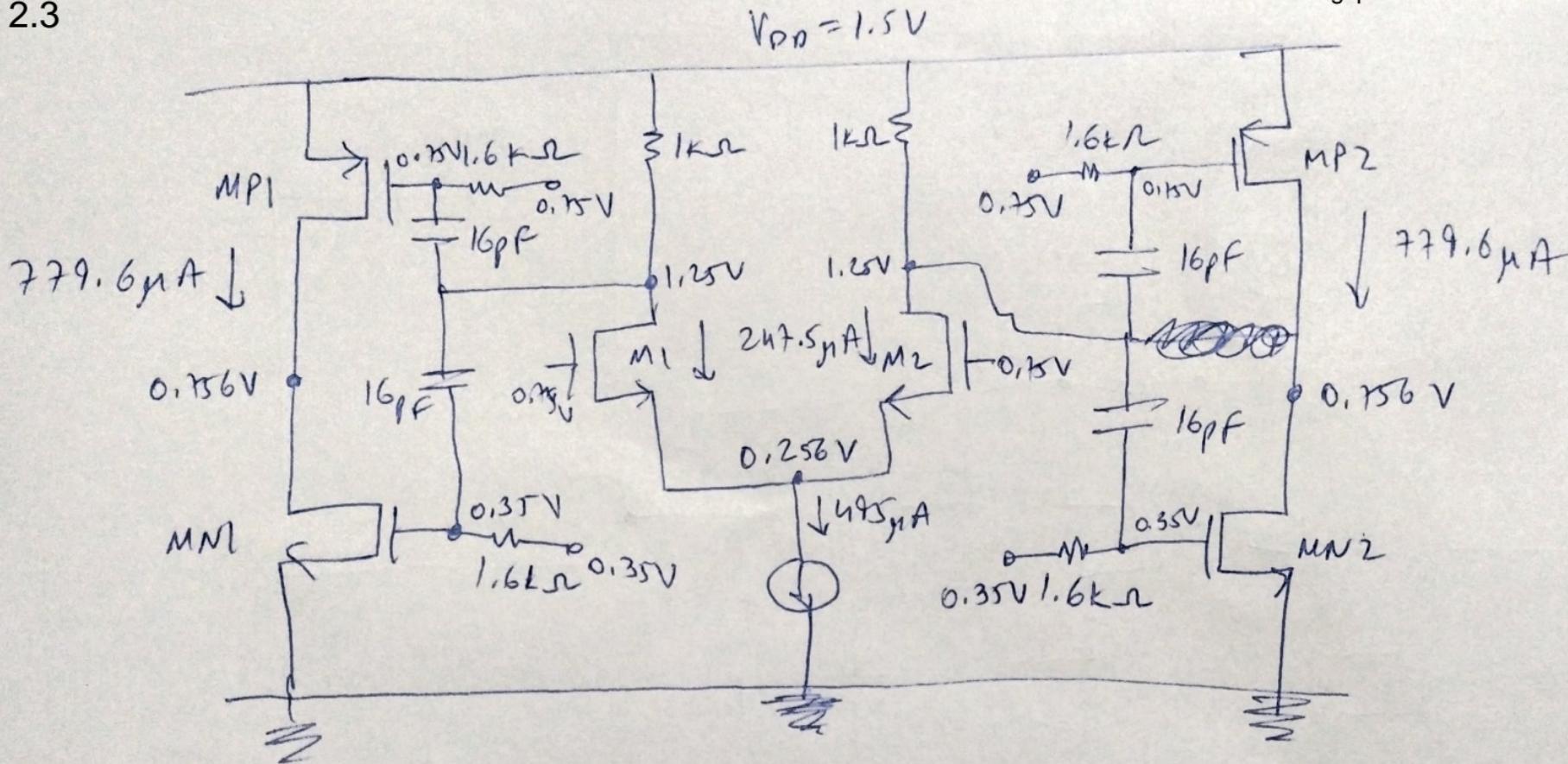
	Iteration1	Iteration2	Iteration3	Final Iteration
DC gain(dB)	76.35	66	72.38	72.38
Phase margin	60.82°	49.36°	26.44°	31.21°
UGF(Ghz)	1.24	2.56	2.61	2.506
Slew Rate(V/uS)	405	997	1060	900
1% Settling time(ns)	-	-	-	6.89ns

## 1.b Values of parameters

	Iteration1	Iteration2	Iteration3	Final Iteration
$R_b$	50kΩ	15kΩ	10kΩ	1.6kΩ
$C_b$	5pF	3pF	5pF	16pF
$(\frac{W}{L})_{MP}$	0.2/0.2	110/0.18	50/0.5	50/0.5
$(\frac{W}{L})_{MN}$	0.2/0.2	245/0.18	100/0.18	100/0.18
$(\frac{W}{L})_{M1/2}$	0.15/0.15	10/0.16	10/0.16	10/0.16

2.3

ngspice: auxOP.cir



Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	10	0.16
M2	10	0.16
MP1	50	0.5
MP2	50	0.5
MN1	100	0.18
MN2	100	0.18

Table: Sizes of transistors in Auxiliary Amplifier

3.1 &amp; 3.2

 $V_{b1}, V_{b2}, V_{b3}$  Design Procedure

We initially used ideal voltage source to generate

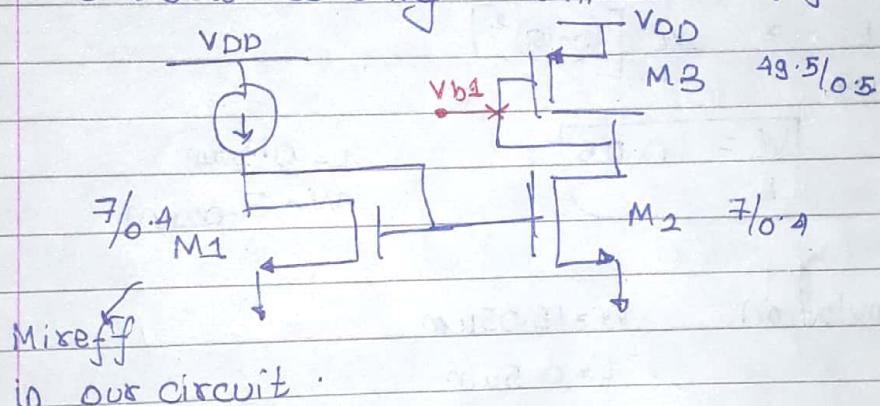
$$V_{b1} = 1.1 \text{ V}$$

$$V_{b2} = 1 \text{ V}$$

$$V_{b3} = 0.46 \text{ V}$$

### Methodology

We would be using current source reference generator ( $50 \mu\text{A}$ )



in our circuit.

$$\Rightarrow \text{From simulations } (V_{TK})_3 = 0.32 \text{ V} \quad \mu_p C_{ox} = 3.07 \times 10^{-4}$$

$$\Rightarrow 50 \times 10^{-6} = \frac{1}{2} (\mu_p C_{ox}) [1.5 - V_{b1} - 0.32] \left( \frac{W}{L} \right) \quad \text{--- (1)}$$

$$V_{b1} \text{ required} = 1.1 \text{ V}$$

~~$$50 \times 10^{-6} = (3.07 \times 10^{-4}) [0.08]^2 \left( \frac{W}{L} \right)$$~~

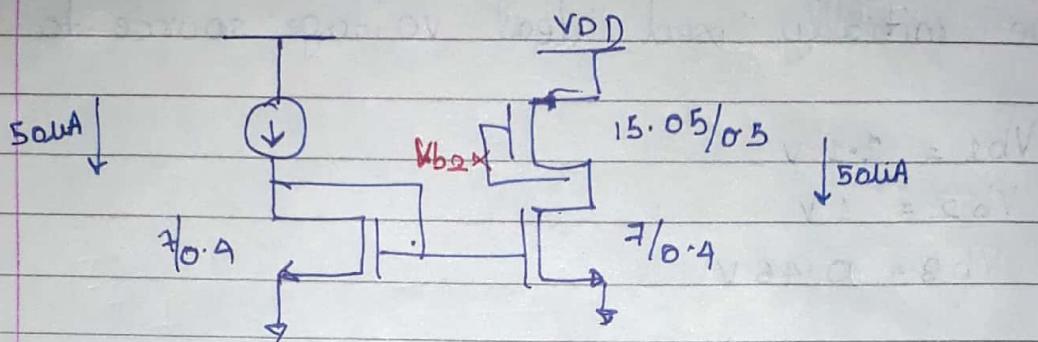
$$\frac{W}{L} = 51$$

$$\begin{aligned} L &= 0.5 \mu\text{m} \\ W &= 102 \mu\text{m} \end{aligned}$$

$$\text{From Simulations} \quad W = 49.5 \mu\text{m} \\ L = 0.5 \mu\text{m}$$

Iterate  $\rightarrow$  Include " $\lambda$ " from Simulation  $[\lambda = 0.074]$   
 $\therefore$  After including  $\lambda$   
 $\frac{W}{L} \approx 51$

$V_{b2}$  (1V)



$$\frac{50 \times 10^6}{2} = \frac{1}{2} \left( 3.07 \times 10^4 \right) \left( \frac{W}{L} \right) [1.5 - 1 - 0.32]^2$$

$$\frac{1}{3.07} = \frac{W}{L} [(0.18)^2]$$

$$\frac{W}{L} = 10.05$$

$$L = 0.5 \mu m$$

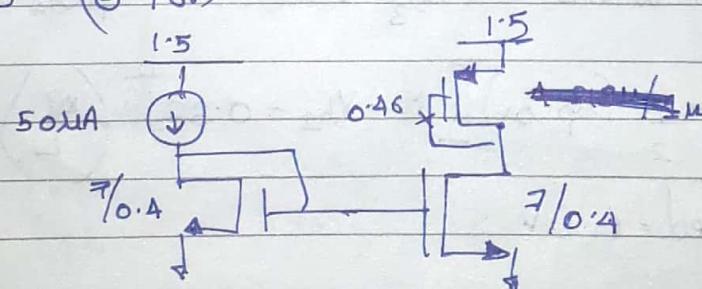
$$W = 5.025 \mu m$$

From simulation

$$W = 15.05 \mu m$$

$$L = 0.5 \mu m$$

$$V_{b3} = 0.46V$$



Same

$$\frac{50 \times 10^6}{2} = \frac{1}{2} \left( 3.07 \times 10^4 \right) \left( \frac{W}{L} \right) [1.5 - 0.46 - 0.32]^2$$

$$\frac{W}{L} = \frac{1}{(3.07)(0.72)^2} = 1.0628$$

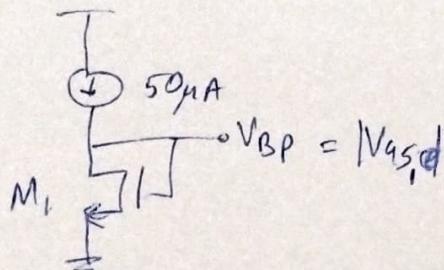
$$= \begin{cases} L = 0.5 \mu m \\ W = 0.328 \mu m \end{cases}$$

Simulation

$$\begin{cases} W = 1.4 \mu m \\ L = 0.5 \mu m \end{cases}$$

### V<sub>BP</sub> -

need a V<sub>BP</sub> of 0.75 V



$$V_{Tn} = \cancel{0.3} \text{ V}$$

$$\mu_n C_{ox} = 3.16 \times 10^{-4} \text{ (simulations)}$$

$$\Rightarrow \frac{\mu_n C_{ox}}{2} \left( \frac{w}{l} \right)_1 (0.75 - 0.3)^2 = 50 \times 10^{-6}$$

$$\Rightarrow \left( \frac{w}{l} \right)_1 = 1.56$$

$$\text{choose } L_1 = 0.15 \mu\text{m} \text{ and } W_1 = 0.234 \mu\text{m}$$

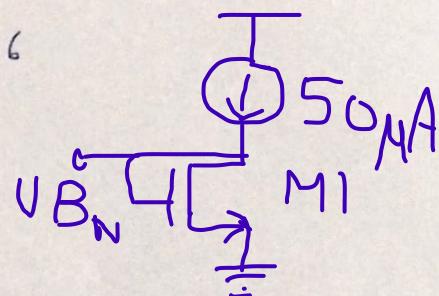
### V<sub>BN</sub> -

need V<sub>BN</sub> of 0.35 V

$$\Rightarrow \frac{\mu_n C_{ox}}{2} \left( \frac{w}{l} \right)_1 (0.35 - 0.3)^2 = 50 \times 10^{-6}$$

$$\Rightarrow \left( \frac{w}{l} \right)_1 = 126$$

$$\text{choose } L_1 = 0.4 \mu\text{m} \text{ & } W_1 = 50.6 \mu\text{m}$$



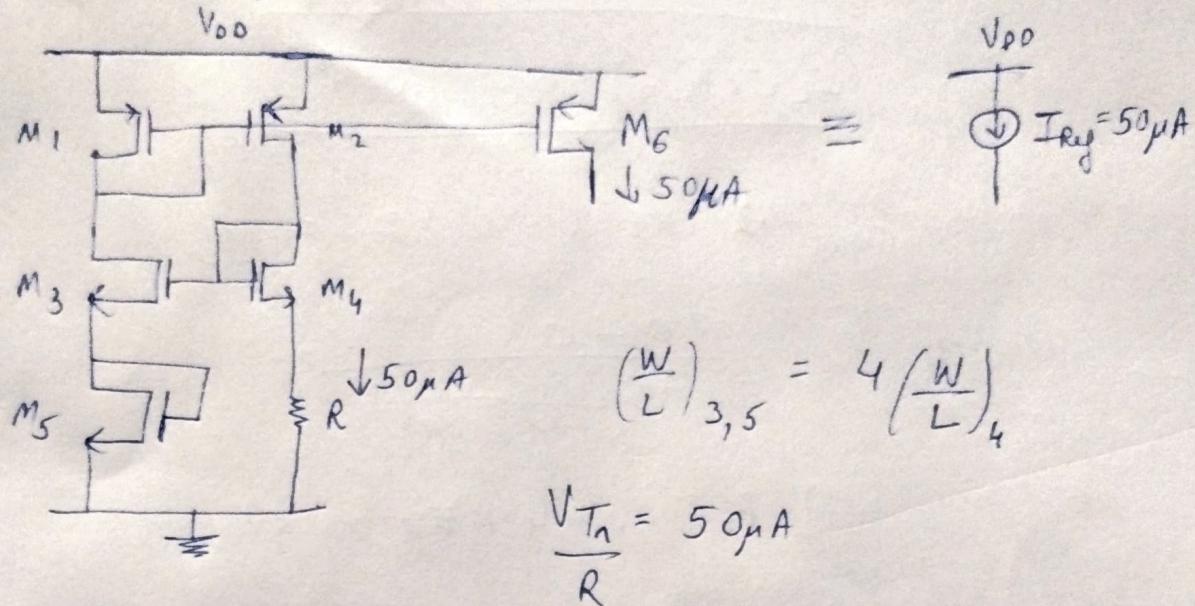
This didn't give the desired value.

Upon decreasing  $[W_1 \text{ to } 37 \mu\text{m}]$ , we got 0.35 V.

## Current Reference Generator -

We will design a supply independent current reference of value  $50\mu A$ .

Circuit - (Hajimiri, lecture 133 N)



$$\left(\frac{W}{L}\right)_{3,5} = 4 \left(\frac{W}{L}\right)_4$$

from simulations (for  $L=1\mu m$ ),  $V_{Th} = 0.345 V$

$$\Rightarrow R = \frac{V_{Th}}{50 \times 10^{-6}}$$

$$\Rightarrow R = 6.9 K\Omega$$

choose  $L=1\mu m$  for  $M_1 - M_5$

We must keep  $|W_{ASAT}|_{1,2,86}$  as low as possible to keep the current constant for a wide range of voltages.

Then, choose  $\left(\frac{W}{L}\right)_{1,2} = 200$

$$\Rightarrow W_{1,2} = 200\mu m$$

Now, choose  $\left(\frac{W}{L}\right)_{3,5} = 4 \left(\frac{W}{L}\right)_4 = 3$

$$\Rightarrow W_{3,5} = 3\mu m \text{ & } W_4 = 0.75\mu m$$

To keep O/p resistance high & size realistic,

choose  $L_6 = 2 \mu\text{m}$  &  $W_6 = 400 \mu\text{m}$

( $\frac{W}{L}$  same as M1 & M2)

3.3

for current source,

	<u><math>W(\mu\text{m})</math></u>	<u><math>L(\mu\text{m})</math></u>
M1	200	1
M2	200	1
M3	3	1
M4	0.75	1
M5	3	1
M6	400	2

## Characteristics of the current source

dc1: Current Reference generator  
uA

— i(vdrain)

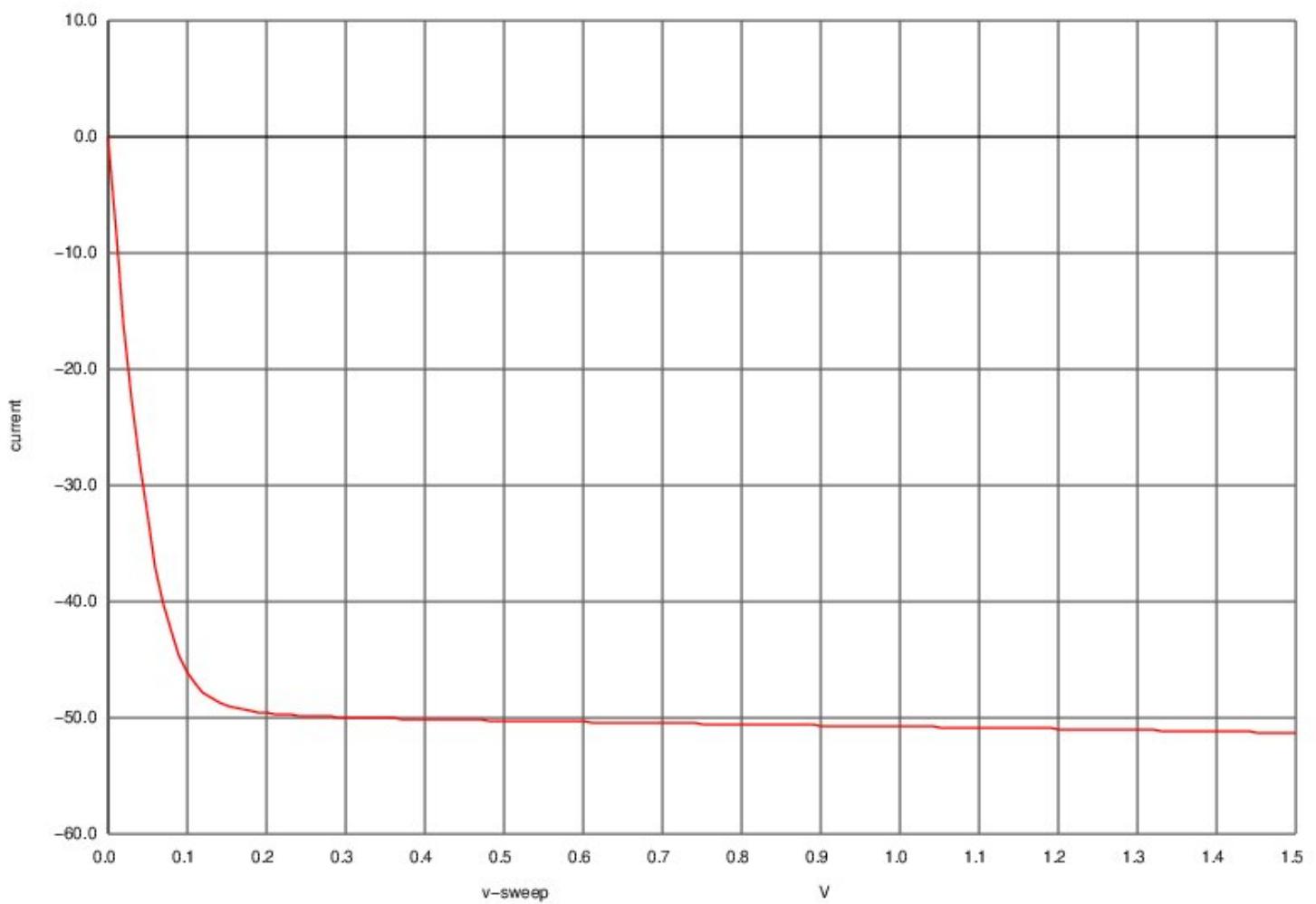


Figure: Output Current vs Voltage

Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	0.234	0.15

Table: Sizes of transistors in VBP (0.75 V) generator

Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	37	0.4

Table: Sizes of transistors in VBN (0.35 V) generator

Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	7	0.4
M2	7	0.4
M3	49.5	0.5

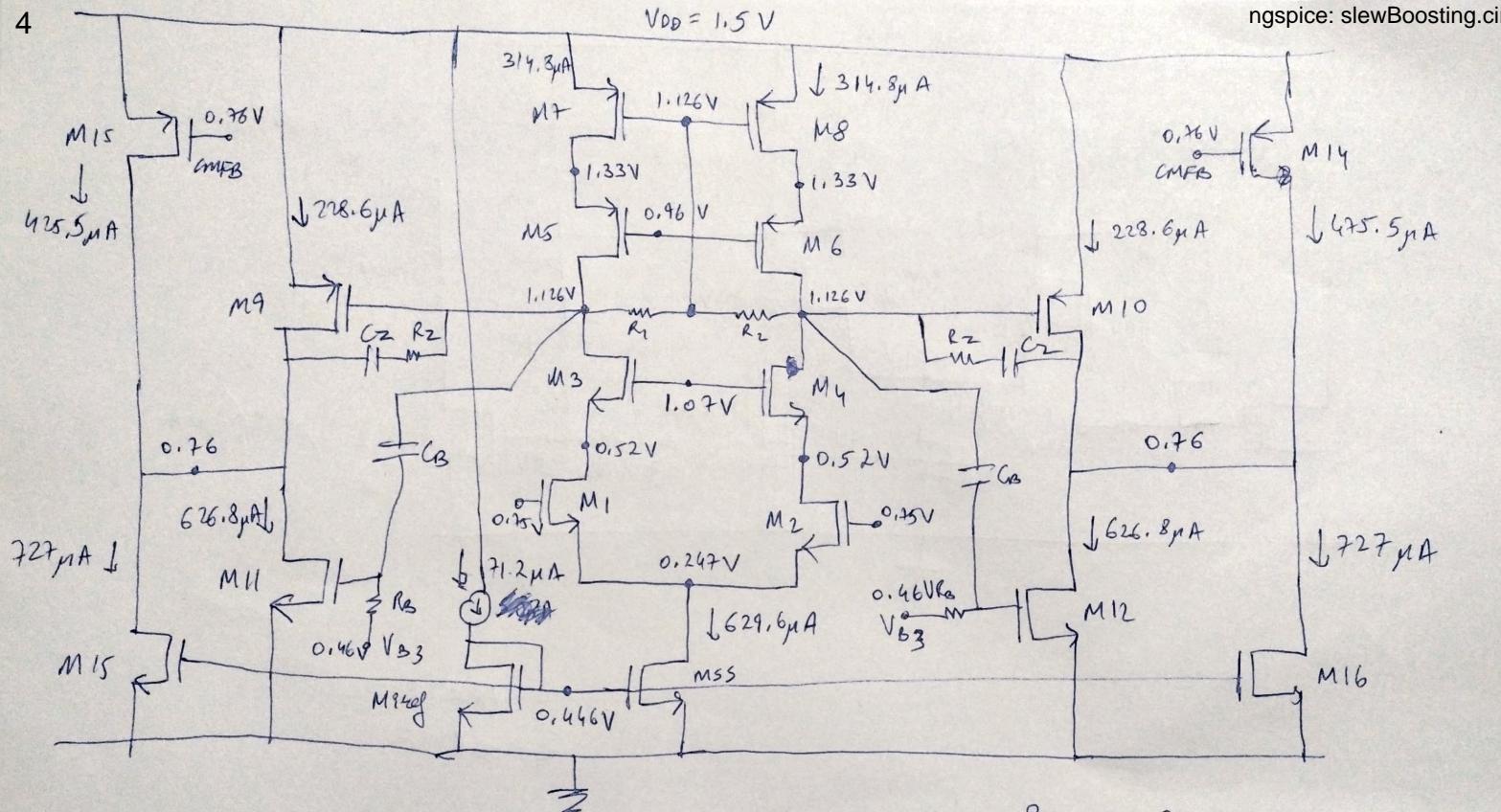
Table: Sizes of transistors in VB1 (1.1 V) generator

Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	7	0.4
M2	7	0.4
M3	15.05	0.5

Table: Sizes of transistors in VB2 (1 V) generator

Transistor	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1	7	0.4
M2	7	0.4
M3	4.218	1

Table: Sizes of transistors in VB3 (0.46 V) generator

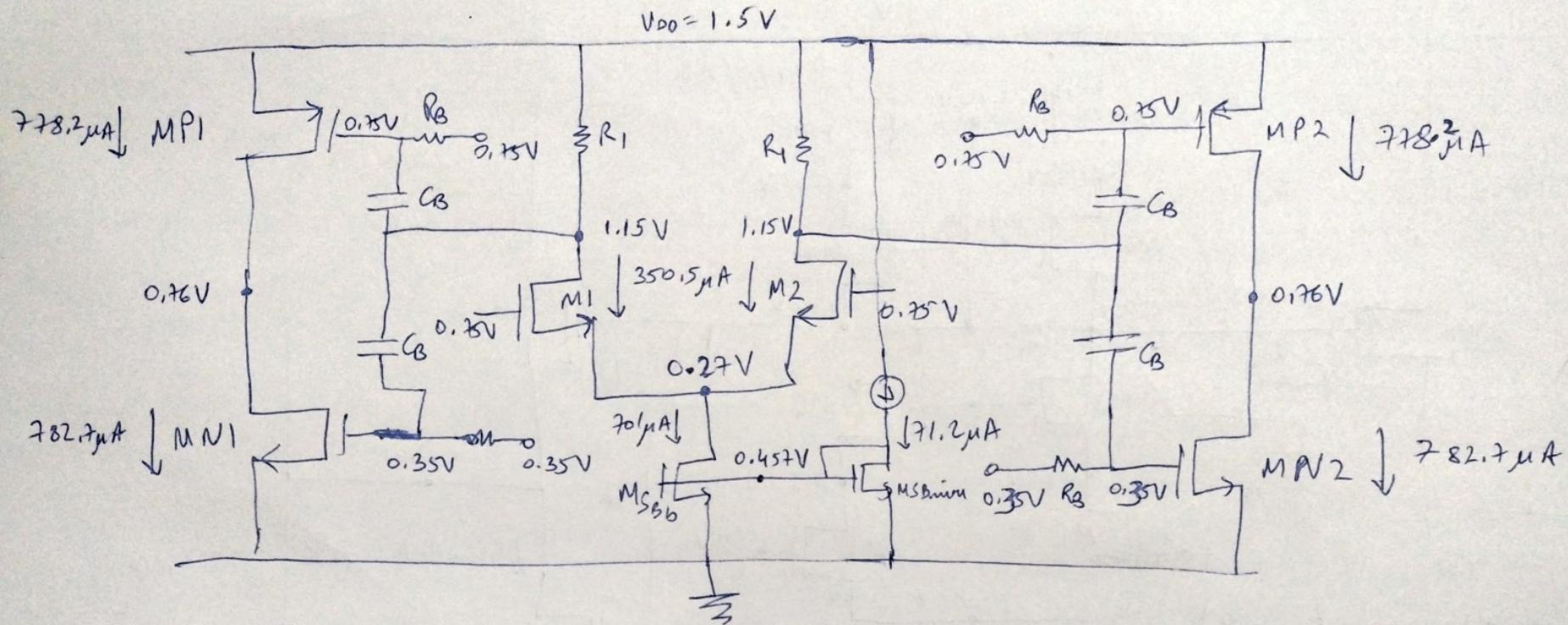


$$R_B = 10k\Omega$$

$$C_B = 0.06\text{pF}$$

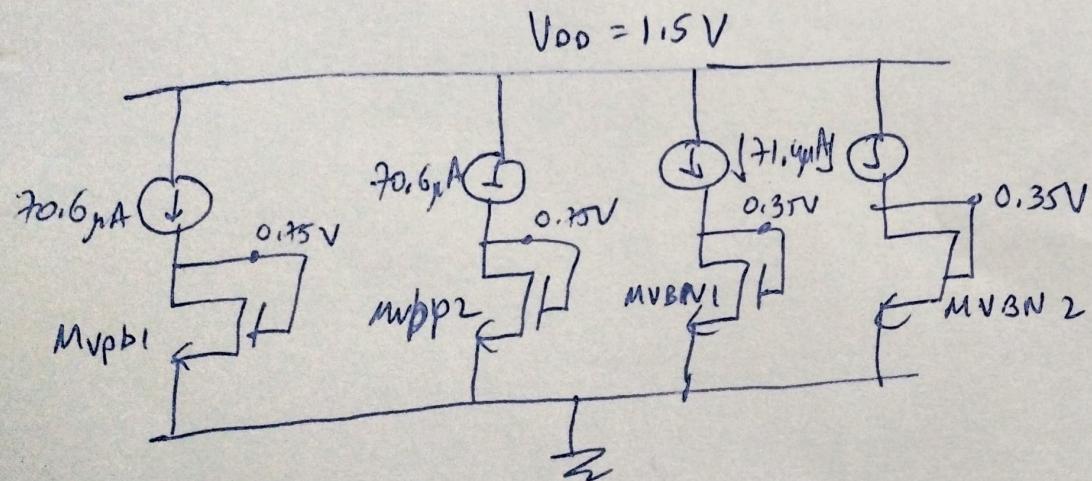
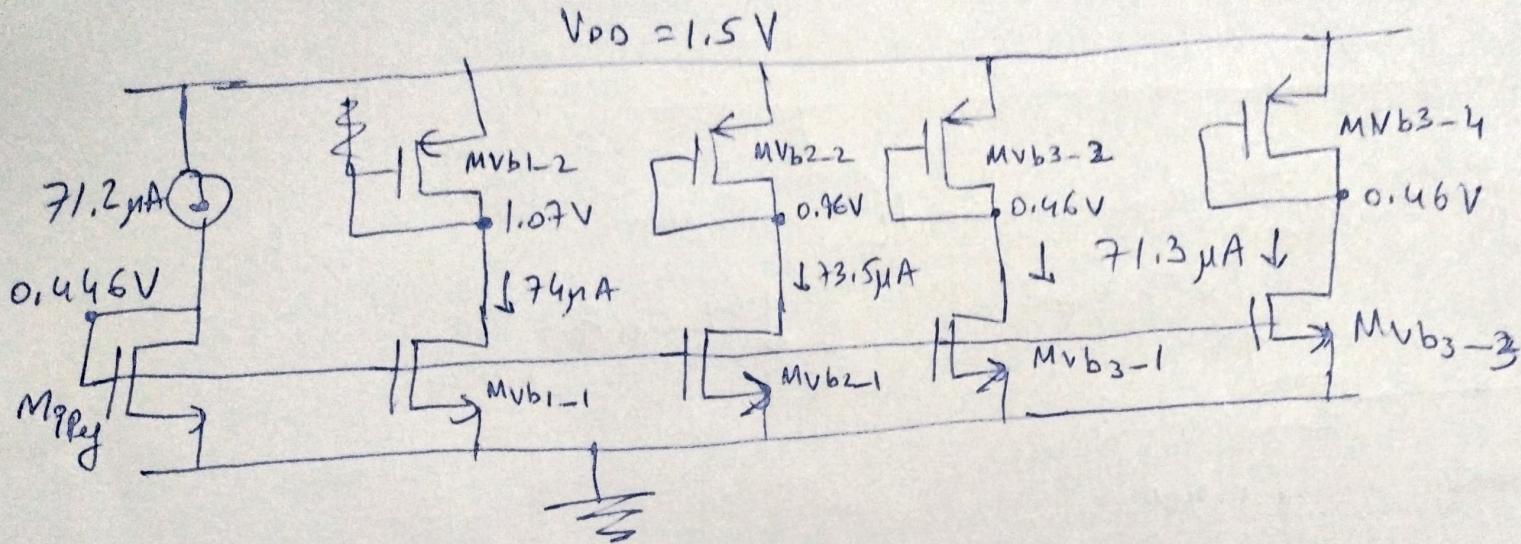
$$R_2 = 370\Omega$$

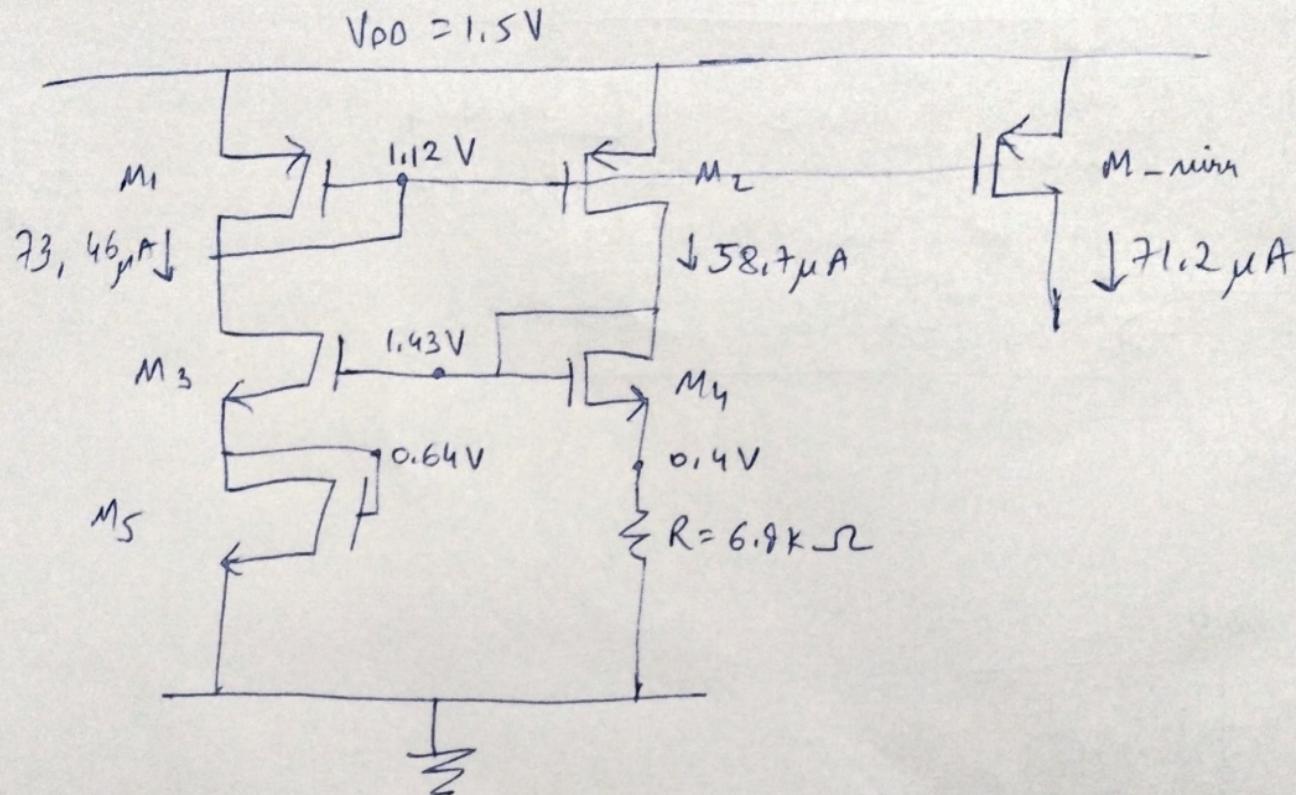
$$C_2 = 0.55\text{pF}$$



$$R_G = \cancel{1.6} k\Omega$$

$$C_B = \cancel{0.16} pF$$





Markings' Legend:

Blue circle - Gain/Phase crossover frequency

Red arrow - DC Gain

Dark blue line - 3dB bandwidth

For Main Amplifier: Phase Margin = 60.7°, UGF = 1.248 GHz, DC Gain = 76.24 dB

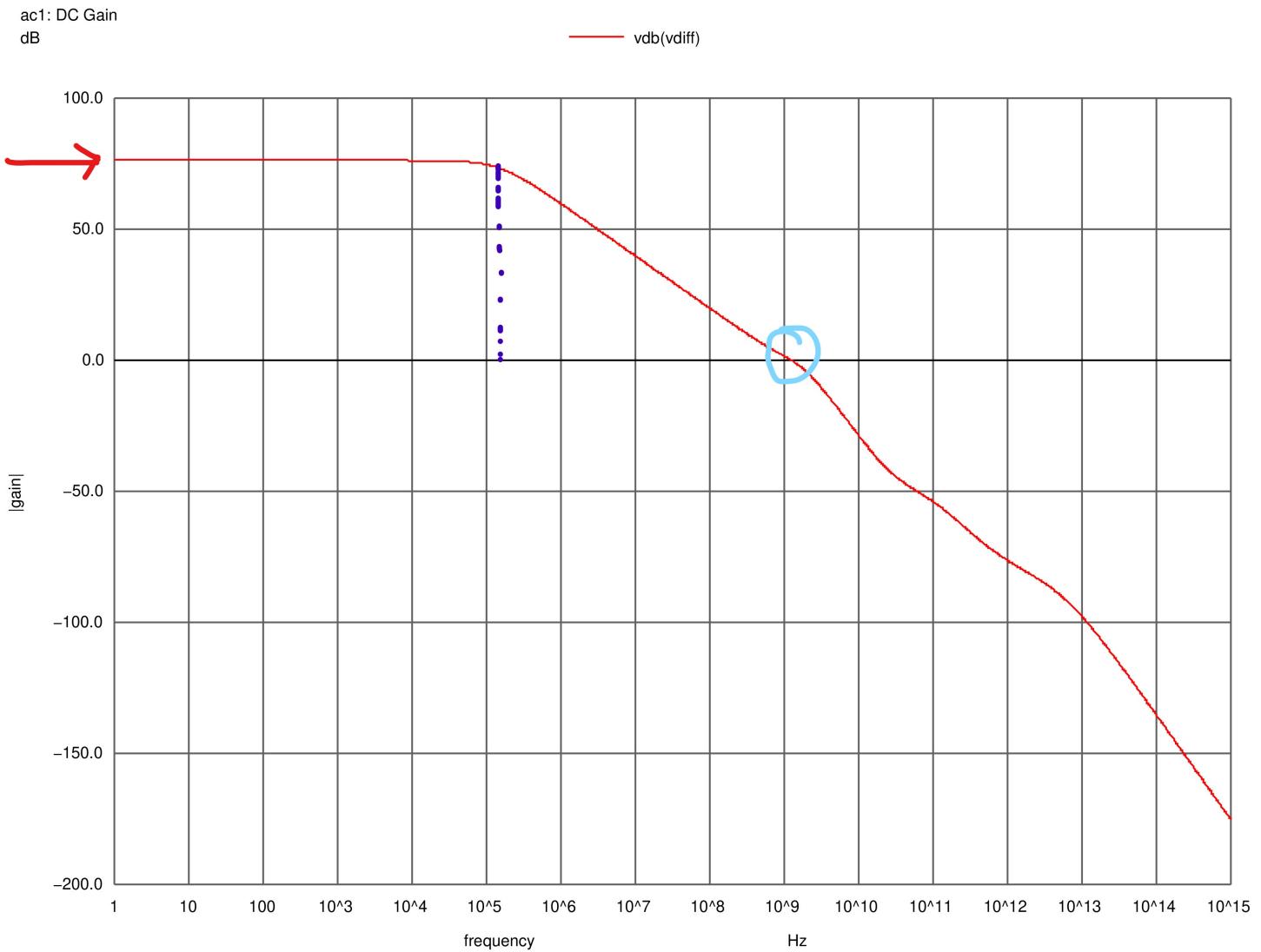


Figure: Bode Amplitude Plot for class AB amplifier only

ac1: Phase

vp(vdiff)\*57.29

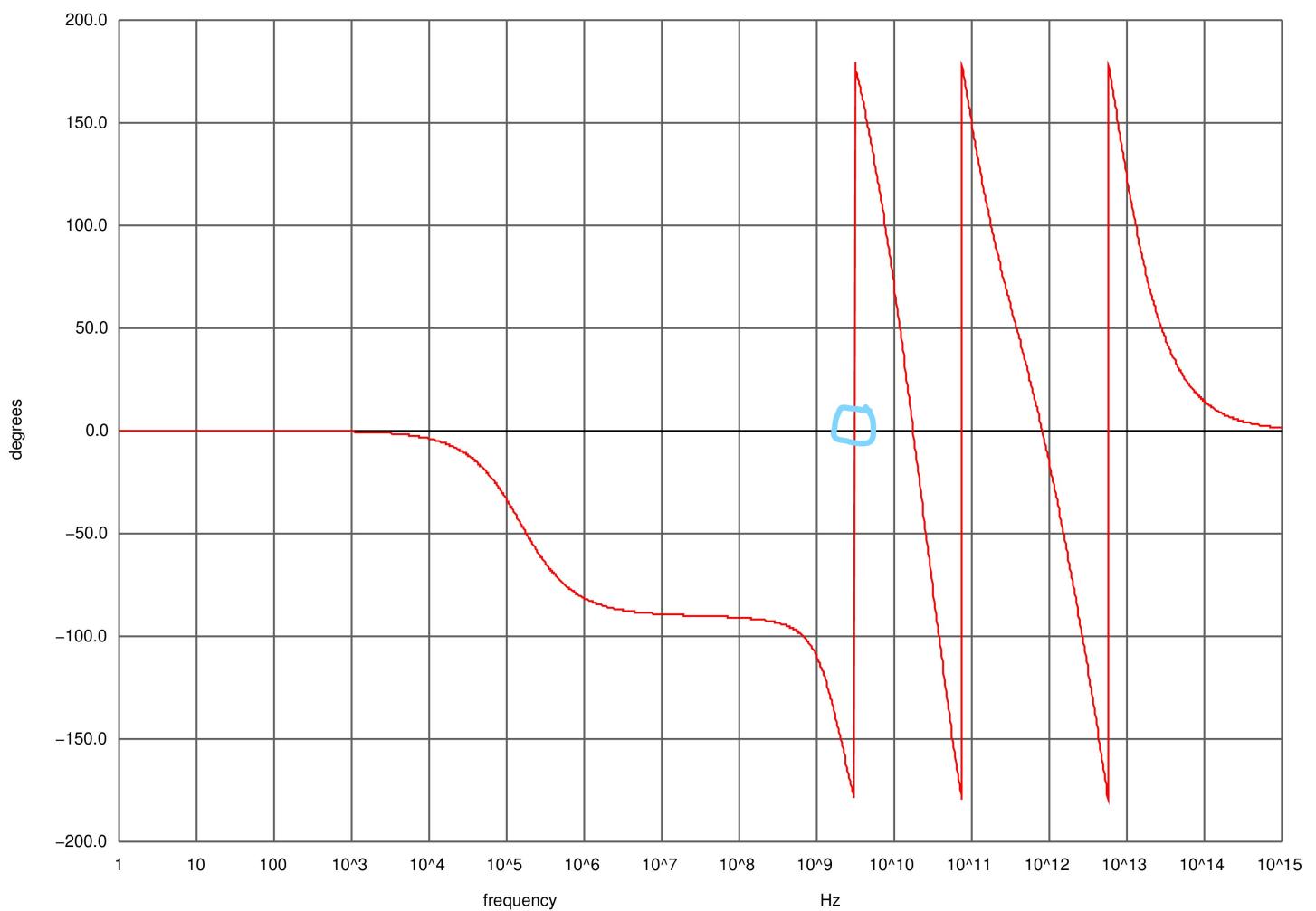


Figure: Bode Phase Plot for class AB amplifier only

For the whole OTA: Phase Margin =  $31.1^\circ$ , UGF = 2.506 GHz, DC Gain = 72.38 dB

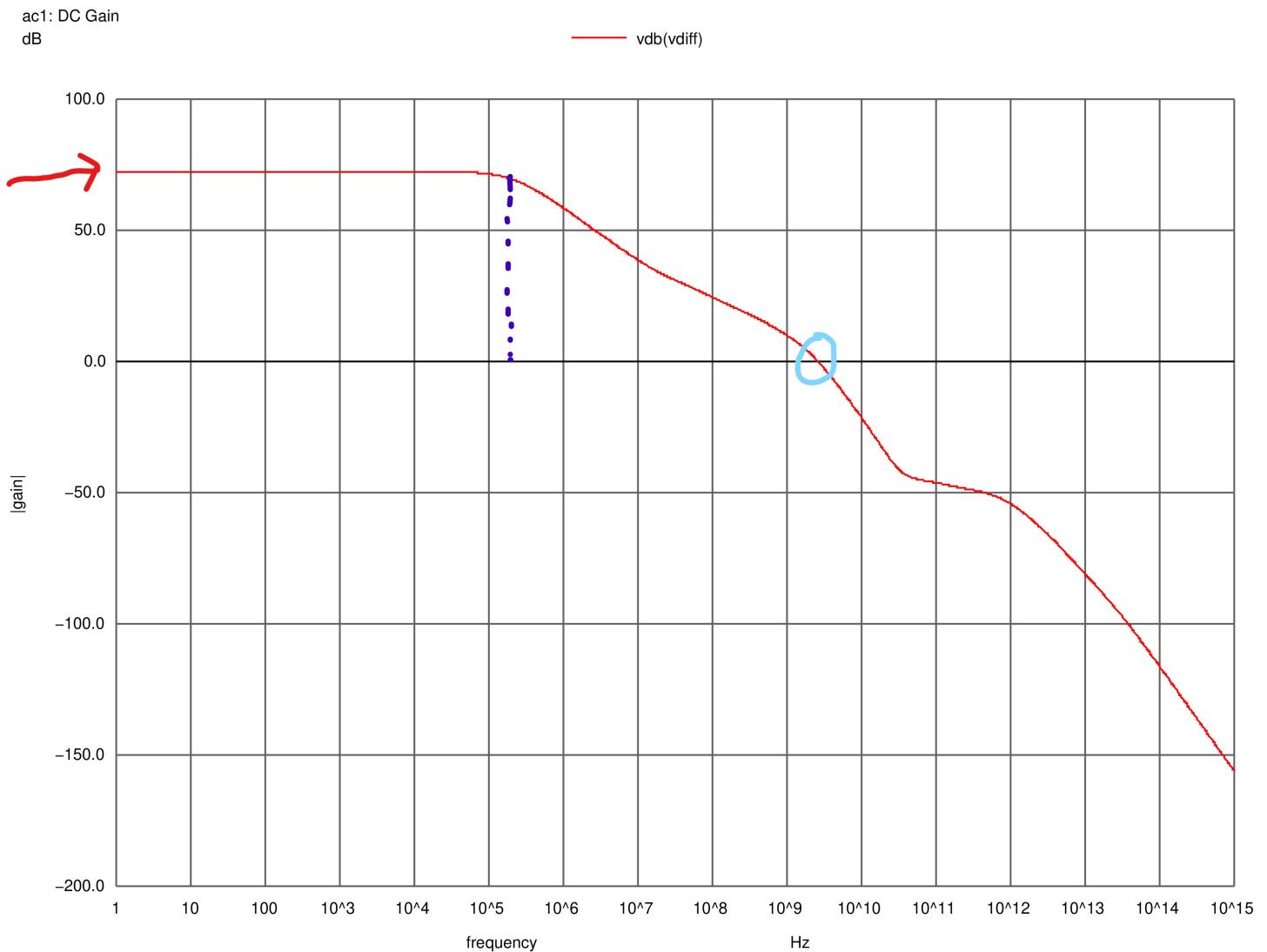


Figure: Bode Amplitude Plot for class AB amplifier with booster circuit

ac1: Phase

vp(vdiff)\*57.29

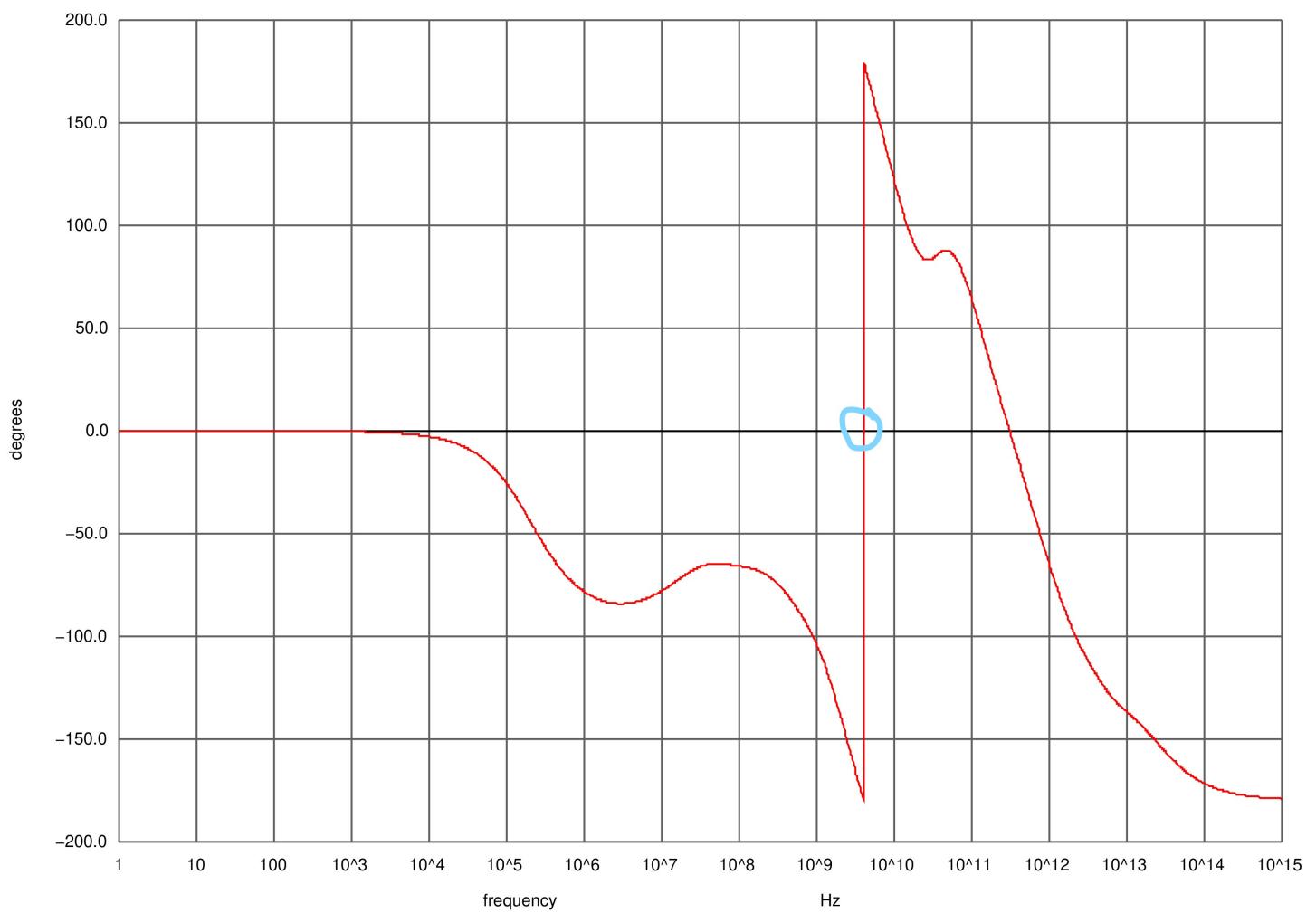


Figure: Bode Phase Plot for class AB amplifier with booster circuit

## 6.2, 6.3, 6.4 & 6.5

ngspice: compositeMainSlew.cir,  
compositeMainSet.cir

Class AB Amplifier:  $SR^+ = 419.5511\mu V/s$ ,  $SR^- = 387.2764\mu V/s$ ,  $SR_{average} = 403.4138\mu V/s$ , settling time =  $3.905667ns$

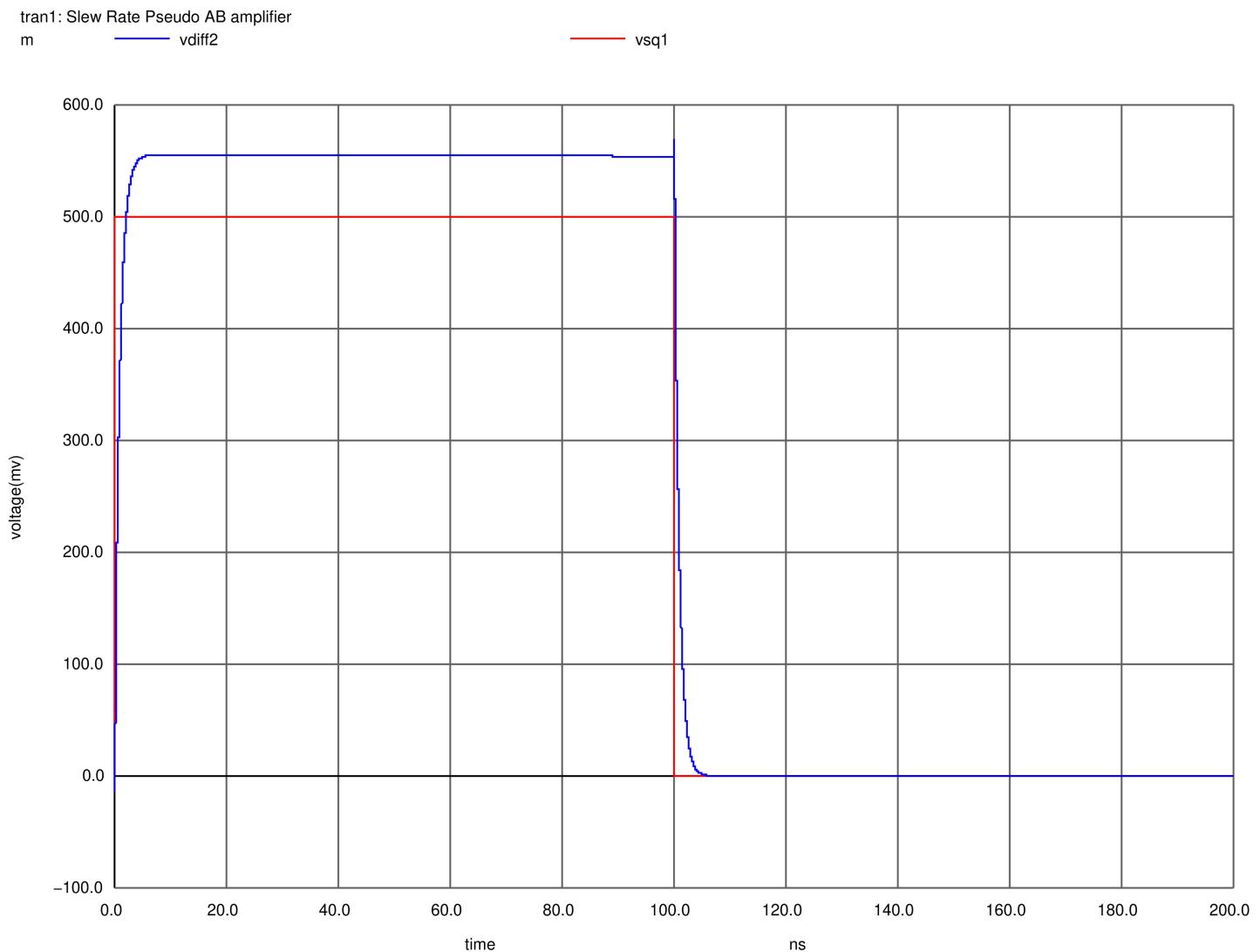


Figure: Vop for class AB amplifier only

tran1: Settling Time Pseudo AB amplifier

m

vsq1

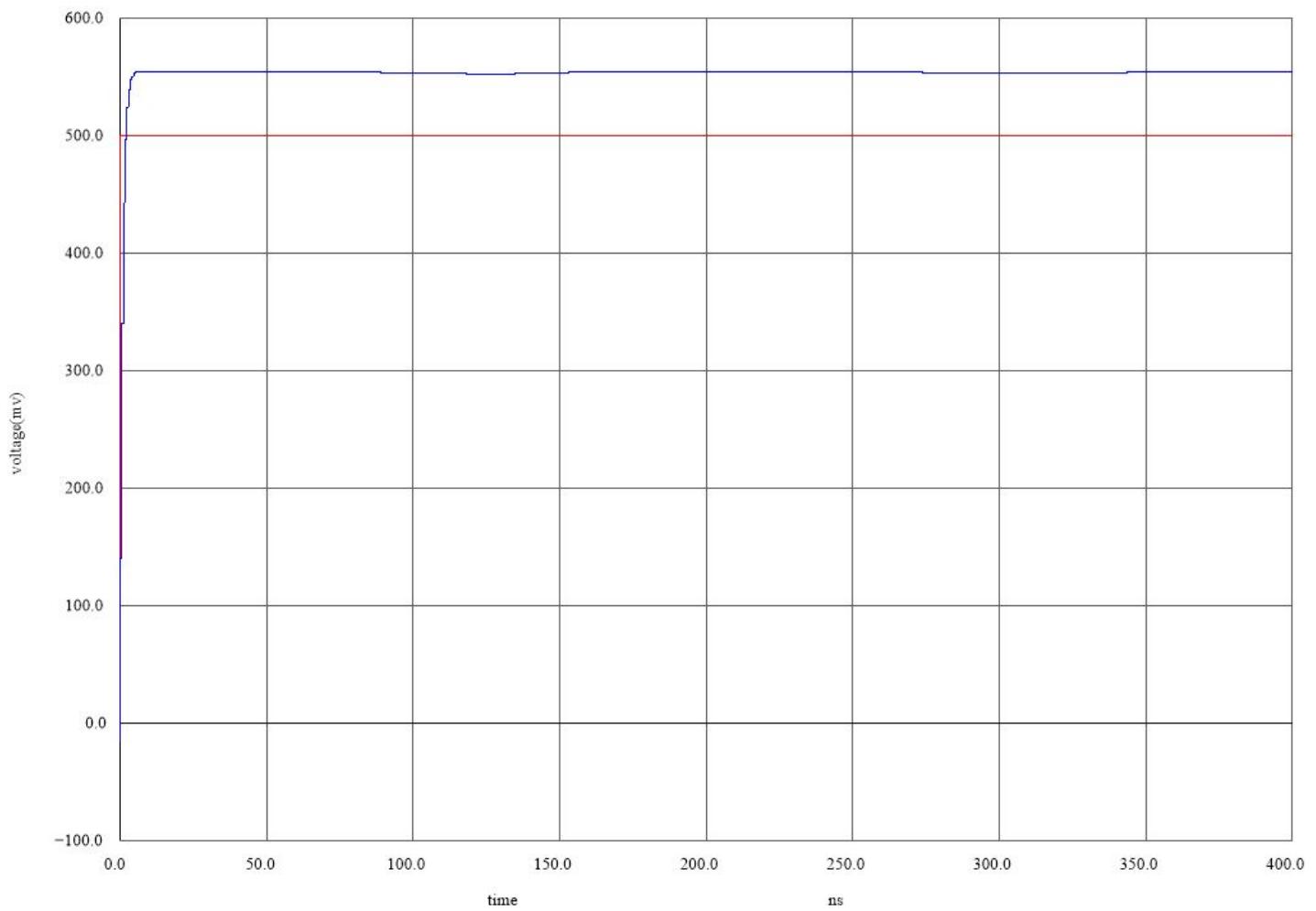


Figure: Settling Time Plot for class AB amplifier

Whole OTA:  $SR^+ = 879.3 \mu V/s$ ,  $SR^- = 920.7 \mu V/s$ ,  $SR_{average} = 900 \mu V/s$ , settling time = 6.89ns

tran1: Slew Rate Pseudo AB amplifier with SR boosting  
m

— vdiff2 — vsq1

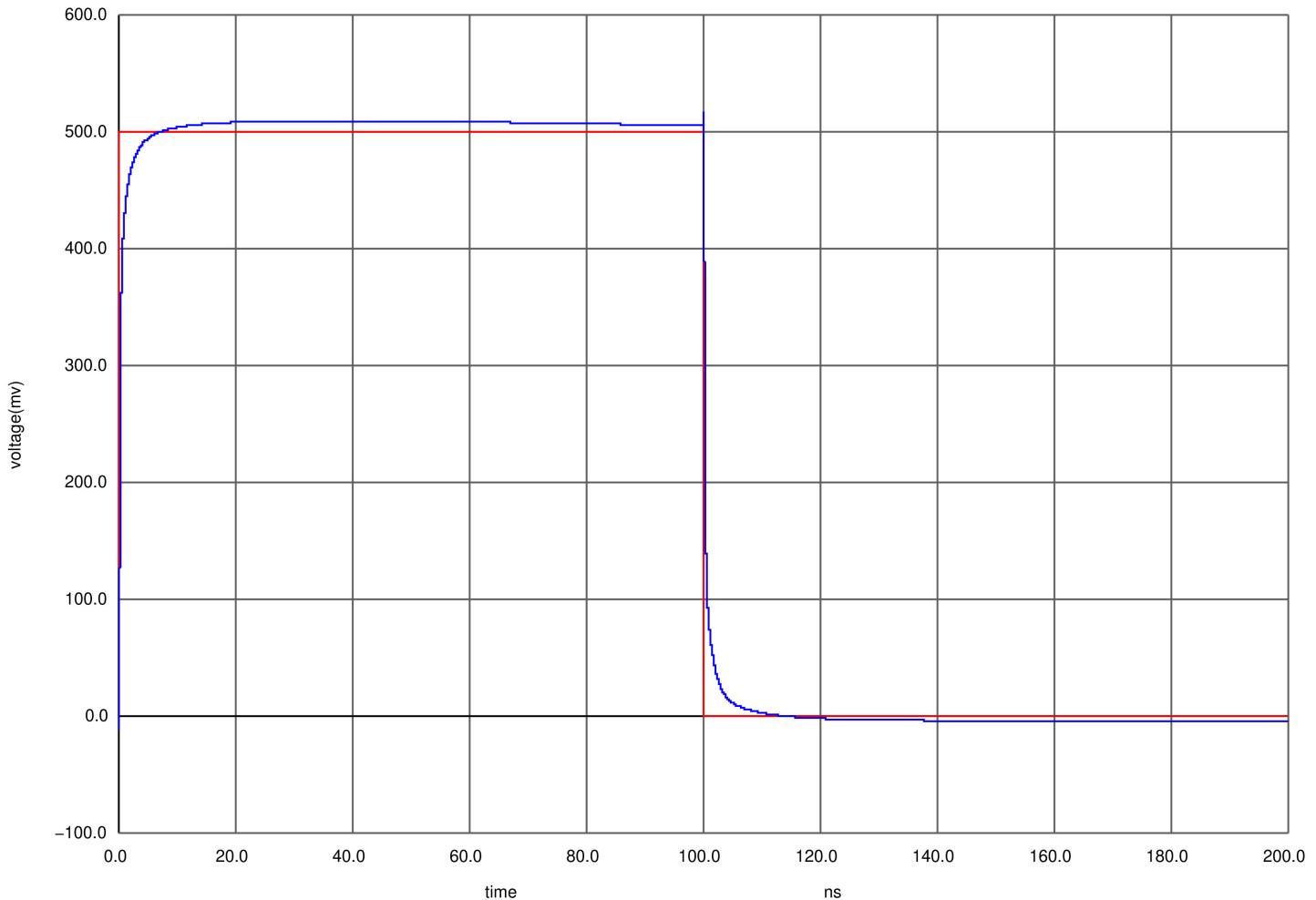


Figure: Vop for class AB amplifier with auxiliary class B booster circuit

tran2: Settling time Pseudo AB amplifier with SR boosting  
m

— vdiff2

— vsq1

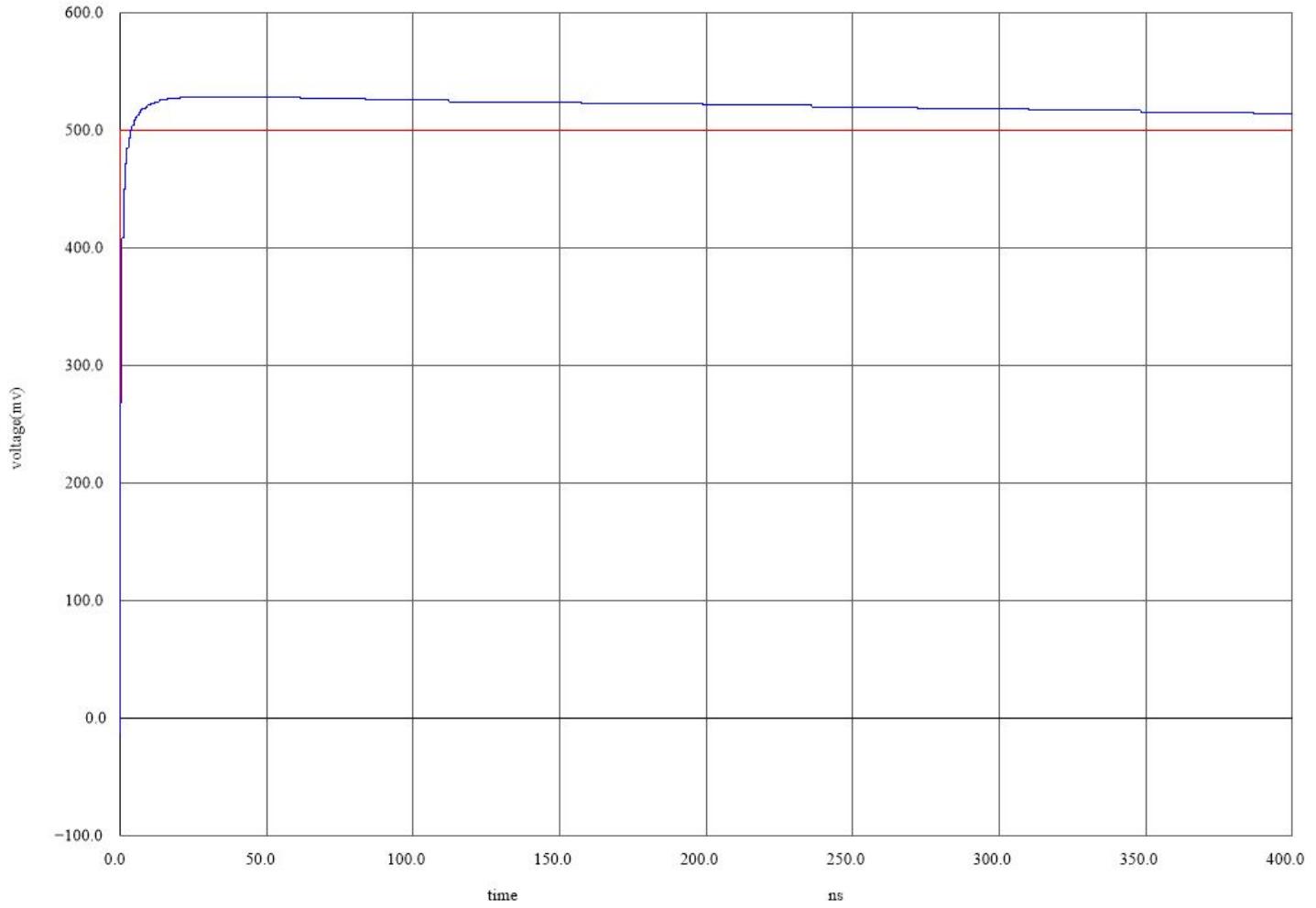


Figure: Settling Time Plot for class AB amplifier with slew boosting

Total integrated input reffered noise for class AB amplifier:  $1.9269 \times 10^{-5} V_{rms}$  (obtained using python code run on the raw files obtained from ngspice)

Corner frequency: 40 kHz (roughly the frequency at which the graph starts rising)

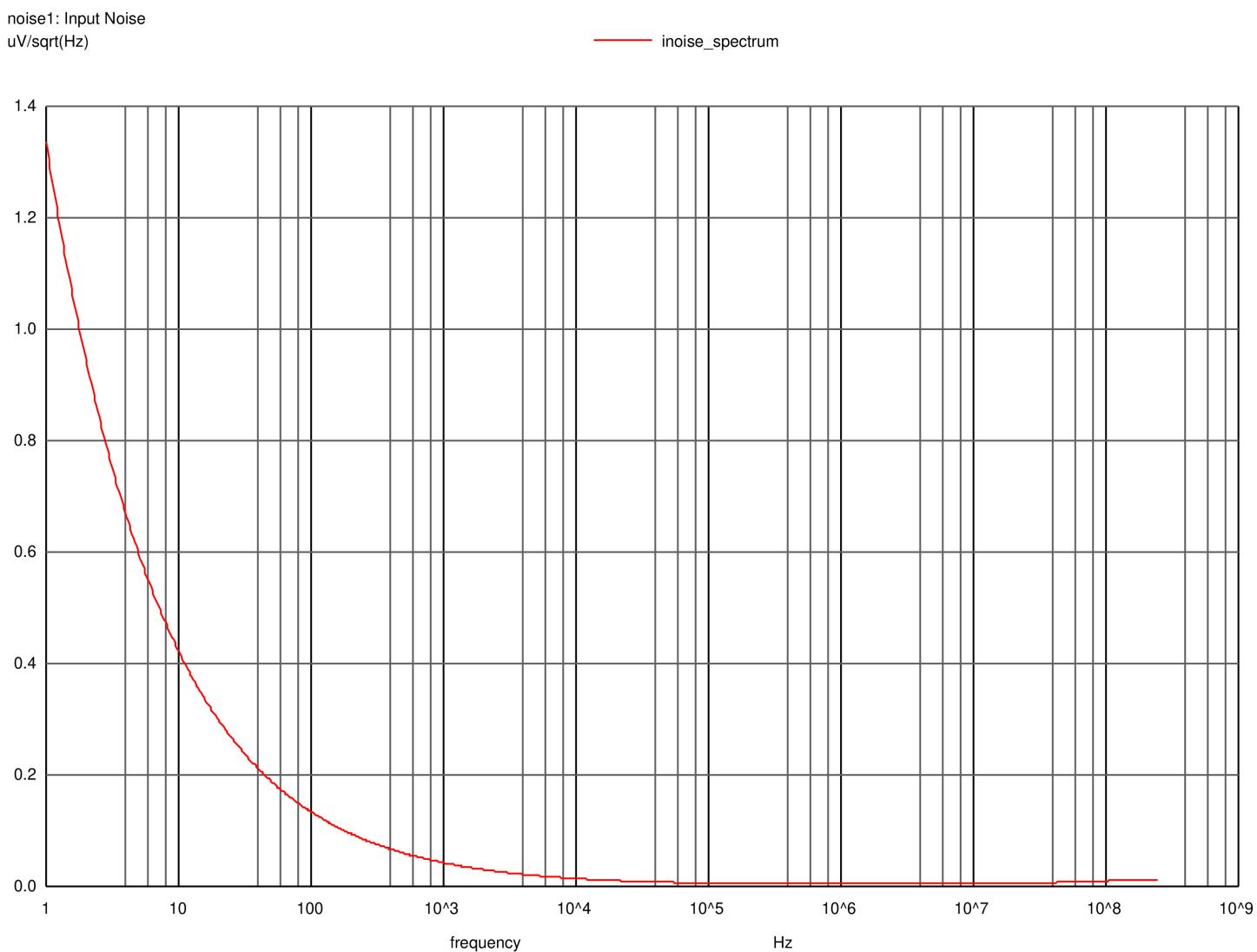


Figure: Input reffered noise in Class AB Amplifier

ngspice: noiseSlew.cir  
raw file: test\_noise1\_slew.raw  
python code: integrateNoise.py

Total integrated input reffered noise for class AB amplifier with slew boosting:  $1.9268 \times 10^{-5} V_{rms}$  (obtained using python code run on the raw files obtained from ngspice)

Corner frequency: 20 kHz (roughly the frequency at which the graph starts rising)

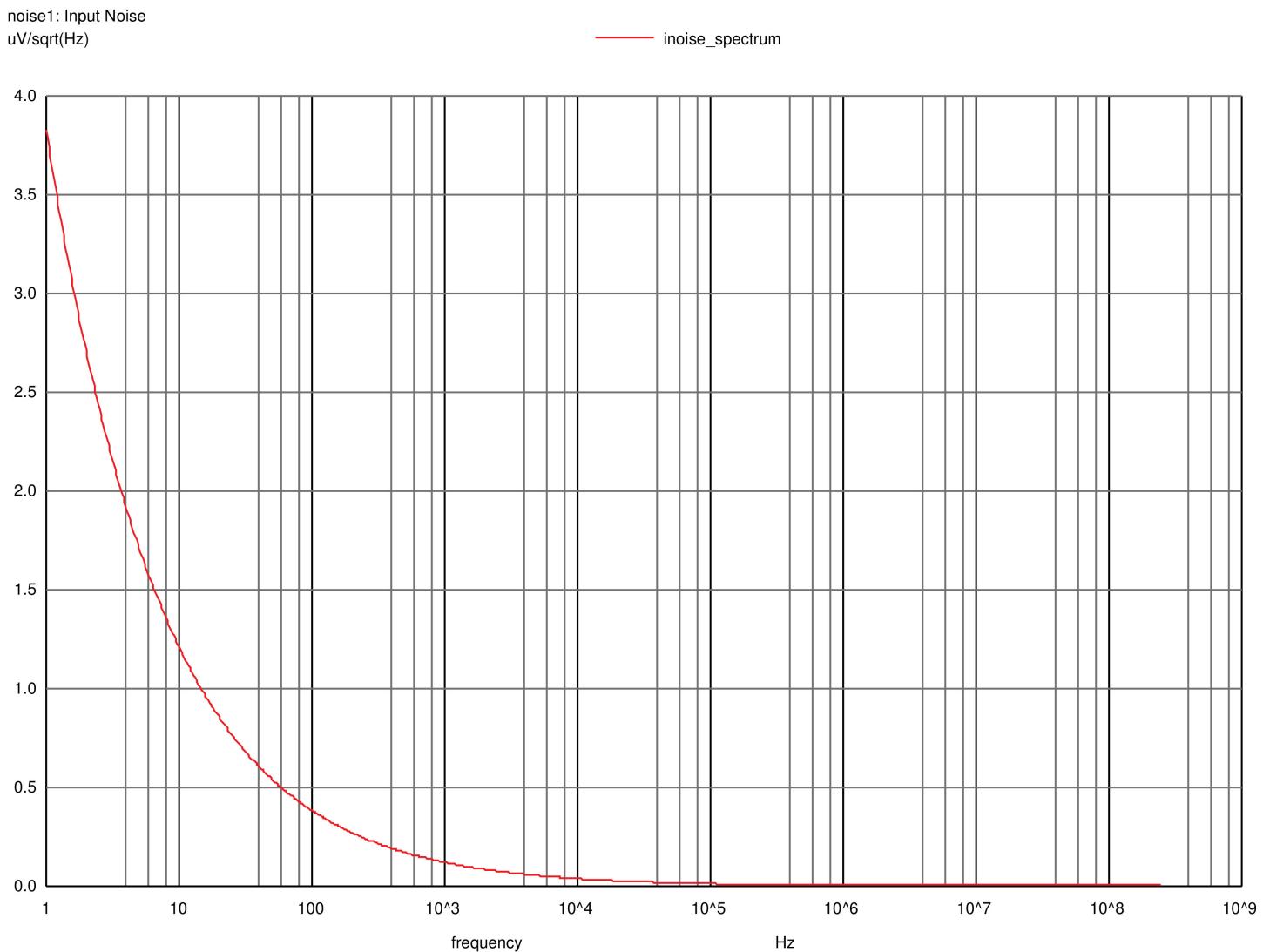


Figure: Input reffered noise in Class AB Amplifier with slew boosting

$$\text{CMRR} = -94.55 - 72.38 = -166.93 \text{ dB}$$

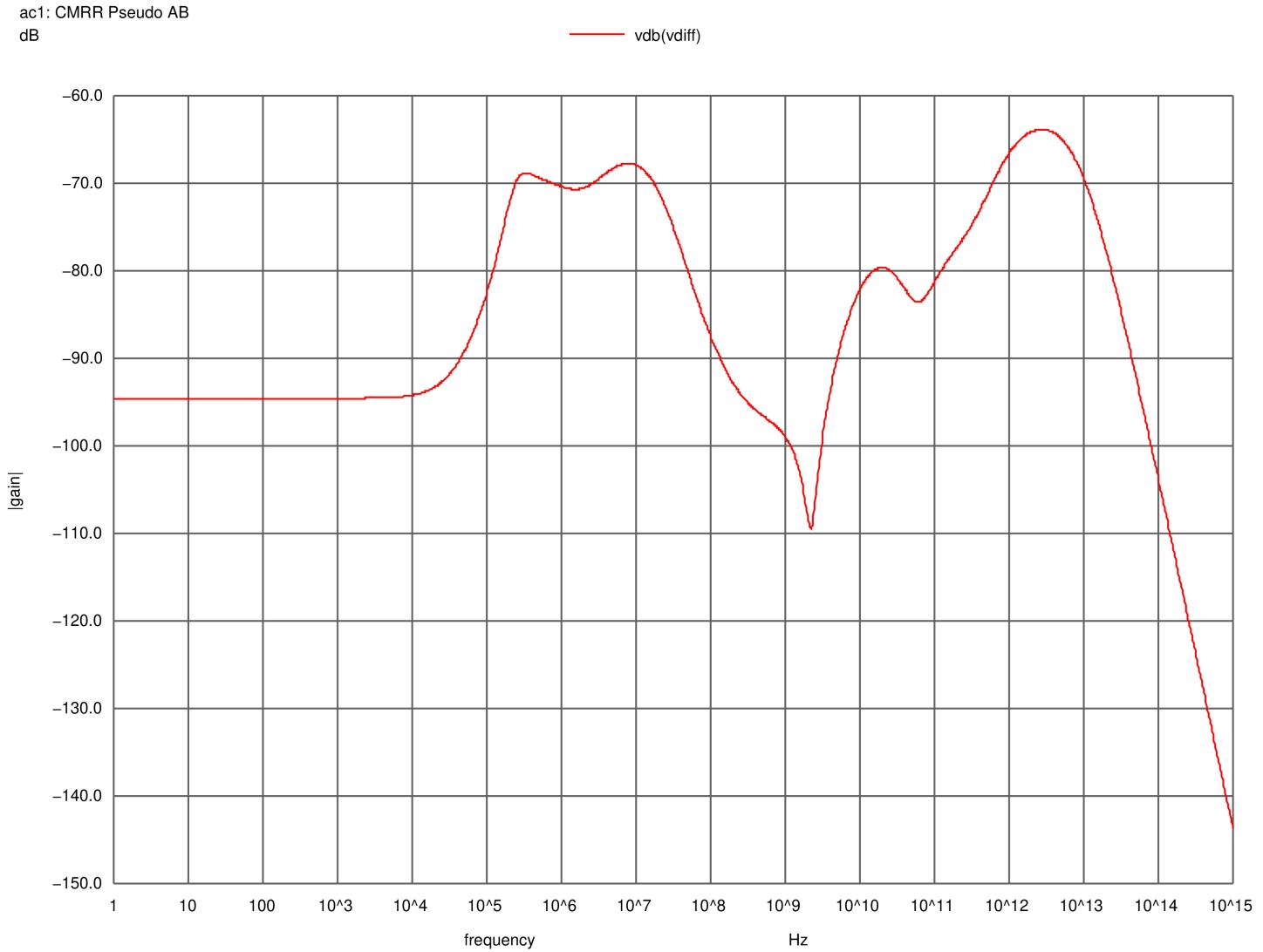


Figure: Bode Amplitude Plot for CMRR

8.1 We simulated the circuit for different values of common mode input and checked the region of operation of each transistor in the class AB amplifier. We found that when the input common mode is 0.42 V, M7 and M8 just go into cut-off and rest are still in sat. We also found that when input common mode is 0.98 V, M1 and M2 are on the verge of going out of saturation region while rest of the transistors are still in saturation. So, the input common mode region is 0.42 V to 0.98 V. (simulation file: main.cir)

ac1: Phase

vp(vdiff)\*57.29

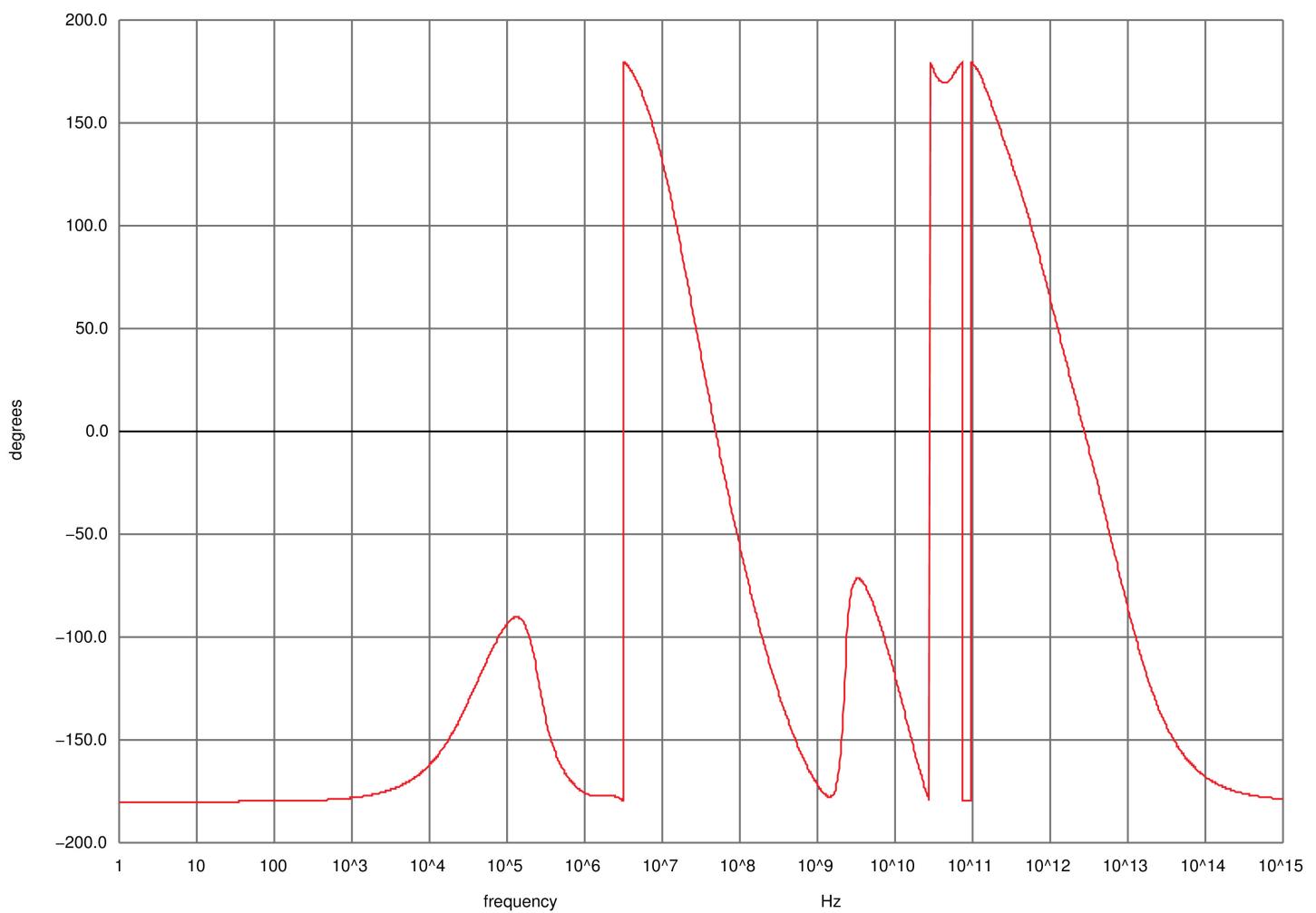


Figure: Bode Phase Plot for CMRR