Project Title: Vectorized Array Multiplication and Multiplication/Reduction using SSE

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I executed my code on the Rabbit server and obtained the results presented in both tabular and graphical formats. Analyzing the graph, which provides a visual representation of the data, I observed a notable trend: as the array size increases, the speedup achieved through both multiplication and multiplication/reduction operations decreases. However, there are a couple of exceptions to this pattern at array sizes of 524288 and 1048576, which might be attributed to specific characteristics of the server used for testing.

Furthermore, it is worth noting that the speedup achieved by the multiplication/reduction operation is approximately 1.5 times greater than that of the multiplication operation alone. This discrepancy can be attributed to the optimization opportunities inherent in the SIMD SSE assembly language code, which enhances the efficiency of the process.

Array Size	Multiplication			Multiplication/Reduction		
	Non-SIMD	SIMD	Speedup	Non-SIMD	SIMD	Speedup
1024	134.53	705.72	5.25	86.97	753.09	8.66
65536	235.97	1309.92	5.55	187.45	1692.13	9.03
524288	307.16	1103.44	3.59	183.53	1675.32	9.13
1048576	327.41	1673.71	5.11	199.5	1672.35	8.38
2097152	308.26	1139.41	3.7	196.55	1764.67	8.98
4194304	316.83	940.78	2.97	197.19	1680.82	8.52
8388608	316.09	964.83	3.05	196.29	1648.33	8.4