School of Electrical Engineering and Telecommunications

Term 1, 2025

Assignment 2

ELEC 2141
Digital Circuit Design

Your assignment solutions are to be submitted in pdf format on Moodle. Combine all scanned copies of your handwritten work and electronic documents into one pdf file for the submission.

In your submission file include a scanned copy of a completed and signed assignment submission form as the front page.

Your design should aim at achieving an optimized implementation. Your report should include your design procedure, choice of technology implementation, and simulation results. The gate input cost must be also calculated. Use Vivado to simulate and verify your design.

Attach all design and simulation materials such as schematic diagram (or HDL), simulation outputs and testing fixtures.

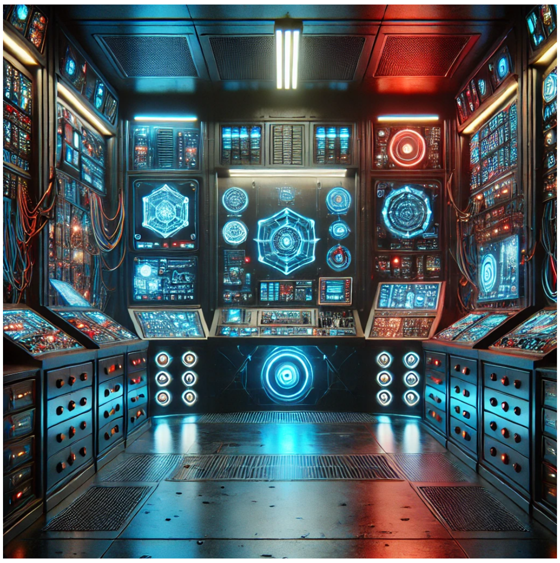
Any output of generative AI software used within your assignment must be attributed with full referencing. If the outputs of generative AI such as ChatGPT form part of your submission and is not appropriately attributed, it will be regarded as serious academic misconduct and subject to the standard penalties, which may include 00FL, suspension and exclusion.

*To cite: OpenAI (Year Accessed). ChatGPT. OpenAI. https://openai.com/models/chatgpt/

*Please note that the outputs from these tools are not always accurate, appropriate, nor properly referenced. You should ensure that you have moderated and critically evaluated the outputs from generative AI tools such as ChatGPT before submission.

DUE DATE: 28th APRIL 2025, 23:59 PM

The Digital Dungeon – Part Two



ARC UNSW is back again. Their sponsor was so impressed with your efforts in assignment 1 that they have a second task for you!

ARC has decided to make the escape room more difficult. To achieve this, teams will be given a limited amount of time to complete the escape room; each challenge will have an equal amount of time. They want you to design a finite state machine (FSM) that controls the amount of time teams available to complete the three challenges in the escape room presented in Assignment 1. The FSM controlling time available to the teams is reset when the start button is pressed (START = 1). The FSM will stay on until the end of the sequence. It sequences through an initial reading time, challenge 1, challenge 2 and challenge 3 and then returns to the start. The same amount of time is allocated to the initial reading time and each of the three challenges.

An external timer tracks the duration allotted for each challenge. It begins ticking as soon as the start button is pressed. The timer generates an output (TIME = 1) at the end of its duration which is fed as an input to the FSM. It then resets itself and starts again. COMP from challenge 1, OUTS from challenge 2 and CODE from challenge 3 are additional inputs to the FSM used to check whether teams have completed the challenges. Teams will stay at initial reading time, challenge 1 and challenge 2 while TIME = 0. They will transition from initial reading time to challenge 1, challenge 1 to challenge 2 and challenge 2 to challenge 3 when TIME = 1 regardless of whether each of these challenges are complete. At challenge 3, if all challenges are complete regardless of the value of TIME, the FSM will provide an output OVER = 1. OVER will be reset when START=1. If when TIME = 1 at challenge 3 and any of the challenges are incomplete (i.e. CODE ≠ 0000 or COMP ≠ 00 or OUTS ≠ 0000), teams will be sent to challenge 1 again to try and complete them. Organisers will have the ability to give teams an unspecified bonus time. They will then manually reset the FSM at the end of the bonus time they choose to give.

For your assignment, you need to

1. Identify the system inputs and outputs.
2. Draw a state diagram for the FSM.
3. Determine if the number of states can be reduced and assign them with binary codes.
4. Design and implement the FSM using D, T and JK flip-flops.
5. Write Verilog HDL models for:
    a. The FSM based on the state diagram in (2) (behavioural modelling)
    b. The JK flip-flop sequential circuit that you implement in (4) (structural or dataflow modelling)
6. Verify the HDL models in (5)

Submission

You must submit your assignment solution as a single pdf on Moodle. This should contain:

- Completed and signed assignment submission form as the front page
- State diagram
- Implementation
- Verilog HDL code (screenshots or text)
- Verilog testbenches (screenshots or text)
- Simulation results (screenshots)

Refer to the marking guidelines for further information.

In addition to the report, you must also submit all your Verilog modules (excluding testbenches) as separate files. As we will be running an autotest script on your code, you will need to use the following structure:

Behavioural Model: Your top-level module must be named ass2_behavioural and must have the following port names **(If these do not exactly match then your design will fail the autotests, order doesn't matter)**:
Inputs: START, TIME, COMP[1:0], OUTS[3:0], CODE[3:0]
Outputs: OVER

Structural/Dataflow Model: Your top-level module must be named ass2_structural and must have the following port names **(If these do not exactly match then your design will fail the autotests, order doesn't matter)**:
Inputs: START, TIME, COMP[1:0], OUTS[3:0], CODE[3:0]
Outputs: OVER

Any file that is not a top-level module can be named whatever you like.