School of Electrical Engineering and Telecommunications

Term 1, 2025

Assignment 2 Marking Guidelines

ELEC 2141
Digital Circuit Design

Assignment 2 has one design problem with the following the marking breakdown as follows:

1. State diagram: (30 marks)
   - Any assumptions made must be explicitly stated.
   - You may concisely re-write the specification including your design assumptions if needed.
   - Clearly draw the state diagram.
   - Clearly describe in words what each state stands for.
   - Draw the state table.
   - Apply state minimization to see if states can be reduced (all steps must be shown).
2. Implementation (40 marks)
   - State assignment and re-draw the state table.
   - Obtain excitation equations (flip-flop input equations) for all flip-flops used (T, JK and D). Show all tables and K-maps used clearly. In the case of K-maps, indicate which essential prime implicates or prime implicates are used.
   - Draw the logic diagram or schematics for each implementation.
   - Indicate the GIC of the associated combinational circuit in each of the implementations and make a comment on the best implementation. Do not include the flipflops in the cost.
3. Verification: (30 marks)
   - Write Verilog test benches for both of your implementations (state diagram and JK FF implementation) – you need to attach screenshots of the files.
   - The test bench should be developed such that each state is visited at least once.
   - Include the simulation results (attach screenshots of the file).
   - It should clearly show the waveforms for the inputs, states, and output.
   - Verilog code autotest results.