Date: 18/04/2013 AN Time: 3 hours Full Marks: 100 Deptt: Computer Science & Engg

No. of students: 92 End-Spring Semester Examination 2012-13

Sub. No.: CS60003 Sub. Name: High Performance Computer Architecture

1st year M.Tech / 4th year M.Tech. (Dual)

Time: 3 hours Marks: 100

Instructions: *Answer all the questions*

All parts of a question must be answered together

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1. Answer the following. **[(2+2)+(5+1)+6+(6+2)=24]**

   a. For a cube network, define the mapping functions for 2^N nodes. What will be the number of recirculations (hops) in the worst case for going from any arbitrary source node to any arbitrary destination node?

   b. Using multiplexers and demultiplexers, design an 8×8 single-stage recirculating cube network. Hence explain the operation with the help of an example.

   c. Show the schematic diagram of an 8×8 multistage Omega network, clearly stating how the individual stage switch boxes are controlled.

   d. State the steps for synthesizing an $a^m \times b^m$ Delta network, and clearly explain how the individual stages are controlled. Hence show the schematic diagram of a $2^3 \times 3^3$ Delta network.

2. Answer the following. **[9+(2+4)+6+5=26]**

   a. Explain how the performance of a cache memory system can be improved by:

      i. Reducing the miss rate

      ii. Reducing the miss penalty

      iii. Reducing the hit time

      by taking one representative approach from each category.

   b. For a two-level cache (L1 and L2), distinguish between the local and global miss rates of the L2 cache. Derive an expression for the average memory access time of a two-level cache system, clearly defining the symbols used.

   c. Explain the snoopy cache coherence protocols for multiprocessors, with the help of cache state transition diagram. Assume a write-back cache, with write invalidation protocol.

   d. Distinguish between tightly-coupled and loosely-coupled multiprocessors with the help of diagrams. Hence mention with justification which cache coherence protocols would be more suited for the two architectures.

3. Answer the following. **[8+(4+4+4+4)+8=32]**

   a. For a simplified MIPS pipeline with the four stages *Issue*, *Read Operands*, *Execution*, and *Write Result*, explain how the scoreboard functions and updates its data structures as an instruction proceeds through the various stages during execution. Also explain clearly how and when the various hazards get detected.

   b. Show the MIPS64 code fragment to implement the following loop:

```
for (i=0; i<200; i++)
  A[i] = B[i] + C[i] * s;
```

   Assume that the arrays A, B, and C start from memory locations 2000, 5000 and 8000 respectively, and the scalar s is stored in location 7000.

   i) Calculate the number of clock cycles required to process the 200 data items, assuming that the normal forwarding/ bypassing hardware has been implemented, and the branch is handled by predicting it as not taken.

   ii) Unroll the loop 4 times (that is, have five copies of the loop body in the modified loop), and calculate the number of clock pulses required to process all the 200 data items.

   iii) Carry out instruction scheduling on the unrolled loop, and calculate the number of clock pulses required to process all the 200 data items.

   iv) For a VLIW processor with two load-store units, two arithmetic units, and one branch unit, schedule the unrolled loop, and estimate the number of clock cycles required to process all the 200 data items.

   c. Clearly explain the roles of branch prediction buffer (BPB) and branch target buffer (BTB) in reducing control hazard related stalls in a typical instruction pipeline. Hence comment on the suitability of these schemes with respect to the MIPS64 pipeline, with proper justification.

4. Write short notes on: **[3x6=18]**

   a. Handling exceptions in the MIPS64 pipeline

   b. Memory interleaving

   c. Role of compiler in improving performance in pipelined processors