High Performance Computer Architecture (CS60003)

Tutorial 1 Solutions

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Probable Solutions

1. Let us denote

   (a) CPI_{xM_1} - average CPI of a class X instruction on M_1.

   (b) CPI_{yM_1} - average CPI of a class Y instruction on M_1.

   (c) CPI_{xM_2} - average CPI of a class X instruction on M_2.

   (d) CPI_{yM_2} - average CPI of a class Y instruction on M_2.

   Assume there are n instructions of class X and class Y each.

   Average cycles required to execute a single instruction (CPI) of both M_1 and M_2 for B_1 is $\frac{1GHz}{100MIPS} = \frac{1\times10^9}{100\times10^6} = 10$.

   Average CPI on M_1 for B_1 can be expressed as:

$$\frac{n \times CPI_{xM_1} + n \times CPI_{yM_1}}{2n} = 10 \tag{1}$$

   Average CPI on M_2 for B_1 can be expressed as:

$$\frac{n \times CPI_{xM_2} + n \times CPI_{yM_2}}{2n} = 10 \tag{2}$$

   Equation (1) and (2) can be simplified to

$$CPI_{xM_1} + CPI_{yM_1} = 20 \tag{3}$$

$$CPI_{xM_2} + CPI_{yM_2} = 20 \tag{4}$$

   After replacing half of the class X instructions with class Y instructions (suite B_2), average CPI on M_1 can be expressed as

$$\frac{(\frac{n}{2} \times CPI_{xM_1} + \frac{n}{2} \times CPI_{yM_1}) + n \times CPI_{yM_1}}{2 \times n} \tag{5}$$

   and average CPI on M_2 can be expressed as

$$\frac{(\frac{n}{2} \times CPI_{xM_2} + \frac{n}{2} \times CPI_{yM_2}) + n \times CPI_{yM_2}}{2 \times n} \tag{6}$$

   It is given that M_1's running time is 80% of M_2. Therefore, we can relate these two average CPIs as

$$\frac{(\frac{n}{2} \times CPI_{xM_1} + \frac{n}{2} \times CPI_{yM_1}) + n \times CPI_{yM_1}}{2 \times n} = 0.8 \times \frac{(\frac{n}{2} \times CPI_{xM_2} + \frac{n}{2} \times CPI_{yM_2}) + n \times CPI_{yM_2}}{2 \times n} \tag{7}$$

   This can be simplified to

$$CPI_{xM_1} + 3 \times CPI_{yM_1} = 0.8 \times CPI_{xM_2} + 2.4 \times CPI_{yM_2} \tag{8}$$

Similarly, for suite B_3, average CPI on M_1 can be expressed as

$$\frac{n \times CPI_{xM_1} + (\frac{n}{2} \times CPI_{xM_1} + \frac{n}{2} \times CPI_{yM_1})}{2 \times n} \tag{9}$$

and average CPI on M_2 can be expressed as

$$\frac{n \times CPI_{xM_2} + (\frac{n}{2} \times CPI_{xM_2} + \frac{n}{2} \times CPI_{yM_2})}{2 \times n} \tag{10}$$

It is given that M_1's running time is 1.4 times of M_2. Therefore, we can relate these two quantities as

$$\frac{n \times CPI_{xM_1} + (\frac{n}{2} \times CPI_{xM_1} + \frac{n}{2} \times CPI_{yM_1})}{2 \times n} = 1.4 \times \frac{n \times CPI_{xM_2} + (\frac{n}{2} \times CPI_{xM_2} + \frac{n}{2} \times CPI_{yM_2})}{2 \times n} \tag{11}$$

This can be simplified to

$$3 \times CPI_{xM_1} + CPI_{yM_1} = 4.2 \times CPI_{xM_2} + 1.4 \times CPI_{yM_2} \tag{12}$$

Solve the 4-variable system of equations formed by Equations (3), (4), (8) and (12). This gives the required CPIs

(a) $CPI_{xM_1} = 8.66$
(b) $CPI_{yM_1} = 11.33$
(c) $CPI_{xM_2} = 3.33$
(d) $CPI_{yM_2} = 16.66$

2. (a) Here, 70% of the computation time can be used by the floating-point processor. Hence, $F_{enh} = 0.7$. The speedup of the floating-point processor is 30% faster. Hence, $S_{enh} = 1.3$. Thus, according to Amdahl's Law,

$$\begin{aligned} \text{Overall Speedup} &= \frac{1}{(1 - F_{enh}) + \frac{F_{enh}}{S_{enh}}} \\ &= \frac{1}{(1 - 0.7) + \frac{0.7}{1.3}} \\ &= \frac{1}{0.3 + 0.538} \\ &= 1.19 \end{aligned}$$

(b) Take **Cost/Speedup** ratio to quantitatively compare between the two options. We will select the Option having lower value of this ratio.

Option 1: Here, 80% of the computation time can be used by the floating-point processor. Hence, $F_{enh} = 0.8$. $S_{enh} = 1.3$ as before. Thus, according to Amdahl's Law,

$$\begin{aligned}
\text{Overall Speedup} &= \frac{1}{(1 - F_{enh}) + \frac{F_{enh}}{S_{enh}}} \\
&= \frac{1}{(1 - 0.8) + \frac{0.8}{1.3}} \\
&= \frac{1}{0.2 + 0.615} \\
&= 1.22
\end{aligned}$$

Cost/Speedup $= 50/1.22 = 40.98$

Option 2: Here, 60% of the computation time can be used by the floating-point processor. Hence, $F_{enh} = 0.6$. The speedup of the floating-point processor, in this case, is 100% faster. Hence, $S_{enh} = 2$. Thus, according to Amdahl's Law,

$$\begin{aligned}
\text{Overall Speedup} &= \frac{1}{(1 - F_{enh}) + \frac{F_{enh}}{S_{enh}}} \\
&= \frac{1}{(1 - 0.6) + \frac{0.6}{2}} \\
&= \frac{1}{0.4 + 0.3} \\
&= 1.42
\end{aligned}$$

Cost/Speedup $= 60/1.42 = 42.25$

Therefore, **Option 1** is better because it has a smaller **Cost/Speedup** ratio.

3. The code after register renaming is as follows:

```
LD    T9,0(Rx)
MULD  T10,F0,T9
DIVD  T11,F0,T9
LD    T12,0(Ry)
ADDD  T13,F0,T12
ADDD  T14,T11,T9
SD    T12,0(Ry)
LD    T15,0(Rx)
MULD  T16,F0,T15
DIVD  T17,F0,T15
LD    T18,0(Ry)
ADDD  T19,F0,T18
ADDD  T20,T17,T15
SD    T18,0(Ry)
```

4. The instruction status table at the end of two loops:

Instruction	**Issue**	**Execute**	**Write**
LD	1	2	10
MULTD	2	11	15
SD	3	16	17
LD	6	10	11
MULTD	7	15	19
SD	8	20	21