High Performance Computer Architecture (CS60003)

Short Test 1

Indian Institute of Technology Kharagpur

Duration: 30 mins **Full Marks: 15**

Answer All Questions

Question set 1: Consider the instruction sequence that executes according to Tomasulo's algorithm with Re-order Buffer (RoB) and Load-Store Queue (LSQ).

Label	Instruction	Operands		
Loop:	LD	R0	3(R2)	
	MUL	R4	R0	R1
	ST	R4	4(R1)	
	SUB	R2	R4	2(R3)
	BNE	R4	R2	Loop

The instructions are issued and committed in order. Assume there are 2-entry reservation station for ADD/SUB and 2-entry reservation station for MUL/DIV. There is one execution unit for ADD/SUB and one execution unit for MUL/DIV. The RoB can hold upto 12 instructions and the LSQ can hold upto 3 instructions . The load/store instruction takes 1 cycle, addition/subtraction instruction takes 4 cycles, multiplication takes 8 cycles whereas the branch decision takes 1 cycle to finish. For LD instruction, the cache miss penalty is 4 cycles. Therefore, for a LD instruction that suffered a cache miss, the total execution time will be (1+4) cycles. We assume the followings-

1. The initial content of the registers R0, R1, R2 and R3 are 4, 2, 0 and 1 respectively.
2. The initial value in any memory address is same as the address. For example, value at MEM[10] is 10.
3. The first L.D instruction faced a cache miss and for the rest of the iterations, it faced cache hit.
4. The ST instruction has a write back stage of 1 cycle.
5. The branch instruction does not require write back stage.
6. The Branch Predictor takes the decision of always Taken in every invocation.
7. Same cycle broadcast and capture is not allowed.
8. Reservation station is freed on broadcast and not on dispatch.

Answer the following questions-

1. What will be the cycle number at which the first occurrence of the instruction BNE is issued, executed and committed ?
2. How many instructions will be flushed from RoB if the branch is mis-predicted in the first iteration of the loop?

Please submit your calculations for the above questions at the end of the exam to Moodle. Your submission has to be a scanned document in your own **handwriting** and it has to contain all the related intermediate tables which need to be computed for this problem.

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Answer All Questions

Question set 2: Consider the instruction sequence that executes according to Tomasulo's algorithm with Re-order Buffer (RoB) and Load-Store Queue (LSQ).

Label	Instruction	Operands		
Loop:	LD	R0	3(R2)	
	MUL	R1	R0	R2
	ADD	R2	R1	R3
	SUB	R4	R0	R1
	MUL	R2	R2	R3
	ST	R4	3(R2)	
	BNE	R4	R2	Loop

The instructions are issued and committed in order. Assume there are 2-entry reservation station for ADD/SUB with and 2-entry reservation station for MUL/DIV. There are two execution units for ADD/SUB and one execution unit for MUL/DIV. The RoB can hold upto 12 instructions and the LSQ that can hold upto 4 instructions. The load/store instruction takes 2 cycles, addition/subtraction instruction takes 3 cycles, multiplication takes 8 cycles whereas the branch decision takes 4 cycles to finish (branch instruction does not require write back). For L.D instruction, the cache miss penalty is 5 cycles. Therefore, for a LD instruction that suffered a cache miss, the total execution time will be (2+5) 7 cycles.

We assume the followings-

1. The initial content of the registers R0, R1, R2 and R3 are 4, 2, 0 and 1 respectively.
2. Assume that the initial value in any memory address is *same as the address*. For example, value at MEM[10] is 10.
3. The first L.D instruction faced a cache miss and for the rest of the iterations, it faced cache hit.
4. The ST instruction has a write back stage of 1 cycle.
5. The branch instruction does not require write back stage.
6. The Branch Predictor takes the decision of always Taken in every invocation.
7. Same cycle broadcast and capture is not allowed.
8. Reservation station is freed on broadcast and not on dispatch.

Answer the following questions-

1. What will be the cycle number at which the first occurrence of the instruction BNE is issued, executed and committed ?
2. How many instructions will be flushed from RoB if the branch is mis-predicted in the first iteration of the loop?

Please submit your calculations for the above questions at the end of the exam to Moodle. Your submission has to be a scanned document in your own **handwriting** and it has to contain all the related intermediate tables which need to be computed for this problem.

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Answer All Questions

Question set 3: Consider the instruction sequence that executes according to Tomasulo's algorithm with Re-order Buffer (RoB) and Load-Store Queue (LSQ).

Label	Instruction	Operands		
Loop:	LD	R1	0(R3)	
	LD	R2	0(R4)	
	MUL	R5	R1	R2
	ADD	R5	R5	R6
	ST	R5	0(R3)	
	SUB	R2	R2	R0
	BNE	R2	R7	Loop

The instructions are issued and committed in order. Assume there is one execution unit for ADD/SUB with a 6-entry reservation station, and one for DIV/MUL operations with a 4-entry reservation station. There is also a Load Store unit. The ROB can hold upto 12 instructions and the LSQ can hold upto 6 instructions.

The load/store instruction takes 2 cycles, addition/subtraction instruction takes 1 cycle, multiplication takes 8 cycles whereas the branch decision takes 2 cycles to finish (branch instruction does not require write back).

Assume that the cache is write-through and the cache miss penalty is 5 cycles. Therefore, for a LD instruction that suffered a cache miss, the total execution time will be (2+5=) 7 cycles. Similarly, for all SD instructions, the execution time will be 7 cycles.

The initial content of the registers R0, R3, R4, R6 and R7 are 5, 10, 20, 50 and 10 respectively. Assume that the initial value in any memory location is same as the address value. For example, value at MEM[10] is 10.

We also assume that the first two LD instruction will face a cache miss and the Branch Predictor takes the decision of "Always Taken" in every invocation. Same cycle broadcast and capture is not allowed. Assume the store instruction also passes through the write-back stage (of one cycle). Reservation entries are freed on dispatch.

1. What will be the cycle number at which the first occurrence of the instruction BNE is issued, executed and committed ?

2. What will be the cycle number at which the second occurrence of the instruction BNE is issued, executed and committed ?

Please submit your calculations for the above questions at the end of the exam to Moodle. Your submission has to be a scanned document in your own **handwriting** and it has to contain all the related intermediate tables which need to be computed for this problem.

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Answer All Questions

Question set 4: Consider the instruction sequence that executes according to the Tomasulo's algorithm with Re-order Buffer (RoB) and Load-Store Queue (LSQ).

Label	Instruction	Operands		
Loop:	L.D	R0	3(R2)	
	MUL.D	R4	R0	R1
	S.D	R4	4(R1)	
	ADD.D	R1	R0	R4
	ADD.D	R3	R1	R1
	SUB.D	R2	R4	R3
	BNE	R4	R2	Loop

The instructions are issued and committed in order. Assume there is a 3-entry reservation station for ADD/SUB unit (only one unit is present), and a 2-entry reservation station is available for MUL/DIV unit (only one unit is present). The RoB can hold up to 12 instructions, and the LSQ can hold up to 3 instructions. A load/store instruction takes 1 cycle, an addition/subtraction instruction takes 2 cycles, a multiplication takes 5 cycles, whereas a branch decision takes 1 cycle to finish (all are execution cycles, a branch instruction *does not* require write back).

For the load instructions, the cache miss penalty is 3 cycles (in addition to the load instruction execution cycles without cache miss). Assume, the store instruction always writes to cache (write-back cache, no penalty).

We also assume that the first load instruction for an address faces a cache miss (applies to all *new* addresses accessed by load), and the branch predictor decides **always taken** for every invocation.

Assume the store instruction has the write-back stage of one cycle, similar to other instructions (i.e. it has issue, execute, write-back, and commit rather than only issue, execute, and commit). Reservation station entries are freed on **dispatch** and same cycle broadcast and capture is not allowed.

The initial contents of the registers R0, R1, R2, and R3 are 4, 2, 0, and 1 respectively. Assume that the initial value at any memory address is the *same as the address*. For example, value at MEM[10] is 10.

1. What will be the cycle number at which the first occurrence of the instruction BNE is issued, executed and committed?

2. How many instructions will be flushed from RoB if the branch is mis-predicted in the first iteration of the loop?

Please submit your calculations for the above questions at the end of the exam to Moodle. Your submission has to be a scanned document in your own **handwriting**, and it must contain all the related intermediate tables which need to be computed for this problem.

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Answer All Questions

Question set 5: Consider the instruction sequence that executes according to Tomasulo's algorithm with Re-order Buffer (RoB) and Load-Store Queue (LSQ).

Label	Instruction	Operands		
Loop:	L.D	R0	3(R2)	
	MUL.D	R4	R0	R1
	SUB.D	R2	R0	R4
	ADD.D	R0	R2	R3
	S.D	R4	3(R0)	
	BNE	R4	R2	Loop

The instructions are issued and committed in order. Assume there are 2-entry reservation station for ADD/SUB with and 2-entry reservation station for MUL/DIV. The RoB can hold upto 12 instructions and the LSQ that can hold upto 4 instructions. The load/store instruction takes 2 cycle, addition/subtraction instruction takes 1 cycle, multiplication takes 5 cycles whereas the branch decision takes 1 cycle to finish (branch instruction does not require write back).

For L.D instruction, the cache miss penalty is 5 cycles. Therefore, a LD instruction that suffered a cache miss the total execution time is (2+5 = 7 cycles).

The initial content of the registers R0, R1, R2 and R3 are 4, 2, 0 and 1 respectively. Assume that the initial value in any memory address is same as the address. For example, value at MEM[10] is 10.
We also assume that the first L.D instruction faced a cache miss and the Branch Predictor takes the decision of always Taken in every invocation. Same cycle broadcast and capture is not allowed. Reservation stations are freed on dispatch.

1. What will be the cycle number at which the first occurrence of the instruction BNE is issued, executed and committed ?
2. How many instructions will be flushed from RoB if the branch is mis-predicted in the first iteration of the loop?

Please submit your calculations for the above questions at the end of the exam to Moodle. Your submission has to be a scanned document in your own **handwriting** and it has to contain all the related intermediate tables which need to be computed for this problem.

Answer:

1. BNE
   (a) Issue: Cycle 6
   (b) Execute: Cycle 18
   (c) Committed: Cycle 24
2. Five(5) entries will be dropped from RoB in case of an exception.