Tutorial - II (ROB and LSQ)

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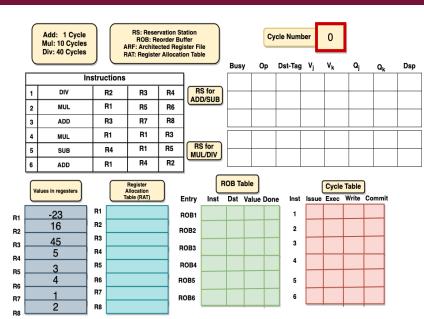


Reorder Buffer Example

Sequence	Instruction	O	oeran	ds
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R4	R1	R2

Consider the above instruction set compromising of 6 instructions. Assume there are two independent execution units for ADD/SUB and MUL/DIV with a 3-entry and 2-entry reservation station per unit respectively. The Reorder Buffer can hold upto 6 instructions. The instructions are issued and committed in order. Fill up the table with the cycle number of each operation for all the instructions under these assumptions.





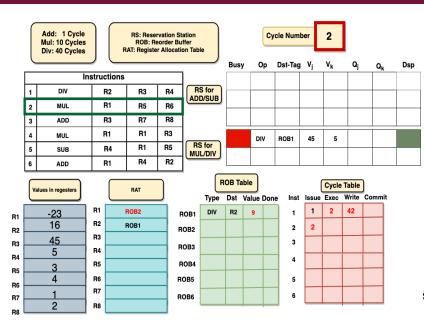


RS: Reservation Station Add: 1 Cycle Cycle Number **ROB: Reorder Buffer** Mul: 10 Cycles ARF: Architected Register File Div: 40 Cycles RAT: RegisterAlias Table Busy Dst-Tag V_i V_k Q_i Dsp Q_k Instructions DIV R2 R3 R4 RS for ADD/SUB R1 R5 R6 2 MUL R7 R8 ADD R3 R3 R1 R1 MUL ROB1 45 DIV 5 R1 R5 R4 5 SUB RS for MUL/DIV R4 R2 R1 ADD **ROB Table** Cycle Table Values in registers RAT Dst Value Done Inst Issue Exec Write Commit Entry Type R1 DIV R2 -23 1 ROB1 R1 16 R2 ROB1 2 ROB2 R2 R3 45 3 R3 ROB3 5 R4 R4 4 R5 ROB4 3 R5 4 R6 ROB5 5 R6 R7 ROB6 6 R7 2

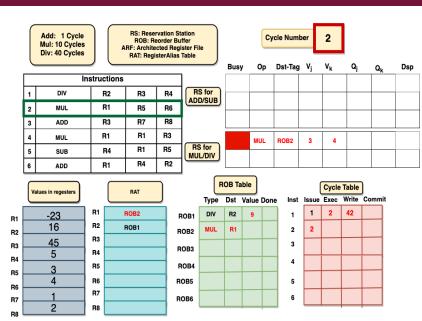


R8

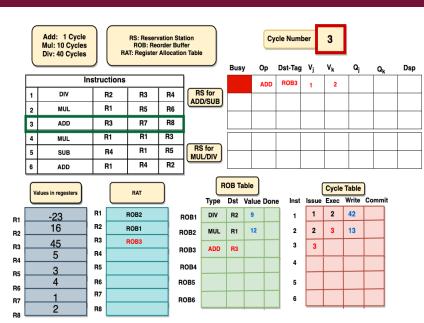
R8



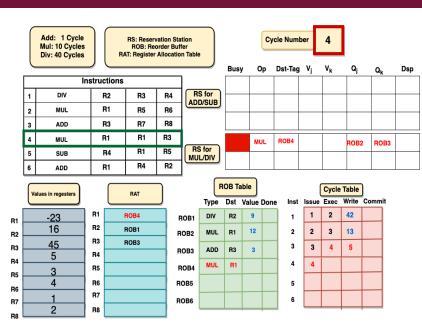




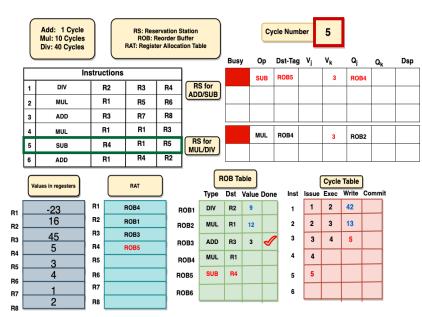




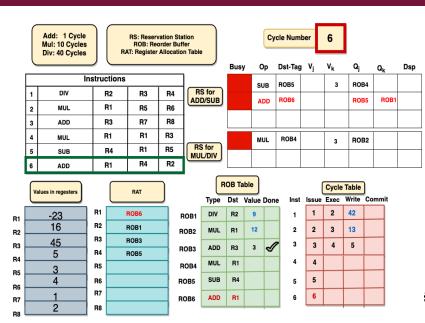




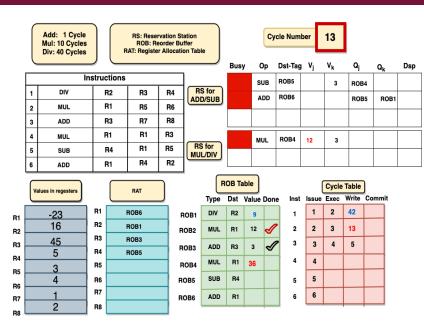




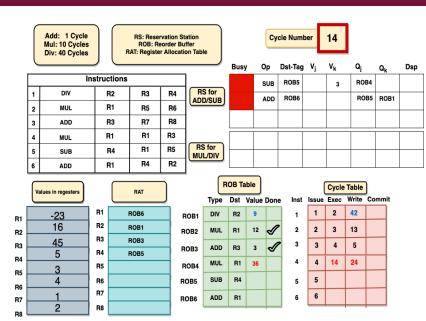




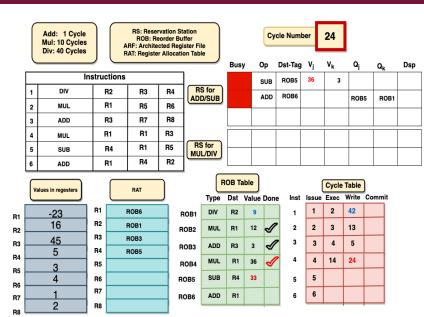




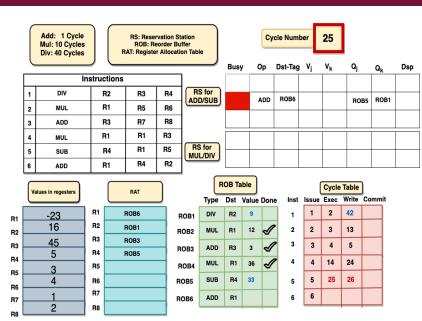




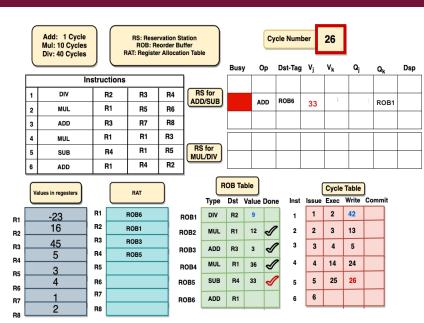




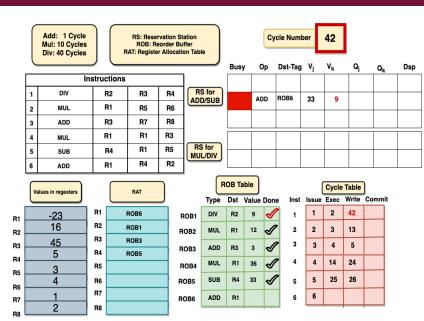




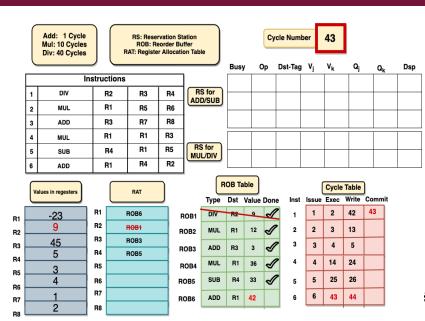














Add: 1 Cycle Mul: 10 Cycles Div: 40 Cycles

RS: Reservation Station ROB: Reorder Buffer **RAT: Register Allocation Table** Cycle Number

Dst-Tag Vi

_				
	Ins	structions		
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

RS for MUL/DIV

ROB5

ROB6

1				
ا				
1				
J				

	Values in regesters		
	12	R1	
R1 R2	9	R2	
R3	45	R3	
R4	5	R4	
R5	3	R5	

4

Register Alias Table (RAT)

R1	ROB6	
R2		
R3	ROB3	
R4	ROB5	
R5		
R6		
R7		
R8		

	Type	Dst	Value	Done	In
ROB1					1
ROB2	MUL	Ri	12	1	2
ROB3	ADD	R3	3	€	3
ROB4	MUL	R1	36	€	4
	CIIR	D/	22	-1	

R1

42

ADD

ROB Table

Busy

	l	Cycle	lable	l	
st	Issue	Exec	Write	Comm	it
1	1	2	42	43	l
2	2	3	13	44	
3	3	4	5		
4	4	14	24		l
5	5	25	26		
6	6	43	44		

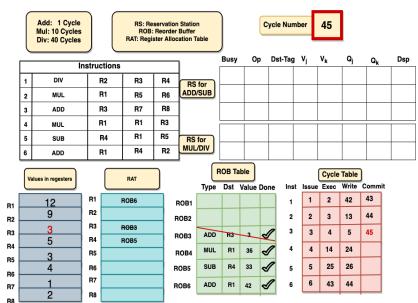
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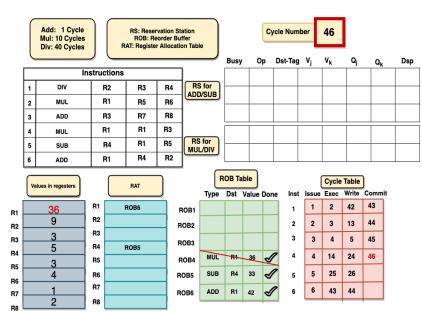
Dsp

R6

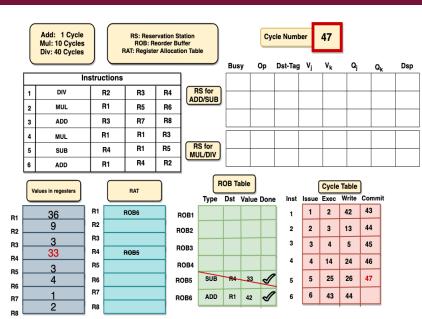
R7 R8



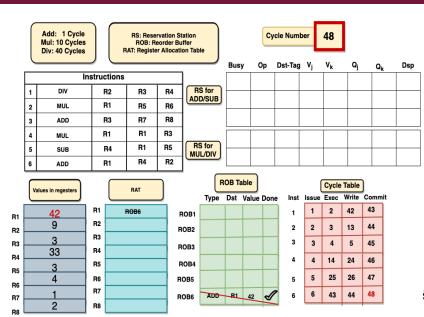














Add: 1 Cycle RS: Reservation Station Cycle Number Mul: 10 Cycles ROB: Reorder Buffer Div: 40 Cycles **RAT: Register Allocation Table** Dst-Tag V_i Q_i Busy Dsp Q Instructions RS for DIV R2 R3 R4 ADD/SUB R1 MUL R5 R6 2 R8 ADD R3 R7 3 R3 R1 R1 MUL RS for R1 R5 SUB R4 5 MUL/DIV R1 R4 R2 ADD **ROB Table** Cycle Table Values in regesters RAT Inst Issue Exec Write Commit Type Dst Value Done 43 R1 2 42 42 ROB1 R1 9 R2 2 3 13 44 ROB2 R2 R3 3 3 45 R3 3 4 5 ROB3 33 R4 R4 46 4 14 24 R5 ROB4 3 R5 25 26 47 4 5 R6 ROB5 5 R6 R7 43 48 44 ROB6 R7 2 R8



R8

ROB and LSQ example

Consider the given instruction set compromising of 12 instructions. Assume there are two independent execution unit, one for ADD/SUB and one for MUL/DIV with a 3-entry and 2-entry reservation station per unit respectively and one load/store execution unit. The Reorder Buffer can hold upto 12 instructions and Load Store Queue can hold upto 6 entries. The branch predictor takes the decision of always Not Taken. The instructions set are issued and committed in order. Fill up the table with the cycle number of each operation for all the instructions under these assumptions.



ROB	Туре	Destination	Value		
1	DIV	R1	R2	R3 Cache hit	
2	LD	R4	10(R2)	Cache III	
3	BNE	R1	R2	label	
4	SUB	R1	R2	R3	
5	LD	R2	15(R1)		
6	ST	R5	10(R3)		
7	ADD	R1	R1	R2	
8	SUB	R4	R4	R3 Cache n	
9	ST	R3	30(R6)	n (10 cycles	penalty)
10	ADD	R5	R2	R3 //	
11	LD	R4	0(R3)	7	
12	LD	R1	0(R6)	\overline{V}	

Load/Store: 1 cycle Add/Sub: 2 cycles Mul: 10 cycles DIV: 20 cycles Branch decision: 2 cycles

Register content	R1	12
	R2	80
	R3	40
	R4	56
	R5	30
	R6	10



	Sequence	Instruction	Issue	Execute	Write	Commit
	1	DIV R1, R2, R3	1	2	22	23
Commit	2	LD R4, 10(R2)	2	3	4	24
	3	BNE R1, R2, label	3	23		25
Issue	4	SUB R1, R2, R3	4	5	7	
	5	LD R2, 15(R1)	5	23	-33-	
	6	ST R5, 10(R3)	6	7	8	
	7	ADD R1, R1, R2	7	-34-	-36-	
	8	SUB R4, R4, R3	8	9	11	
	9	ST R3, 30(R6)	9	10	11	
	10	ADD R5, R2, R3	10	-37-	-39 -	
	11	LD R4, 0(R3)	11	12	13	
(<u> </u>	12	LD R1, 0(R6)	12	13	23	



CYCLE: 25

	J				
ROB	Туре	Destination	Value	Done	Commit
ROB1	DIV	R1	2	1	1
ROB2	LD	R4	11	1	1
ROB3	BNE	R1	!	1	1
ROB4	SUB	R1	40	1	0
ROB5	LD	R2			0
ROB6	ST	R5	10	1	0
ROB7	ADD	R1			0
ROB8	SUB	R4	16	1	0
ROB9	ST	R3	15	1	0
ROB10	ADD	R5			0
ROB11	LD	R4	15	1	0
ROB12	LD	R1	2	1	0

Regester content			
R1	12 2		
R2	80		
R3	40		
R4	-56- 11		
R5	30		
R6	10		

RAT

R1	ROB1 ROB7
R2	ROB5
R3	
R4	ROB2
R5	
R6	

RS for	
ADD/SUE	
ADDISOL	

ROB Table

_	UР	DSt-Tag	. ")	. *k	۳,	. uk	
r_	SUB	ROB4	80	40			ı
JB	ADD	ROB7	2		ROB1	ROB5	
	SUB	ROB8		10	ROB2		
	ADD	ROB10		40	ROB5		ſ

	Op	Dst-Tag	Tag1	Tag2	Val1	Val2
RS for MUL/DIV	DIV	ROB1	80	40		

LSQ

L/S	Address	Value	Commit
LD	80+10= 90	11 (assume)	
LD	ROB1+15=17	5 (assume)	
ST	10+40= 50	10 (assume)	
ST	30+10= 40	15 (assume)	1
LD	40	15 🕡	
LD	10	2 (assume)	



Thank You 1

¹Most of the material are taken from the famous book on Comp Arch by Hen/Pat, Comp Arch course by Milos Prvulovic for teaching purposes

