



Dr. H N National College of Engineering
Approved by All India Council for Technical Education
(AICTE), Govt. of India and affiliated to Visvesvaraya
Technological University (VTU)
36B Cross, Jayanagar 7th block, Bangalore – 560070



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course: Electronic Principles and Circuits

**Course Code: BEC303
III-SEMESTER**

**[AS PER OUTCOME BASED EDUCATION (OBE) AND CHOICE BASED CREDIT
SYSTEM (CBCS) 2025 SCHEME]**

Academic Year – 2025-2026

LAB MANUAL

Prepared by:

Dr. Ravindra S

Department of ECE

Our Vision

To impart perseverant education leading to greater heights

Our Mission

- By providing well-designed physical infrastructure with technology with a supportive community
- By building resilience through self-awareness, stress management and growth mind set
- By developing a sense of responsibility and accountability
- By developing empathy, integrity, self-reflection and self-improvement

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Electronics and Communication Engineering

Scheme of Teaching and Examinations 2022

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2025 - 26)

Integrated Professional Core Course (IPCC)

Refers to Professional Theory Core Course Integrated with Practical is of the same course

Course: Electronic Principles and Circuits

Course Code: BEC303

TABLE OF CONTENTS

| Item | Page No. |
|---|----------|
| Program Outcomes (POs) and Program Specific Outcomes (PSOs) | ii |
| Syllabus- Course Objectives & Suggested Learning Resources | vi-viii |
| Course Outcomes- Mapping of Course Outcomes with POs & PSOs | ix |
| Assessment Details (both CIE and SEE) -Scheme of Evaluation | x-xii |
| List of Major Equipment | xiv |
| List of Experiment/Programs & Additional Experiment/Programs | xv |

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

After 4 years of graduation, graduates will be able to

PEO1: To develop in students, the ability to solve real life problems by applying fundamental science and elementary strengths of computer science courses.

PEO2: To mould students, to have a successful career in the IT industry where graduates will be able to design and implement the needs of society and nation.

PEO3: To transform students, to excel in a competitive world through higher education and indulge in research through continuous learning process.

PROGRAM OUTCOMES (POs)

- PO1: Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- PO2: Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- PO3: Design/Development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- PO4: Conduct Investigations of Complex Problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- PO5: Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
- PO6: The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- PO7: Environment and Sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- PO8: Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- PO9: Individual and Team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- PO10: Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- PO11: Project Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- PO12: Life-Long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

At the end of the program, graduates will be able to

- PSO1:** Apply engineering principles, professional ethics and fundamental science in designing systems and communication models (protocols).
- PSO2:** Design and develop smart and intelligent based applications in computational environment.

SYLLABUS

ELECTRONIC PRINCIPLES AND CIRCUITS LABORATORY

[As per Choice Based Credit System (CBCS) scheme]

(Effective from the academic year 2022 -2023)

SEMESTER – III

| | | | |
|--------------------------------|--|-------------|-----|
| Course Code | BEC303 | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:2:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 20 Hours of Practicals | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

Course Learning Objectives:

CLO 1: Design and analysis of bridge rectifier, voltage regulator, clippers and clampers.

CLO 2: Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions

CLO 3: Design and testing of Precision Half wave and full wave rectifiers.

CLO 4: Design and testing of RC phase shift oscillator

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk
2. Live Demo with experiments
3. Power point presentation

Module-1

Transistor Biasing: Voltage Divider Bias, VDB Analysis, VDB Load line and Q point, Two supply Emitter Bias, Other types of Bias.

BJT AC models: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier, H parameters, Relations between R and H parameters.

Voltage Amplifiers: Voltage gain, Loading effect of Input Impedance.

CC Amplifiers: CC Amplifier, Output Impedance.

[Text1]

Module-2

MOSFET

Biassing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower.

[Text 2]

Module-3

Linear Opamp Circuits: Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis.

Oscillator: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.

The 555 timer: Monostable Operation, Astable Operation.

[Text1]

Module-4

Negative Feedback: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).

Active Filters: Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters.

[Text1]

Module-5

Power Amplifiers: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation.

Thyristors: The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors. [Text1]

PRACTICAL COMPONENT OF IPCC

| Sl. No | Experiments Simulation packages preferred: Multisim, Modelsim, PSpice or any other relevant |
|-----------|--|
| 1 | Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator |
| 2 | Design and Test Biased Clippers – a)Positive, b) Negative , c) Positive-Negative Positive and Negative Clampers with and without Reference. |
| 3 | Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor. |
| 4 | Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor. |
| 5 | Design and test Emitter Follower |
| 6 | Design and plot the frequency response of Common Source JFET/MOSFET amplifier |
| 7 | Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve. |
| 8 | Design and test Full wave Controlled rectifier using RC triggering circuit. |
| 9 | Design and test Precision Half wave and full wave rectifiers using Opamp |
| 10 | Design and test RC phase shift oscillator |

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

CO1: Understand the characteristics of BJTs and FETs for switching and amplifier circuits.

CO2: Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions

CO3: Understand the feedback topologies and approximations in the design of amplifiers and oscillators.

CO4: Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.

CO5: Understand the power electronic device components and its functions for basic power electronic circuits.

Suggested Learning Resources:**Textbooks**

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015. ISBN:978-0-19-808913-1

Weblinks and Video Lectures (e-Resources):

1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Assign the group task to Design the various types of counters and display the output accordingly
Assessment Methods

- Lab Assessment (25 Marks)
- GATE Based Aptitude Test

COURSE OUTCOMES

At the end of the course the student will be able to:

CO1: Understand the characteristics of BJTs and FETs for switching and amplifier circuits.

CO2: Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions

CO3: Understand the feedback topologies and approximations in the design of amplifiers and oscillators.

CO4: Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.

CO5: Understand the power electronic device components and its functions for basic power electronic circuits.

Mapping of Course Outcomes with POs & PSOs

| Course Outcomes (COs) | Program Outcomes (POs) | | | | | | | | | | | | Program Specific Outcomes (PSOs) | |
|-----------------------|------------------------|----------|----------|----------|----------|---|---|---|----------|----------|----|----|----------------------------------|----------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| CO1 | 2 | 2 | - | - | 3 | - | - | - | 1 | 1 | - | - | 1 | - |
| CO2 | 2 | 2 | 2 | 2 | 3 | - | - | - | 1 | 1 | - | - | 1 | - |
| CO3 | 2 | 2 | - | - | - | - | - | - | - | - | - | - | 1 | - |
| CO4 | 2 | 2 | - | - | - | - | - | - | - | - | - | - | - | 1 |
| CO5 | 2 | 2 | 2 | - | - | - | - | - | - | - | - | - | - | 1 |
| Average | 2 | 2 | 2 | 2 | 3 | - | - | - | 1 | 1 | - | - | 1 | 1 |

ASSESSMENT DETAILS (BOTH CIE AND SEE)

- The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).
- A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.
- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CONTINUOUS INTERNAL EVALUATION (CIE) for IPCC:

CIE THEORY + CIE PRACTICAL

❖ CIE for the theory component of the IPCC (Maximum Marks 25)

- **25 marks for the theory component** are split into
 - **15 marks** for two Internal Assessment Tests (Average of Two Tests each of 25 Marks , scale down the marks scored to 15 marks)
 - The first test at the end of 40-50% coverage of the syllabus and
 - The second test after covering 85-90% of the syllabus
 - **10 marks** for other assessment methods mentioned in 22OB4.2.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).
- The student has to secure 40% of 25 marks (10 marks) to qualify in the CIE of the theory component of IPCC.

❖ CIE for the practical component of the IPCC (Maximum Marks 25)

- **25 marks for the practical component** are split into
 - **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
 - On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.

- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for **50 marks** and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

Split-up of Marks used Practical Sessions

| Rubrics No. | Practical Sessions- Continuation Evaluation (CE) Methodology / Process Steps per Experiment | Marks |
|--|--|---------------------------|
| #R1 | Observation | 10 |
| #R2 | Record writing: Write up of Procedure / Algorithm/ Program and Execution/conduction of experiment | 30 |
| #R3 | Viva – Voce (Questions & Answers on relevant Experiment /Topic) | 10 |
| Total Marks | | 50 |
| (Note: Conduction of experiment's and Preparation of Laboratory records etc. for 50 Marks scale down the marks scored to 15 marks) | | (Scale down to 15) |
| Rubrics No. | Practical Sessions-Internal Assessment (IA) | Marks |
| #R1 | Write-up of Procedure/Program/Algorithm | 10 |
| #R2 | Conduction/Execution | 30 |
| #R3 | Viva-Voce | 10 |
| Total Marks | | 50 |
| (Note: One test after all experiment's conduction for 50 Marks scale down the marks scored to 10 marks) | | (Scale down to 10) |

SEMESTER END EXAMINATION (SEE) for IPCC:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.
- Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

To put it simply, evaluation techniques/methods are listed in the table for further understanding

| Evaluation Type | Maximum Marks | Minimum Passing Marks | Evaluation Details |
|--|---------------|-----------------------|---|
| CIE-IA Tests | 15 | 06 | Average of Two Tests each of 25 Marks, scale down the marks scored to 15 marks |
| CIE-CCAs | 10 | 04 | Any two assignment methods as per clause 22OB4.2 of Regulations (if assessment is project based, then one assessment method may be adopted) |
| Total CIE Theory | 25 | 10 | Scale down marks of tests and assignments to 25 |
| CIE Practical | 15 | 06 | Conduction of experiment's and Preparation of Laboratory records etc.... |
| CIE Practical Test | 10 | 04 | One test after all experiment's conduction for 50 Marks scale down the marks scored to 10 marks |
| Total CIE Practical | 25 | 10 | Scale down marks of experiment's record and test to 25 |
| TOTAL CIE= Total CIE Theory + Total CIE Practical | 50 | 20 | |
| SEE | 50 | 18 | SEE exam is a theory exam, conducted for 100 marks are scaled down to 50 marks |
| CIE+SEE | 100 | 40 | |

LIST OF EXPERIMENT/PROGRAMS

| Expt. No. | Details | Page No. |
|------------------|--|-----------------|
| | INTRODUCTION | 1-24 |
| 1 | Design and Test (iii) Bridge Rectifier with Capacitor Input Filter (iv) Zener voltage regulator | 25 |
| 2 | Design and Test Biased Clippers – a)Positive, b) Negative , c) Positive-Negative Positive and Negative Clampers with and without Reference. | 26 |
| 3 | Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor. | 26 |
| 4 | Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor. | 26 |
| 5 | Design and test Emitter Follower | 27 |
| 6 | Design and plot the frequency response of Common Source JFET/MOSFET amplifier | 28 |
| 7 | Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve. | 30 |
| 8 | Design and test Full wave Controlled rectifier using RC triggering circuit. | 32 |
| 9 | Design and test Precision Half wave and full wave rectifiers using Opamp | |
| 10 | Design and test RC phase shift oscillator | |
| | VIVA-VOCE | 42 |
| | APPENDIX | 43-44 |

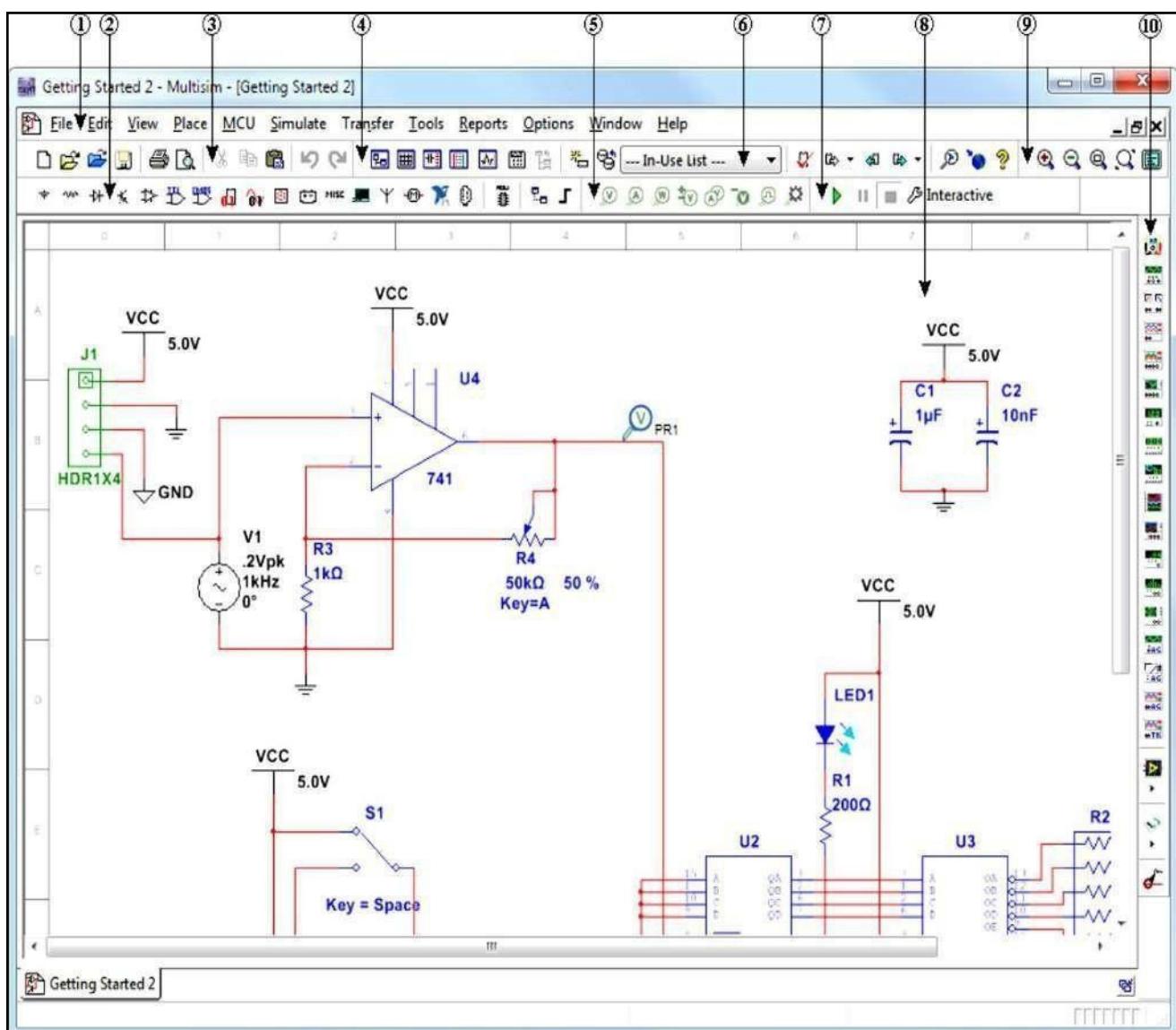
INTRODUCTION

❖ Introduction to the Multisim Interface

Multisim is the schematic capture and simulation application of National Instruments Circuit Design Suite, a suite of EDA (Electronics Design Automation) tools that assists you in carrying out the major steps in the circuit design flow. It provides a virtual environment for designing, testing, and simulating electronic circuits. Multisim allows users to create schematic diagrams, simulate circuit behavior, and analyze circuit performance. Multisim is designed for schematic entry, simulation, and feeding to downstage steps, such as PCB layout.

Multisim User Interface

The Multisim user interface includes the following elements:



Refer to the table below as needed:

| | Element | Description |
|----|---------------------|--|
| 1 | Menu Bar | Contains the commands for all functions. |
| 2 | Component Toolbar | Contains buttons that you use to select components from the Multisim database for placement in your schematic. |
| 3 | Standard Toolbar | Contains buttons for commonly-performed functions such as Save, Print, Cut, and Paste. |
| 4 | Main Toolbar | Contains buttons for common Multisim functions. |
| 5 | Place Probe Toolbar | Contains buttons that you use to place various types of probes on the design. You can also access Probe Settings from here. |
| 6 | In-Use Toolbar | Contains a list of all components used in the design. |
| 7 | Simulation Toolbar | Contains buttons for starting, stopping and pausing simulation. |
| 8 | Workspace | This is where you build your designs. |
| 9 | View Toolbar | Contains buttons for modifying the way the screen is displayed. |
| 10 | Instruments Toolbar | Contains buttons for each instrument. |

Installation steps are given below: Install Multisim by obtaining the software from National Instruments and following the provided installation instructions.

1. Launch Multisim and choose to **create a new project** or open an existing one from the start page.
2. Create a **new project** by giving it a name and choosing a save location.
3. Within the project, create a schematic by clicking "**New**" and selecting "**Schematic**."
4. Build your circuit on the schematic canvas by dragging components from the library and connecting them with wiring tools.
5. Optionally, add virtual instruments like oscilloscopes or multimeters to visualize and analyze your circuit during simulation.
6. Simulate your circuit by clicking on the "**Simulate**" tab, choosing the simulation type, adjusting settings, and **clicking "Run."**
7. Analyze simulation results using built-in instruments, graphs, and charts to understand circuit behavior.
8. Optionally, transfer your schematic to NI Ultiboard for PCB layout by clicking "Transfer to Ultiboard."
9. Save your project periodically, export simulation results or other data as needed, and close Multisim when finished.

Standard Toolbar

The **Standard** toolbar contains buttons for commonly performed functions. Its buttons are described below:

| Button | Description |
|--------|--|
| | New button. Creates a new circuit file. |
| | Open button. Opens an existing circuit file. |
| | Open Sample button. Opens a folder containing sample and getting started files. |
| | Save button. Saves the active circuit. |
| | Print Circuit button. Prints the active circuit. |
| | Print Preview button. Previews the circuit as it will be printed. |
| | Cut button. Removes the selected elements and places them on the Windows clipboard. |
| | Copy button. Copies the selected elements and places them on the Windows clipboard. |
| | Paste button. Inserts the contents of the Windows clipboard at the cursor location. |
| | Undo button. Undoes the most recently performed action. |
| | Redo button. Redoes the most recently performed undo. |

Components Toolbar

The buttons in the Components toolbar are described below. Each button will launch the place component browser (Select a Component browser) with the group specified on the button pre-selected.

| Button | Description |
|--------|---|
| | Place Source button. Selects the Source components group in the browser. |
| | Place Basic button. Selects the Basic components group in the browser. |
| | Place Diode button. Selects the Diode components group in the browser. |
| | Place Transistor button. Selects the Transistor components group in the browser. |
| | Place Analog button. Selects the Analog components group in the browser. |
| | Place TTL button. Selects the TTL components group in the browser. |
| | Place CMOS button. Selects the CMOS component group in the browser. |
| | Place Miscellaneous Digital button. Selects the Miscellaneous Digital component group in the browser. |
| | Place Mixed button. Selects the Mixed component group in the browser. |
| | Place Power Components button. Selects the Power component group in the browser. |
| | Place Indicator button. Selects the Indicator component group in the browser. |

| Button | Description |
|--------|---|
| | Place Miscellaneous button. Selects the Miscellaneous component group in the browser. |
| | Place Advanced Peripherals button. Selects the Advanced Peripherals component group in the browser. |
| | Place RF button. Selects the RF component group in the browser. |
| | Place Electromechanical button. Selects the Electromechanical component group in the browser. |
| | Place MCU button. Selects the MCU component group in the browser. |
| | Place Hierarchical Block button. Opens a file to be embedded as a hierarchical block. Refer to the <i>Hierarchical Design</i> section of Chapter 4, <i>Working with Larger Designs</i> , for more information. |
| | Place Bus button. Places a bus with segments created as you click on the workspace. Refer to the <i>Buses</i> section of Chapter 4, <i>Working with Larger Designs</i> , for more information. |

Simulation Toolbar

The **Simulation** toolbar contains buttons used during simulation.

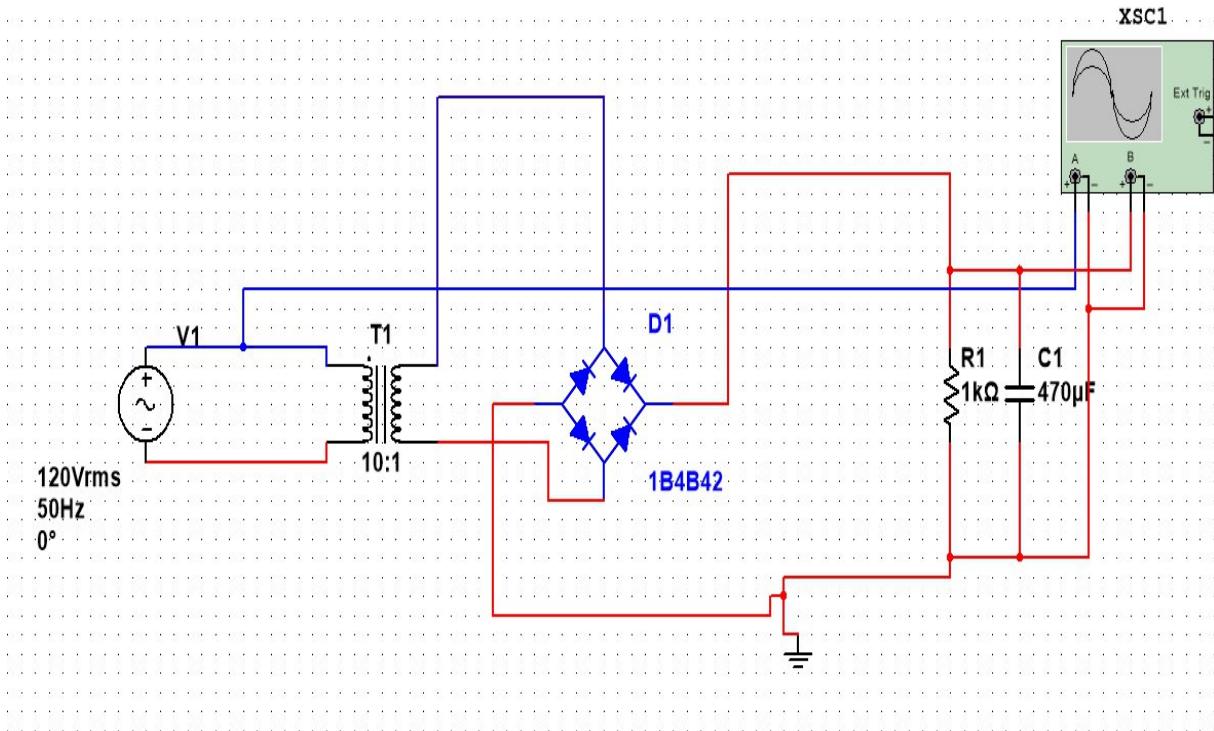
| Button | Description |
|---|---|
|  | Run/resume simulation button. Starts/resumes simulation of the active circuit. Refer to the <i>Start/Stop/Pause Simulation</i> section of Chapter 8, <i>Simulation</i> , for more information. |
|  | Pause simulation button. Pauses simulation. Refer to the <i>Start/Stop/Pause Simulation</i> section of Chapter 8, <i>Simulation</i> , for more information. |
|  | Stop simulation button. Stops the simulation. Refer to the <i>Start/Stop/Pause Simulation</i> section of Chapter 8, <i>Simulation</i> , for more information. |
|  | Pause at Next MCU Instruction Boundary button. Refer to the <i>Stepping and Breaking</i> section for more information. |

Experiment 1.1

Bridge Wave Rectifier with Filter

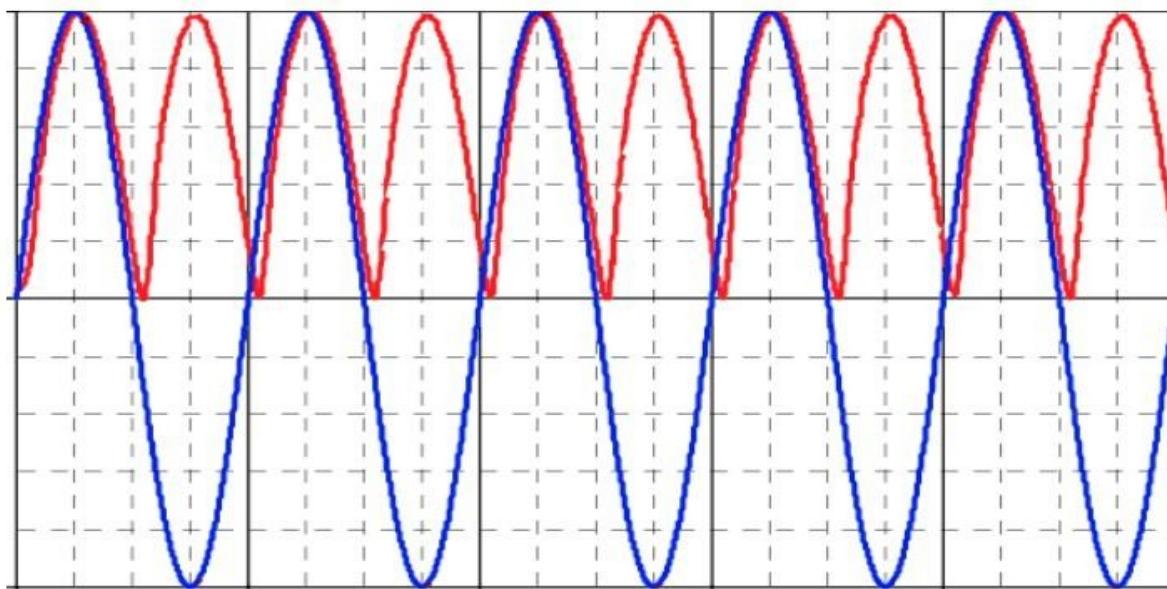
Aim: Test and verify the bridge wave rectifier using multisim software

Circuit diagram:

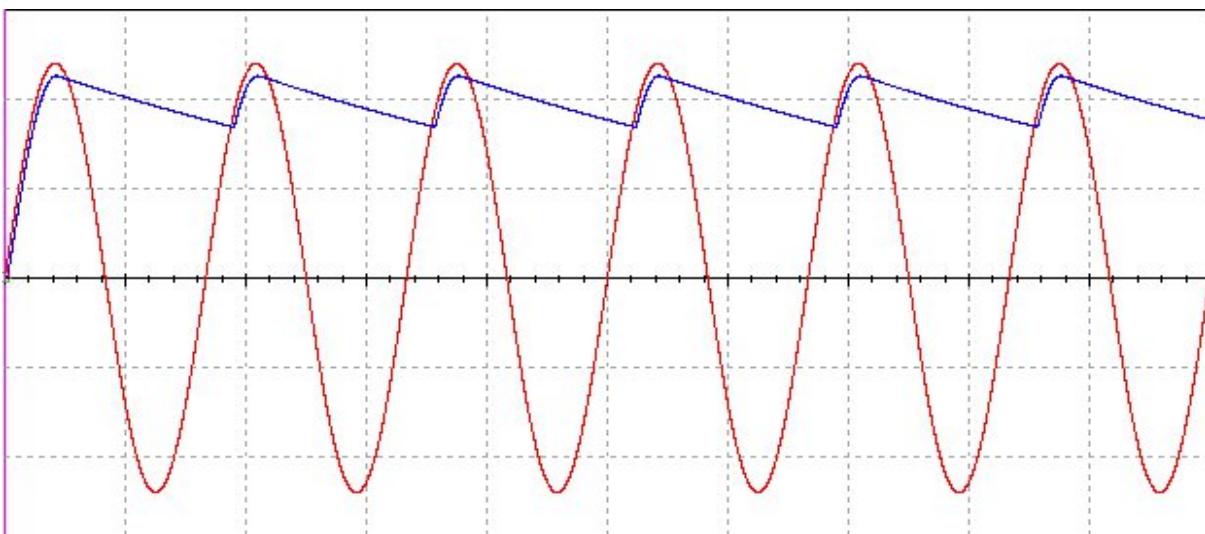


Waveforms:

Bridge wave Rectifier without Filter



Bridge wave Rectifier with Filter



Theory:

Bridge Rectifier is a type of Full Wave Rectifier that uses four diodes to form a close-loop bridge. The diodes conduct in pairs through each positive and negative half cycle, leading to no wastage of power.

Bridge Rectifier does not require a center tap over the secondary winding of the transformer. The input is fed through a transformer to the diagonal of the diode bridge. The transformer of this circuit is always busy because it supplies power all the time in both cycles of input AC, unlike the center tap rectifier that uses 50% of the transformer.

Bridge Rectifier comes in various types-

1. Single Phase and Three Phase Bridge Rectifier
2. Uncontrolled Bridge Rectifier
3. Controlled Bridge Rectifier

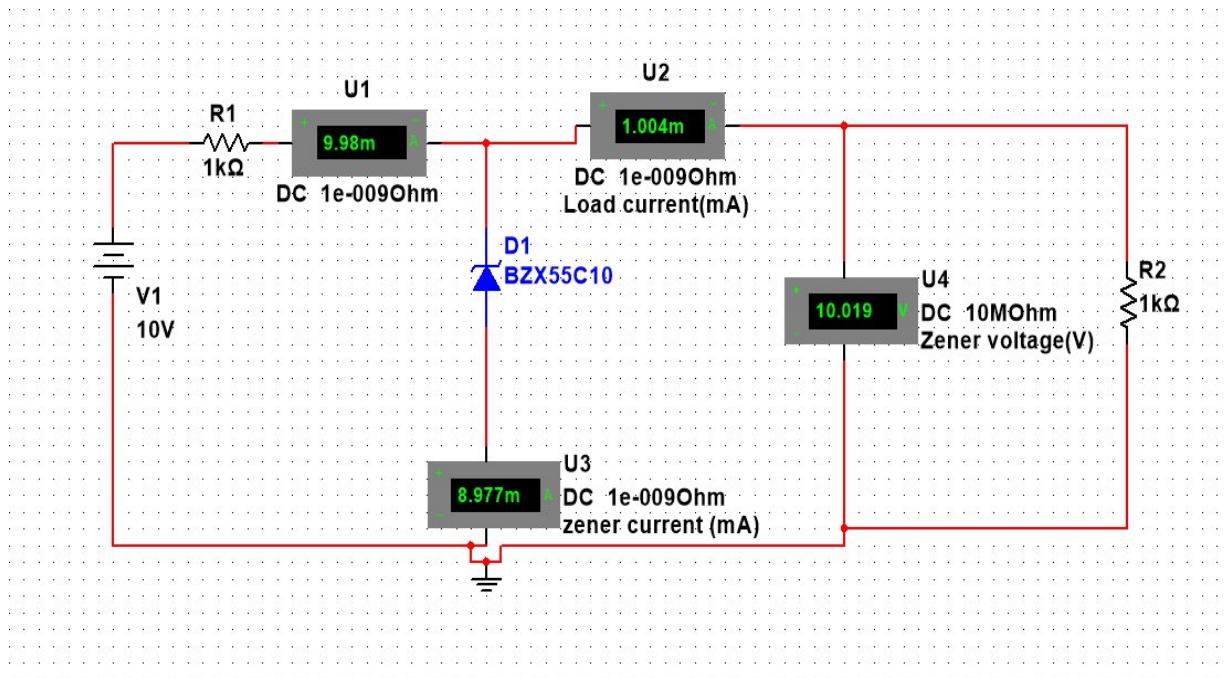
Procedure:

- 1) Make the connection as per circuit diagram
- 2) Observe the bridge wave rectifier output on simulation without connecting capacitor(filter)
- 3) Observe the bridge wave rectifier output on simulation with connecting capacitor(filter)

Experiment 1.2

Zener Voltage Regulator

Aim: Test and verify the zener voltage (line and load) regulator using multisim software

Circuit diagram:**Tabular Column:****Zener Diode as Line Regulator**

| Supply Voltage (V) | Zener Voltage (V) | Zener Current (mA) | Load Current (mA) |
|--------------------|-------------------|--------------------|-------------------|
| 0 | | | |
| 10 | | | |
| 20 | | | |
| 30 | | | |
| 40 | | | |
| 50 | | | |
| 60 | | | |
| 70 | | | |
| 80 | | | |
| 90 | | | |
| 100 | | | |

Zener Diode as Load Regulator

| Load Resistance | Zener Voltage (V) | Zener Current (mA) | Load Current (mA) |
|-----------------|-------------------|--------------------|-------------------|
| 100Ω | | | |
| 500Ω | | | |
| 1KΩ | | | |
| 2 KΩ | | | |
| 4 KΩ | | | |
| 6 KΩ | | | |
| 8 KΩ | | | |
| 10 KΩ | | | |

Theory:

Zener Diode as a Voltage Regulator helps to regulate voltage across small loads. A Zener diode is a semiconductor device with a p-n junction causing the current to flow in a forward or backward direction. The current conducted by the diode in the reverse mode is constant and the voltage drop is also constant. Hence Zener diode as a voltage regulator is extremely useful in circuits. There is a typical flow of current from anode to cathode in a Zener diode.

1. When loaded in the forward direction, Zener diode acts as a general-purpose diode with a silicon p-n junction.
2. However, if the voltage exceeds a certain limit – the Zener or the breakdown voltage, the forward current can be reverted.
3. Zener Diode acts as a voltage regulator when it is given reverse bias feedback.
4. A small leakage current is generated until a constant voltage is obtained

Procedure:**Zener Diode as Line Regulator**

- 1) Make the connection as per circuit diagram
- 2) By varying the supply voltage note down the Zener current, Zener voltage and load current

Zener Diode as Load Regulator

- 1) Make the connection as per circuit diagram
- 2) By varying the load resistance note down the Zener current, Zener voltage and load current

Observation:

- 1) Zener Diode as Line Regulator ☺ By varying the input supply voltage Zener diode maintains the load current remains same
- 2) Zener Diode as Load Regulator ☺ By varying the load resistor Zener diode maintains the Zener voltage remains same and by decreeing the load current as resistance increases

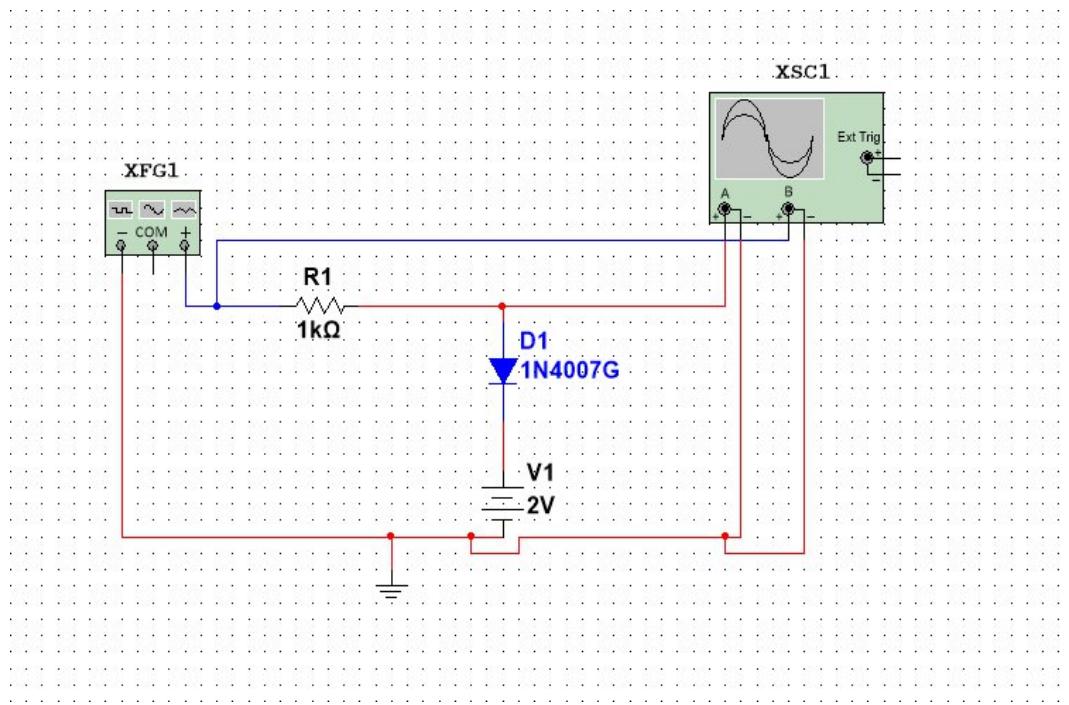
Experiment 2.1

Positive, Negative & Double ended Clipper

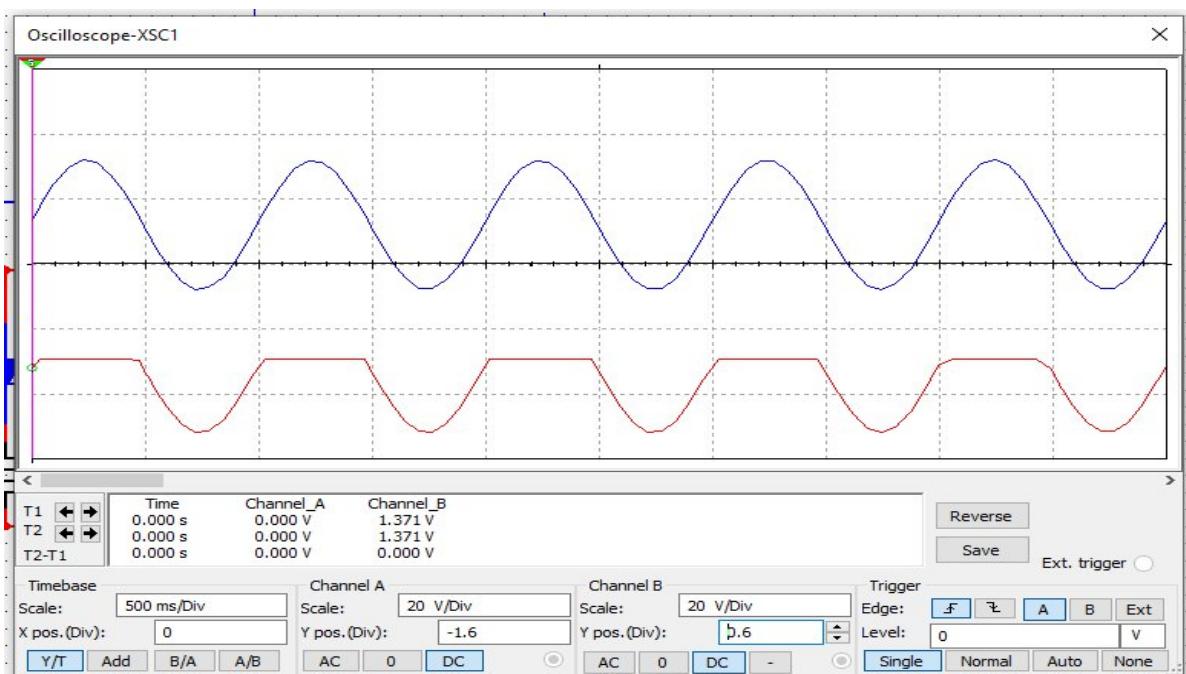
Aim: Observe the positive,negative and double ended clipper with biased waveforms using multisim software

Circuit diagram:

Positive Clipper



Wave form:



Theory:**Positive Clipper**

A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper**

Positive Cycle of the Input – When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B. This makes the diode forward biased and hence it conducts like a closed switch. Thus the voltage across the load resistor becomes zero as no current flows through it and hence V_0 will be zero.

Negative Cycle of the Input – The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode reverse biased and hence it behaves like an open switch. Thus the voltage across the load resistor will be equal to the applied input voltage as it completely appears at the output V_0 .

Positive Shunt Clipper with positive V_r

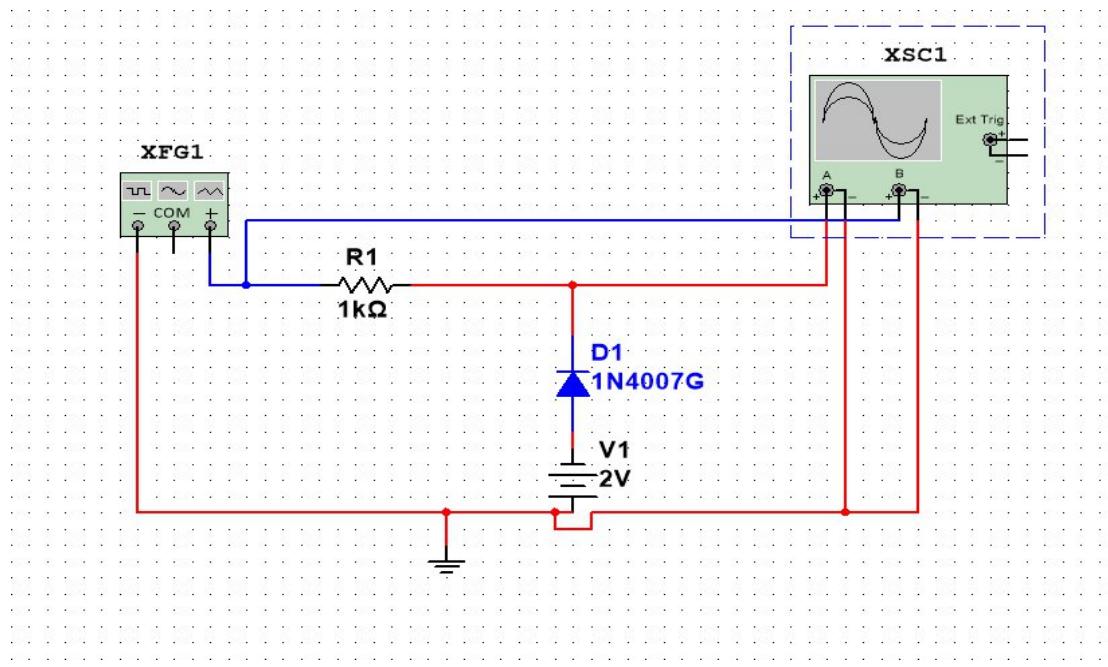
A Clipper circuit in which the diode is connected in shunt to the input signal and biased with positive reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper with positive V_r**

During the positive cycle of the input the diode gets forward biased and nothing but the reference voltage appears at the output. During its negative cycle, the diode gets reverse biased and behaves as an open switch. The whole of the input appears at the output. Hence the output waveform appears as shown in the above figure

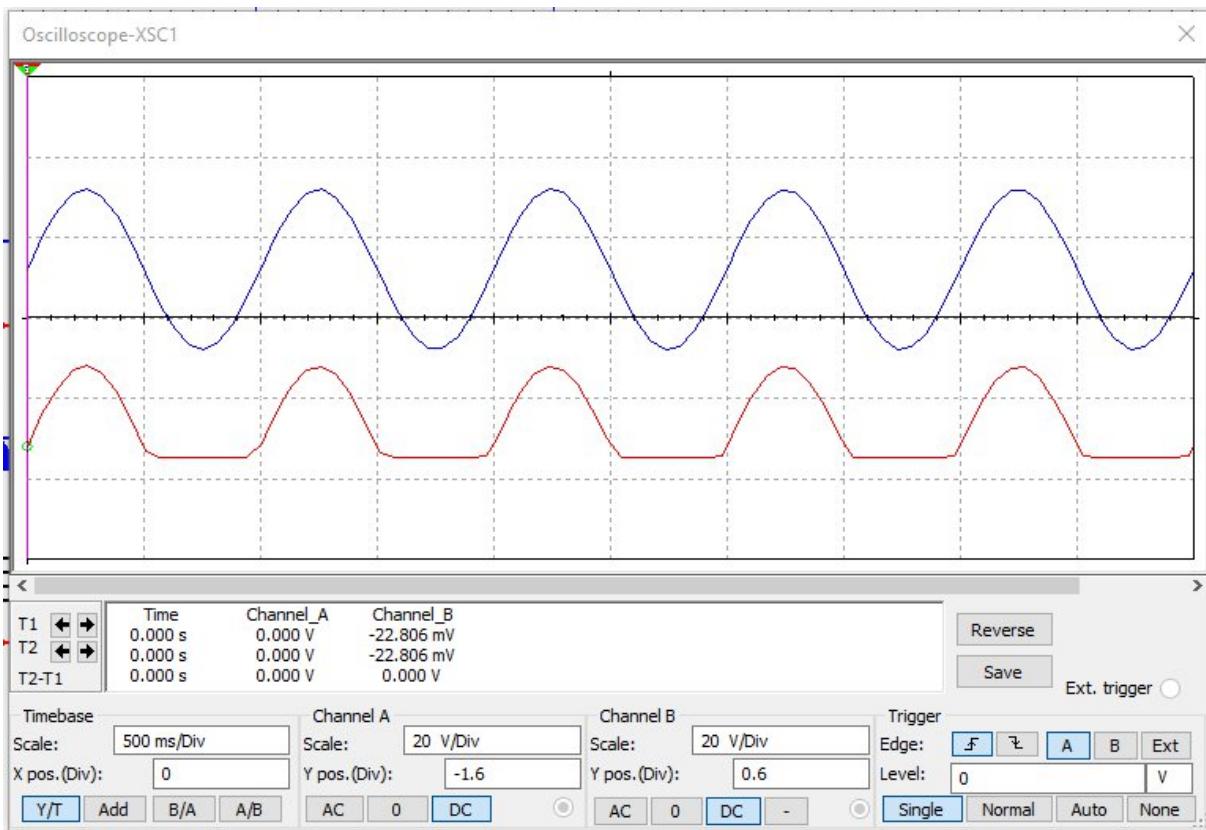
Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and out waveform

Negative Clipper



Wave form:



Theory:**Negative Clipper:**

A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the negative portions of the waveform, is termed as Negative Shunt Clipper

Positive Cycle of the Input – When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B. This makes the diode reverse biased and hence it behaves like an open switch. Thus the voltage across the load resistor equals the applied input voltage as it completely appears at the output V_0

Negative Cycle of the Input – The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode forward biased and hence it conducts like a closed switch. Thus the voltage across the load resistor becomes zero as no current flows through it.

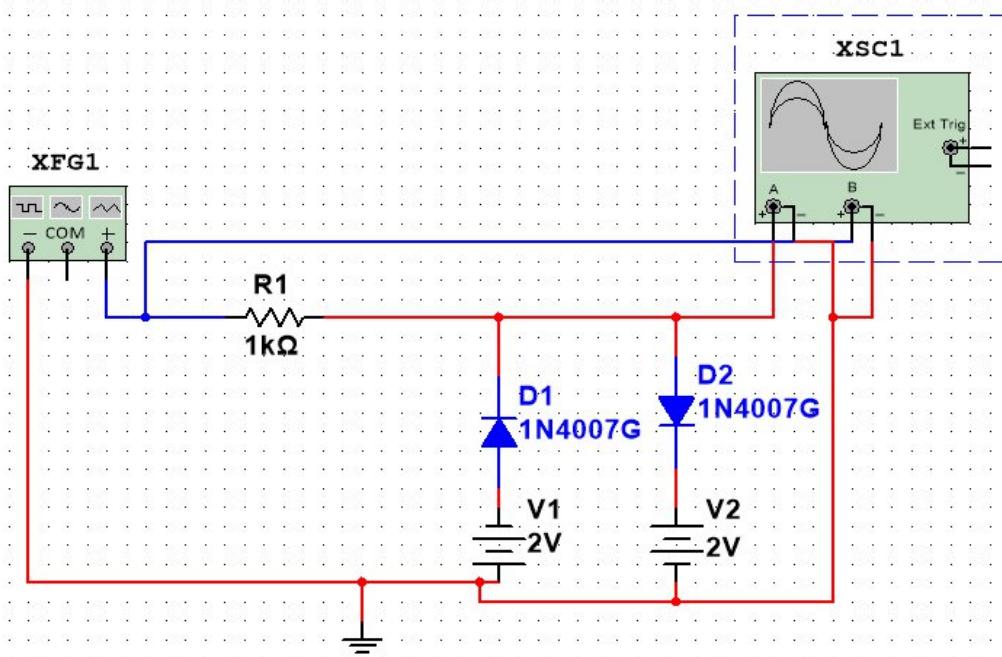
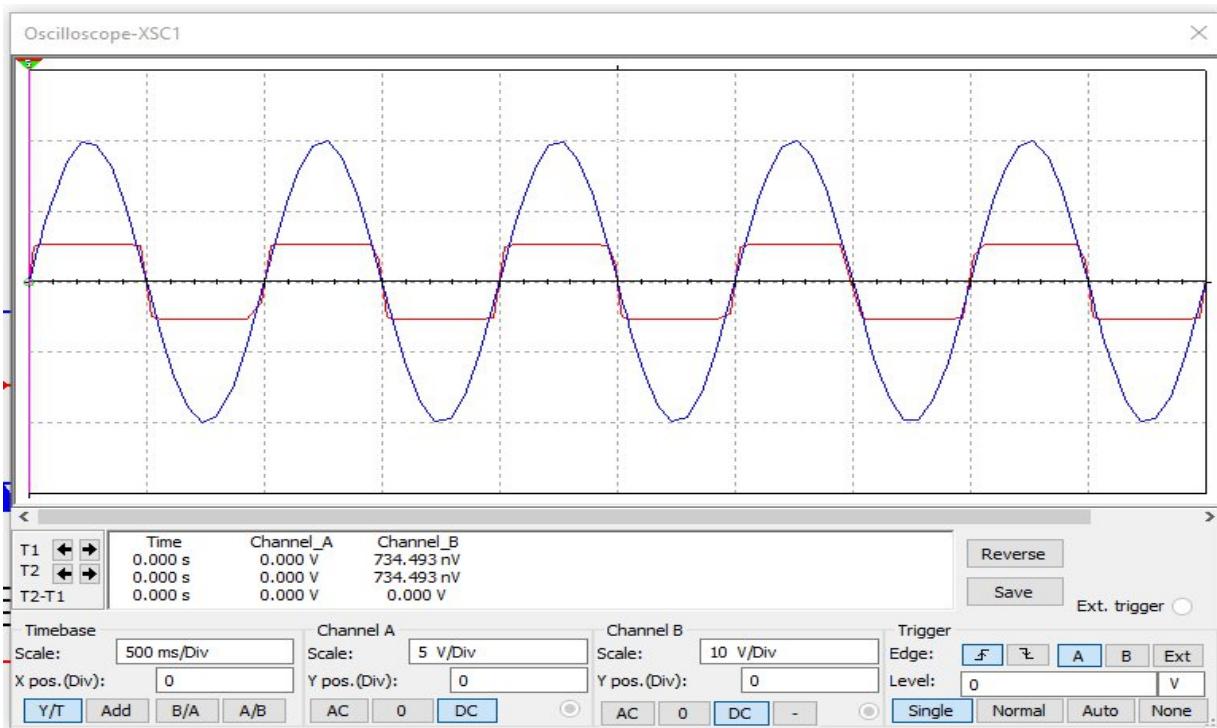
Negative Shunt Clipper with Negative V_r

A Clipper circuit in which the diode is connected in shunt to the input signal and biased with negative reference voltage V_r and that attenuates the negative portions of the waveform, is termed as **Negative Shunt Clipper with negative V_r**

During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, appears at the output V_0 . During the negative half cycle, the diode gets forward biased. The negative voltage up to the reference voltage, gets at the output and the remaining signal gets clipped off

Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and out waveform

Double Ended Clipper**Wave form:**

Theory:**Double Ended Clipper:**

This is a positive and negative clipper with a reference voltage V_r . The input voltage is clipped two-way both positive and negative portions of the input waveform with two reference voltages. For this, two diodes D1 and D2 along with two reference voltages V_{r1} and V_{r2} are connected in the circuit.

During the positive half of the input signal, the diode D1 conducts making the reference voltage V_{r1} appear at the output. During the negative half of the input signal, the diode D2 conducts making the reference voltage V_{r2} appear at the output. Hence both the diodes conduct alternatively to clip the output during both the cycles. The output is taken across the load resistor

Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and output waveform

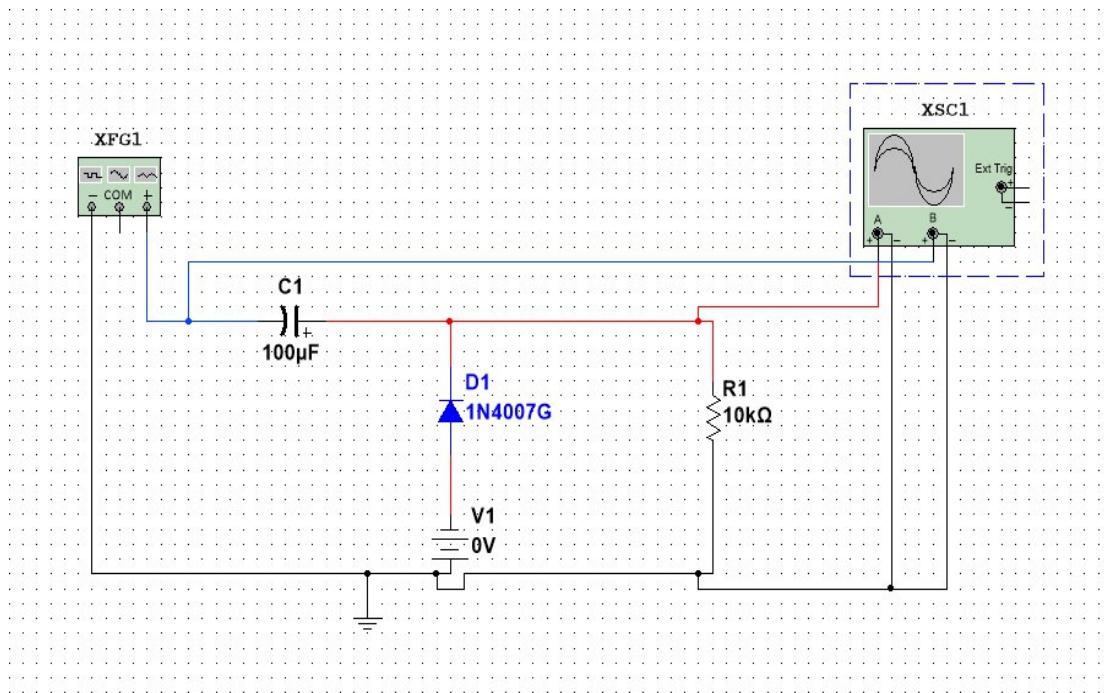
Experiment 2.2

Positive, Negative Clampers

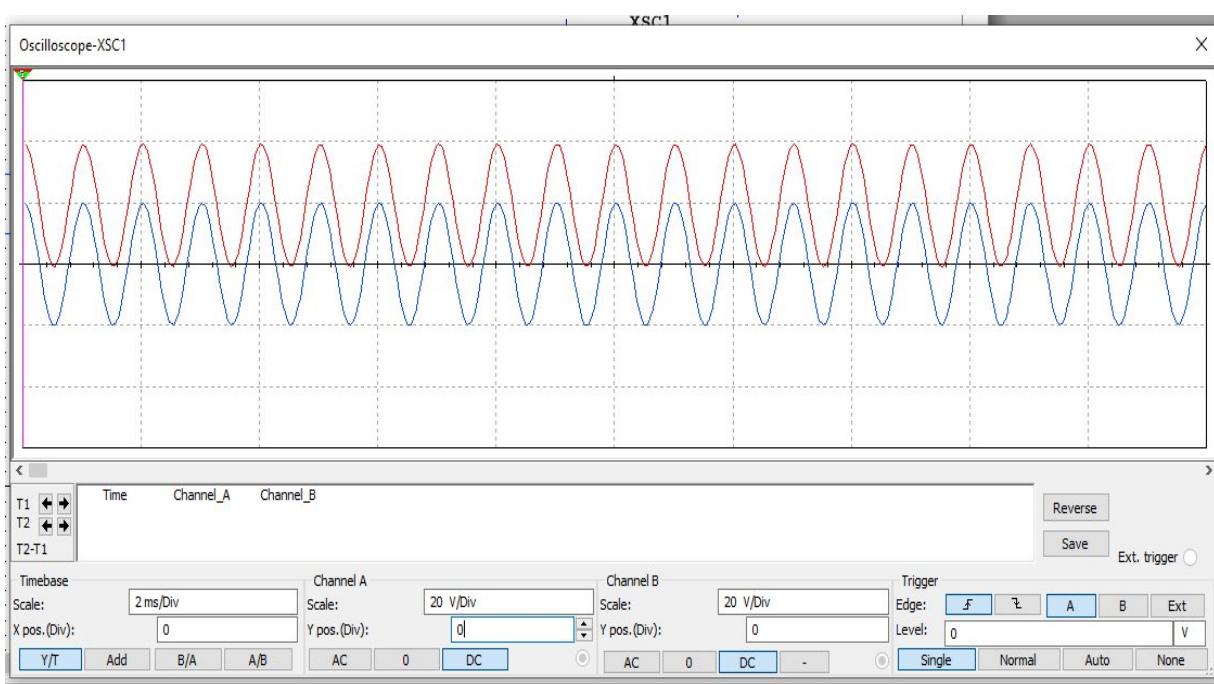
Aim: Observe the positive and negative clampers with and without referenced waveforms using multisim software

Circuit diagram:

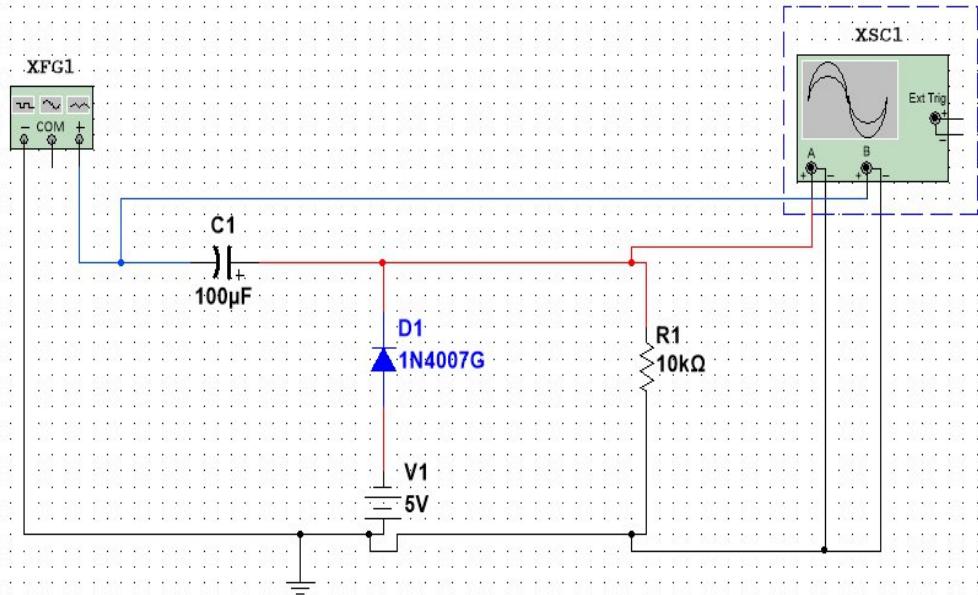
Positive Clamp without reference



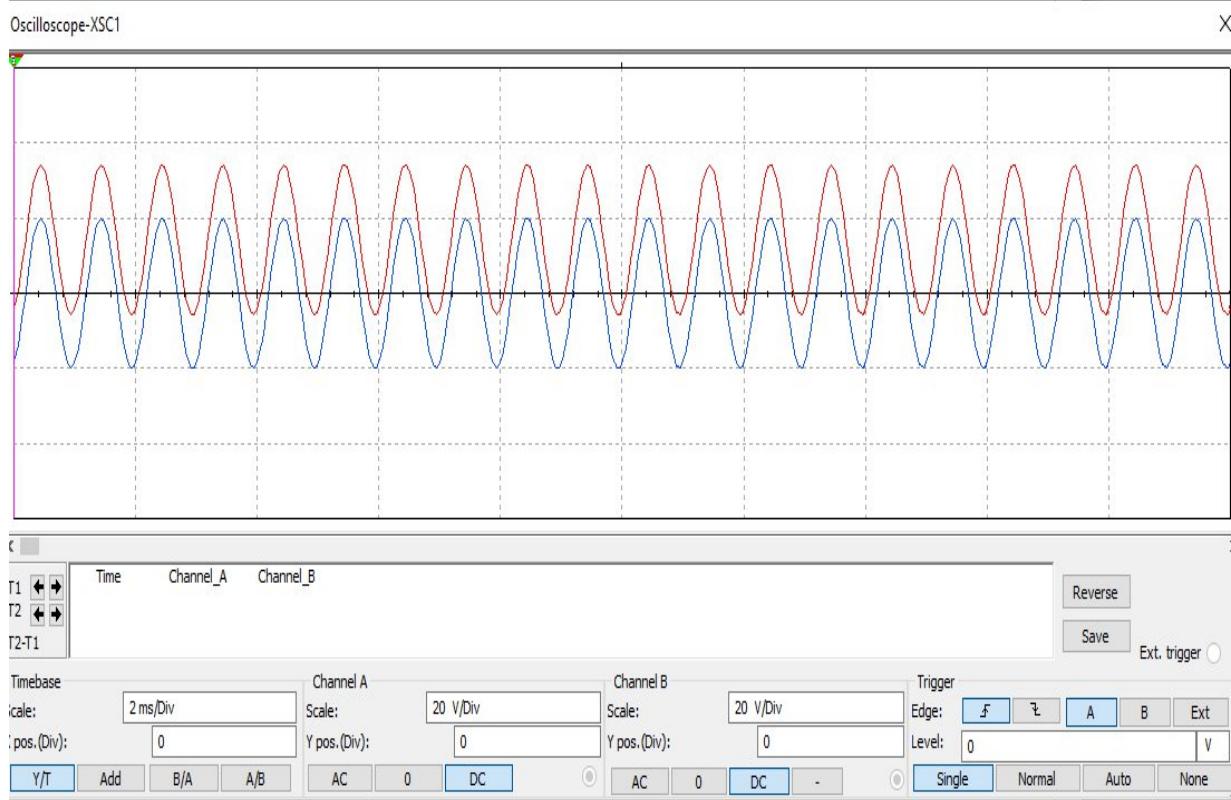
Wave form:



Positive Clamp with reference



Wave form:



Theory:**Positive Clamper**

A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal

Positive Clamper Circuit

A Clamping circuit restores the DC level. When a negative peak of the signal is raised above to the zero level, then the signal is said to be **positively clamped**. A Positive Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the positive portion of the input signal

Initially when the input is given, the capacitor is not yet charged and the diode is reverse biased the output is not considered at this point of time. During the negative half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on the other. The capacitor is now charged to its peak value V_m . The diode is forward biased and conducts heavily.

During the next positive half cycle, the capacitor is charged to positive V_m while the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be $V_o = V_i + V_m$

Hence the signal is positively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Positive Clamper with Negative V_r

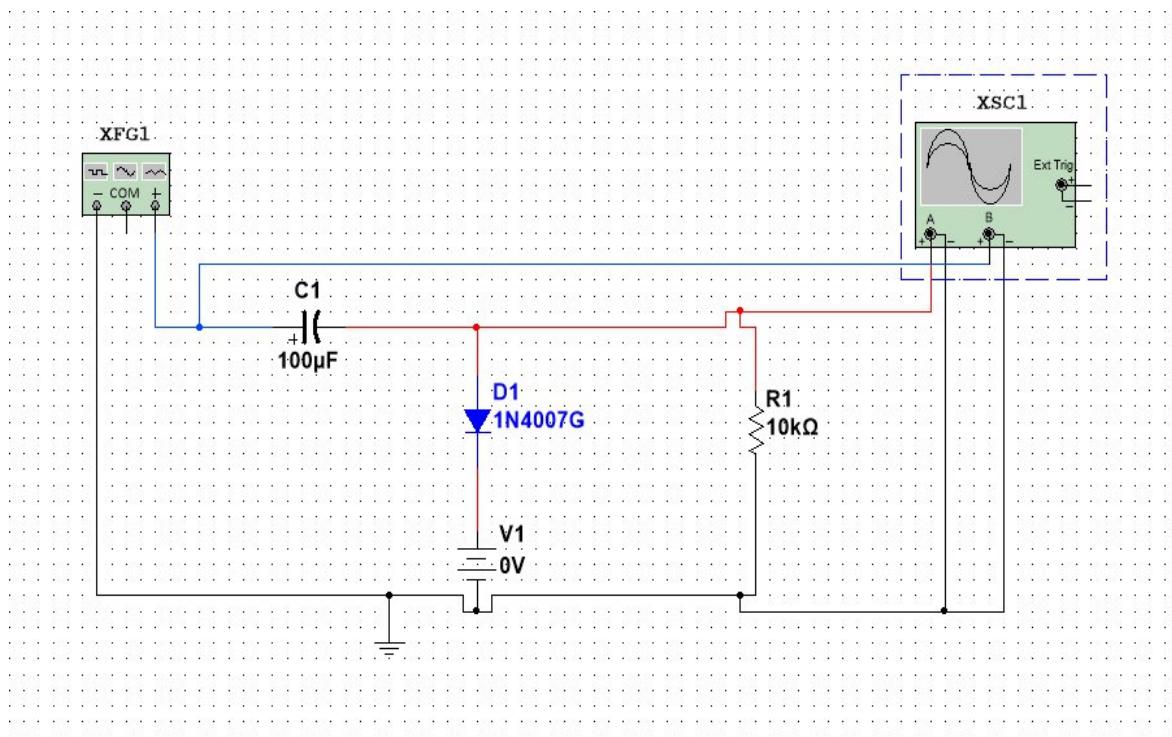
A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level.

During the positive half cycle, the voltage across the capacitor and the reference voltage together maintain the output voltage level. During the negative half-cycle, the diode conducts when the cathode voltage gets less than the anode voltage.

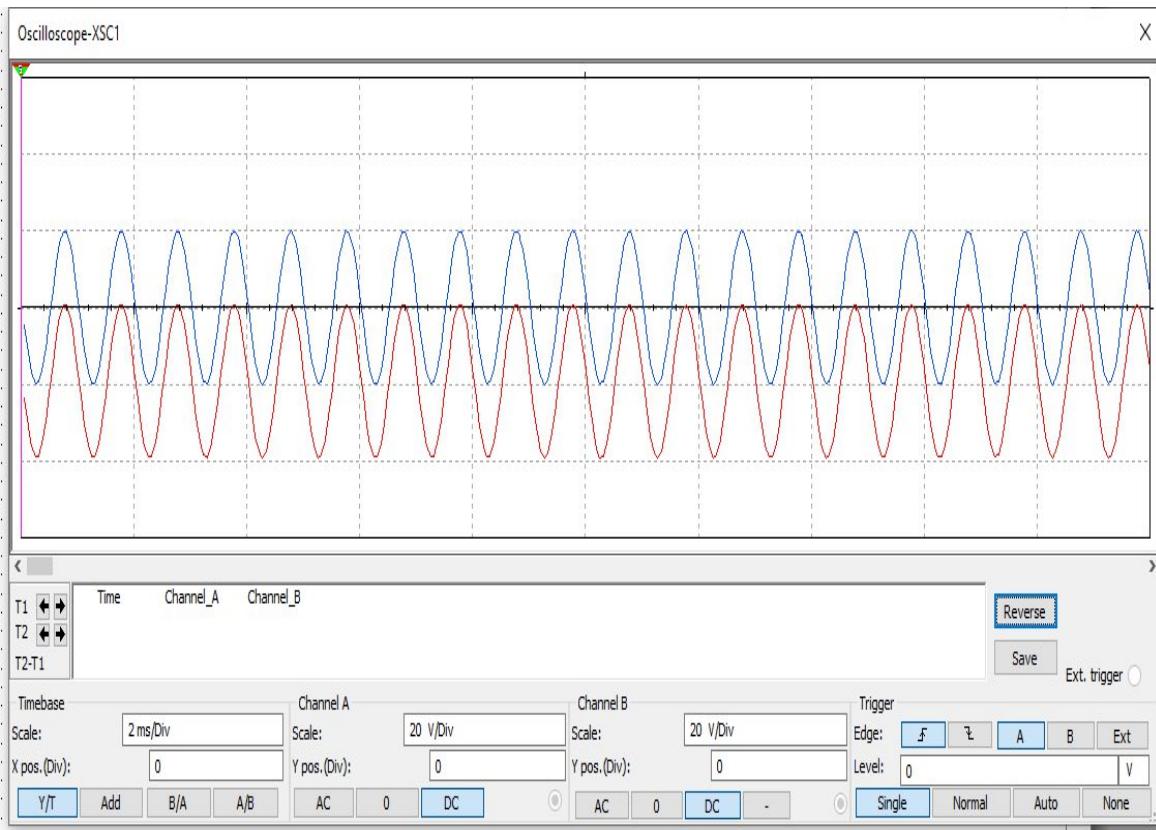
Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and out waveform

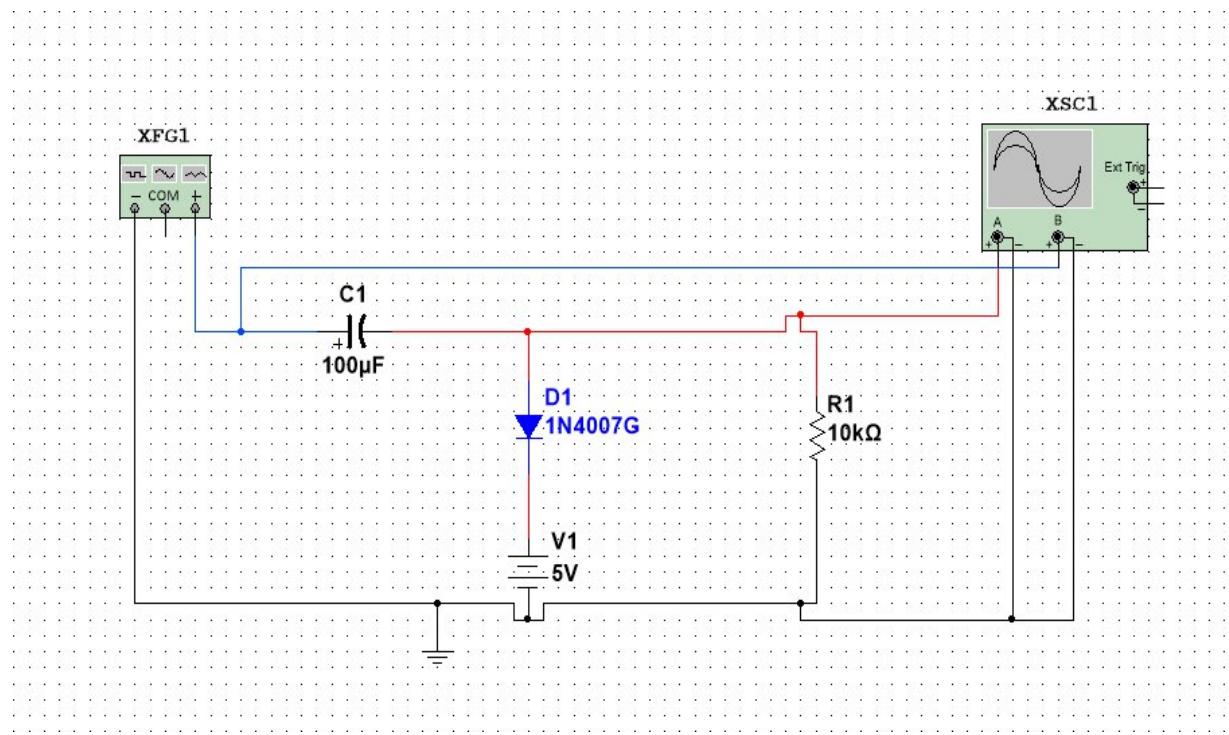
Negative Clamper without reference



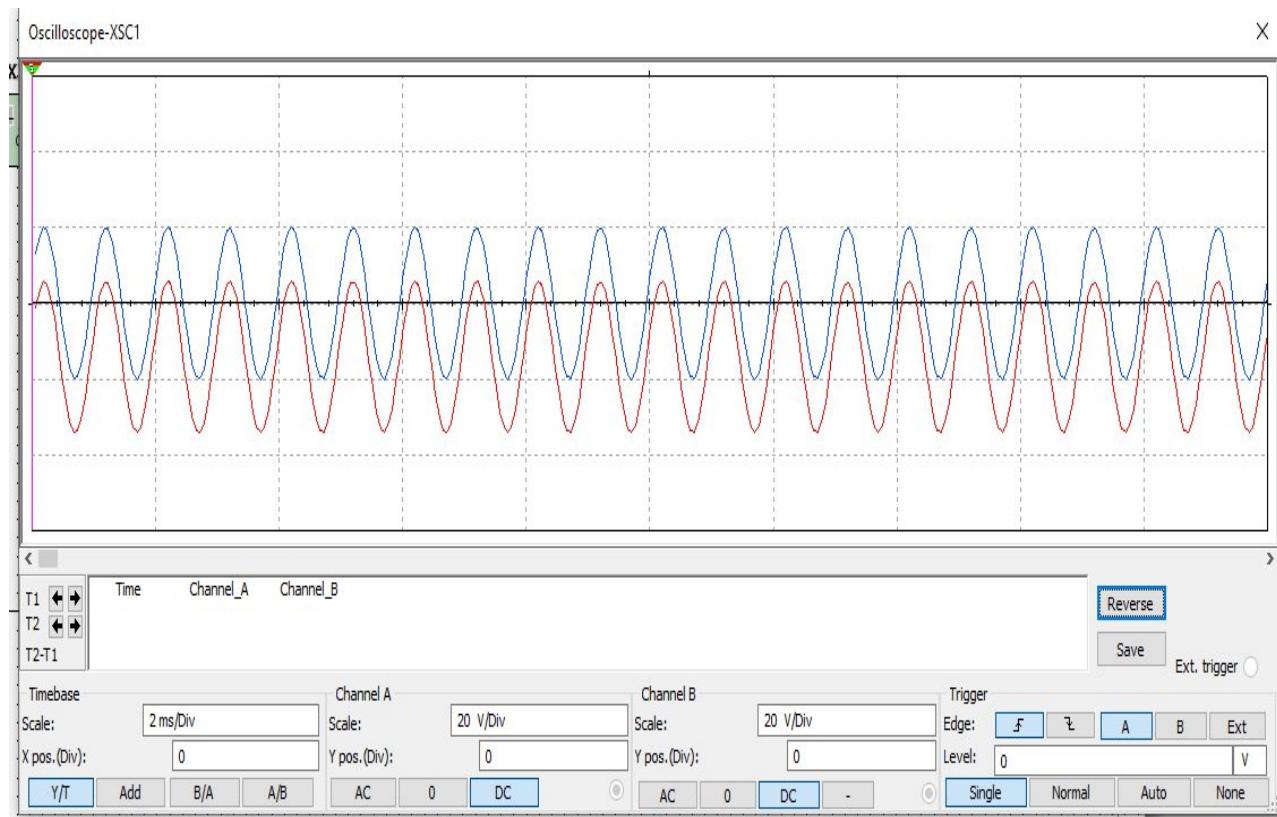
Wave form:



Negative Clamper with reference



Wave form:



Theory:**Negative Clamper**

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. During the positive half cycle, the capacitor gets charged to its peak value v_m . The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be $V_0 = V_i + V_m$.

Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Negative clamper with positive V_r

A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level.

Though the output voltage is negatively clamped, a portion of the output waveform is raised to the positive level, as the applied reference voltage is positive. During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied. During the negative half cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.

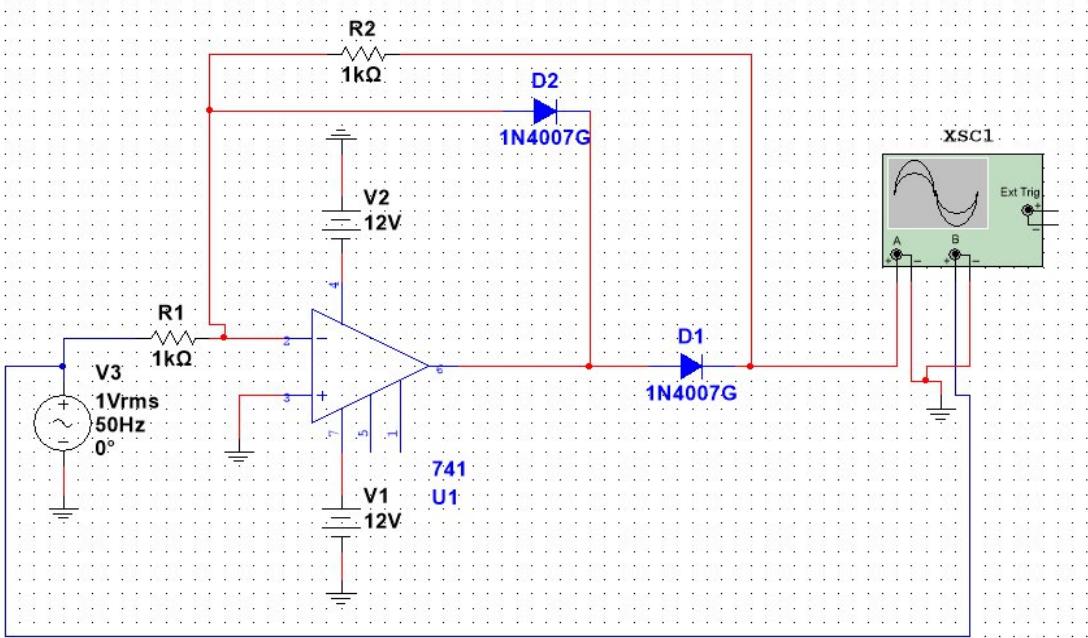
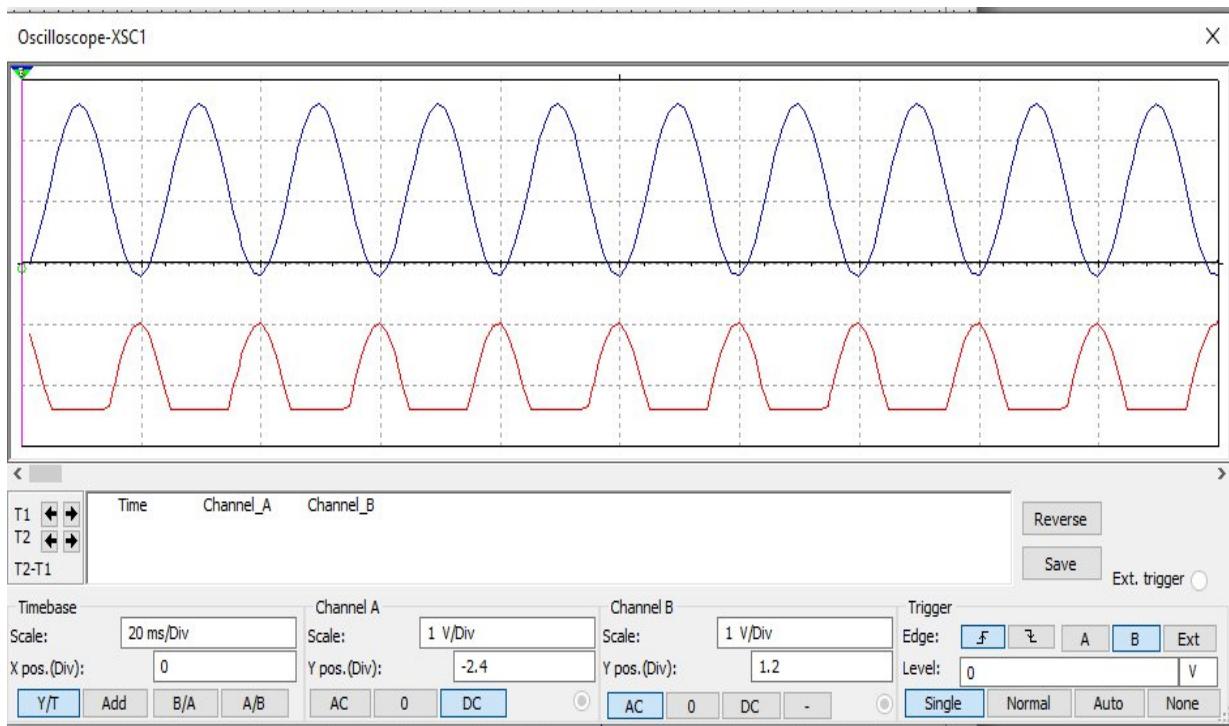
Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and output waveform

Experiment 3.1

Precision Half Wave Rectifier using Opamp

Aim: Design and observe the input and output waveform of precision Half Wave Rectifier using Op-amp in multisim software

Circuit diagram:**Wave form:**

Theory:

The precision rectifier is another rectifier that converts AC to DC, but in a precision rectifier we use an op-amp to compensate for the voltage drop across the diode, that is why we are not losing the 0.6V or 0.7V voltage drop across the diode, also the circuit can be constructed to have some gain at the output of the amplifier as well.

A half-wave rectifier converts an AC signal to DC by passing either the negative or positive half-cycle of the waveform and blocking the other. Half-wave rectifiers can be easily constructed using only one diode, but are less efficient than full-wave rectifiers.

Procedure:

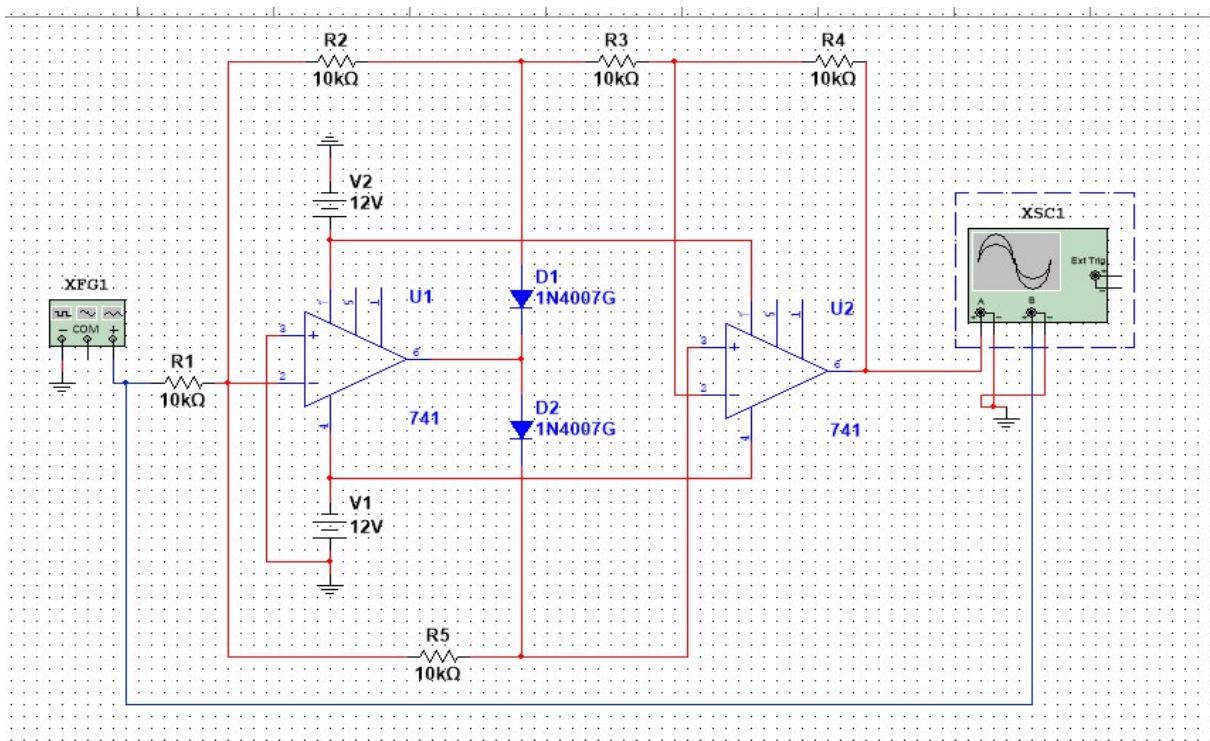
- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and out waveform

Experiment 3.2

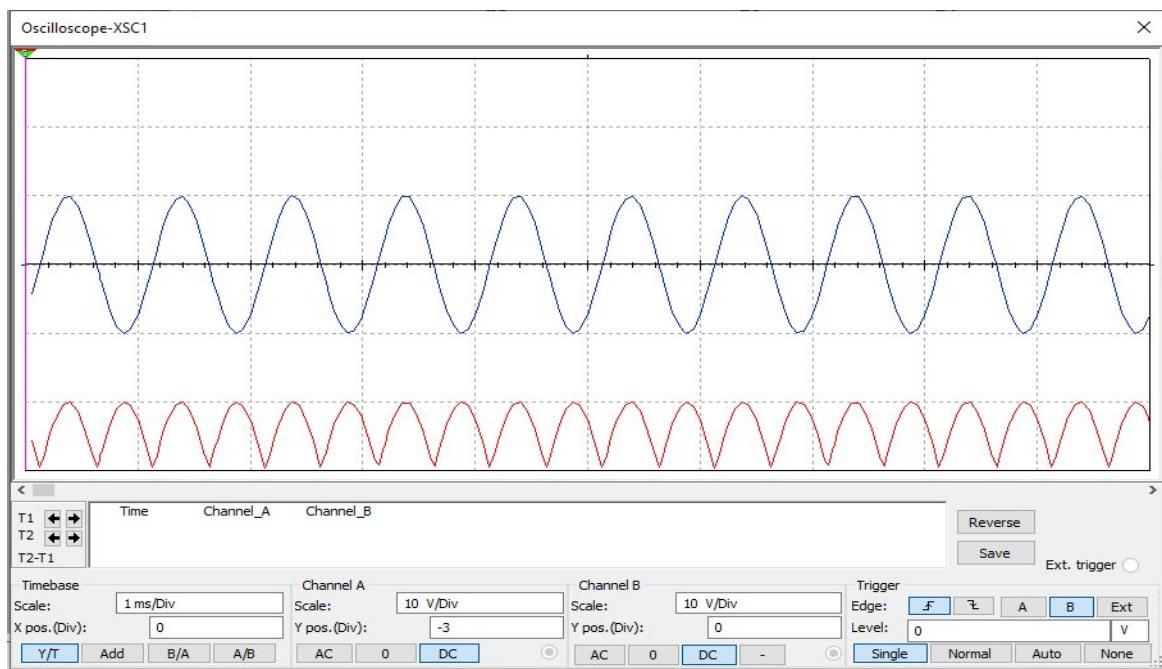
Precision Full Wave Rectifier using Opamp

Aim: Design and observe the input and output waveform of precision Full Wave Rectifier using Op-amp in multisim software

Circuit diagram:



Wave form:



Theory:

A Precision Full-Wave Rectifier is a circuit that uses operational amplifiers (op-amps) to rectify an AC signal and provide both the positive and negative halves of the input waveform as separate outputs. This type of circuit can be useful in applications where you need to extract both the positive and negative cycles of an AC signal with high accuracy. Here's how to create a Precision Full-Wave Rectifier using op-amps

The two op-amp outputs from op-amp 1 and op-amp 2 can be combined to obtain the full-wave rectified output.

- The output of op-amp 1 is the positive half of the AC signal.
- The output of op-amp 2 is the negative half of the AC signal (inverted).

To obtain the full-wave rectified output, you can sum these two signals. You can use a summing amplifier configuration or simply connect the outputs of op-amp 1 and op-amp 2 together (keeping their polarities in mind). The Precision Full-Wave Rectifier ensures that both the positive and negative cycles of the AC input are rectified accurately. The diodes play a critical role in allowing only one op-amp to be active at a time, depending on the polarity of the input signal, to achieve full-wave rectification.

Procedure:

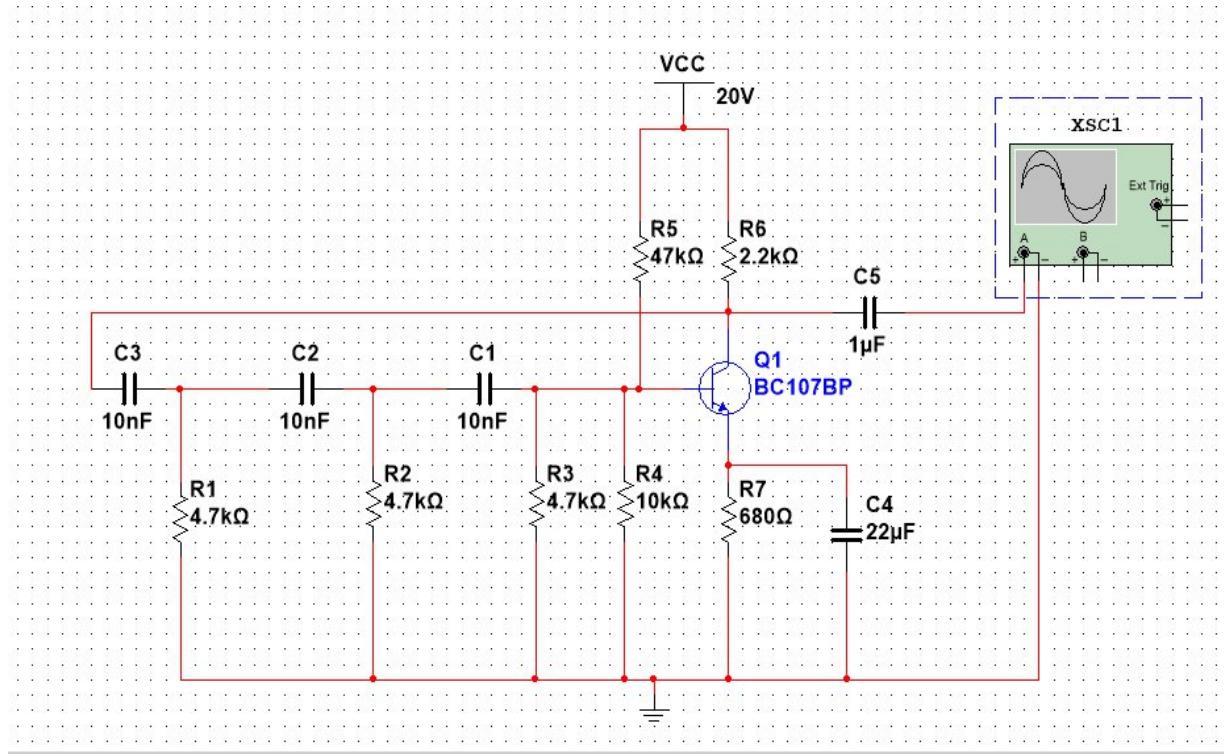
- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the input and out waveform

Experiment 4

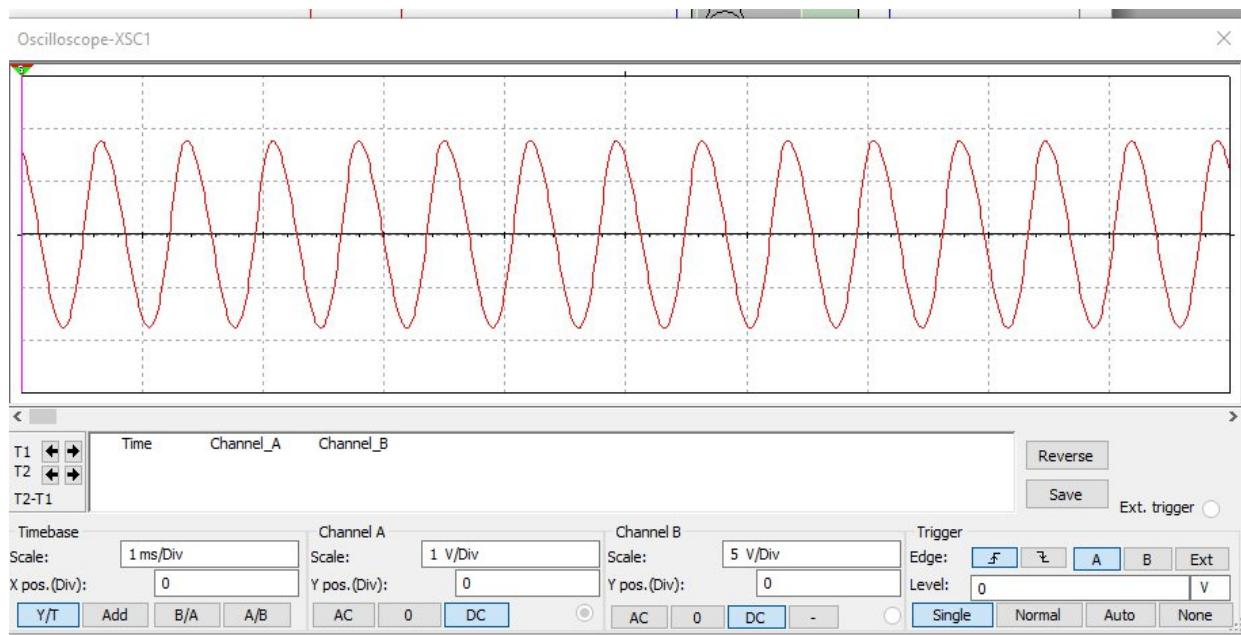
R-C Phase Shift Oscillator

Aim: Design and observe the output waveform of RC phase shift oscillator using multisim software

Circuit diagram:



Wave form:



Theory:

A Phase-Shift Oscillator using Bipolar Junction Transistors (BJTs) is another type of oscillator circuit that generates a sinusoidal waveform without an external input signal. Unlike the op-amp-based RC Phase-Shift Oscillator, this version uses transistors for amplification and phase shift

- 1) The heart of this BJT-based oscillator is the RC network (R1-C1, R2-C2, R3-C3), which provides the phase shift.
- 2) Each RC section introduces a phase shift of approximately 60 degrees at the desired oscillation frequency. In total, the three RC sections provide 180 degrees of phase shift, which is necessary for oscillation.
- 3) The RC network and the transistor stages collectively provide a total phase shift of 360 degrees (or 0 degrees, as oscillations are in phase). This is necessary for sustained oscillation.
- 4) The frequency of oscillation is determined by the values of the resistors and capacitors in the RC network and can be calculated using the formula:

$$f = 1 / (2 * \pi * R * C)$$

Where f is the oscillation frequency, R is the resistance in one RC section, and C is the capacitance in one RC section.

- 5) The amplitude of the oscillations depends on the gain of the transistor amplifiers, which can be adjusted using appropriate resistor values and biasing.
- 6) The oscillations will continue as long as the loop gain (product of the transistor gains and the RC network's phase shift) is greater than or equal to 1. The amplitude of the oscillations will stabilize to a constant value determined by the circuit components.

Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the out waveform

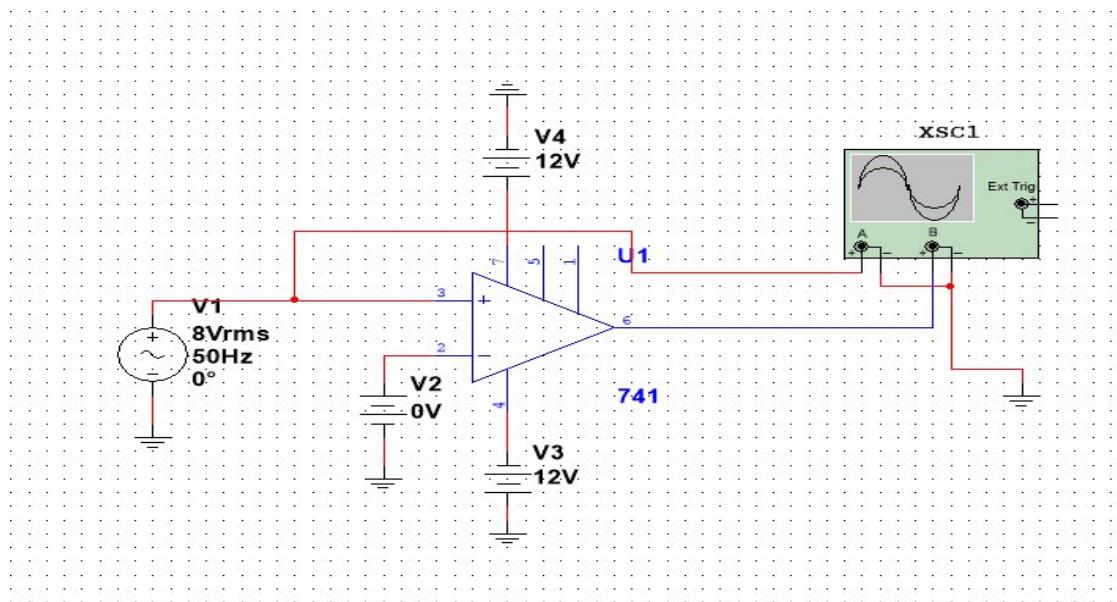
Experiment 5

Op-Amp as Comparator

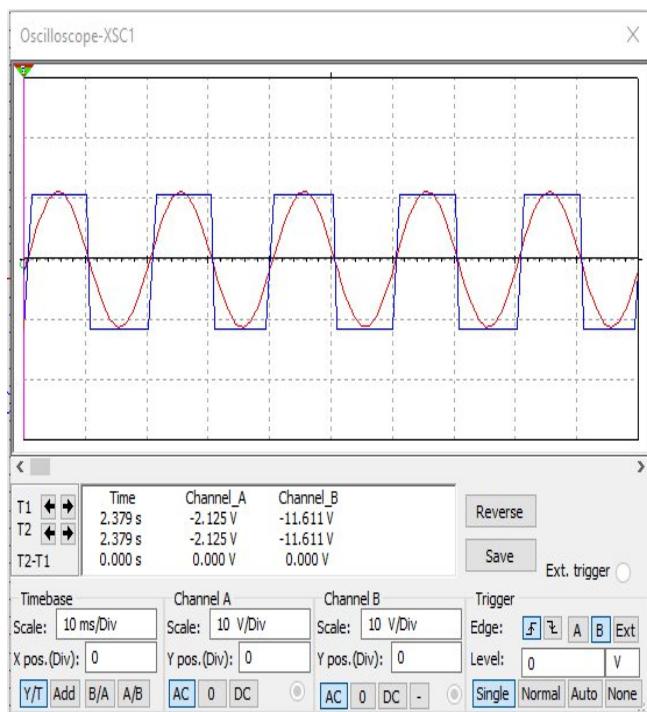
Aim: Design Op-amp as comparator with and without reference and obtain hysteresis curve using multisim software

Circuit diagram:

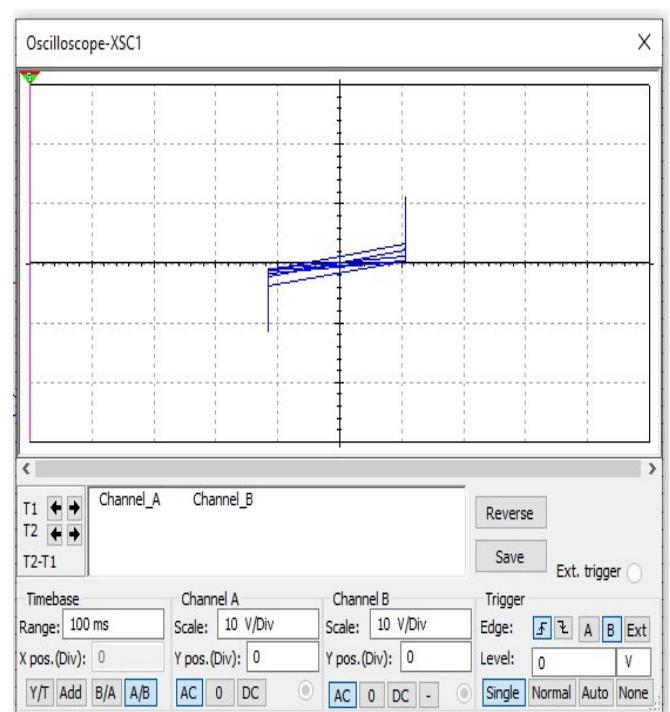
Op-amp as comparator (zero reference)

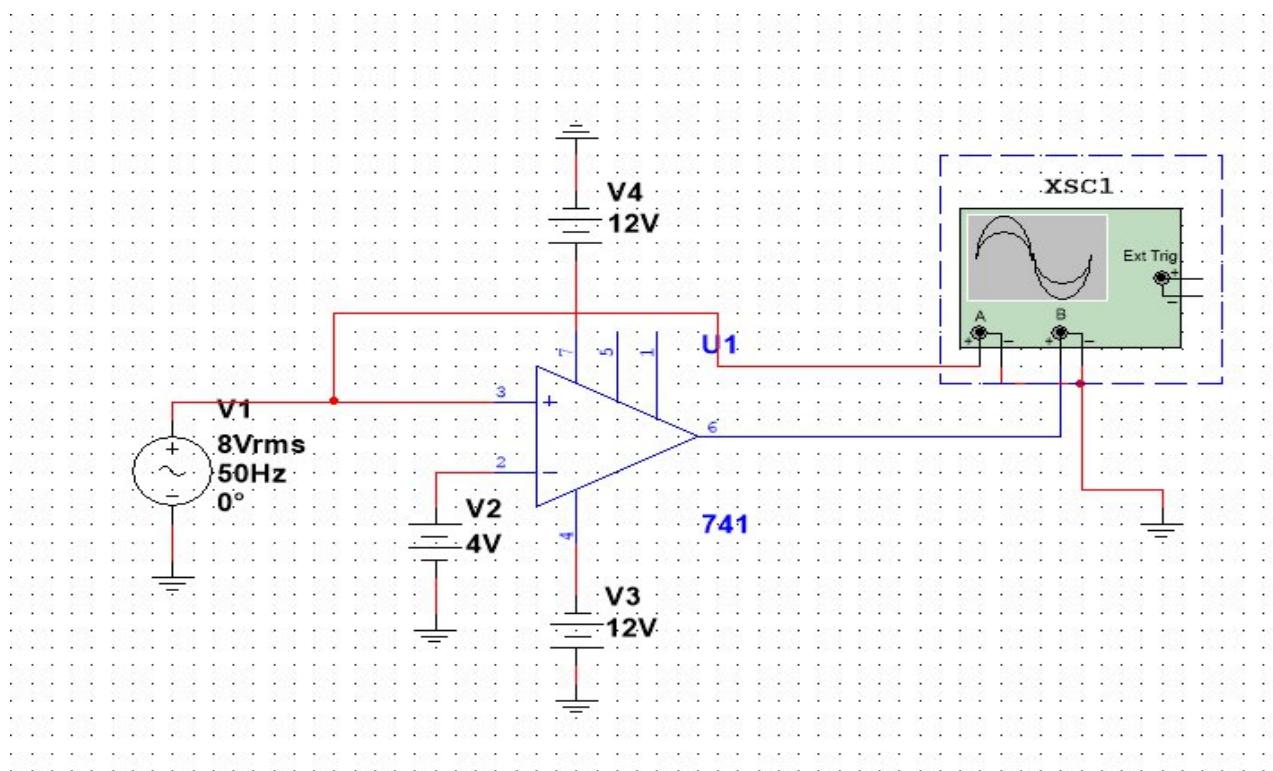
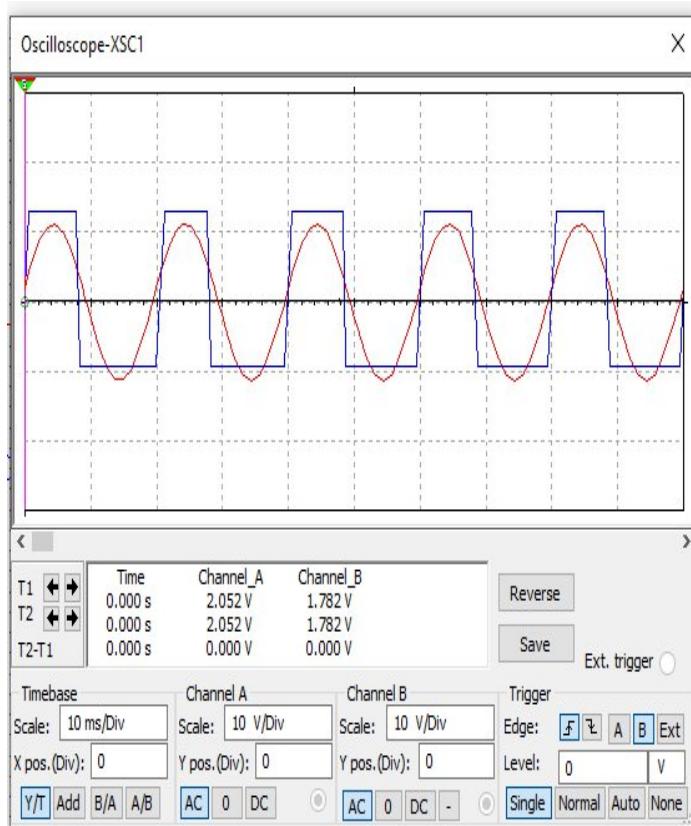
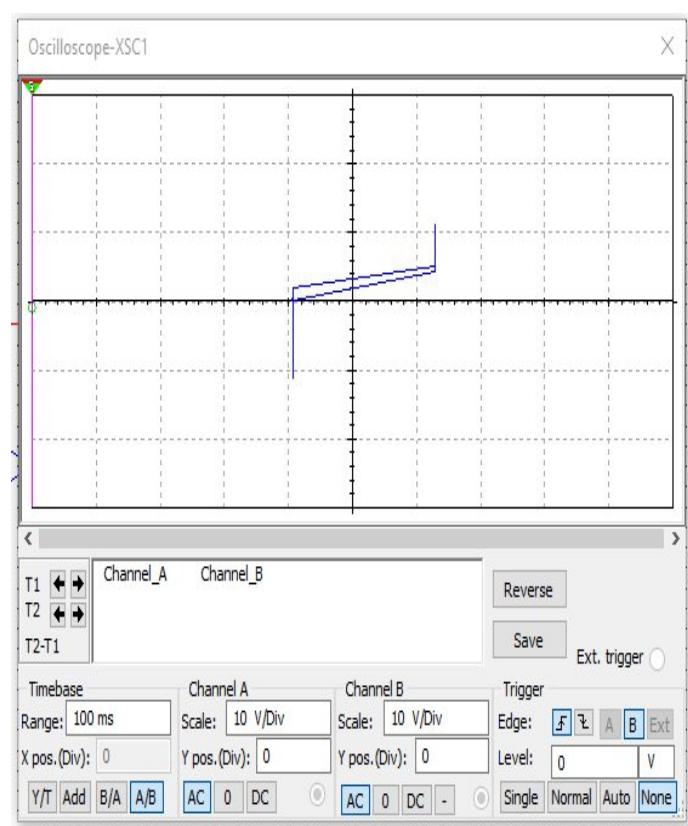


Wave form:



Hysteresis Curve:



Op-amp as comparator (with reference voltage)**Wave form:****Hysteresis Curve:**

Theory:

Generally, in electronics, the comparator is used to compare two voltages or currents which are given at the two inputs of the comparator. That means it takes two input voltages, then compares them and gives a differential output voltage either high or low-level signal. The comparator is used to sense when an arbitrary varying input signal reaches the reference level or a defined threshold level.

The device consists of two input terminals, in which the reference input signal is fed to one terminal and the actual value of the signal is fed to another terminal. Then, an output signal is generated at the output terminal based on the difference between the two input signals fed to the two input terminals. This generated output signal is either 0 (low) or 1 (high)

While using an op-amp as a comparator in instrumentation, the open-loop can be used to compare the two voltages. Therefore, depending on the difference between the input voltage value and the reference voltage value, the output V_{out} will be equal to the maximum high value or minimum low value (input voltage value will be greater than or less than the reference voltage value few by microvolts)

Procedure:

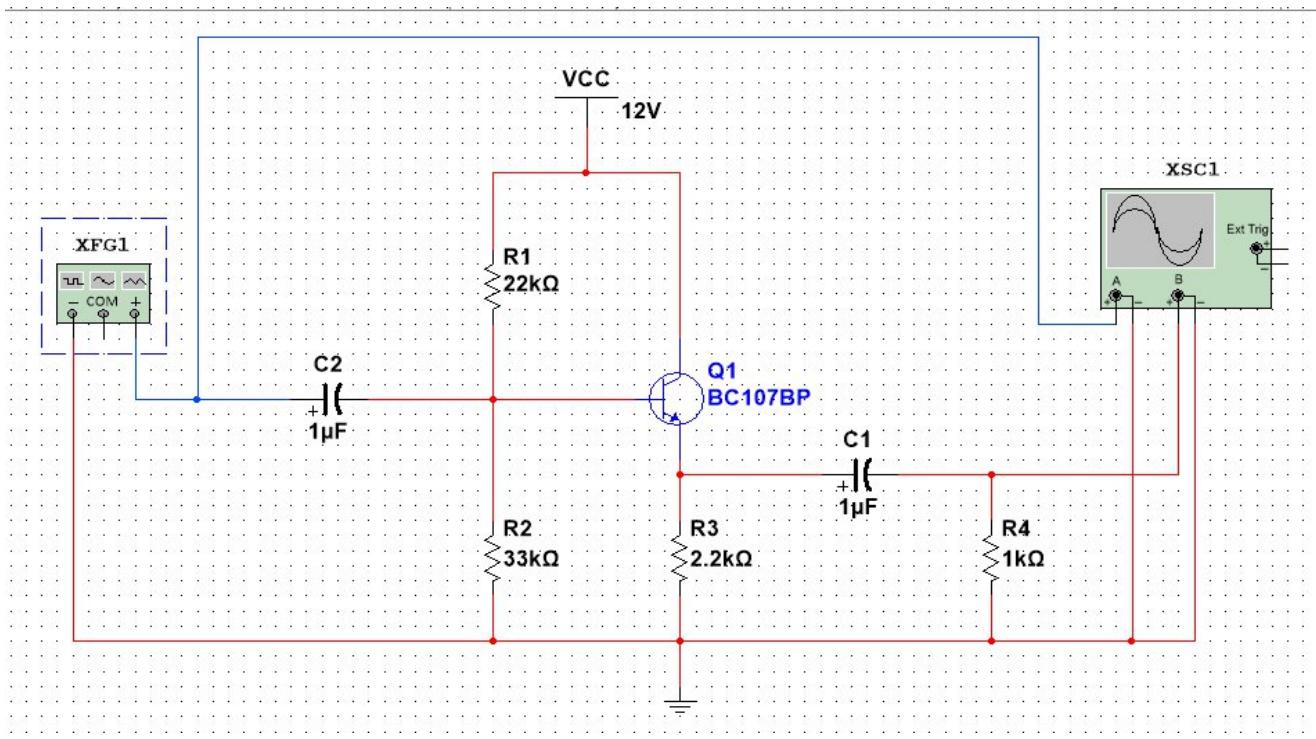
- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the out waveform
- 3) If the input waveform is sinusoidal than output will be square waveform
- 4) Also obtain the hysteresis curve by pressing A/B button in simulation

Experiment 6

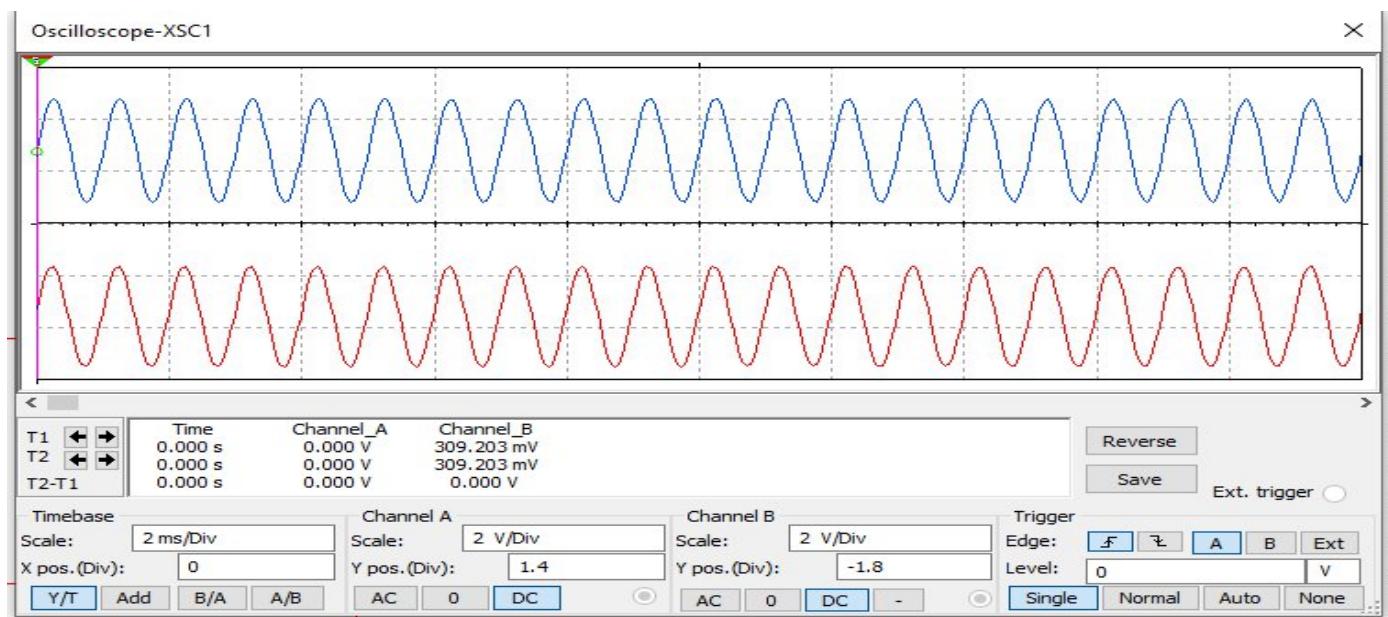
Emitter Follower

Aim: Test the Emitter Follower Amplifier circuit using multisim software

Circuit diagram:



Wave form:



Theory:

Emitter follower circuit has a prominent place in feedback amplifiers. Emitter follower is a case of negative current feedback circuit. This is mostly used as a last stage amplifier in signal generator circuits. The important features of Emitter Follower are

- 1) It has high input impedance
- 2) It has low output impedance
- 3) It is ideal circuit for impedance matching
- 4) The constructional details of an emitter follower circuit are nearly similar to a normal amplifier. The main difference is that the load R_L is absent at the collector terminal, but present at the emitter terminal of the circuit. Thus the output is taken from the emitter terminal instead of collector terminal.
- 5) The biasing is provided either by base resistor method or by potential divider method

The major characteristics of the emitter follower are as follows

- 1) No voltage gain. In fact, the voltage gain is nearly 1.
- 2) Relatively high current gain and power gain.
- 3) High input impedance and low output impedance.
- 4) Input and output ac voltages are in phase

Procedure:

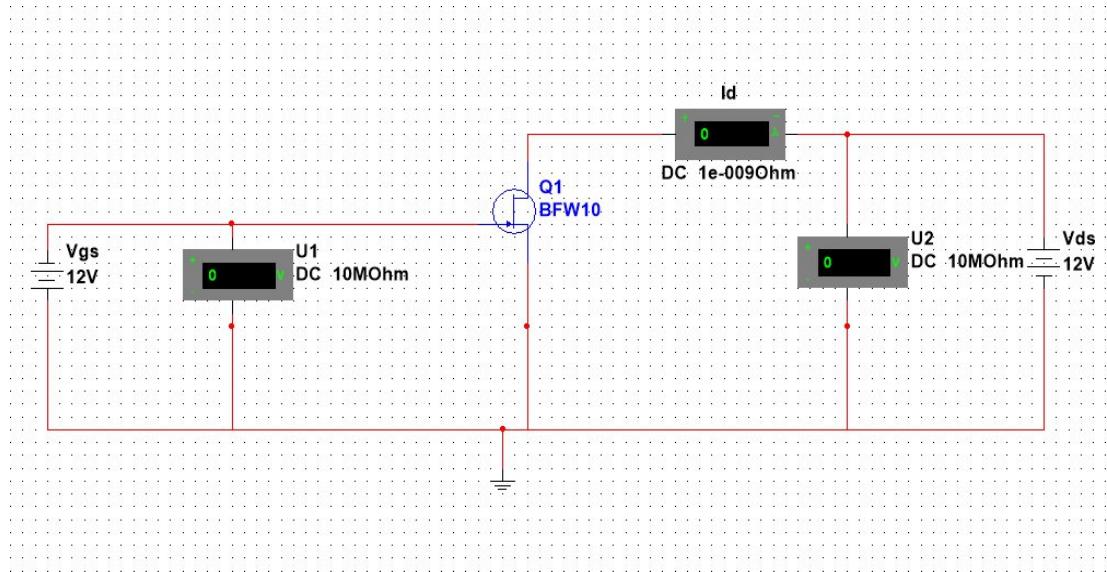
- 1) Make the connection as per circuit diagram
- 2) Apply the input of 1V amplitude and 1KHz frequency from signal generator
- 3) Observe the output waveform at oscilloscope by running the simulation
- 4) Observe that output which will be same as input which proves the emitter follower circuit (output follows the input)

Experiment 7

Transfer and Drain Characteristics of JFET

Aim: Study of Transfer and Drain Characteristics of JFET using multisim software

Circuit diagram:



Procedure:

- 1) Make the connection as per circuit diagram in Multisim
- 2) Perform the following steps to obtain the drain characteristics

- a) Simulate \Rightarrow analyses \Rightarrow Dc sweep
- b) Analysis parametre

| | |
|----------------------------|----------------------------|
| Source1 \Leftarrow Vds | Source1 \Leftarrow Vgs |
| Start value \Leftarrow 0 | Start value \Leftarrow 0 |
| Stop value \Leftarrow 10 | Stop value \Leftarrow 2 |
| Increment \Leftarrow 0.5 | Increment \Leftarrow 0.5 |

- c) Output \Leftarrow add expression \Leftarrow abs() \Leftarrow click on I(Vds) \Leftarrow copy variable to expression \Leftarrow OK \Leftarrow RUN

- 3) Perform the following steps to obtain the transfer characteristics

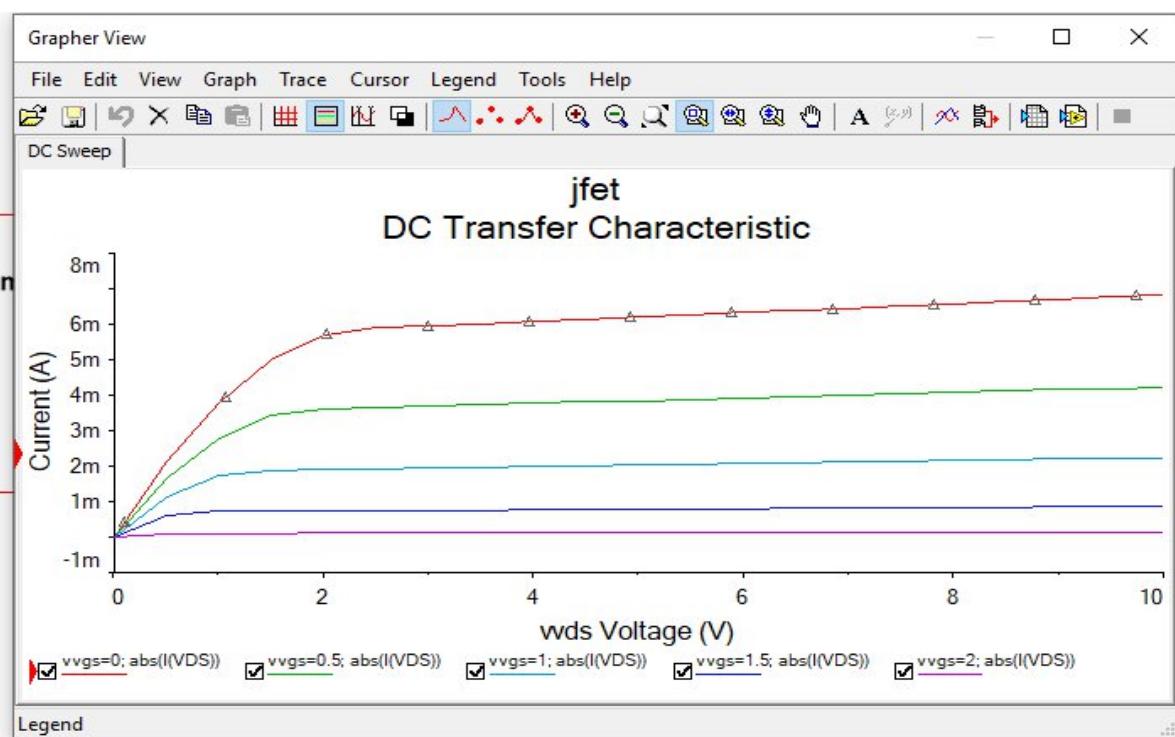
- a) Simulate \Rightarrow analyses \Rightarrow Dc sweep
- b) Analysis parametre

| | |
|----------------------------|----------------------------|
| Source1 \Leftarrow Vgs | Source1 \Leftarrow Vds |
| Start value \Leftarrow 0 | Start value \Leftarrow 2 |
| Stop value \Leftarrow 2 | Stop value \Leftarrow 4 |
| Increment \Leftarrow 0.5 | Increment \Leftarrow 2 |

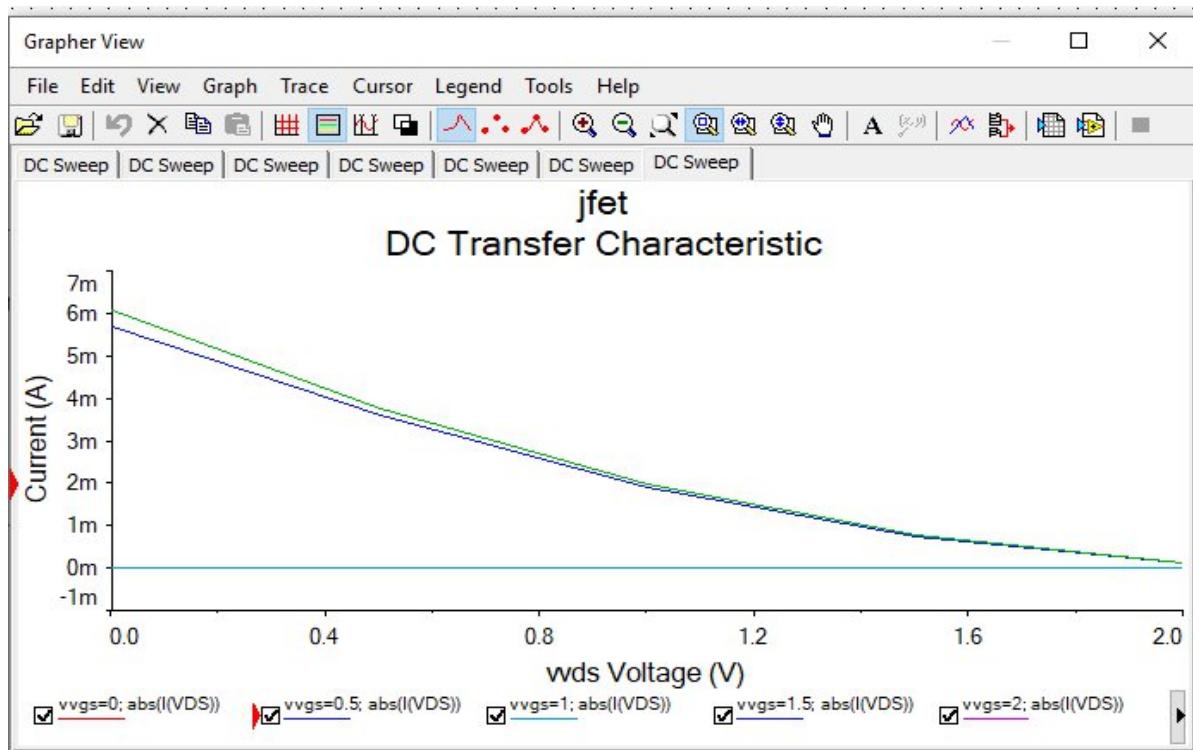
- c) Output \Leftarrow add expression \Leftarrow abs() \Leftarrow click on I(Vgs) \Leftarrow copy variable to expression \Leftarrow OK \Leftarrow RUN

Output Graph:

Drain Characteristics



Transfer Characteristics



Theory:

The transfer and drain characteristics of a Junction Field-Effect Transistor (JFET) are two important graphical representations that describe the behavior of the JFET in response to changes in its control voltage and drain current. Understanding these characteristics is crucial when working with JFETs, as they help in selecting, biasing, and analyzing the device's performance.

1. Transfer Characteristics (Id vs. Vgs):

The transfer characteristics of a JFET illustrate the relationship between the gate-source voltage (V_{gs}) and the drain current (I_d). These characteristics are used to understand how the JFET operates and controls the drain current based on the gate-source voltage.

In the transfer characteristics curve:

- 1) As V_{gs} increases in the negative direction (for an N-channel JFET), I_d decreases. This represents the JFET's voltage-controlled current reduction.
- 2) As V_{gs} decreases in the negative direction, I_d increases. This region is called the saturation region, where the JFET operates as a voltage-controlled current source.
- 3) The transfer characteristics are typically nonlinear and can be divided into three regions: cutoff, ohmic, and saturation.
- 4) The gate-source voltage at which I_d becomes zero represents the pinch-off voltage (V_p), and it is a crucial parameter in JFET operation.

2. Drain Characteristics (Id vs. Vds):

The drain characteristics of a JFET illustrate the relationship between the drain-source voltage (V_{ds}) and the drain current (I_d) with the gate-source voltage held constant. These characteristics help understand how the JFET operates in response to variations in the drain voltage.

In the drain characteristics curve:

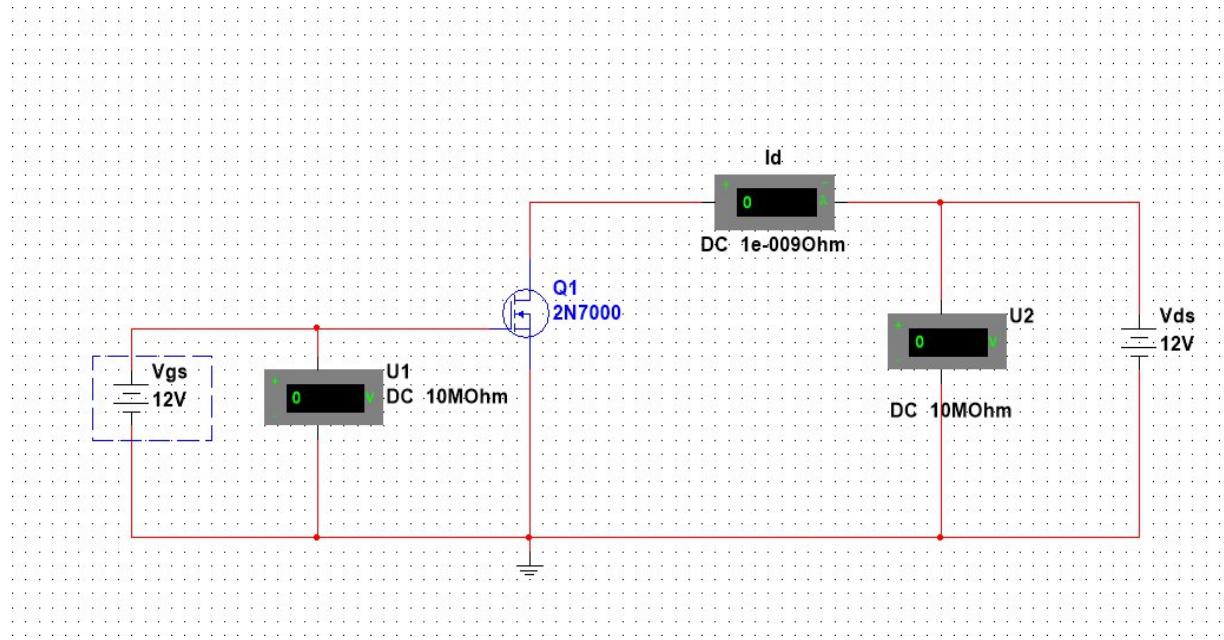
- 1) Initially, as V_{ds} increases, I_d increases linearly, following Ohm's law ($I_d \propto V_{ds}$).
- 2) Beyond a certain point, called the pinch-off point, the drain current remains relatively constant (saturation region) and is no longer directly proportional to V_{ds} .
- 3) The saturation region typically starts when V_{ds} is greater than or equal to the pinch-off voltage (V_p).
- 4) In the saturation region, the JFET operates as a voltage-controlled current source with V_{gs} held constant.
- 5) The drain-source voltage at which I_d saturates represents the drain-to-source breakdown

Experiment 8

Transfer and Drain Characteristics of n channel MOSFET

Aim: Study of Transfer and Drain Characteristics of n channel MOSFET using multisim software

Circuit diagram:

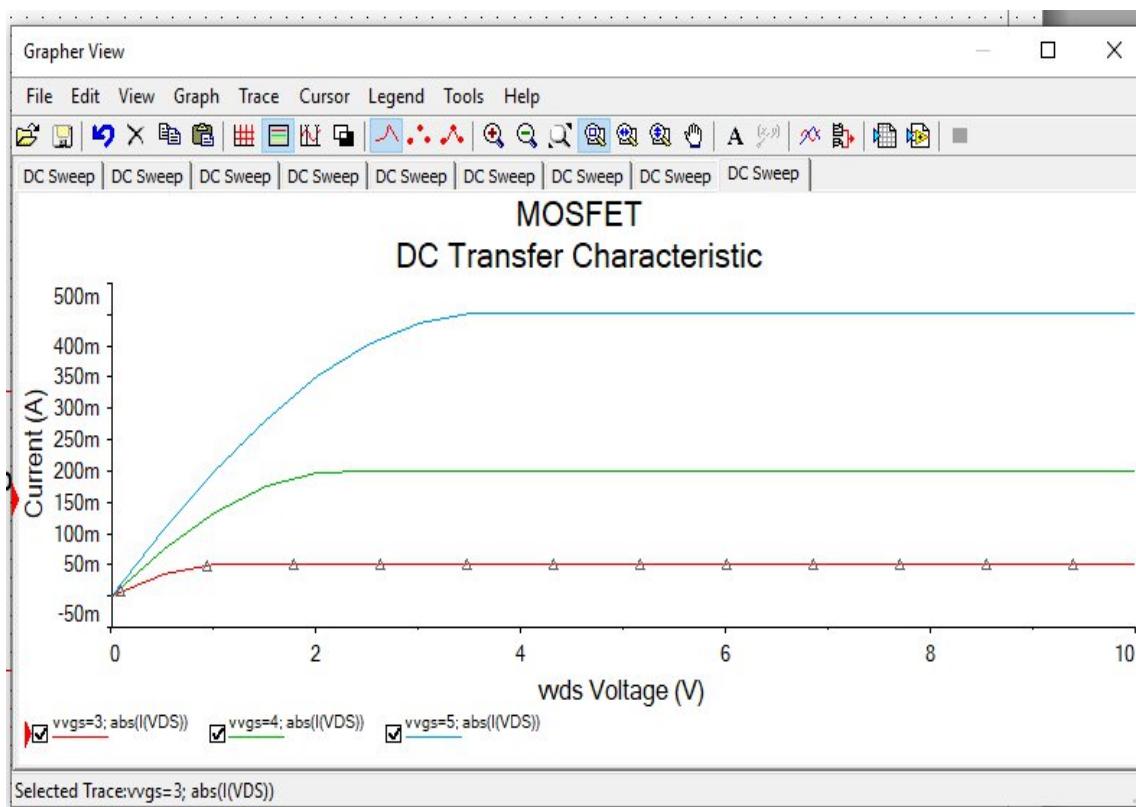
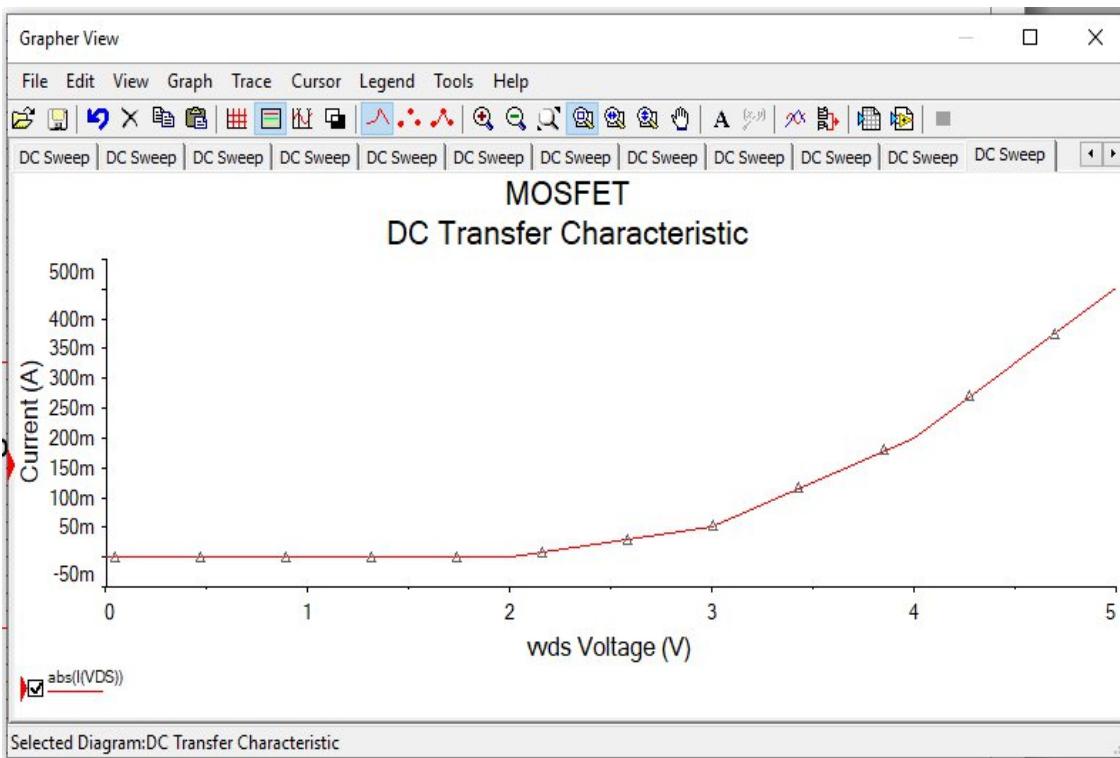


Procedure:

- 1) Make the connection as per circuit diagram in Multisim
- 2) Perform the following steps to obtain the drain characteristics
 - a) Simulate \Rightarrow analyses \Rightarrow DC sweep
 - b) Analysis parametre

| | |
|----------------------------|----------------------------|
| Source1 \Leftarrow Vds | Source1 \Leftarrow Vgs |
| Start value \Leftarrow 0 | Start value \Leftarrow 3 |
| Stop value \Leftarrow 10 | Stop value \Leftarrow 5 |
| Increment \Leftarrow 0.5 | Increment \Leftarrow 1 |
 - c) Output \Leftarrow add expression \Leftarrow abs() \Leftarrow click on I(Vds) \Leftarrow copy variable to expression \Leftarrow OK \Leftarrow RUN
- 3) Perform the following steps to obtain the transfer characteristics
 - a) Simulate \Rightarrow analyses \Rightarrow DC sweep
 - b) Analysis parametre

| |
|----------------------------|
| Source1 \Leftarrow Vgs |
| Start value \Leftarrow 3 |
| Stop value \Leftarrow 5 |
| Increment \Leftarrow 1 |
 - c) Output \Leftarrow add expression \Leftarrow abs() \Leftarrow click on I(Vds) \Leftarrow copy variable to expression \Leftarrow OK \Leftarrow RUN

Output Graph:**Drain Characteristics****Transfer Characteristics**

Theory:

The transfer and drain characteristics of an N-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) are two essential graphical representations that describe the behavior of the MOSFET in response to changes in its gate-source voltage and drain current. Understanding these characteristics is crucial for working with N-channel MOSFETs, as they help in selecting, biasing, and analyzing the device's performance.

1. Transfer Characteristics (Id vs. Vgs):

The transfer characteristics of an N-channel MOSFET illustrate the relationship between the gate-source voltage (V_{gs}) and the drain current (I_d). These characteristics help understand how the MOSFET operates and controls the drain current based on the gate-source voltage.

In the transfer characteristics curve:

- 1) As V_{gs} increases in the positive direction (more positive for an N-channel MOSFET), I_d increases, representing the MOSFET's voltage-controlled current enhancement.
- 2) The MOSFET typically operates in the saturation region for V_{gs} greater than the threshold voltage (V_{th}).
- 3) The region to the left of the threshold voltage (V_{th}) is the cutoff region, where I_d is very low.
- 4) The transfer characteristics are usually nonlinear and show a steep increase in I_d as V_{gs} increases beyond the threshold voltage.
- 5) The threshold voltage (V_{th}) is a crucial parameter in MOSFET operation, and it determines when the device starts conducting.

2. Drain Characteristics (Id vs. Vds):

The drain characteristics of an N-channel MOSFET illustrate the relationship between the drain-source voltage (V_{ds}) and the drain current (I_d) with the gate-source voltage (V_{gs}) held constant. These characteristics help understand how the MOSFET operates in response to variations in the drain voltage.

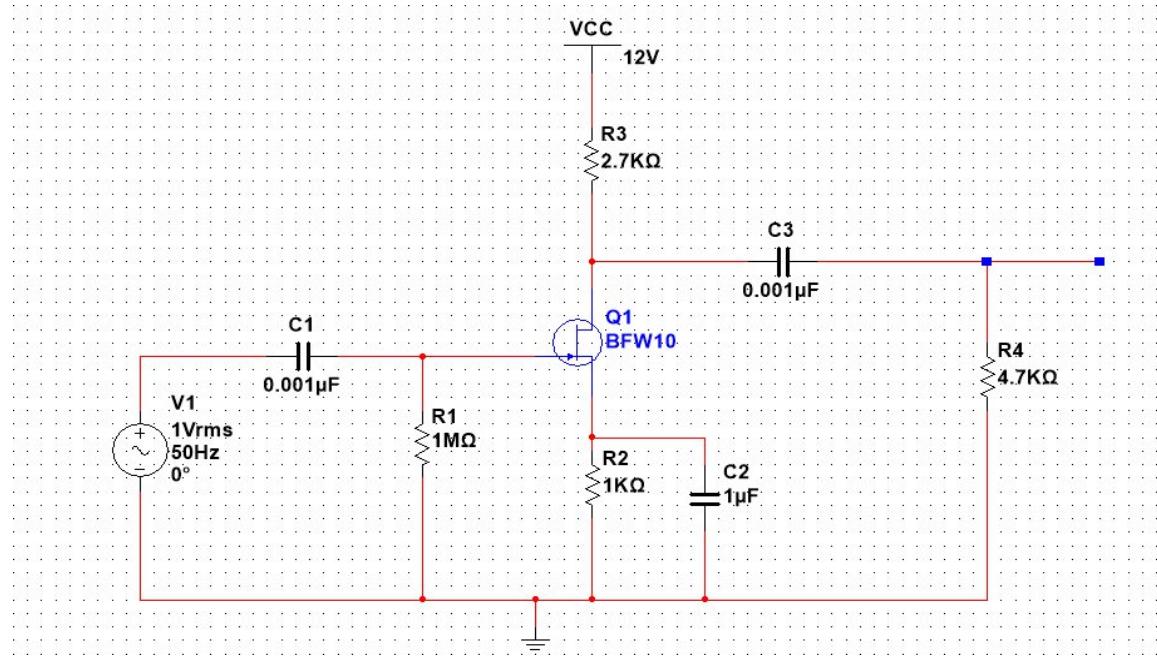
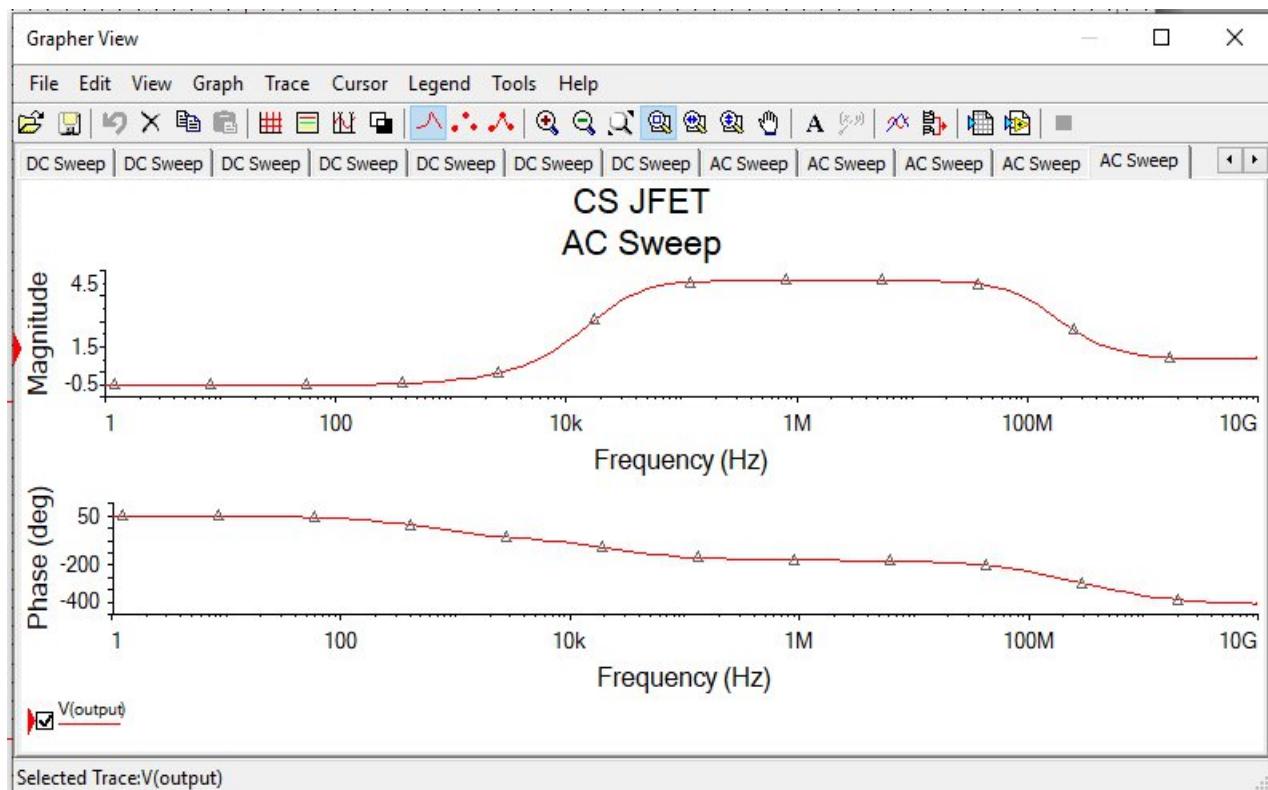
In the drain characteristics curve:

- 1) Initially, as V_{ds} increases, I_d increases linearly, following Ohm's law ($I_d \propto V_{ds}$).
- 2) Beyond a certain point, the drain current reaches a saturation level, and it no longer increases significantly with increasing V_{ds} . This saturation region typically occurs when V_{ds} is sufficiently higher than $V_{gs} - V_{th}$.
- 3) The MOSFET operates as a voltage-controlled current source in the saturation region.
- 4) The saturation region is desirable for many applications because it allows the MOSFET to operate as an amplifier or a switching device.
- 5) The drain-source voltage at which I_d saturates represents the drain-to-source breakdown voltage (BV_{dss}).

Experiment 9:

Common Source JFET/MOSFET Amplifier

Aim: Study of Transfer and Drain Characteristics of jfet using multisim software

Circuit diagram:**Output Graph:**

Theory:

In the Common Source JFET configuration, the Source terminal of JFET is common to both input and output. In this configuration, we will consider the Gate and Drain terminals of the JFET as the input and output terminals.

The Common Source JFET amplifier is like the Common Emitter (CE) amplifier. In this JFET Amplifier, the AC (sinusoidal) voltage waveform applied at the Gate terminal will be amplified and produced at the Drain terminal. But there will be an 180° phase difference between the input and output waveforms.

Both the input and output resistances of this JFET amplifier have a medium value. Even this amplifier's voltage and current gain are of medium value. We can use a CS amplifier as a power amplifier, just like a CE amplifier, since it has high power gain

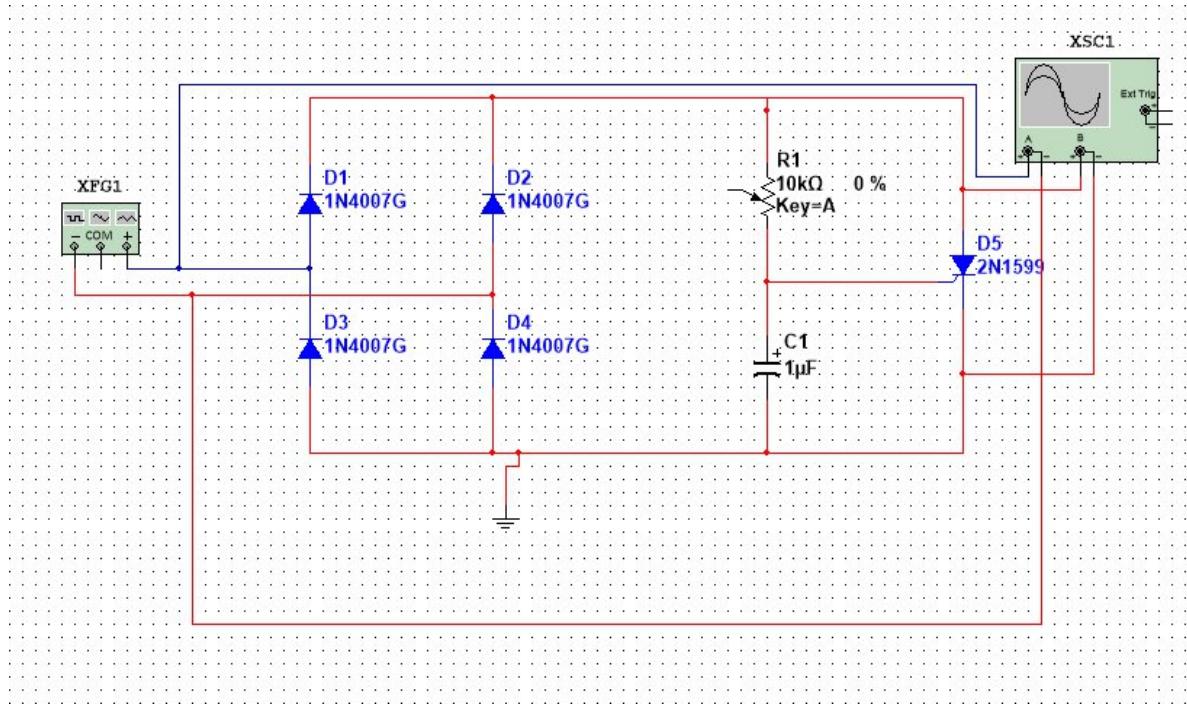
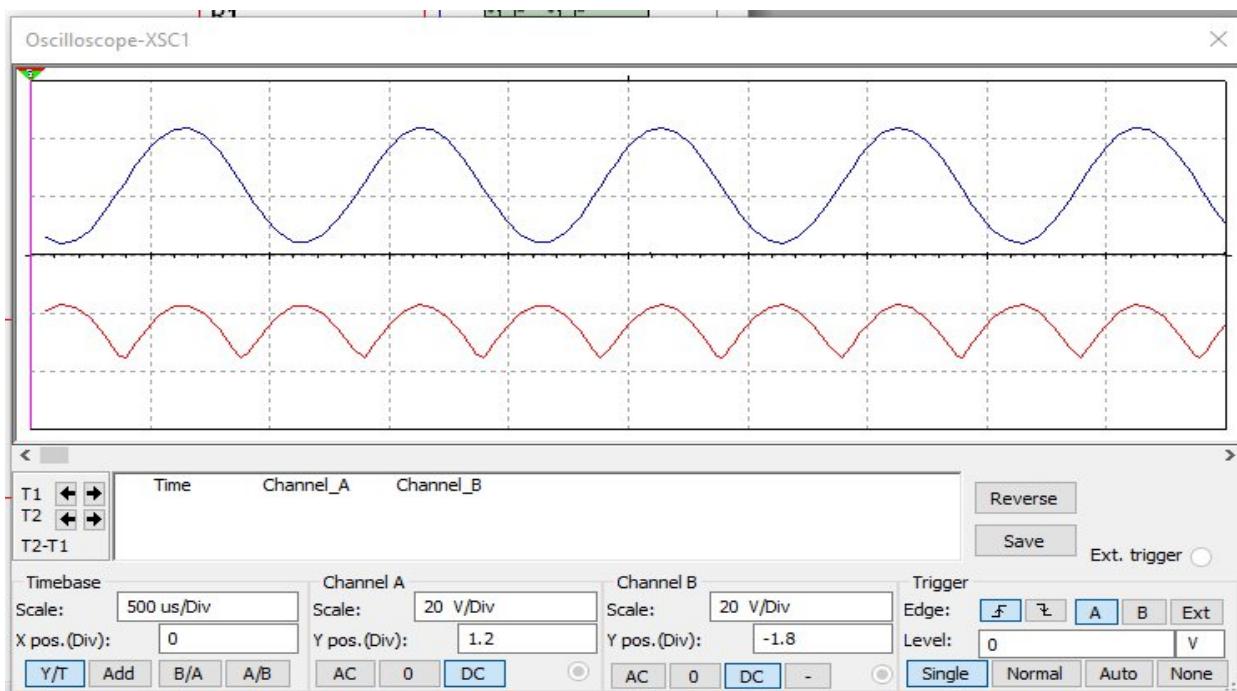
Procedure:

- 1) Make the connection as per circuit diagram in Multisim
- 2) Place the junction at a point of $0.001\mu F$ capacitor and $4.7K\Omega$ resistor
(place \cap junction \cap name it as output)
- 3) Perform the following steps to obtain the frequency response
 - a) Simulate \cap analyses \cap AC sweep
 - b) Frequency parameters \cap vertical scale \cap linear
 - c) Output \cap click on V(output) \cap Add \cap Run

Experiment 10

Full Wave Controlled Rectifier using RC Triggering

Aim: Study of Full Wave Controlled Rectifier using RC Triggering using multisim software

Circuit diagram:**Waveform:**

Theory:

A Full-Wave Controlled Rectifier using RC triggering is a circuit that controls the rectification of an AC signal into a full-wave rectified output using an RC (Resistor-Capacitor) network to trigger the thyristors (SCRs or Silicon-Controlled Rectifiers). This type of rectifier allows you to control the firing angle of the thyristors, enabling precise control over the output waveform. It's often used in applications like AC motor speed control and power supplies

Resistance – Capacitance (RC) Firing Circuit

- 1) The limitation of resistance firing circuit can be overcome by the RC triggering circuit which provides the firing angle control from 0 to 180 degrees. By changing the phase and amplitude of the gate current, a large variation of firing angle is obtained using this circuit
- 2) By varying the variable resistance, triggering or firing angle is controlled in a full positive half cycle of the input signal
- 3) When the capacitor charging voltage is equal to the gate trigger voltage, SCR is turned ON and the capacitor holds a small voltage. Therefore the capacitor voltage is helpful for triggering the SCR even after 90 degrees of the input waveform.

Procedure:

- 1) Make the connection as per circuit diagram in multisim
- 2) Run the simulation and observe the out waveform