Date:02/05/2019

Name: Nischith C N

Report on "NAND flash memory system based on the Harvard buffer architecture for multimedia applications"

The goal of the paper is to design a high-performance Non-volatile flash memory which provides method of executing programs directly from long term storage rather than copying it into RAM. NAND flash with high density and low cost can be made as an alternative to NOR flash memory. It was proposed that by reducing the number of read and write frequency and with improvement in the average memory access time the performance of the flash could improve drastically.

The main disadvantage of NAND over NOR is the initial access time which is around 25micro second for NAND and 50 to 100 nano second for NOR. It is mainly because of this reason NOR is preferred over NAND. There are two important features which play a key role in performance such as spatial locality and temporal locality, Spatial locality related to data elements that are relatively at close storage locations and also when a particular location is referenced at a particular time and it is possible that nearby memory locations will be referenced in the near future. The temporal locality refers to the reuse of specific data, and resources, within a relatively small-time duration. Using the spatial locality feature a large amount of data can be fetched at once and thus reducing the number of cache entries and the performance of temporal locality is improved by increasing the number of cache entries and by decreasing the block size. But both the locality features cannot be satisfied with unified cache system.

In order to overcome the above drawbacks researchers followed a different approach and proposed a high-performance NAND flash based on the Harvard architecture. The proposed solution introduces a data buffer along with SDRAM/SRAM This architecture has greater performance by having separate physical memories for instructions and data and thus going beyond the limitations of unified buffer. An experiment was conducted by the researches by building a prototype consisting of ARM9 based processor and buffers for instruction and data (SRAM and SDRAM) with NAND flash. The result of this experiment showed increased performance in terms of write and erase operations. The write operation is decreased by 73% along with the improved erase operation by 74%. Thus an approximate 75% improvement in the memory access latency.

Reference

1. Guthaus MR et al. (2001) MiBench: A free, commercially representative embedded benchmark suite. Proc. of the 4th Ann. IEEE Int'l Workshop Workload Characterization, pp. 3–14Hennessy JL, Patterson DA (2006) Computer architecture: a quantitative approach (4/E). Morgan Kaufmann