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Design of a single ended mirrored cascode OTA

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Design Specifications and targets

Table 1. Design Specifications

Open Loop Differential Gain (Ad)	50dB
Unity gain frequency (f_u) or f_{gc}	500MHz
Supply Voltage (VDD)	1.8V
Load Capacitance (CL)	200fF
Power Consumption	1mW

Design Architecture

Mirrored cascode is one of the often-used OTA architectures for driving on chip capacitive loads. It has most of the times all the nodes except for the output node at high impedance. In this design project we aim to achieve a relatively high f_{gc} (Gain crossover frequency) of around 2π x 500MHz for a reasonable open loop differential gain of around 50dB. Table 1. shows our target specifications and figure 1 shows the architecture that the design is based upon.

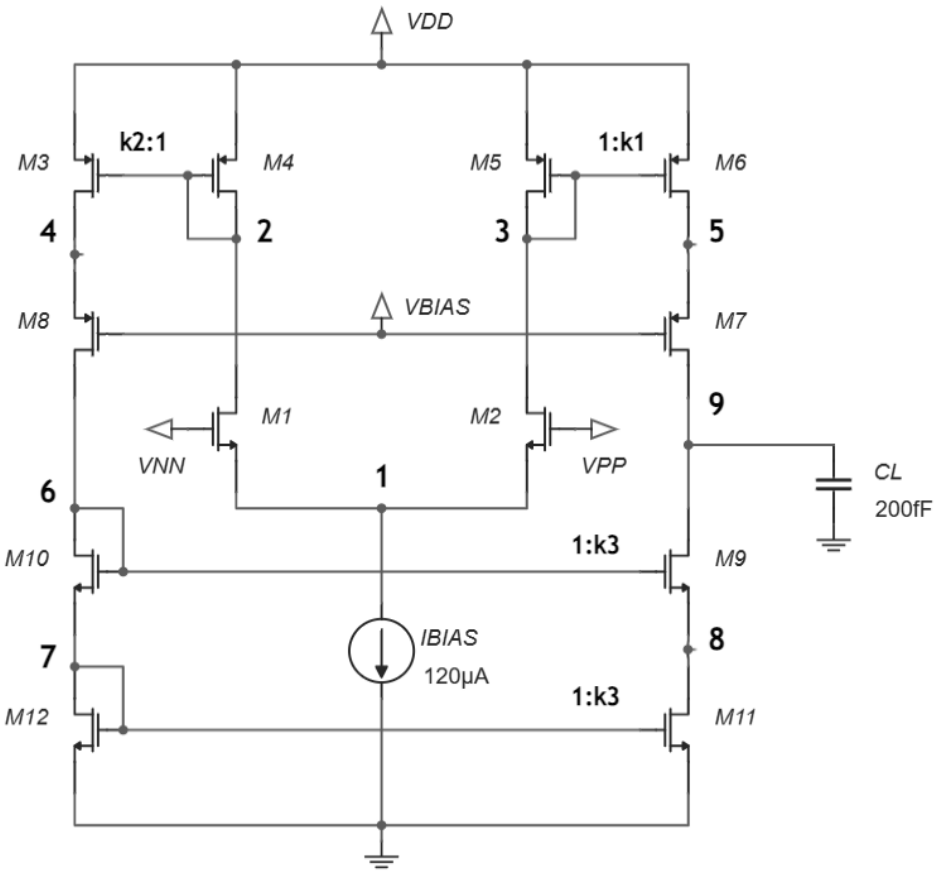

Figure 1. Mirrored Cascode OTA

Transistor Modelling

Before starting with any design, we need to know which technology we are working with and what are its specifications. For this design, we are working with 90nm Generic Process Design Kit (GPDK90). We start by extracting the parameters like $\mu_o C_{ox}$ and the Vth for the p-mos and n-mos transistors that will be used for the design. The table 2 shows the extracted values for the respective transistors.

Table 2: Extracted parameters

Parameter (for W= 10u, L= 400n)	P-mos	N-mos
$\mu_o C_{ox}$	130u	220u
Vth	457mV	480mV

DC operating points of the MOS transistors

For the correct operation of the topology and before sizing we need to intuitively assume some parameters like overdrive voltage Vov or Vdsat keeping in mind:
All the transistors will be in saturation.
Reasonable voltage swing at the output.
Assuming Vov≈200mV and using Vth n,p from Table 1.1

Input common-mode voltage (Vcm) = VDD/2 ≈ 900mV
VBIAS = M6(Vdsat) + M7(Vgs) ≈ 900mV *w.r.t VDD
Vout Max ≈ M6(Vdsat) + M7(Vdsat) ≈ 400mV w.r.t VDD i.e., 1.4V w.r.t GND
Vout Min ≈ M9(Vdsat) + M12(Vgs) ≈ 900mV w.r.t GND

We can see that the voltage swing is not symmetrical with the supply and reference. The lower limit of swing is smaller due to the presence of a cascode current mirror. The limits and voltages above will be compared with the simulated results for obtaining the desired design specifications.

Standard design approach

The process of designing starts by looking at the given specifications.

1. **Gain Crossover Frequency and Unity Gain Frequency (f_{gc}):**

$$\mathrm{fu} = \frac{k g_{m_1}}{C_L}$$

Given, C_L = 200fF
So, for getting a f_{gc} of 2π x 500MHz, we require a gm_1 ≈ 628uS
Keeping a margin for inaccuracies, gm_1 ≈ 1mS.

2. **Sizing of input transistors:**

We assume the bias current IBIAS = 120uA
The target gm_1 ≈ 1mS
Current in M1 branch (I_1) = IBIAS/2 = 60uA
Using,

$$g_{m1} = \sqrt{2 I_1 u_o C_{ox} \left[\frac{\omega}{L}\right]_0}$$

$[W/L]_o$ ≈ 38. Let's keep, L = 280nm Fixed for the whole design. W_0 ≈ 10um. Using this value, we simulate and get gm_1 ≈ 751uS.Clearly, this is around 75% of the gm_1 we desire. Sweeping W_0 , we get the desired gm_1 at a W_0 of ~30um as shown in Figure 2.

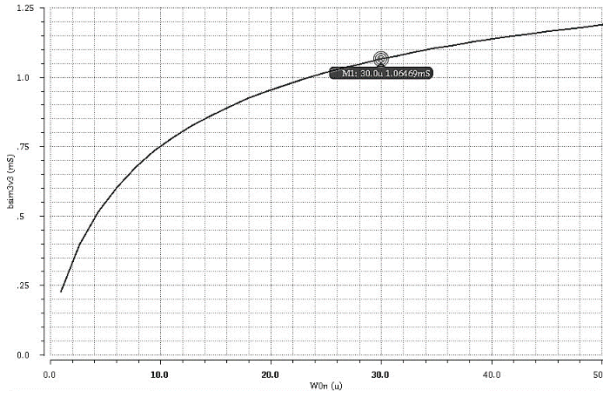

Figure 2. Input transistor size

3. Naming convention used:

As shown in figure 3. Below, creating a variable is convenient for convenient sizing of the transistors by using sweeps.

	Name	Value
1	IREF	120u
2	VBIAS	840m
3	VX	520m
4	CL	200f
5	L	280n
6	L1	280n
7	L2	310n
8	L3	405n
9	L4	385n
10	W0n	30u
11	W0p	30u
12	W1	8.2u
13	W1a	8u
14	W1b	8u
15	W2	9u
16	W3	2u
17	W4	5u

Figure 3. Input transistor size

- The input transistors have a subscript of “0” on their W.
- The upper branch of transistors namely M3,M4,M5 and M6 have a subscript of “$_1$” on their W. for e.g., *W_1 or w1*.
- M7,M8 have a subscript of “$_2$” on their W.
- M9,M10 have a subscript of “$_3$” on their W.
- M11,M12 have a subscript of “$_4$” on their W.
- The length of all the transistors follows the same convention.
- *IREF OR IBIAS* is the bias current provided at the tail of the differential pair.
- *VBIAS* is the bias voltage to be applied to the gates of M7 and M8.
- Resistance seen at the drain of M7 looking upwards is named as *Rout_upper*
- Resistance seen at the drain of M9 looking downwards is named as *Rout_lower*

4. Sizing of output stage:

The main motive of the output stage comprising of 4 transistors is for having a high Rout. We have already arrived at a good enough input transconductance i.e., gm1 that we would rarely touch. After initial sizing for achieving saturation conditions in all the transistors we move forward for obtaining our gain requirements.
Considering the mirror factor(k) with which the upward branch is mirrored, k=1.
We have our DC gain as:

$$A_v = \mathrm{k} \times g_{m1} \times R_{\mathrm{OUT}}$$

Rout is gds_6 amplified by intrinsic gain of M7 *parallel to* gds_{11} amplified by intrinsic gain of M9.

$$R_{\mathrm{OUT}} = \left(\frac{g_{m7}}{g_{\mathrm{ds7}} \times g_{\mathrm{ds6}}}\right) \Big| \Big| \left(\frac{g_{m9}}{g_{\mathrm{ds9}} \times g_{\mathrm{ds11}}}\right)$$

We sweep widths of transistors starting from the bottom current mirror and looking at our Rout_upper and Rout_lower. Since Rout_upper and Rout_lower are in parallel, we try to match the values as close as possible. Figure 4. Shows the values of Rout_upper and Rout_lower obtained using the sizes in the table in Figure 3.

	Name/Signal/Expr	Value
1	Av	wave
2	Phase	wave
3	Gmi	1.06475m
4	Rout_upper	727.515K
5	Rout_lower	940.861K
6	unityGainFreq(VF("/net18"))	503.45M
7	phaseMargin(VF("/net18"))	59.8837

Figure 4.

We have,
gm_1 ≈ 1mS and Rout ≈727KΩ
k ≈ 0.975
Av = 0.975 x 1mS x 727KΩ ≈ 709
Gain in dB ≈ 20log(709) ≈ 57dB

So, having the sizes in figure 3. and the gm_1, Rout values we expect the gain of somewhat close to *57dB*. On plotting, we obtain a gain of *~50dB* with a unity gain bandwidth of *~503MHz*.

5. Power supply section:

For carrying out our testbench setup and characterizing the designed operational amplifier firstly in the figure 5. below we have our power supply section.

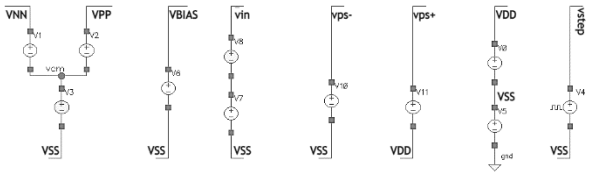

Figure 5. Power supply section

VDD is the maximum voltage that is applied to the operational amplifier i.e., 1.8V.
VSS is the minimum voltage that is applied to the operational amplifier i.e., 0V.
VBIAS is the bias voltage applied to M7 transistor and is given in figure 3.
vin is input common mode voltage applied to the operational amplifier.
vps- is the modelled power supply harmonics introduced to the negative supply terminal of the operational amplifier.
vps+ is the modelled power supply harmonics introduced to the positive supply terminal of the operational amplifier.
vstep is the step voltage applied to the unity gain configuration of the operational amplifier to measure the positive and negative slew rate.

6. Layout of the circuit

We go with the stick diagram approach for the layout of the circuit. While making the stick diagram it is crucial to make the Width scaled, maintain symmetry wherever possible and the same number of fingers in each stack.
We divide the whole circuit used into 4 stacks and go forward with the stick diagram.
We have 8 fingers in each stack and at least 2 fingers per transistor. The final stick diagram of the circuit shown is given in figure a.
Pmos and Nmos in the label signify the fingers for each type of the transistor.

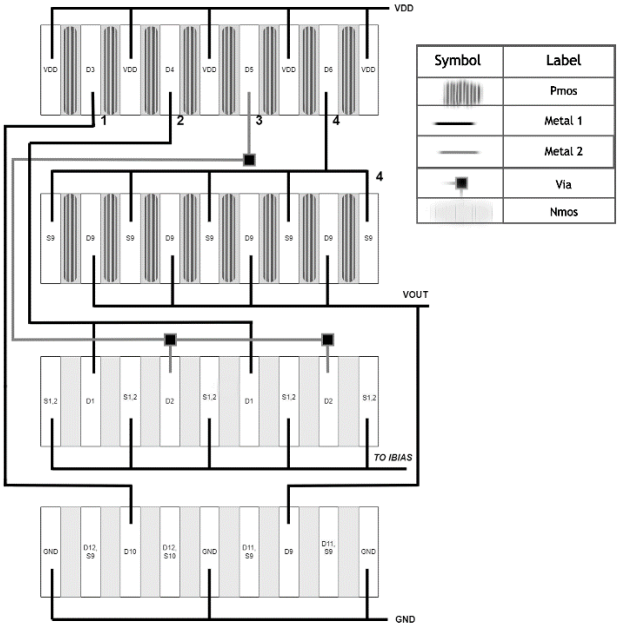

Figure a. Stick diagram of the circuit used

Operational amplifier performance characterization

1. Differential Gain (Ad) and phase :

The target open loop gain of our design was around 50dB and we managed to achieve the gain. The figure 6. Below shows the setup to measure and plot the open loop differential gain and phase.

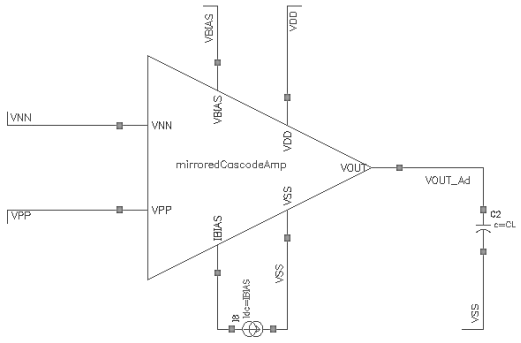

Figure 6. Open loop differential gain and phase setup

After simulating for the gain and phase we obtained the plot shown in figure 7. which shows the following data:

a) Open loop differential gain(Ad) ≈ 50dB
b) Phase margin(PM) ≈ 60 degrees
c) Gain margin(GM) ≈ 16dB
d) Gain crossover frequency(f_{gc}) ≈ 500MHz
e) Phase crossover frequency(f_{pc}) ≈ 1.84GHz

The stability conditions for any system are:

- $f_{gc} < f_{pc}$: Stable
- $f_{gc} > f_{pc}$: Unstable
- $f_{gc} = f_{pc}$: Marginally stable

We can see that our system is stable from two observations:

1) PM > 60 degrees and
2) $f_{gc} < f_{pc}$.

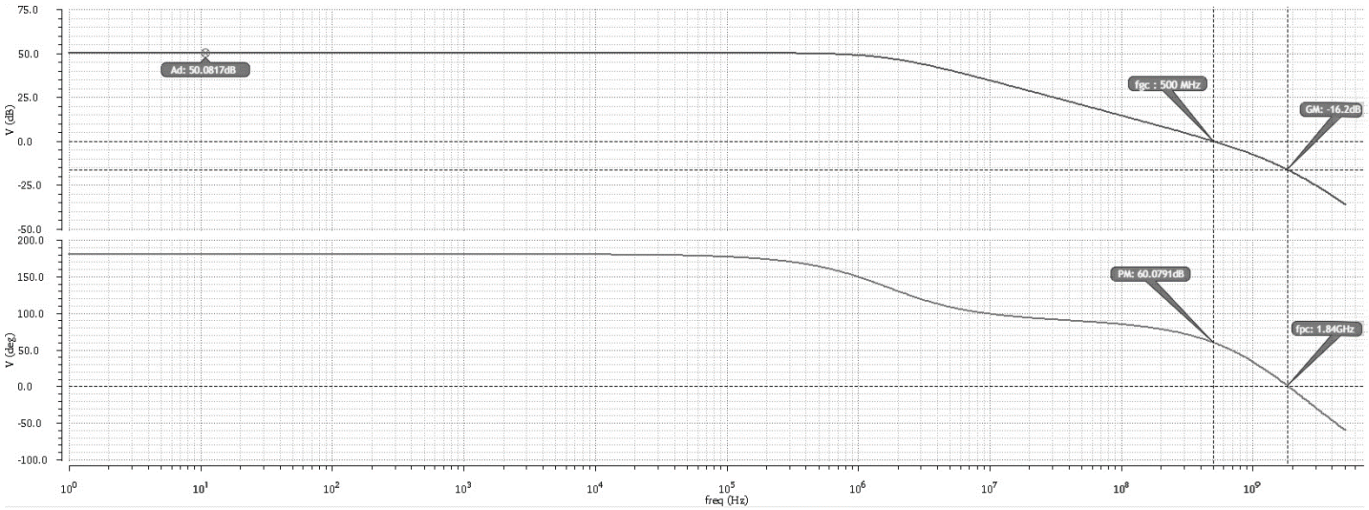

Figure 7. Open loop differential gain and phase with phase and gain margins

2. Common mode gain(Acm) and Common mode rejection ratio(CMRR):

It is the open loop gain observed in the amplifier with a small signal i.e., vin (given in the power supply section) applied at both of its input terminals like shown in figure 8. A low Common mode gain for a range of frequencies is desirable for an opamp.

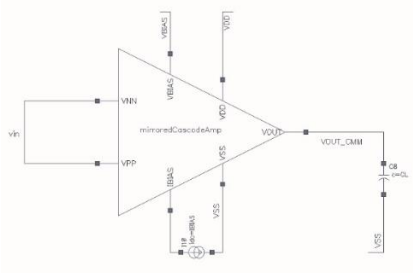

Figure 8. Testbench setup for measuring Acm.

CMRR is the ratio between the Ad and Acm.

$$CMRR = \frac{Ad}{Acm}$$

Since we are using dB scale in our simulations. So,

$$CMRR_{dB} = Ad_{dB} - Acm_{dB}$$

After simulating our design in cadence. We have observed that at low frequencies the Acm is a very good value of around -64dB and even at around our unity gain frequency of 500MHz we have the Acm of around -42dB.We previously obtained our Ad as 50dB. So, our *CMRR comes out to be around 114dB*. The figure 9. Below shows the obtained values of Ad, Acm and CMRR from our simulation.

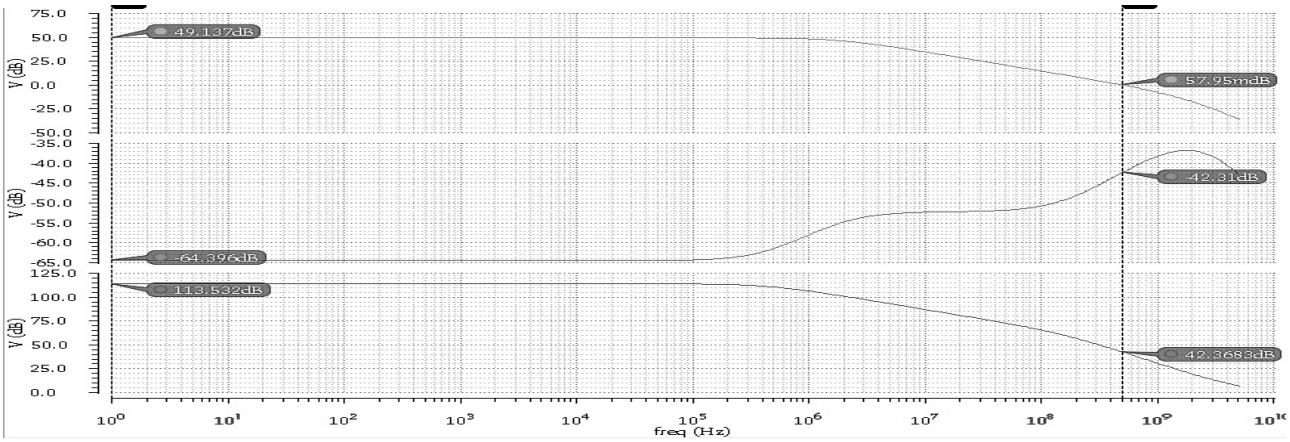

Figure 9. Ad, Acm and CMRR in dB.

3. Power supply rejection ratio (PSRR):

The power supplies we use could be dependent on battery source which could be a constant dc source. Also, there can be scenarios when we would have to use supplies that are wall powered and has some ac harmonics in them. To model the power supply harmonics, we apply to the positive and the negative side vps- and vps+ to the VSS and the VDD terminals respectively. And without applying a signal at the input and only tying the inputs to a Commonmode value we measure the gain due to the harmonics in the positive (Adps+) and negative(Adps-) rail of the opamp.

The testbench setup for PSRR- and PSRR+ is given in the figure 10. and figure11. respectively. As per our simulations we obtained the *Adps+ as around 9dB and Adps- as around 20dB*. Our *PSRR- is around 30dB and PSRR+ is around 41dB*. These values are not that promising yet acceptable. The figure 12. and figure 13. Shows the simulated values of PSRR- and PSRR+ respectively.

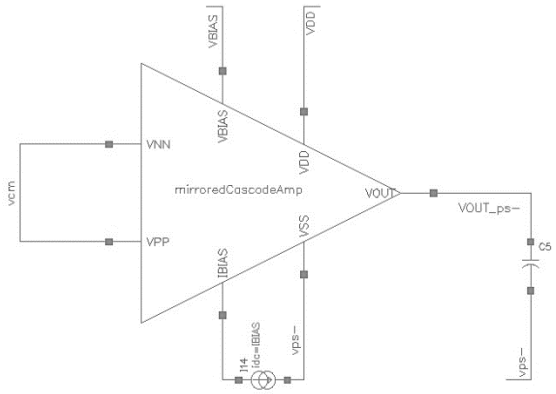

Figure 10. Testbench setup for measuring Adps-

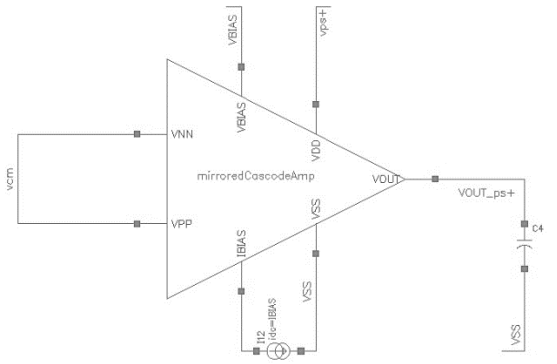

Figure 11. Testbench setup for measuring Adps+

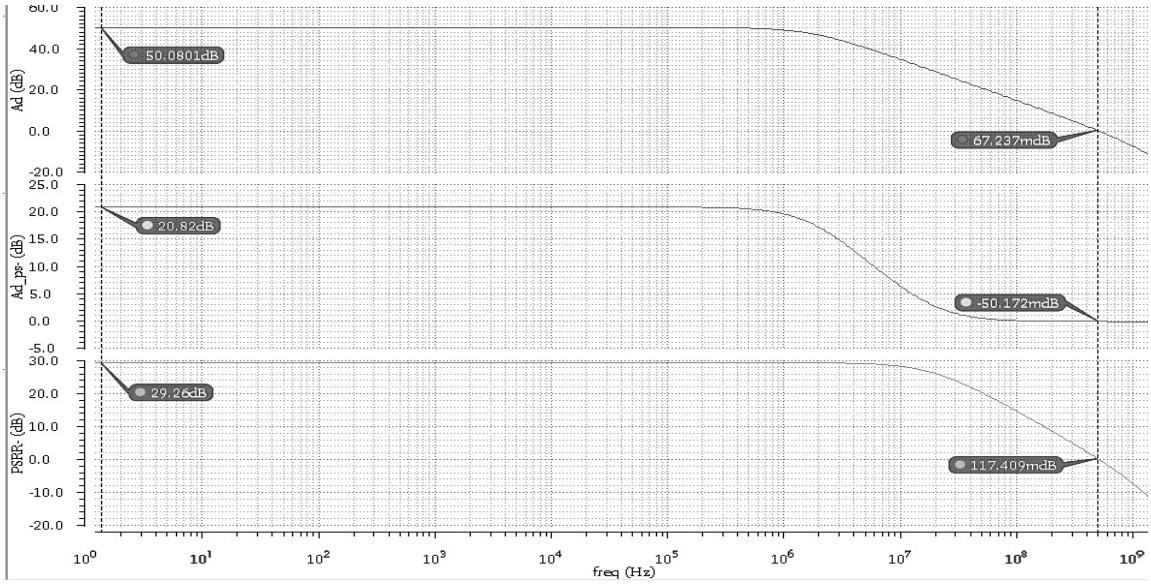

Figure 12. Ad , Adps- and PSRR-

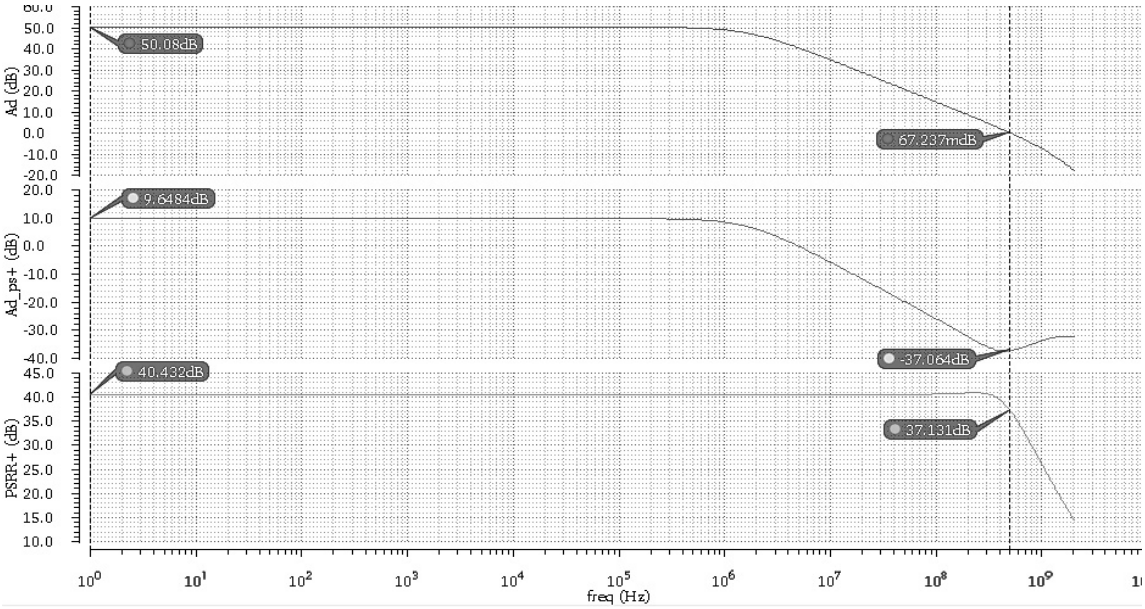

Figure 13. Ad , Adps+ and PSRR+

4. Slew rate

It is the measure of the speed of the circuit. It is defined as the maximum rate of change of voltage at the output with a step at the input.
The testbench setup for slew rate measurements is given in the figure 14.

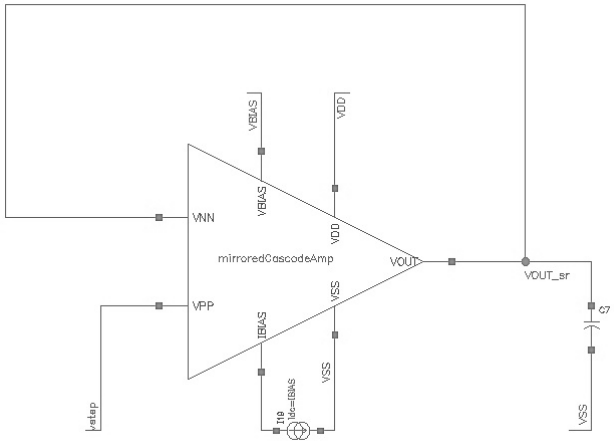

Figure 14. Testbench setup for measuring Slew rate.

The slew rate expression for this OTA is given by:

$$SR_+ = SR_- = \frac{K \times IBIAS}{CL}$$

Where IBIAS is the tail current of our differential pair, K is the mirror factor and CL is the load capacitor value.
In our design:

$K = 0.975$

$IBIAS = 120uA$

$CL = 200fF$

We expect:

$SR \approx 598V/uSec$

The Simulated results for slew rate positive and negative are around 339 V/uSec and 288V/uSec respectively. The figure 15. Shows the plot for the simulated results.

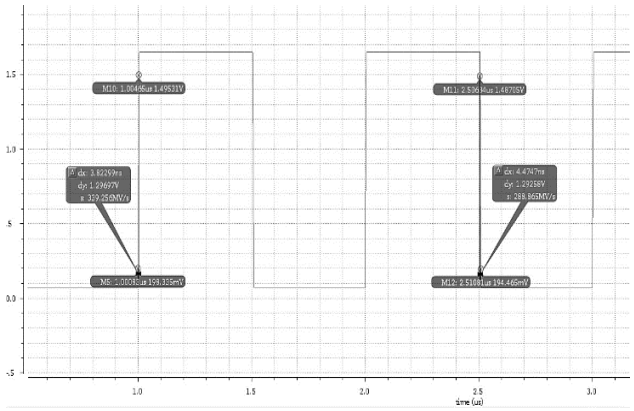

Figure 15. Slew rate positive and negative

5. Transient response

For the transient response, we connect the OTA in a well-known configuration like for e.g., Inverting amplifier as shown in figure 16.

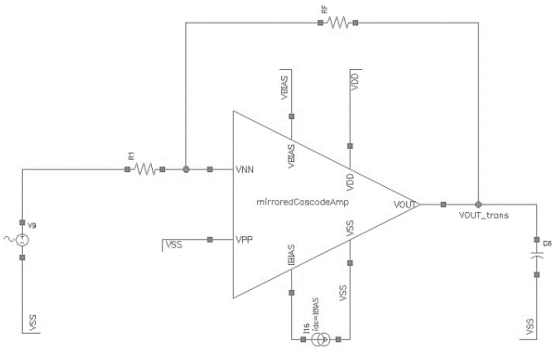

Figure 16. OTA connected in inverting configuration

We apply a large signal voltage of 10mV at the input and the resistive network consists of
Rf = 10MΩ and R1= 1MΩ.
For the inverting amplifier configuration, we have the gain expression as:

$$\frac{Vout}{Vin} = \frac{Rf}{R1}$$

Putting the values, we expect our Vout to be 100mV peak to peak i.e., 10 times the input as per the expression for inverting amplifier given above. The figure 17. Shows the simulated results for our OTA and we see that our peak-to-peak output is around 106mV which is around our expected value.

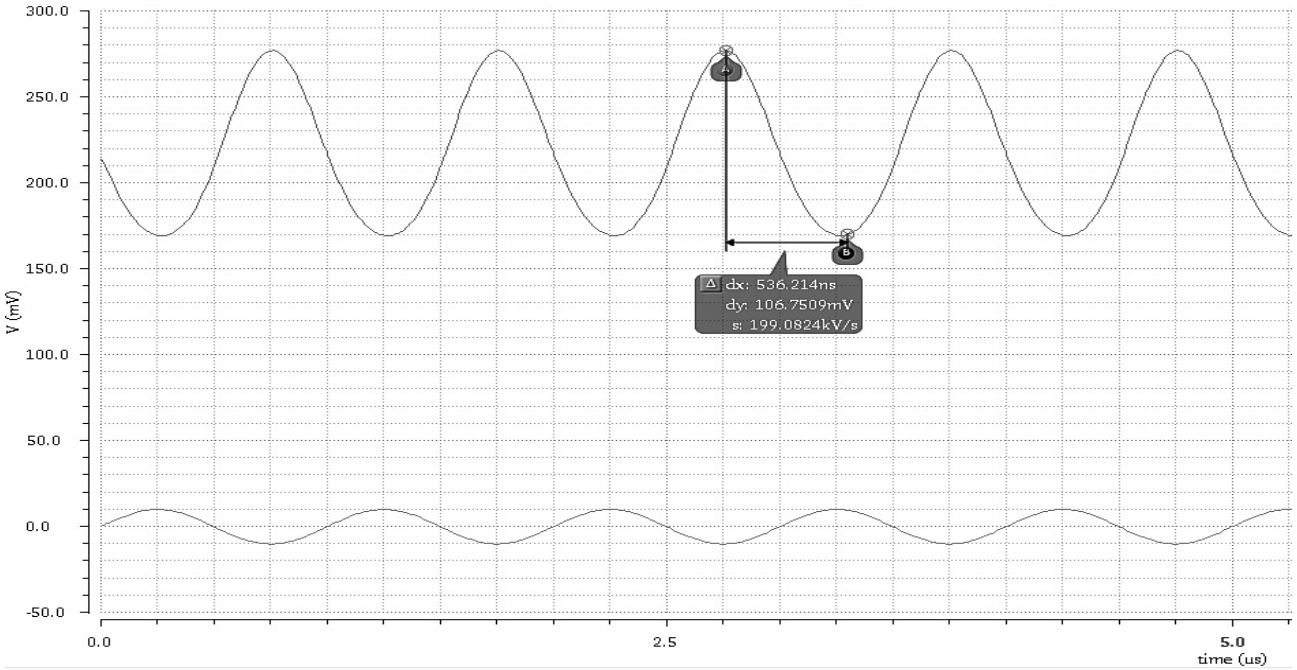

Figure 17. Transient response

Problems faced and learning outcomes

- **Phase margin issue**

The so called non-dominant poles came into picture to degrade the phase margin considerably. The approach to tackle the problem was by reading of "*ANALOG DESIGN FOR CMOS VLSI SYSTEMS by Franco Maloberti*" where I found that I could improve the phase margin by a small tweak in the circuit which was removal of transistor M8. But the book left me in a search for the reason why! Which was when I stumbled upon the book "*Analog integrated circuit design by Tony Chan Carusone, David A. Johns, Kenneth W. Martin*". In the book I found an interesting concept related to modelling all the non-dominant pole frequency through an equivalent pole frequency. Also, a handy table to refer to given below in figure 18.

Table 5.1 The relation ship betw een PM, ω_t/ω_{eq}, Q fact or, and percentage overshoot

PM (Phase margin)	ω_t/ω_{eq}	Q factor	Percentage overshoot for a step input
55°	0.700	0.925	13.3%
60°	0.580	0.817	8.7%
65°	0.470	0.717	4.7%
70°	0.360	0.622	1.4%
75°	0.270	0.527	0.008%
80°	0.175	0.421	-
85°	0.087	0.296	-

Figure 18.

for me to have a good phase margin of 60°, I need to have the ratio of ωt/ωeq less than 0.6.For achieving that, I need to have a large value of ωeq. Where, ωeq = sum of(ω due to non-dominant poles). So, removing one non-dominant pole, tweaking the values of aspect ratios, and accepting an offset at the output was the way I tackled the problem. I could not trade Frequency or Gain as both requirements were high.

Summary of results

Feature	Achieved Result
Open Loop differential gain	50dB
Unity Gain Bandwidth	503MHz
Phase margin	60°
Gain margin	16dB
Phase crossover frequency	1.84GHz
Gain crossover frequency	500MHz
CMRR	114dB
PSRR+	41dB
PSRR-	30dB
Slew rate +	339 V/μs
Slew rate -	288V/μs
Power consumption	381μW

References

1. *ANALOG DESIGN FOR CMOS VLSI SYSTEMS by Franco Maloberti, Chapter 5*
2. *Analog integrated circuit design by Tony Chan Carusone, David A. Johns, Kenneth W. Martin, Chapter 5, 6*
3. A NOTE ON STABILITY ANALYSIS USING BODE PLOTS JUERGEN HAHN, THOMAS EDISON, THOMAS F. EDGAR The University of Texas at Austin • Austin, TX 78712-1062
4. Design of Analog CMOS Integrated Circuits Second Edition, Behzad Razavi , Chapter 8