

Interview Experience – Texas Instruments (Embedded Software Engineer)

For Online Test- Aptitude, Microprocessor and Microcontrollers, OS, COA, Basic C programming, Searching and Sorting Algorithms.

Interview-

- 1) Introduction, discussion on resume, Projects, Tinker CAD models and Arduino Programming.
- 2) What is a PLC? Explain the internal architecture of a PLC. Explain Ladder Logic programming. How to get time delay in a motor using ladder logic, explain latching and unlatching.
- 3) How would you configure NodeMCU Microcontroller to act as a data server? What tech stack will you use to make the backend?
- 4) What is a sensor? Sensor vs Transducer? How does a gas pressure sensor work?
- 5) What is Paging and Swapping? Explain Thrashing. What is the best page size when designing an operating system?
- 6) Explain Process States, What is RR scheduling Algorithm?
- 7) Explain the memory hierarchy. Why Cache is faster than RAM?
- 8) Draw SRAM and DRAM cell. Which one has more density?
- 9) Which component would you use to make cache? What is L1/L2/L3?
- 10) What are registers? What is memory management unit?
- 11) What are interrupts? Why do we use subroutines?
- 12) Write a C Program to copy the contents of a memory location to another? You should not use memcpy. (The algorithm should be efficient and should work for any data type)
- 13) <https://www.geeksforgeeks.org/position-of-rightmost-set-bit/>
- 14) What are generics in JAVA? How would you implement generics in C?
- 15) What are the steps of compilation of a C Program?
- 16) What is Linker? What is volatile?
- 17) (The interviewer asked me to choose a subject of choice, I chose Computer Networks) What is Network Security? What is OSI model?
- 18) Which layer is used to implement security in network? What is TCP, what are sockets?
- 19) Which layer is used for error correction?
- 20) Explain Circular Redundancy Check.
- 21) Explain Checksum, he gave me a problem to solve on checksum and was asking follow-up questions on my approach.
- 22) Explain QuickSort, comment on its time complexity .

Texas Instruments Intern Hiring (Embedded Software Profile)

First of all, he confirmed that am I really interested in embedded and whether I gave interviews for Analog/digital profile as well or not.

I told him that I gave test for embedded software only and I am interested in this.

Q. Do you know C language?

Ans. Yes Sir, I am comfortable in C language. Although, I prefer C++ for all my coding and DSA stuffs but I know C language well.

Q. Write code to set a given bit in an unsigned integer. (He want to see only function, no need to compile and run the code)

Ans.

```
unsigned int setBit (unsigned int x, int bit)
{
    unsigned int ans;
    ans = x | 1 << bit;
    return ans;
}
```

Q. Write code to clear a given bit in an unsigned integer.

Ans.

```
unsigned int clearBit(unsigned int x, int bit)
{
    unsigned int ans;
    ans = x & ~(1 << bit);
    return ans;
}
```

Q. Swap all even and odd bits of an unsigned integer.

Ans. I told him that we can use a loop to iterate over all the bits while swapping the bits.

He asked not to use a loop and do it only by using some mask sort of thing.

I took some time (keep talking with interviewer even when you are thinking or writing something on paper) and wrote the below code then he was satisfied.

Odd Bits and even bits can be extracted by using mask (0x55555555 and 0xAAAAAAA here) then shifting the bits to change their positions.

At last, doing an OR operation of even and odd bits will give us the required result.

```
unsigned int swapBit(unsigned int x)
{
    unsigned int ans;
    unsigned int oddBits = x & 0x55555555;
    unsigned int evenBits = x & 0xAAAAAAA;
    evenBits >>= 1;
    oddBits <<= 1;

    return evenBits | oddBits;
}
```

Follow up question- He told what if a signed integer was given where the last bit will denote the sign of the number. The above code will not work.

I was a bit confused in this question and took lot of time, he helped with some hints like try to do by changing the order of the steps or adding some more operations.

He himself told to shift the number in between somewhere then I gave the solution:

```
int swapBit2(int x)
{
    int ans;
    int oddBits = x & 0x55555555;
    x >>= 1;
    int evenBits = x & 0x55555555;
    evenBits >>= 1;
    oddBits <<= 1;
    return evenBits | oddBits;
}
```

Q. You are given an array of unsigned char, count the total number of set bits in the array.

Ans. I told him a $O(N^2)$ solution but, he said it will take a huge time if array is large so optimize it using some space as we will have only 8 bits and numbers from 0 to 255 for unsigned char.

In between small questions like:

Q. What is the range of unsigned char.

Ans. 0-255

Q. How many bits unsigned char have?

Ans. 8

Final Code:

```
unsigned char lookUpTable[256];

int countBits(unsigned char arr[], int n)
{
    int ans = 0;
    for (int i = 0; i < n; i++)
    {
        unsigned char num = arr[i];
        ans += lookUpTable[num];
    }
    return ans;
}
```

Follow up question: What if I allow you to use look up table of size 16 only?

He gave me hint to divide the 8 bits of number in to two halves and try.

Another question: How will you extract the first 4 and last 4 bit using mask?

Ans. Below two lines will do the work:

```
unsigned char num1 = num >> 4; (For extracting the last 4 bits, as first 4 bits will fall off)
unsigned char num2 = num & (0xF); (For extracting the first 4 bits)
```

Final code:

```
unsigned char lookUpTable[16];

int countBits(unsigned char arr[], int n)
{
    int ans = 0;
    for (int i = 0; i < n; i++)
    {
        unsigned char num = arr[i];
        unsigned char num1 = num >> 4;
        unsigned char num2 = num & (0xF);
        ans += lookUpTable[num1];
        ans += lookUpTable[num2];
    }
    return ans;
}
```

Q. What is the term for what we did just now (decreasing the time first using lookuptable(256 size) then increasing some time while decreasing the space to 16 only)

Ans. Space-Time Trade Off.

After this question he was satisfied with my knowledge about C language, then he asked whether I know microprocessor/microcontroller etc.

I told him that we will have these in our 6th semester but I went through OS, memory management etc. for this interview what was given in the syllabus of prep for TO interview.

After that, he started asking question from RTOS.

Q. What is mutex and Semaphore?

Ans. Mutex is just a variable which stops a task from entering in to critical section while other task is completing its execution in the same section.

Semaphore is also a counting variable that does the same task but it can allow a definite number of tasks to access the critical section at a time, it can be increased or decreased.

Q. What is binary and counting semaphore?

Ans. Binary semaphore can only take value 0/1 but counting semaphore can take value up to a limit and can be increased or decreased accordingly.

Q. What is difference between mutex and binary semaphore.

I couldn't answer this.

Q. Assume we have two tasks one is printing even numbers and other is printing odd, we want numbers to be printed in sequence write a code using semaphore to implement the same.

Ans. We can use 2 semaphores (se and so) the task even function will wait while task odd is working then it will release the so semaphore signalling that even numbers can be printed and vice versa.

```
se = 0, so = 0; // Defining the semaphores

void taskEven() // task to print even numbers
{
    wait(so);
    printf();
    signal(se);
}

void taskOdd() // task to print odd numbers
{
    wait(se);
    printf();
    signal(so);
}
```

Then he told me the difference that same semaphore (here, se and so) can be accessed by multiple tasks as I did in the code, but the same is not true for mutexes.

At last, he asked do I have any question?

My question: What advice would you give to a fresher like me to perform well and excel in this embedded role?

He told to learn pointers deeply (we should understand how it works, how its implemented) then learning assembly language, microprocessor, microcontroller, ARM etc. as moving forward.

Interview Duration: **55-60 minutes**

Status: **Offered**

Tips for interview: Learn the C language basics very well.

- A deep knowledge of pointers will help a lot. (Yes, I was not asked about pointers but many of my batchmates were asked about function pointers etc.)
- Bit manipulation, Bit masking, intro about RTOS concepts and memory management.
- Don't go blank on any question, keep interacting with the interviewer. Tell him what you are thinking and what can be done.
- Be honest about what you know and what you don't. Don't fake it at all.
- Always, have some question related to the role for interviewer at the end. (It makes interviewer to be sure that you are really interested in the role).

By- **Mohammad Saif Jamal Khan**

ALL THE BEST!!!!

Interview experience for TI - Digital

Interview started with a brief introduction, followed by question based on my project where one was Verilog based project.

Q1) Write a code for Full Adder in Verilog? Some cross question about the code (*basic ones on syntax*).

Q2) Region of operation of MOSFET and its characteristic curve. Followed by what happens when the channel length modulation is considered, the slope at the saturation region and the Y-intercept it will have when extended backwards.

Q3) CMOS inverter characteristic curve. Power calculations of CMOS.

Q4) Static Timing Analysis (*all the terms used in STA should be very clear, they may ask definition of any term*).

Q5) Setup and hold time equations, maximum clock frequency (*prepare them and practice some questions on this*)

Here a circuit was asked and question were such that what will happen if clock skew is added, delay is increased.

Q6) Clock divider circuit (both even division and odd division)

Here you should know what the duty cycle will be in all cases.

Q7) Counter circuits both synchronous and asynchronous.

Q8) Characteristic equation of J-K flip flop, FF conversion from J-K to D and T FF.

Q9) Generating Gate level circuit using Boolean expression. (*Here I was asked a trick question as the Boolean expression reduced to single element*).

Q10) Generating other Gates using Universal Gates.

Q11) Implementing basic Gates using 2:1 Mux.

I had two interviewers, one was highly interested in MOSFETS, CMOS its workings. While other focused on the digital circuits and STA .

Interview was for around 50-60 mins.

You can tell interviewer what you are not comfortable with, its likely that they will give you some hint or may change the question.

If you are wrong also, they always tell you to think again, so take a pause...think...then answer again, no need to panic.

Prepare and Practice well. Best wishes.

Digital :- [polar]

1. Tell me about NMOS. In brief, you know.
(Both depletion and enhancement type)
2. What will happen if we connect body terminal with a higher potential respective to source terminal.
3. What are the different ways to connect the body terminal.
4. Which one is faster, NMOS or PMOS and why?
Different regions of operation of NMOS.
5. (a) Draw band diagram of PN junction even no external source is connected.

(b) A lot of question from the band diagram which is plotted. (like:- amount of bending, what does the gap signify between P & N region, location of fermi level for different amount of doping)
- (c) Why fermi level is flat?
(d) About the electric field (drift & diffusion)
(e) Questions on depletion region
- (f) When we apply a positive potential at P side, plot the Energy band diagram

- (b) why valence band and conduction bands are not flat? why it is tilt in a particular direction?
- (c) why the amount of bending decreases between p & n regions?
 (tips:- Be careful while drawing the fermi level of P and N type when doping varies)
- (d) what is body effect?
 (e) threshold voltage increases due to body effect, so as a designer how will you decrease it as it is undesirable.
- (f) what is mux? draw 4:1 mux using 2 2:1 mux.
- (g) difference between flip flop and latch?
 They asked me to draw J-K f/f using NAND gate. Master slave f/f and how can we get the o/p at positive edge and negative edge.
- (h) basic question on binary and non-binary counter.
- (i) (a) they asked me to draw ring counter.
 (b) they asked me to draw self starting ring counter.
- (j) (a) what is Mealy and Moore state machine?
 (b) which one is faster?
 (c) detect a sequence (1011) using FSM.

(13) Basic questions on pass transistors and
~~CMOS~~ CMOS.

(14) Q They asked me, do you know STA?

→ I said, very basic things about setup
and hold time.

(15) They gave a question based on STA
to find out ~~for~~ of clock

(16) They asked do you know Verilog?

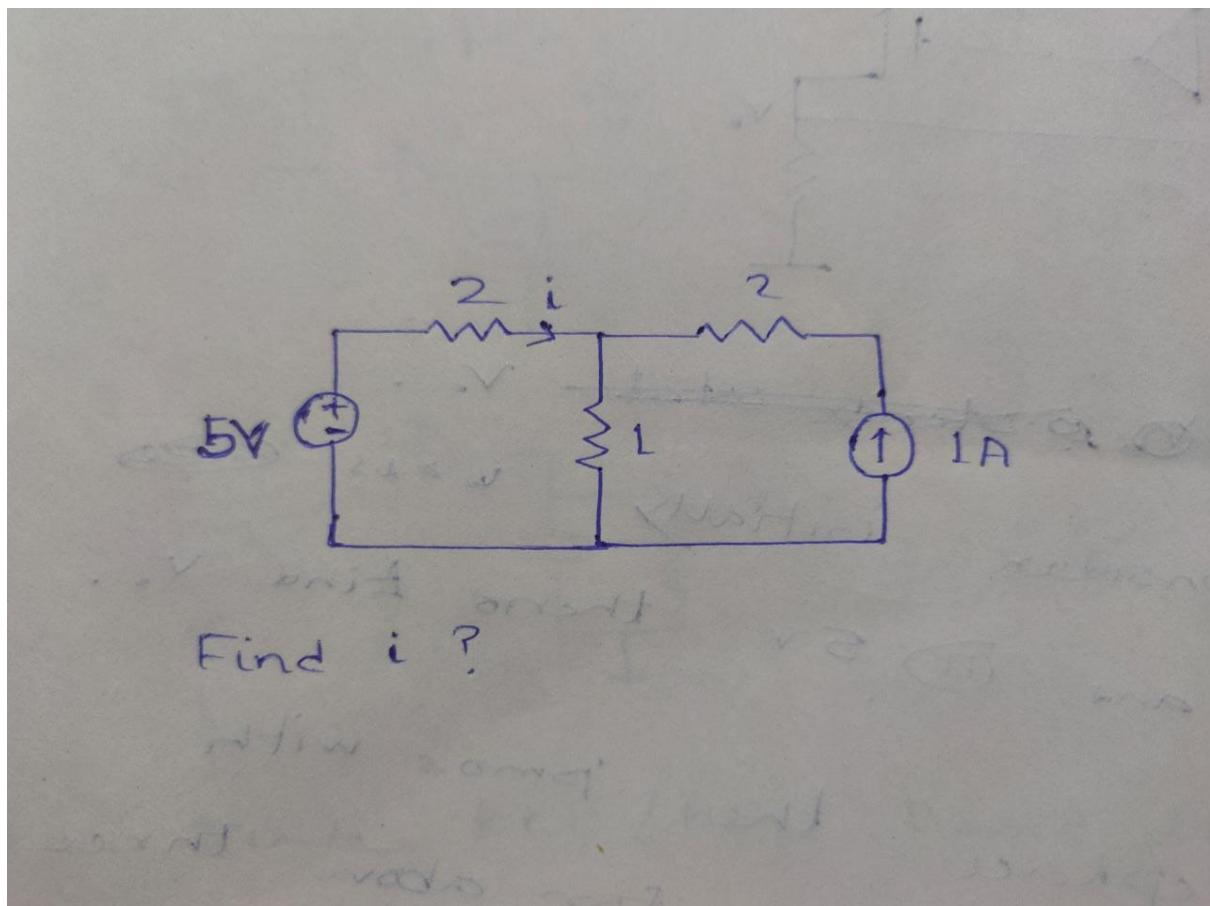
→ I said, no sir. I know very basic of
VHDL.

(17) How will you swap two numbers w/o
using third variable.

Hi, I am Ashim Biswas, UG 4th Year(ETC), IEST Shibpur. Through this pdf I will be sharing my interview experience in TI Analog Design Engineer profile.

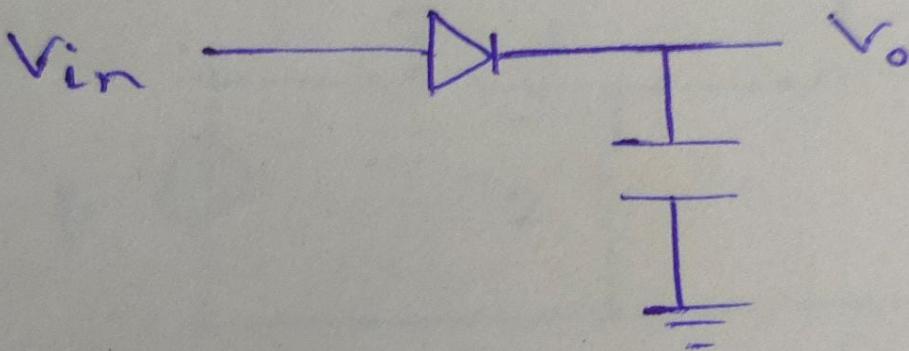
Q.1

Simple KVL/KCL concept based question:



Q. 2

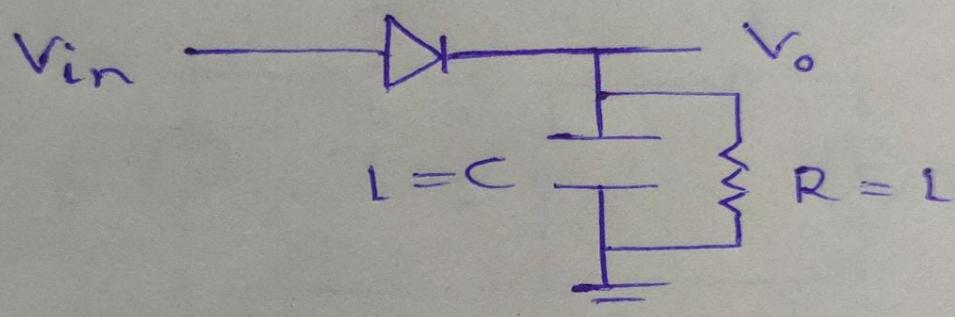
Capacitor Diode based circuit:



$$V_{in} = 5 \sin(\omega t);$$

Plot V_{out} and its steady state value.

Then it was modified with a resistor in parallel with the capacitor.

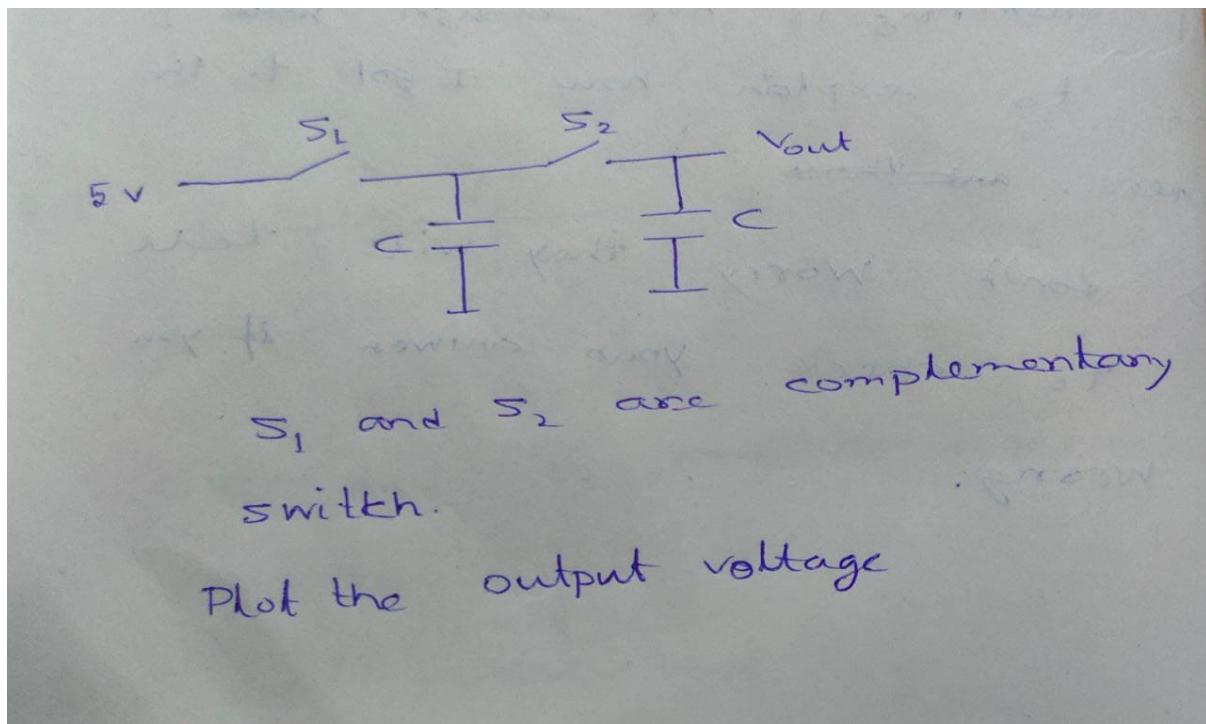


Plot V_{out} and its steady state value.

Q3.

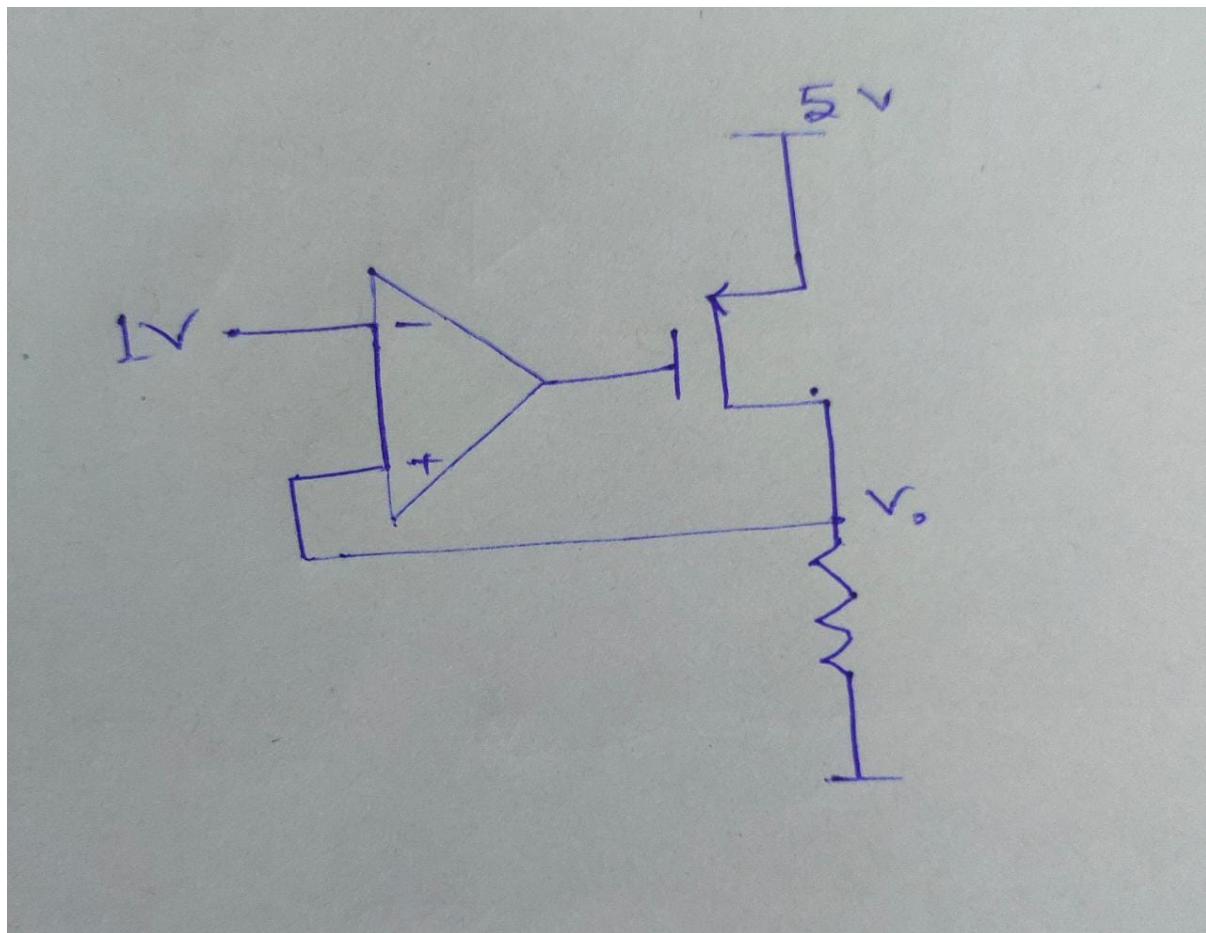
Only Capacitor based circuit:

I don't exactly remember the exact circuit but the question was based on the below given question's concept of capacitor charging and discharging.



There were two/three more questions based on RC circuit, mosfet gain, opamp but I am unable to recall them right now but they were not that difficult.

Final question:



Find which type of feedback is present in the circuit.

Find V_o ?

Then if initially i. $V_o = 2V$ and ii. $V_o = 5V$ what will the steady state value of V_o .

Now, replace pmos with nmos and answers the above questions again.

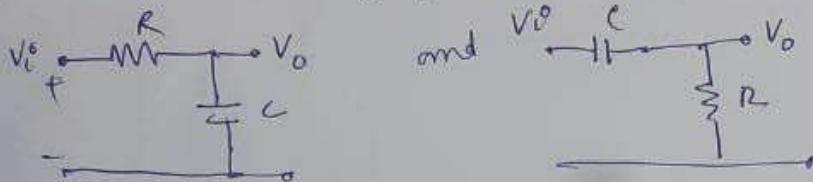
And that's it.

Q> Tell me about yourself.

Q> Asked me to explain about my undergrad research Internship from scratch.

Q> Asked about my image processing course in MATLAB.

Q> RC circuit charging/discharging



For pulse input

(i) $RC \ll T$ and (ii) $RC \gg T$

Do the same for square wave from +10V to -10V.

Q> Follow up question on what will happen if capacitor is initially charged with +10V.

Q> Difference between ideal and non ideal op-amp.

Q> How to determine offset voltage and how to remove it?

Q> What is Boost converter? [couldn't answer]

Q> Simple op-amp circuit with negative feedback.

Q> You have one circular cake. You have to divide it equally between 8 persons with 3 cuts only. How?

Q> There are 10 bags full of identical balls. Each bag has equal no. of balls. One of the bag is full of defective balls and others are good. The defective bag weighs 9 gms and others weigh 10 gms each. You cannot differentiate by holding or seeing the balls. By measuring ONLY ONCE; find which bag has defective balls.

Analog :-

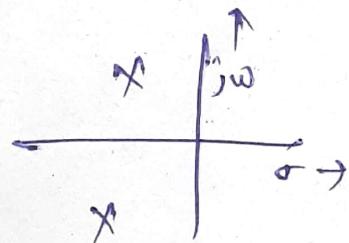
- 1> a) Draw RC high pass filter. (1)
- b) Draw impulse and step signal. (1)
- c) Voltage and current waveform across capacitor and resistor for input step function (1)
- 2> A basic question @ superposition theorem.
- 3> ~~Step and d.c. amplifier~~ (1)
- 3> Time constant for complex RC circuit (1st order) (1)
- 4> Case 1:-) four bulbs are connected in series.
Case 2:-) four bulbs are connected in parallel.
~~In which case, bulb glow brighter and why?~~ (1)
- 5> Disadvantages of ideal Integrator and how we can overcome from this problem? (1)

Texas Instruments FTE: On Campus Hiring
(after PPO rejection)

* Briefly told me to explain my TI project.
It had some use of control system
So, he asked me questions on control systems mainly
on "step response of second order system"

Q. What is underdamped S/S. Draw pole location.
Draw bode plot

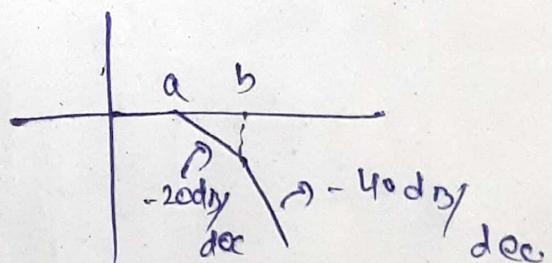
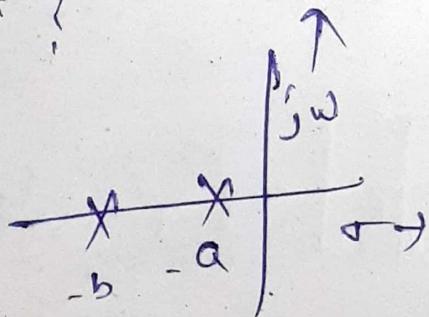
→



Bode plot not possible.

Q. pole-zero location for overdamped S/S and bode-
plot?

→



Q. What happens if we shift pole 'a' in right half
of s-plane?

→ Bode plot not possible.

Q. Simple RC ckt's with step current and voltage input.

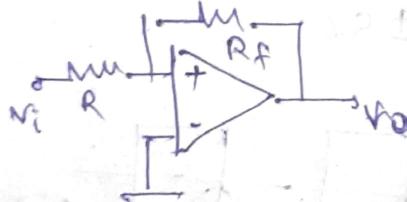
→ Same as YT channels.

Q. Draw ~~as~~ an inverting amplifier and write the gain.

Q. Derive gain formula. Why you have applied virtual ground?

Q. Condition for virtual short

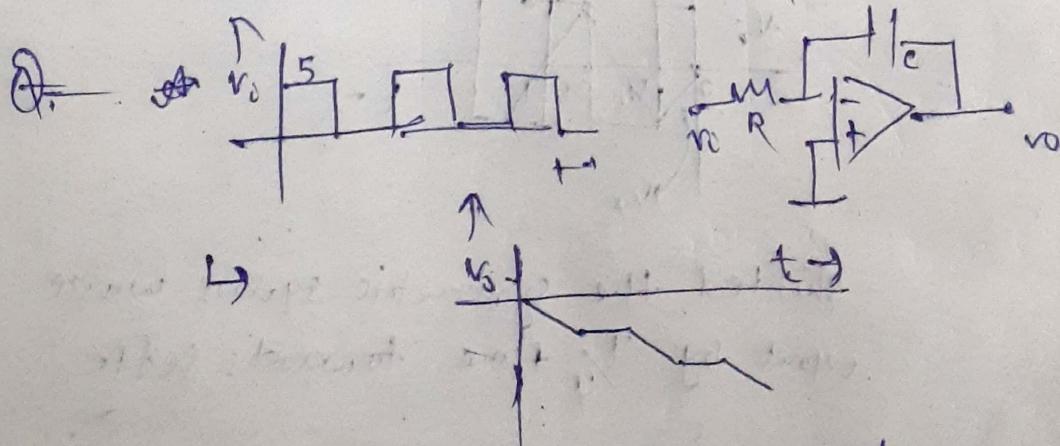
Q. Suppose in this config your polarity is interchanged. What would happen?



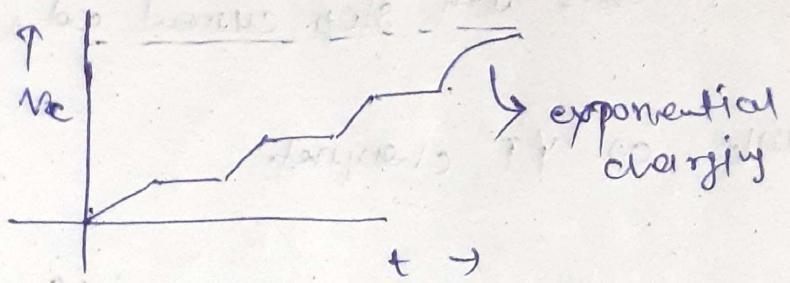
↳ non-inverting schmitt trigger

Q. Analyze the ckt. Draw transfer characteristic. Tell lower threshold voltage (Derivation)

Q. Draw an op-amp integrator. O/P waveform for pulse train input of 5v.



Q. Assume after a certain time, O/P saturates. Voltage waveform across capacitor?



Q. Steady state capacitor voltage?

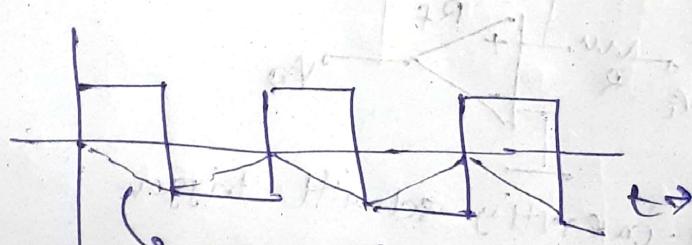
$\rightarrow V_{in} + V_{sat}$

(Detailed explanation: Op-amp integrator

integrator concept by Hinschky (original)

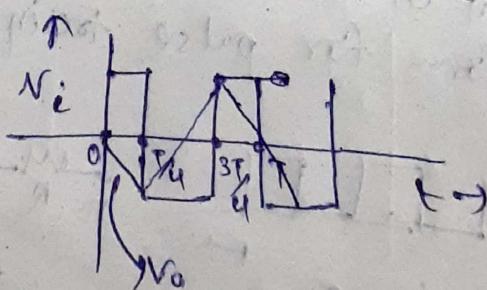
Q. Draw O/P waveform for symmetric square wave i/p of $\pm 5V$

\rightarrow



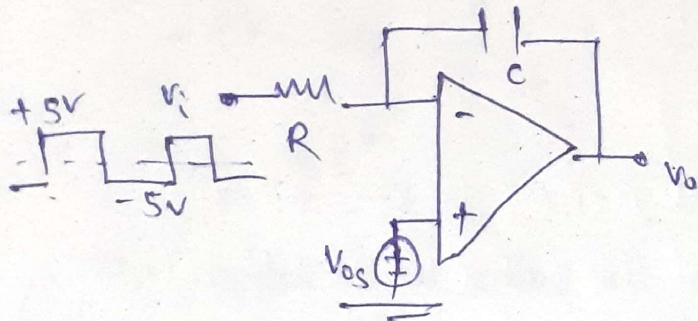
Q. What changes you would make in input to get a symmetric triangular pulse O/P?

\rightarrow



Shifted the symmetric square wave input by $T/4$ time towards left.

Q. Suppose you integrator have some offset voltage and you have symmetric square wave at I/p.



What would be the avg steady state capacitor current?

→ I went on ~~derivation~~ deriving it.

$$= \frac{\frac{5-V_{OS}}{R} \times \left(\frac{T}{2}\right) + \left(-\frac{5-V_{OS}}{R}\right) \frac{T}{2}}{T}$$

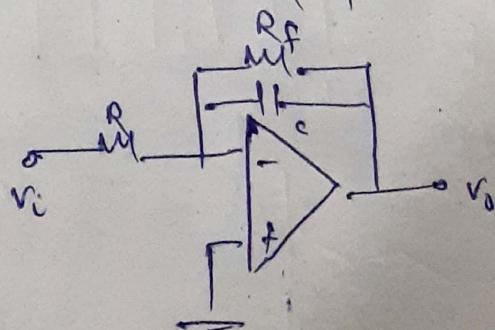
$$= -\frac{V_{OS}}{R} \text{ Aps.}$$

Q. Now what will happen to o/p voltage at steady state?

→ capacitor linearly charge with $\frac{V_{OS}}{R}$ current and o/p saturates.

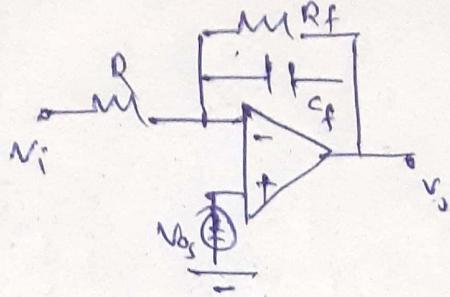
Q. How can we ~~prevent~~ prevent it? Draw ckt?

→ Add a resistor in parallel to capacitor.



Q. Tell how the effect of offset is nullified here.

→

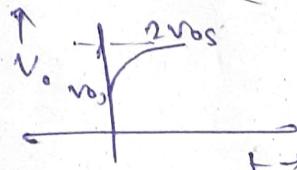


Let's consider the effect of offset only.

$V_i \rightarrow$ Short circuited

$$v_o(0^+) = v_{os}$$

$$v_o(\infty) = 2v_{os} \quad (R_f = R)$$



O/P doesn't saturate.

Q. Swap the values of X and Y without using 3rd variable. Write logic

→ (Couldn't answer in interview)

$$X = X + Y$$

$$Y = X - Y$$

$$X = X - Y$$

Q. Draw a cubicle. An ant is on one corner. It wants to go on the diagonally opposite corner. What is the shortest path?

→ My answer: $(\sqrt{2} + 1)a$

Wrong

Right answer is ₹59

Think about it

Interview duration: 70 minutes.

Status:- ~~Accepted~~. Offered.

BEST WISHES !!

(Also, subscribe to "Himanshu Agarwal")

Digital Interview

Himanshu Agarwal

- ↳ Asked me to introduce myself.
- ↳ Asked me if I'm interested in digital? (Because I forgot to mention digital electronics in my CV. I had put control, analog, EDC, Comm' as my fav sub.)
- ↳ Asked me basic Questions like what is min-term or max term. What is FF and latch. What is the major difference?
- ↳ ~~What~~ Make a S-R latch using NOR Gate.
Write truth Table.
 - ↳ What you should do to avoid "invalid" cod?
 - ↳ (Good Question. Think about it)
- ↳ Asked me de-morgan's theorem and some basic logical expression reduction questions.
- ↳ Asked me some numericals on Flip-Flops.
(Mostly GATE level Questions)
- ↳ Asked me what is a MOS device.
- ↳ Asked me what is body effect
- ↳ Asked me How does body voltage affect threshold voltage.
- ↳ Asked me what's setup time and hold time.
- ↳ He wanted to ask further. I said I'm comfortable with STA numericals and not theory.
- ↳ Asked me to explain charge conservation.
- ↳ Interview duration → 55-60m
status → Rejected!
(I was doing minor mistakes. I should have studied STA deeply. Showed lesser interest towards digital domain)

BEST WISHES!!

Teacher's Sign.

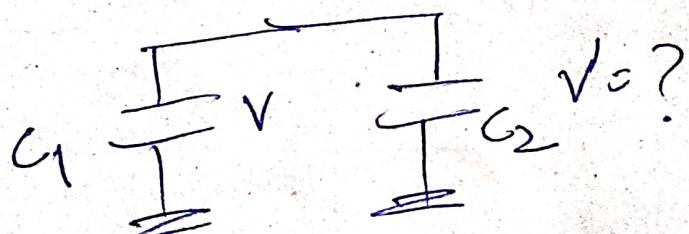
T-I Interview Questions

Q1) There is an ant at one end of the corner and it needs to go to the opposite corner what will be the shortest distance covered by the ant? (Ans: \sqrt{a})

Q2) There are two glass (transparent) and a tap, how will you fill $\frac{3}{4}$ th of the glass? (no scale reading on glass & you can hold the glass).

Q3) There is a digital multimeter and you gotta find the value of resistance using, here the probe also has a resistance, then how will you find the correct resistance?

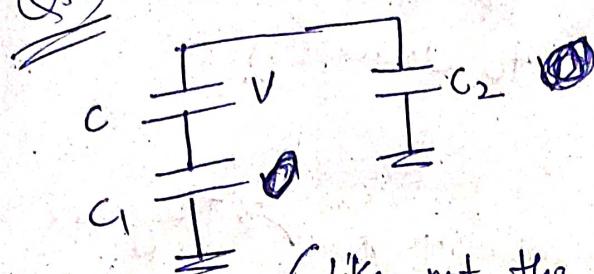
Q4) There are two capacitor C_1 & C_2 (C_1 is charged initially to 'V' volt) then final charge on C_2 is?



{ They will ask the final answer & the correct procedure

Note: Sir also asked what is happening in the circuit and how the relation between C & V (like extreme basics).

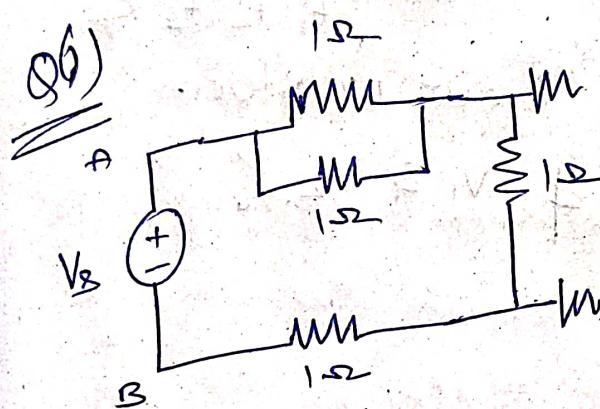
(Q5)



explain how you will solve this problem intuitively?

(Like not the answer, just the procedure.)

(Q6)

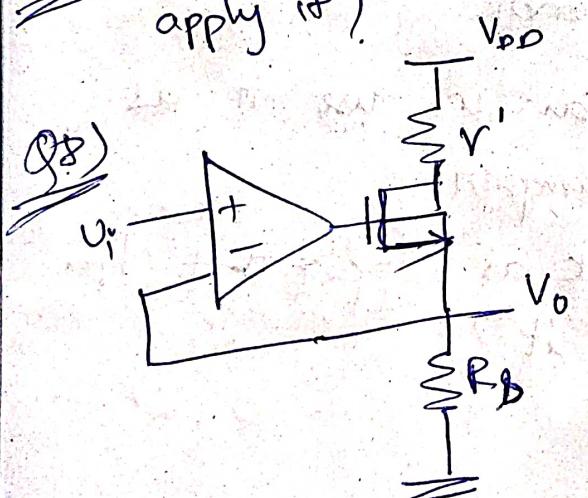


find $R_{eq}=?$ across AB terminals.

(Q7)

what is virtual ground? (when do you apply it?)

(Q8)



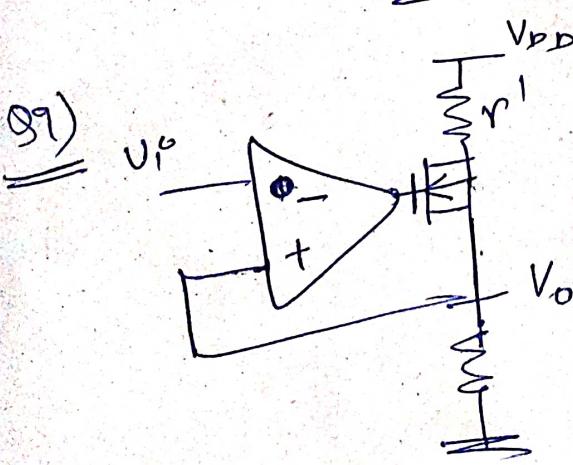
type of feedback?

and how do you analyse it.

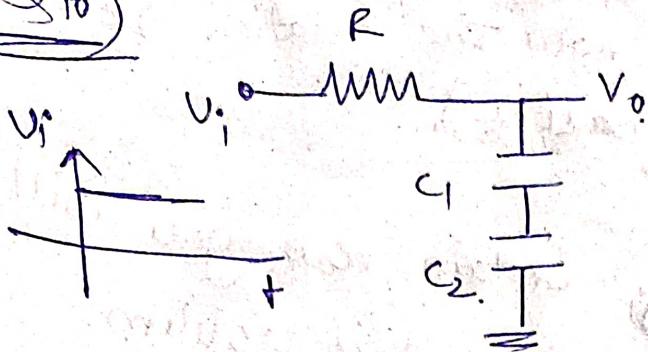
(just the procedure is being checked),

type of feedback?

(Q9)



Q10)

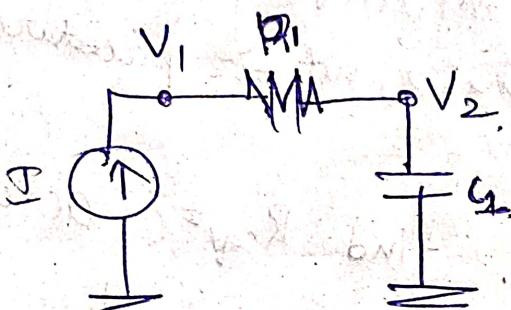


wave form

explanation

(sir did n't ask
to draw).

Q11)



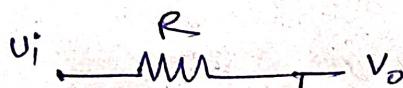
they are uniform

Draw waveform

of V_1 & V_2 ?

Q12)

Zener-diode :



i) Draw V-I curve of zener.

$$6V = \text{Zener Voltage}$$

ii) Can we use it as clumper?

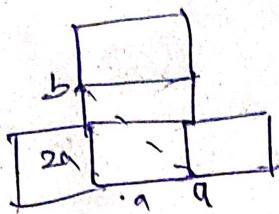
iii) If we want it to work as clipper that clips 30V. How will you do it?

Interview : 40 - 45 min.

Tips: Refer prep for TI - interview series by
Himanshu Agarwal,

Hints & Answers

Q1) Unfold the cube then you can get it



$$AB = \sqrt{4a^2 + a^2} = \sqrt{5}a$$

Q2) fill the glass completely now pour it into another glass so that by comparing it becomes 50%. now similarly by comparing it simultaneously pour the water by changing reference level.



Q3) The reading with resistor: $R+x+y$ (resistance of wires)
Short the wires then check the reading: $x+y$
So actual resistance is $(R+x+y) - (x+y)$

Q4) now initial charge = final charge. ($Q_i = Q_f$)

$$C_1 V = C_1 V' + C_2 V'$$

$$\Rightarrow V' = \frac{C_1 V}{C_1 + C_2}$$

this will be the final voltage across each capacitor.

Q5) Since, the capacitors are in series charge through each and every capacitor is same so we can write V' on C , $\frac{C V'}{C_1}$ on C_1 & $\frac{C V'}{C_2}$ on C_2 then write KVL and get V' .

(Q6) Write KVL or as we know that

$$\frac{V_o}{I} = \text{Req. } \text{So, } V_o - \frac{1}{2} I - I = 0$$

$$\boxed{\frac{V_o}{I} = \frac{3}{2} \Omega}$$

(Q7) When there open loop-gain $\rightarrow \infty$

& negative feedback is present.

then $V_+ = V_-$ this virtual ground.

(Q8) first you increase small amount

of V_i and observe the changes
in circuit accordingly & finally

observe whether V_o is increasing or decreasing
respectively as we increase or decrease V_i .

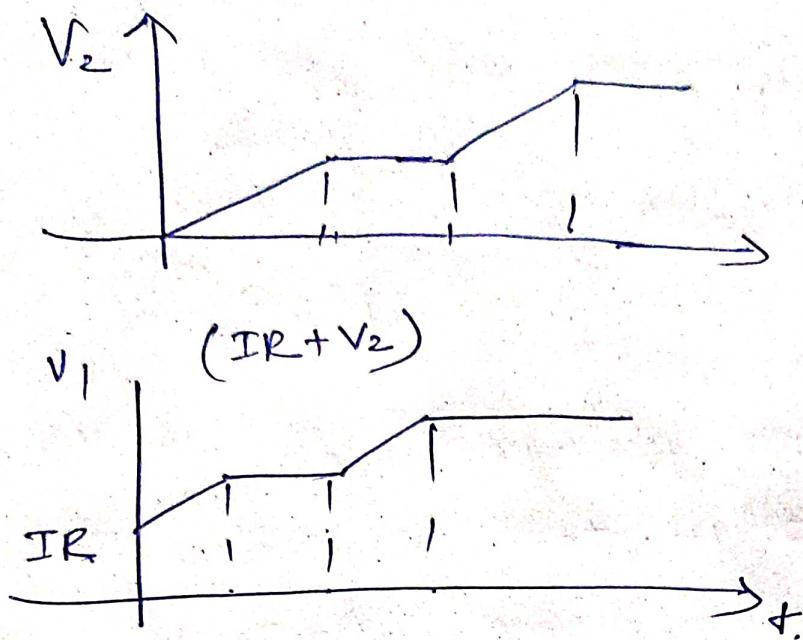
(Q9) like first effective capacitance $\frac{C_1 C_2}{C_1 + C_2}$ then.

at $t=0$ Voltage is zero and it starts increasing

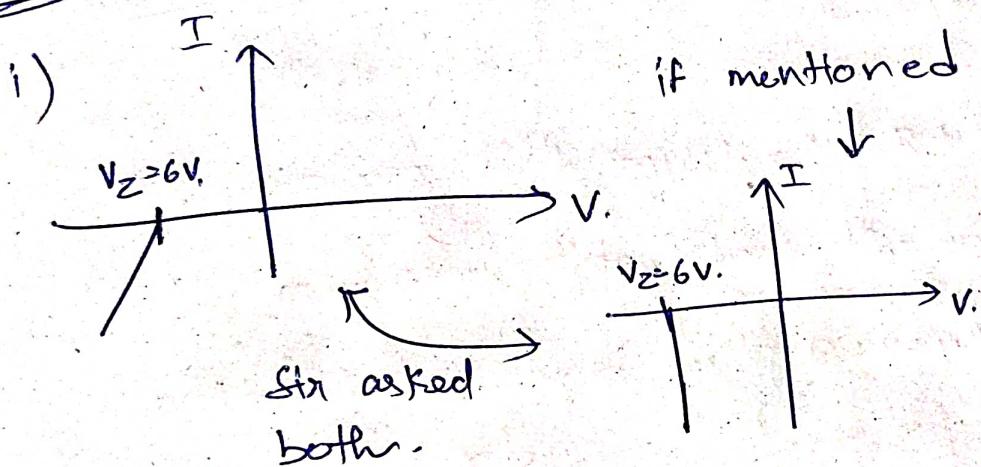
to V_i but C_1 will be charging to $\frac{C_2 V}{C_1 + C_2}$

$$\& C_2 \rightarrow \frac{C_1 V}{C_1 + C_2}$$

Q11)



Q12)



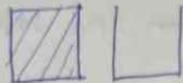
- ii) No, we can use it as clipper only.
- iii) place a battery & it will serve our purpose.

TEXAS INSTRUMENTS ANALOG INTERVIEW

First questions were two Aptitude questions:

- a) You have two identical beakers (with no volume markings) and unlimited supply of water. How will you fill $\frac{3}{4}$ th of the volume with water using these two beakers.

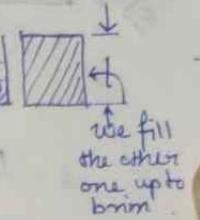
→ I started with filling one of the beakers upto the brim



And then thought about transferring water from the filled to the empty one until both the levels match.



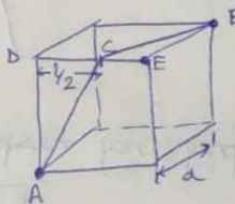
In the same way, we fill $\frac{1}{4}$ th of the beaker.
we have $\frac{3}{4}$ and $\frac{1}{4}$, so after we can drop $\frac{3}{4}$
water from the filled one (using the length $\frac{1}{4}$).
So that $2 - \frac{1}{4} = \frac{3}{4}$



The interviewer said 'its nearly a solution, think about filling the beakers' and moved on to the next question.

- b) You have a cube. An ant wants to move from point A to point B. what will be the shortest path?

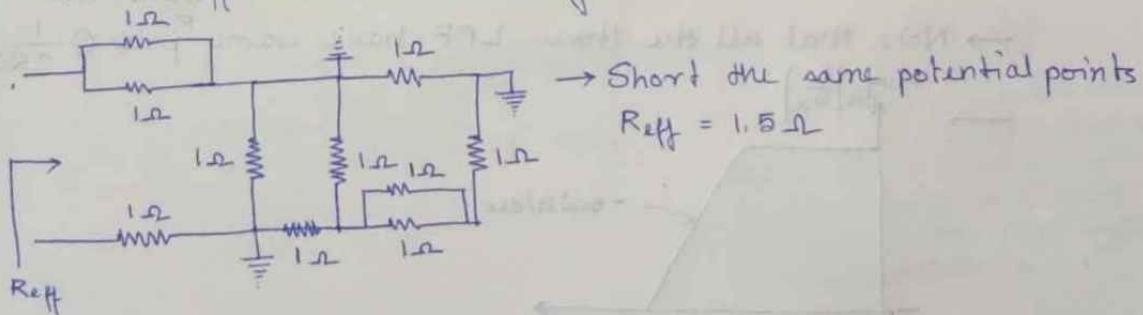
→ A to C and then C to B
[C is the midpoint of side DE]

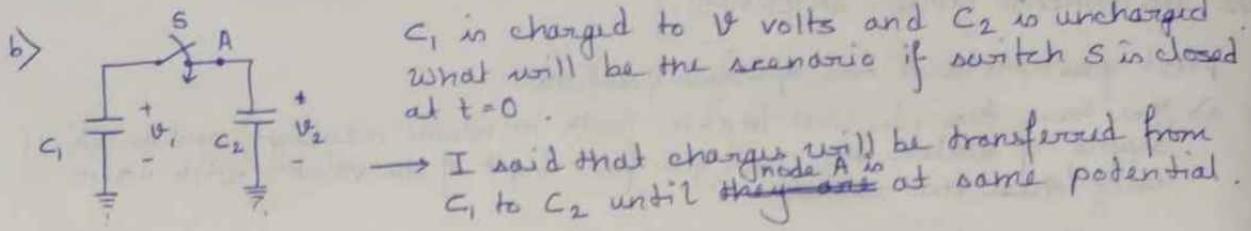


Answer: $\sqrt{5}a$

Next questions were about Network theory, R-C circuits, Zener diode circuits and OPAMP circuits.

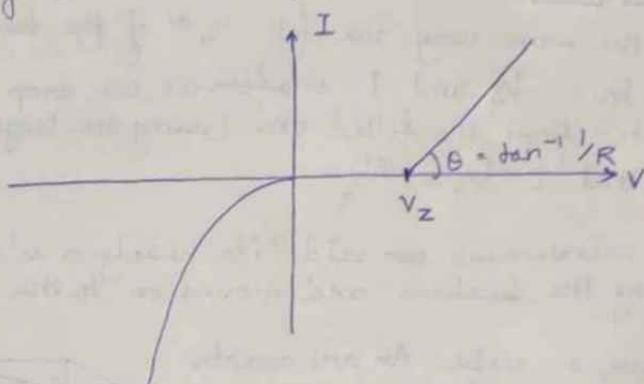
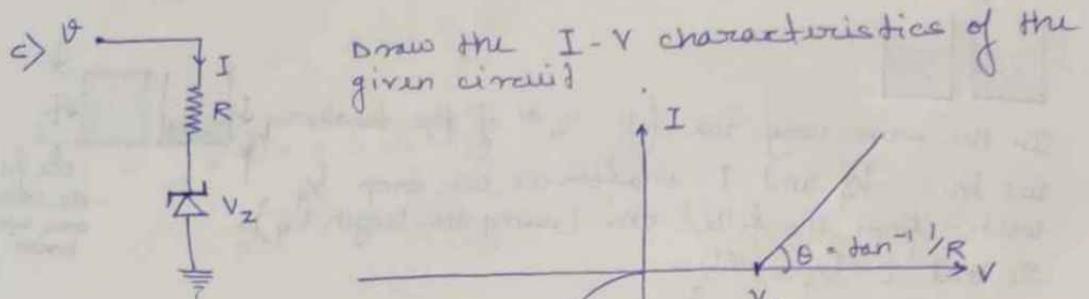
- a) Find the effective resistance of the network:



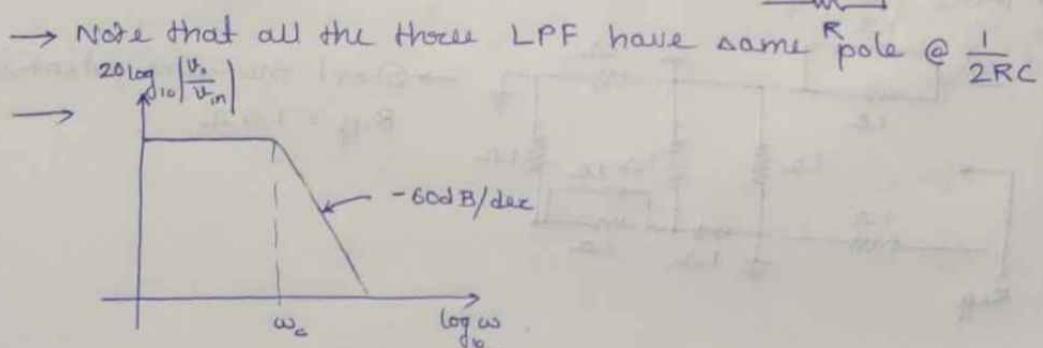
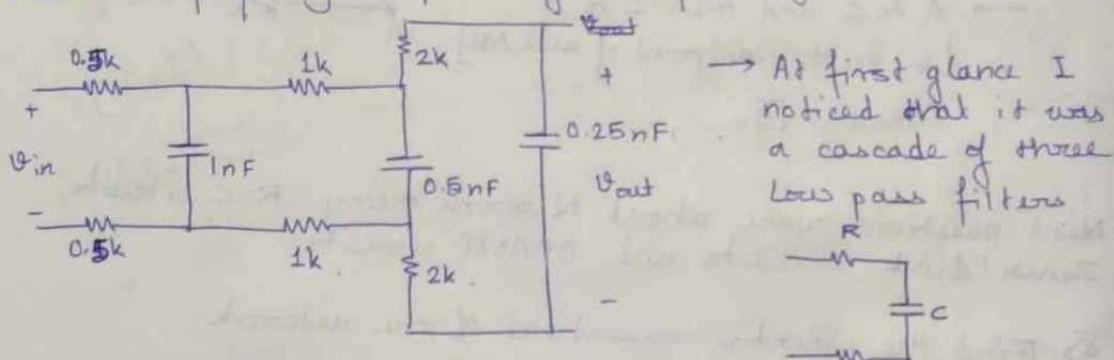


Calculate V_2 at steady state.

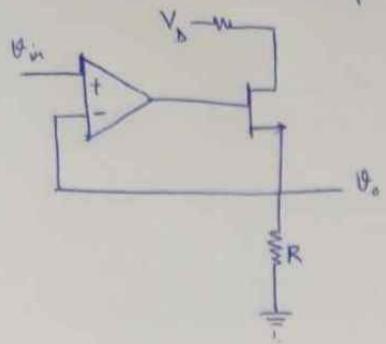
$$V_2 = \frac{C_1}{C_1 + C_2} V \quad [\text{Applying charge conservation and taking } V_{C_1} = V_{C_2} \text{ at SS}]$$



d) Draw the frequency response of the following R-C circuit:



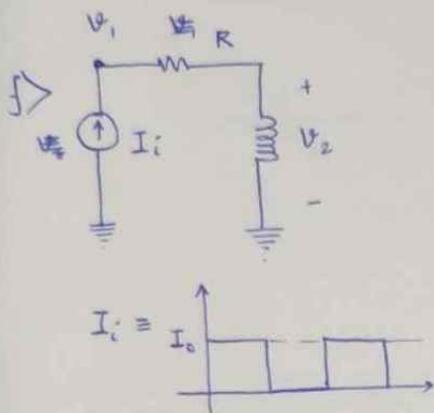
e) Comment about the stability of the following circuit in terms of feedback and what will be the output? Consider ideal OPAMP.



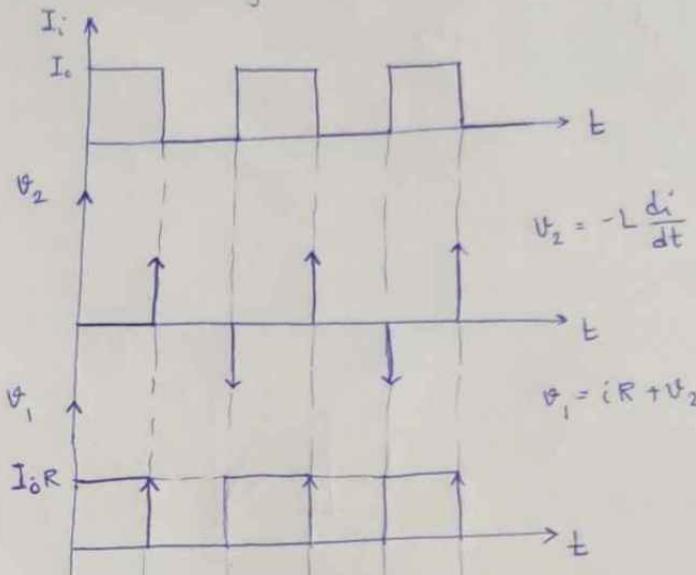
→ First I said that assuming virtual ground, OPAMP is not saturated, $V_{in} = V_o$ (V.G)

Then he asked whether the feedback is +ve or -ve:

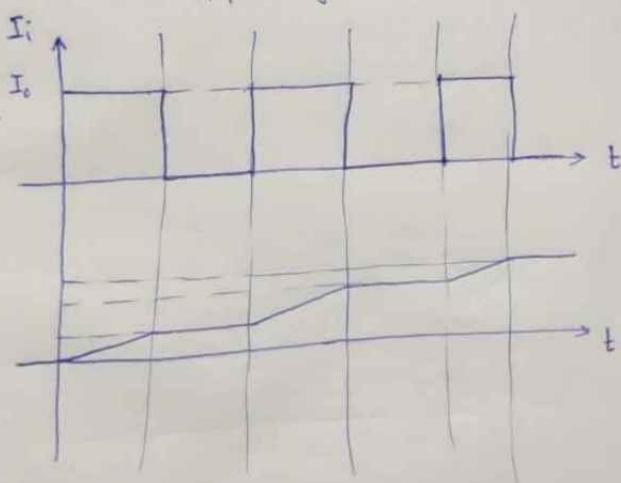
→ I said that since output opposes input, it's a negative feedback



Plot $V_2(t)$, $V_1(t)$ for given I_i :



g) what will happen to V_2 if inductor is replaced by capacitor?



$$q = CV$$

Here for the time when $I = I_0$,

$$V = \frac{1}{C} \int I_0 dt$$

$$V = \frac{I_0 t}{C}$$

Capacitor will charge linearly when $I_0 = 0$, charge will remain same and again increase in the next cycle until breakdown

h) Draw the basic structure of an nMOS and explain pinch off, body effect, origin of capacitances.

→ Took me about 10 mins to explain.