nPOWER ISA Using TL-Verilog

SUBMITTED BY:

Nishant N Nayak	**191CS141**
Addhyan Malhotra	**191CS202**
Shreya Shaji Namath	**191CS249**
Aditya Santhosh	**191CS105**

SUBMITTED TO:

Dr. Basavaraj Talawar **Department of CSE**

COURSE:

Computer Organization and Architecture (CS250)

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,
SURATHKAL - 575025

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Project Description

The nPOWER ISA is a (very small) subset of the POWER ISA v3.0. It is a 64bit ISA . All registers are 64 bits (numbered 0 (MSB) to 63 (LSB)). Our project aims to simulate a processor using Transaction Level Verilog (TL-Verilog), which is an emerging extension to SystemVerilog that supports a new design methodology, called transaction-level design. In this project, we have created a pipelined structure of an nPOWER CPU, which is capable of processing instructions defined in the nPOWER ISA.

The *nPOWER_ISA.tlv* file holds the module definitions for the register file, data memory, instruction memory and the pipelined CPU. Instructions are loaded into the instruction memory, which are then fetched by the CPU. The CPU then decodes the instruction, extracts the relevant fields, checks the validity of those fields and passes these values to the execution stage. The execution stage performs the necessary ALU operation, based on the decoded instruction and data from the register files. The PC value is updated based on whether the last instruction was a branch instruction. Finally, the result is displayed on the waveform and any memory/write-back operations take place.

Block Diagrams

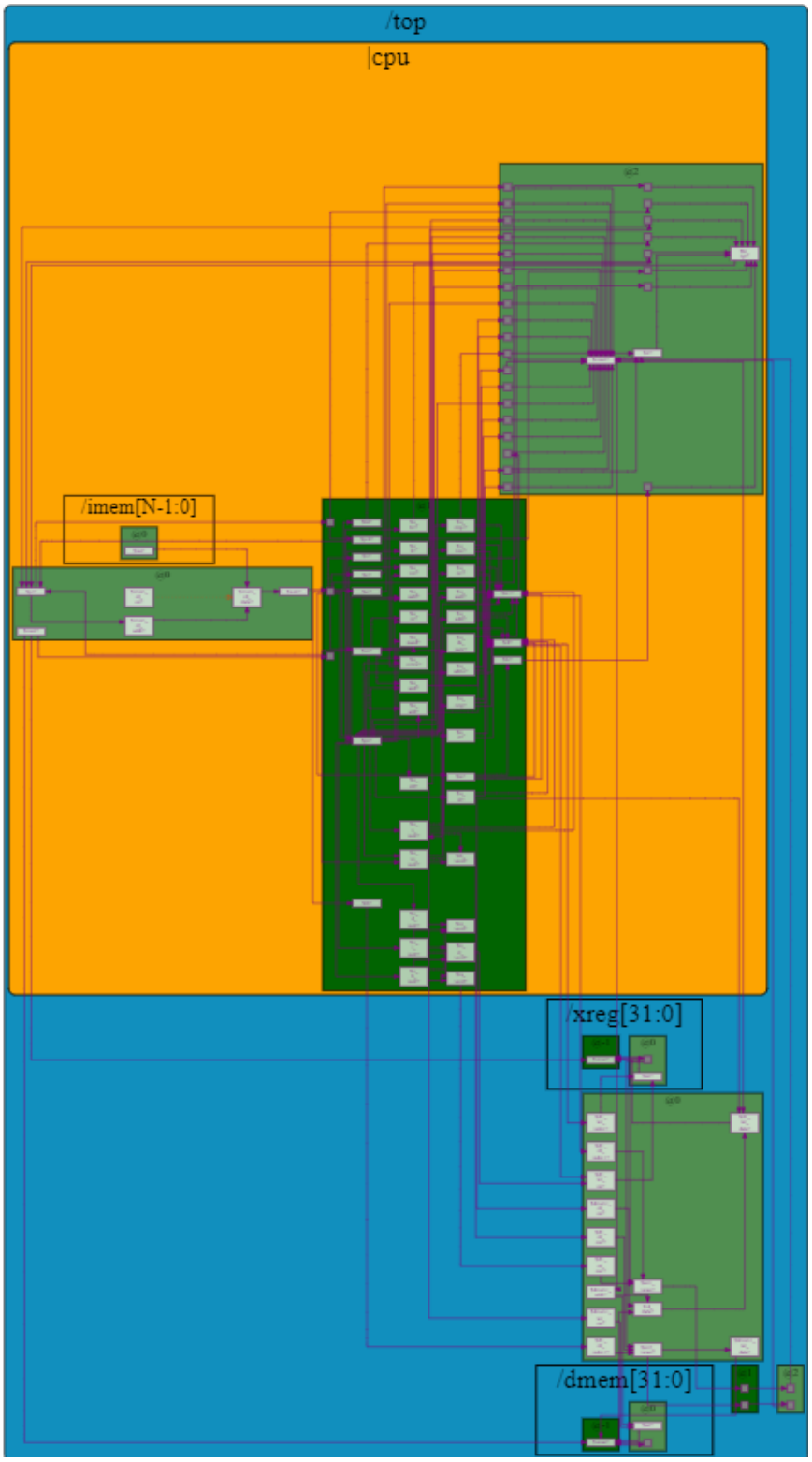

Figure 1: High Level Block Diagram

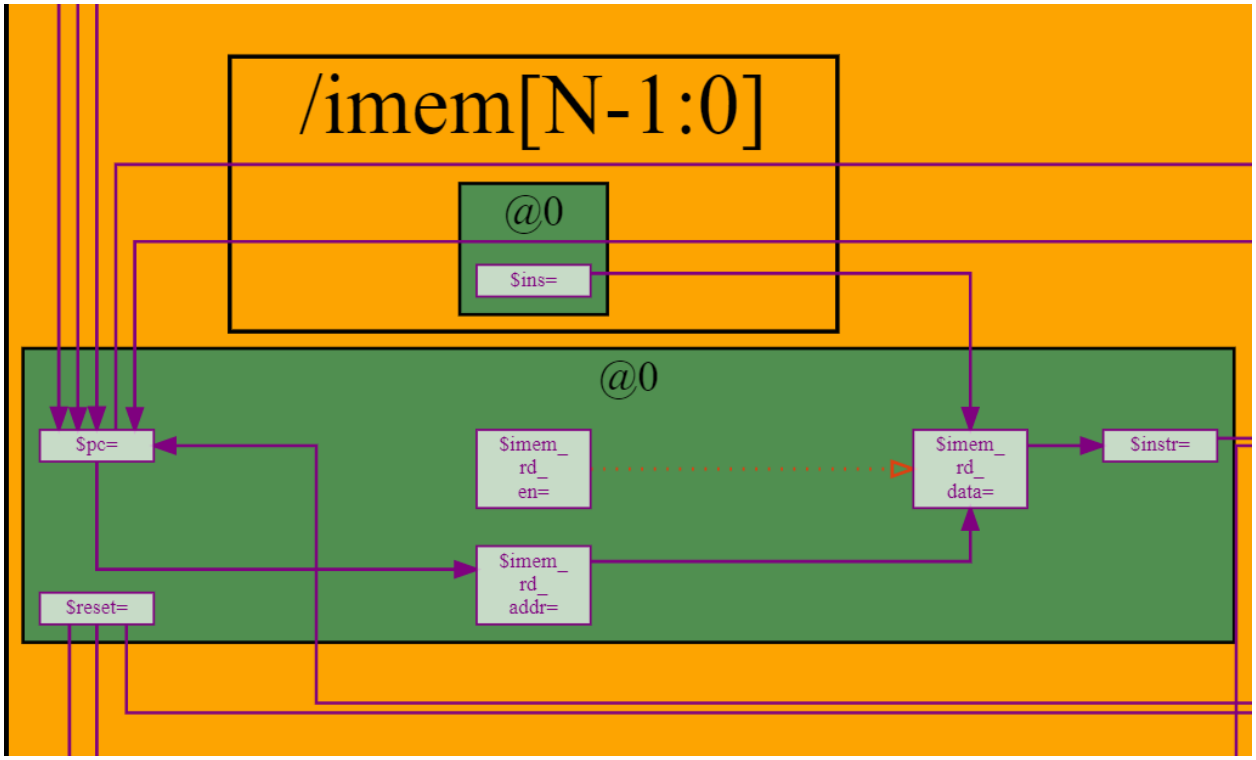

Figure 2: Instruction Fetch Stage

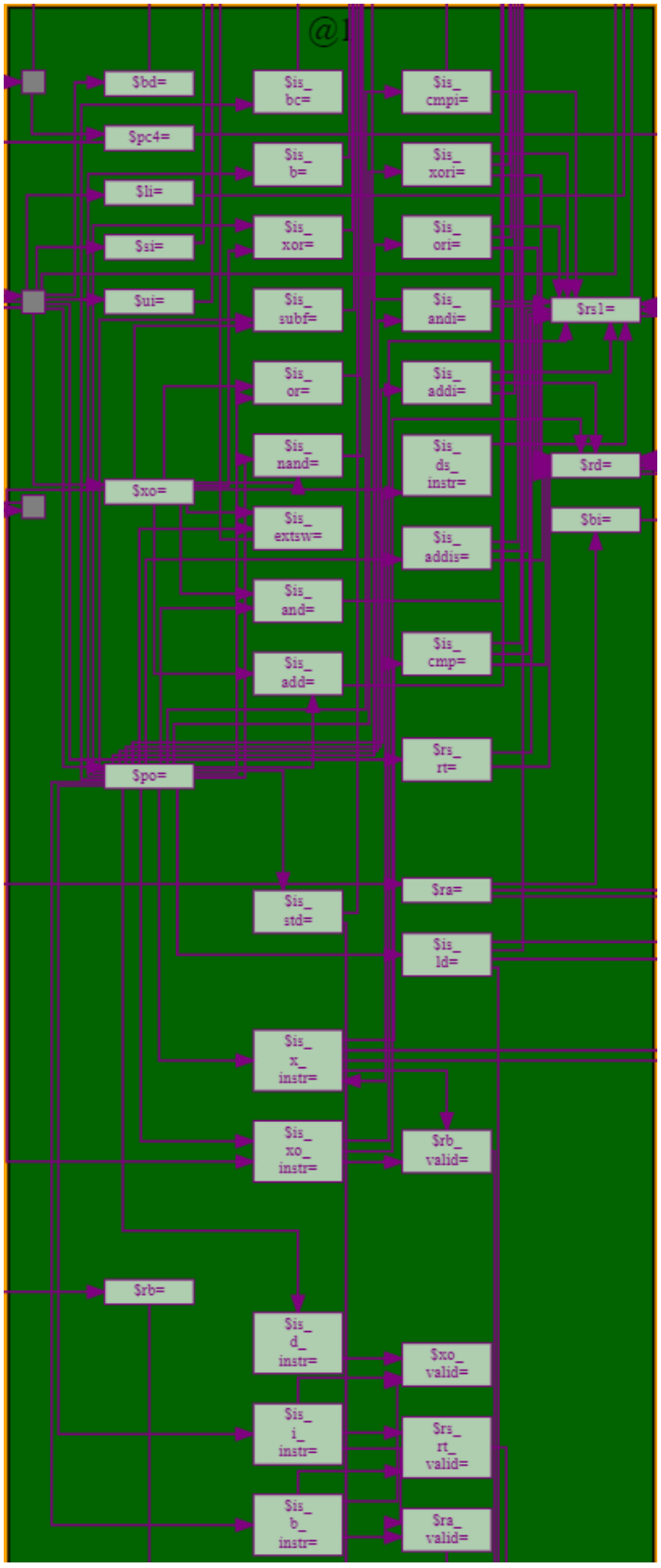

Figure 3: Instruction Decode Stage

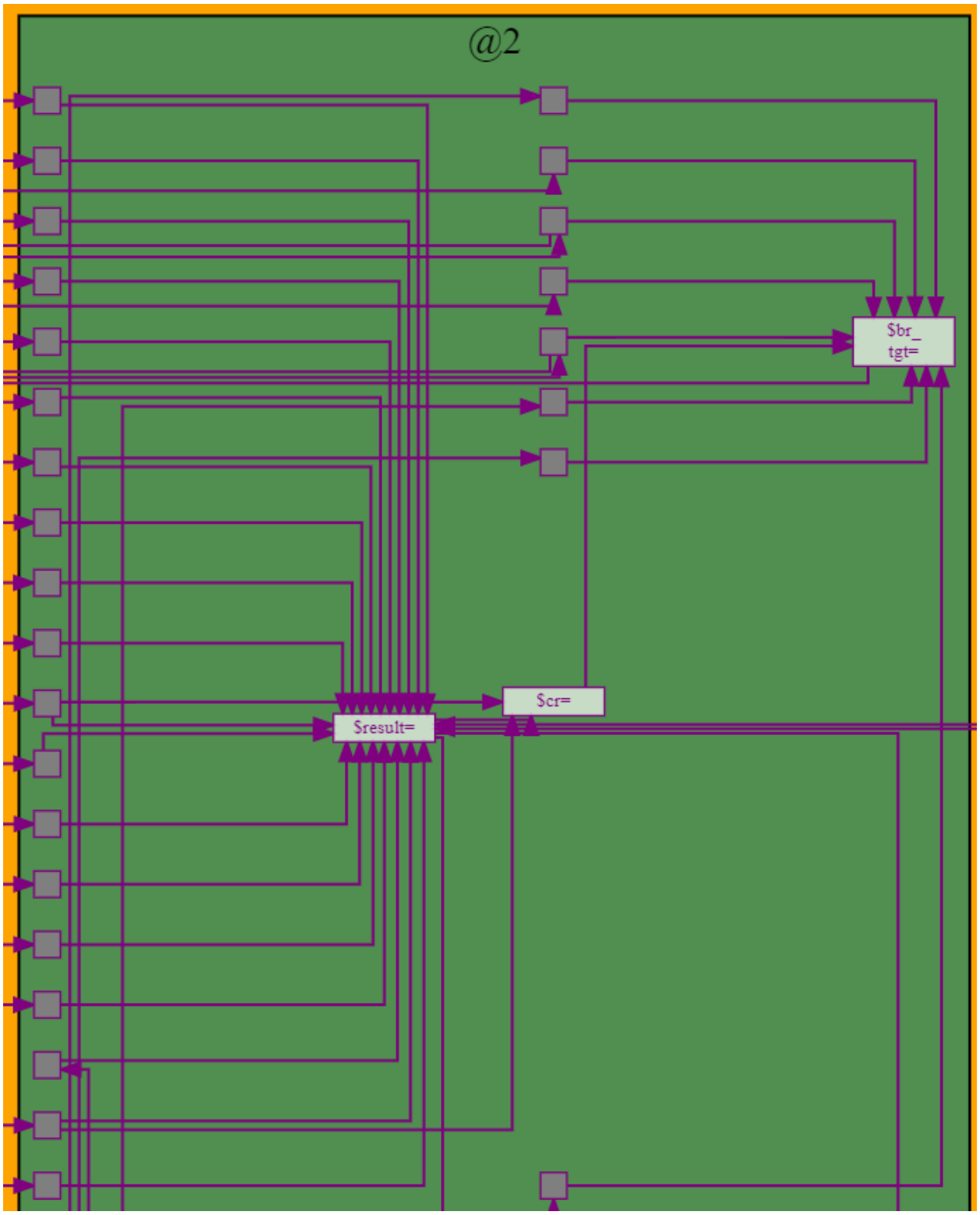

Figure 4: Execution Stage

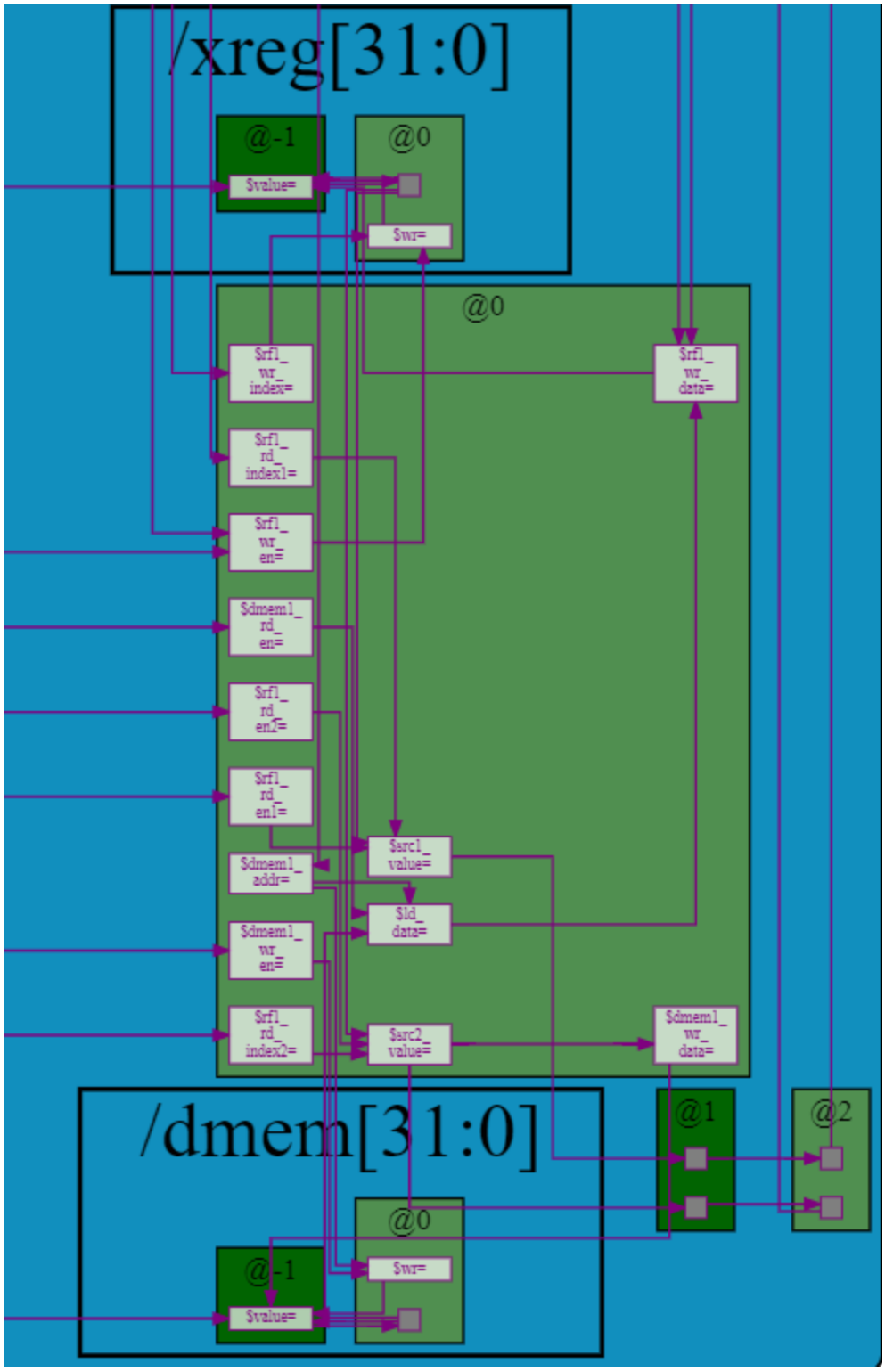

Figure 5: Data Memory, Register File and Top Level Module

Waveforms

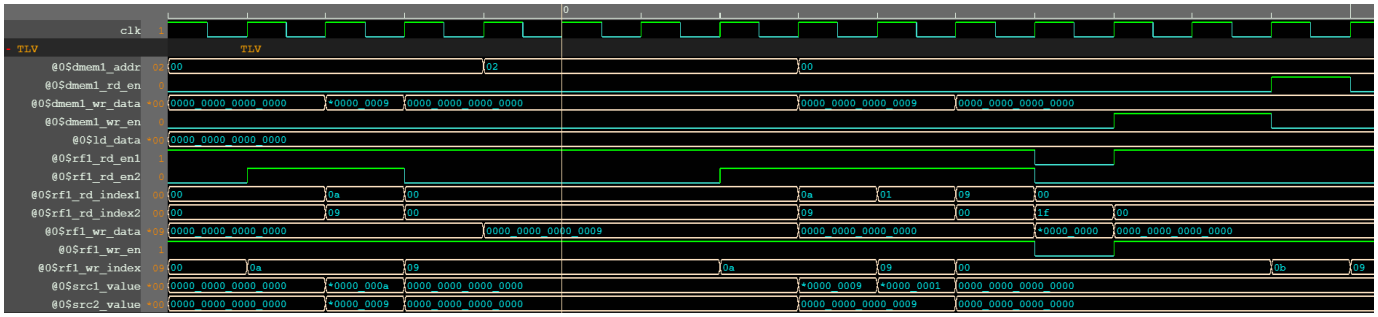

Figure 6: Waveform of clk and TLV signals

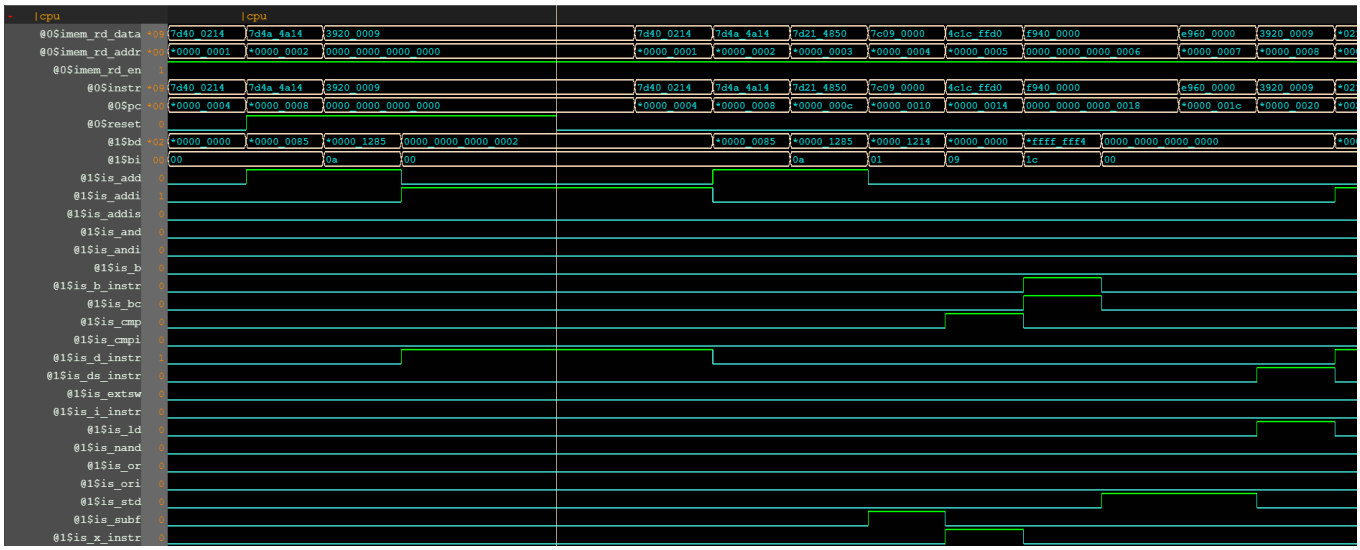

Figure 7: Waveform of CPU Signals (1)

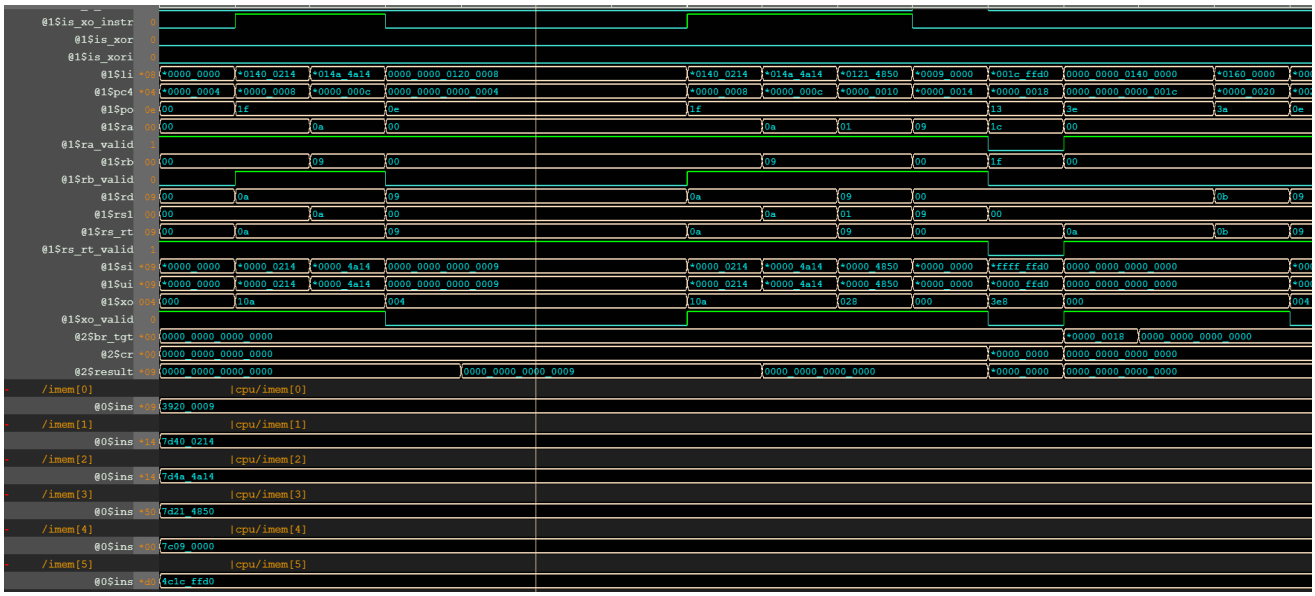

Figure 8: Waveform of CPU Signals (2)

References and Bibliography

- Building a RISC-V CPU Core | edX
- TL-Verilog | Redwood EDA
- OpenPOWER Foundation | IBM Power ISA™ Version 3.0B
- Makerchip