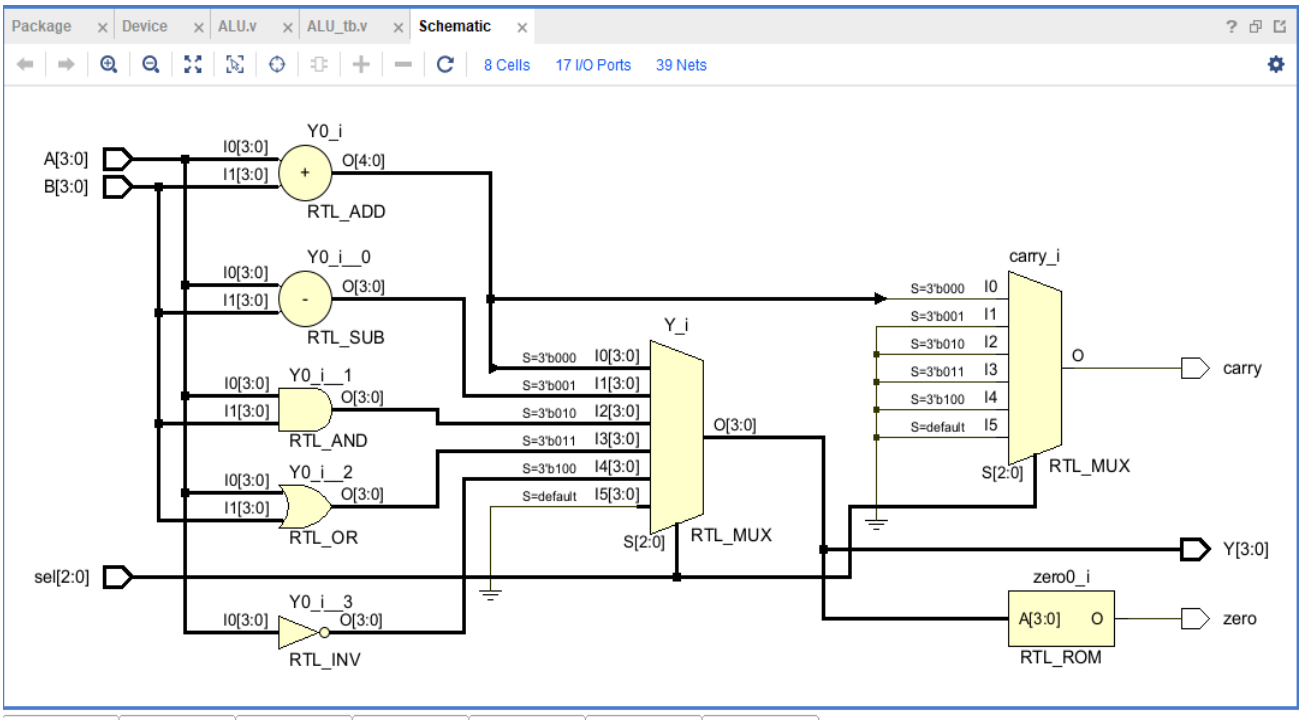
Simulation Report – Basic ALU in Verilog

1. Module Overview

The ALU module performs five basic operations based on a 3-bit selector input:
- Addition (sel = 3'b000)
- Subtraction (sel = 3'b001)
- Bitwise AND (sel = 3'b010)
- Bitwise OR (sel = 3'b011)
- Bitwise NOT (sel = 3'b100)

2. Schematic

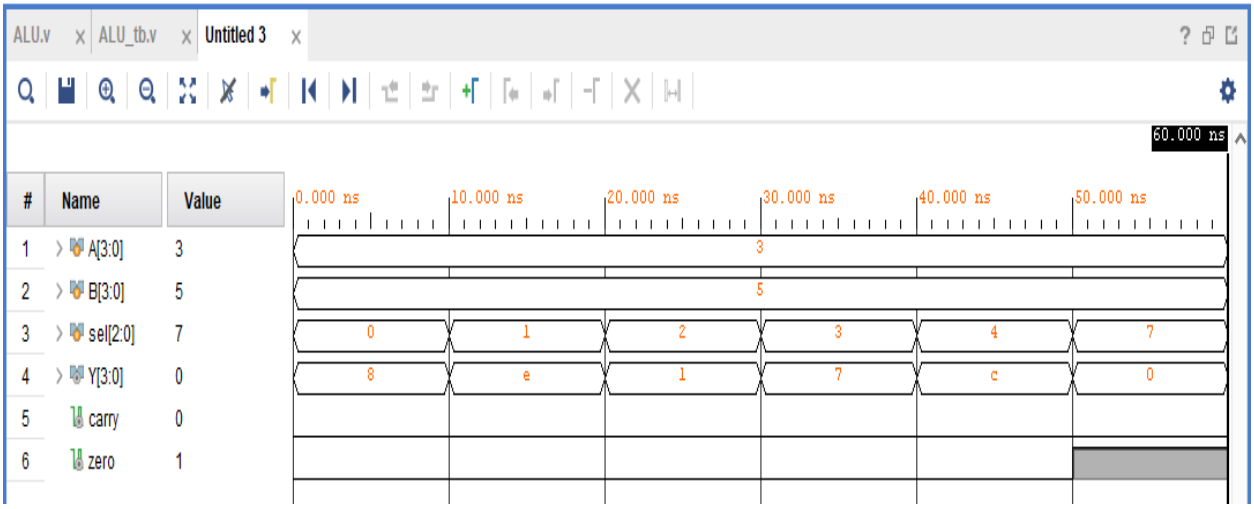


3. Testbench Setup

Inputs:
- Operand A: 4'b0011 (3)
- Operand B: 4'b0101 (5)
- sel values cycled from 000 to 100 to test each function

Simulation Tool: Vivado
Timescale: 1ns / 1ps

4. Testbench waveform



5. Simulation Output

Time (ns)	A	B	sel	Operation	Output Y	Carry	Zero
10	0011	0101	000	ADD	1000 (8)	0	0
20	0011	0101	001	SUB	1110 (-2)	0	0
30	0011	0101	010	AND	0001	0	0
40	0011	0101	011	OR	0111	0	0
50	0011	xxxx	100	NOT A	1100	0	0
60	0011	0101	111	Default/Idle	0000	0	1

6. TCL output

```
# run 1000ns
A=  3, B=  5, Select= 0 | Output=  8, Carry= 0, Zero Flag= 0
A=  3, B=  5, Select= 1 | Output= 14, Carry= 0, Zero Flag= 0
A=  3, B=  5, Select= 2 | Output=  1, Carry= 0, Zero Flag= 0
A=  3, B=  5, Select= 3 | Output=  7, Carry= 0, Zero Flag= 0
A=  3, B=  5, Select= 4 | Output= 12, Carry= 0, Zero Flag= 0
A=  3, B=  5, Select= 7 | Output=  0, Carry= 0, Zero Flag= 1
$finish called at time : 60 ns : File "D:/Xilinx/vivado codes/ALU 1/ALU 1.srcs/sim 1/new/ALU tb.v"
```

4. Observations

- The ALU correctly performed all operations.
- The zero flag was asserted when the output was 0000.
- No overflow or unexpected behavior occurred in 4-bit operations.
- The NOT operation uses only operand A.

5. Conclusion

The simulation validates that the ALU performs the required operations correctly. This implementation is suitable for integration into a larger CPU or as an educational reference for combinational logic design.