Nishant Gurunath

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Education and Work Experience

Jul 2011 - Aug 2016 — **Indian Institute of Technology Bombay**, Mumbai, India
B.Tech in **Electrical Engineering**
M.Tech in **Microelectronics**
Minor in **Computer Science and Engineering**
Major CGPA: **8.57/10** (Combined for B.Tech and M.Tech)

Jul 2016 - Present — **Texas Instruments India Pvt. Ltd.**
Digital Hardware Design R&D
Microcontrollers Business Division

Publication

Saurabh Pandey, Venkatseema Das, Arif Mohammed, **Nishant Gurunath**. "Simulation Based Pre-Silicon Characterization" DVCON - Design and Verification Conference and Exhibition, Bangalore, 2014. Link

Master's Thesis

Apr 2015 - Jun 2016 — **Artificial Neural Network Acceleration over Network-On-Chip**
Guide: Prof. Sachin Patkar, *Department of Electrical Engineering, IIT Bombay*

Background FPGA based hardware implementation for testing phase of artificial neural networks(ANN) could benefit a lot of real-time applications such as diagnostics of high speed aeroplane or video analysis in autonomous cars. In this work, we propose a design time programmable generic hardware architecture for feed forward ANNs. Link to Thesis

Results

- Proposed a programmable FPGA compatible design to ensure scope for **re-learning** in ANNs
- Eliminated the clutter due to connections among neurons by adopting a *Network-On-Chip* based architecture and making it feasible to fit a complex ANN system on a **single FPGA**
- Efficiently utilized the inherent parallelism present in the each layer of ANN and pipelined the architecture to reduce latency **50 folds**; devised a scheme for efficient resource utilization
- Demonstrated that the performance(CPPS) of the proposed architecture is better than most of the existing commercial devices using the same amount of resources

Ideology Extension

- Applied the FPGA programmable NoC based architecture to accelerate logic simulation and applied the concepts of graph theory to increase the efficiency of the architecture

Industrial Experience

Jul 2016 - Present — **Digital IP Design and SoC Integration**
Microcontroller Business Division, Texas Instruments India Pvt. Ltd.

Details

- Worked on more than 10 IPs, integrated a subsystem and evaluated multiple design tools
- Integrated the **first** ever ARM core based subsystem for the team; **first** IPXACT based integration; automated the entire design generation; **fewer than 10** integration bugs
- Designed data translation bridges to reconcile data across third-party and in-house protocols, across asynchronous clock domains and across faster to slower clock domains
- Implemented synchronization schemes to transfer data across asynchronous clock domains
- Proposed design techniques to support Design For Testability(DFT) at system level
- **First** in the team to design a digital control block and lock generation logic for the PLL; chalked down the DFMEA document to identify possible failures and risks in the design
- Performed simulation, lint, clock domain crossing, DFT and LEC checks to ensure quality

May 2014 - Jul 2014 — **Simulation Based Pre-Silicon Characterization (Internship)**
Microcontroller Business Division, Texas Instruments India Pvt. Ltd.

Details

- Performed timing analysis using RTL simulation to determine setup and hold time requirement prior to the static timing analysis(STA)
- Developed a module that adds the user provided delay to the signal and thereby, stressing the timing margins of flip-flops; module is adaptable to verification of all the processors
- Obtained 99% accuracy using the proposed method in verification of data sheet timings
- Received a **Pre-Placement Offer** in recognition of the impact of the above contributions

R&D Projects

May 2013 - Jul 2013 **Offshore Wind and Wave Renewable Energy Solutions as Live Data Repositories – The Potential of Wireless Sensor Networks (WSN)**
Guides: Dr. Vikram Pakrashi *Director, Dynamical Systems and Risk Laboratory, University College Dublin* and Dr. Emanuel Popovici *Electrical and Electronic Engineering, University College Cork*

Details
- Proposed WSN as a potential solution to the problems of offshore wind and wave energy farms; used sensor data to harness energy efficiently and monitor marine life
- Implemented a star topology wireless sensor network communication between a base station (receiver) and 5 end devices (sender) in both unicast and broadcast fashion
- Devised an experiment to characterize a mini wind turbine; obtained a closed form expression of wind energy as a function of intensity, angle and time using MATLAB with **99.5%** accuracy
- Received a **letter of excellence** in recognition of the impact of above contributions

Aug 2014 - May 2015 **VLSI Testing –Output Compactor**
Guide: Prof. Virendra Singh, *Department of Electrical Engineering, IIT Bombay*

Details
- Worked on scan-chain output compactors for VLSI testing to reduce test data volume
- Devised a Masking-cum-Compaction strategy, that can tolerate unknown (X) values to scan-chain inputs with negligible design overhead; **10 fold** increase in compaction and speed
- Proposed a scheme to efficiently utilize all tester channels, thereby increasing scan-chain output observability by **90%**

Artificial Intelligence Projects

Spring 2016 **T-20 Cricket : Match Predictor** | Foundations of Machine Learning
Instructor: Prof. Ganesh Ramakrishnan
- Identified representative feature set for predicting the match result and mined the required data to create the training data set
- Used the AdaBoost algorithm for training and obtained an accuracy of 83.5% on the test data

Spring 2013 **TIC-TAC-TOE** | Digital Systems Lab
Instructor: Prof. Mahesh B. Patil
- Implemented a state machine based algorithm to impart intelligence to the game
- Created a matrix of LEDs to represent Os and Xs and used keyboard interface for gameplay

Academic Achievements

- Scored a Grade Point Average of **10.0/10.0** in both the semesters of final year project at IIT Bombay
- Secured All India Rank of **250 in IIT JEE 2011** among **500,000** aspirants
- Secured All India Rank of **454 in All India Engineering Entrance Examination(AIEEE) 2011** among a **million** aspirants
- Awarded certificate of merit for nationwide top **1% in Indian National Chemistry Olympiad 2011**

Academic Services

Teaching Assistant
EE 677: Foundation of VLSI CAD *Autumn 2015*
EE 224: Digital Systems *Spring 2016*

Relevant Coursework

Computer Science	Computer Programming and Utilization, Data Structures and Algorithms, Foundations of Machine Learning, Computer Networks, Graph Theory
Mathematics and Statistics	Data Analysis and Interpretation, Calculus, Linear Algebra, Ordinary and Partial Differential Equations, Complex Analysis, Probability and Random Processes, Advanced Computing

Technical Skills

Languages	C++, Python, SQL, HDL
Packages	MATLAB, Scilab, LaTeX
Hardware	Ngspice, LTspice, RC Compiler, Spyglass, Magillem