Description of Basys 3 FPGA Board

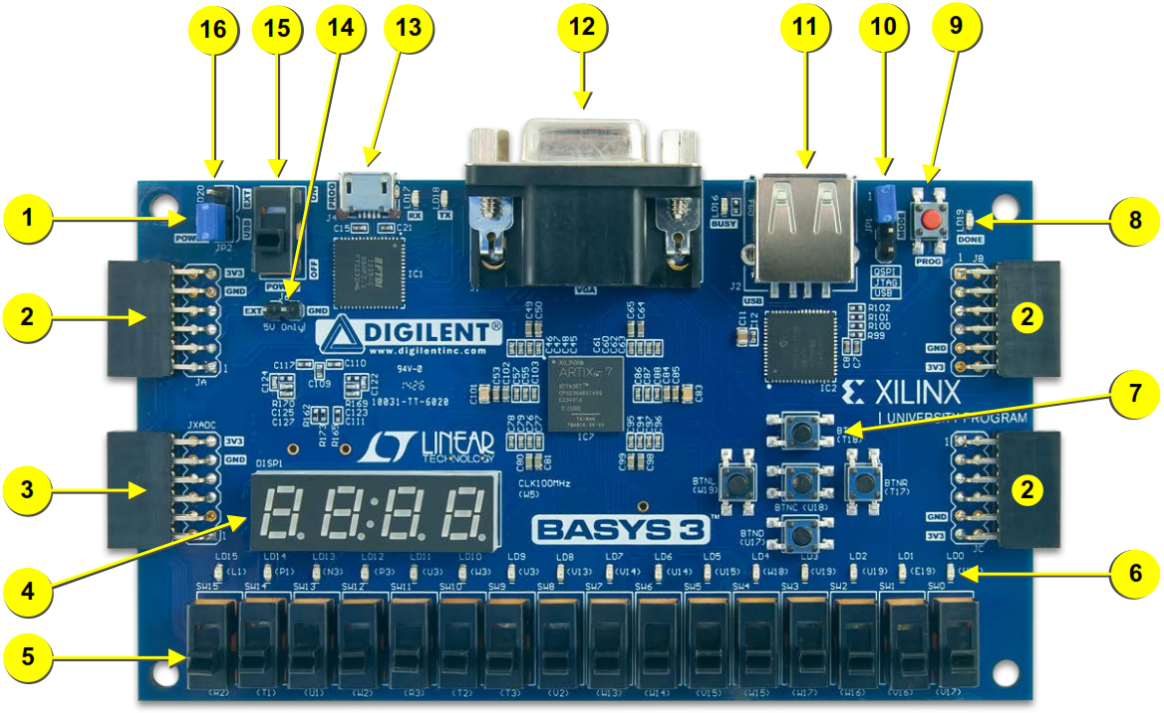
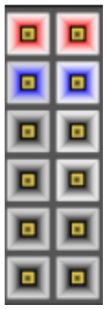
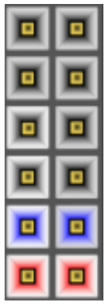


Figure 1: Board with callouts

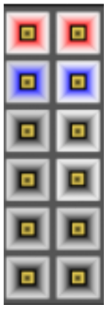
Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod connector(s)	10	Programming mode jumper
3	Analog signal Pmod connector (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power switch
8	FPGA programming done LED	16	Power select jumper

JA12:PWR		JA6:PWR
JA11:GND		JA5:GND
JA10:G3		JA4:G2
JA9:H2		JA3:J2
JA8:K2		JA2:L2
JA7:H1		JA1:J1

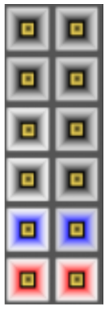
Pinout Detail for Pmod A (Upper-Left)

JB1:A14		JB7:A15
JB2:A16		JB8:A17
JB3:B15		JB9:C15
JB4:B16		JB10:C16
JB5:GND		JB11:GND
JB6:PWR		JB12:PWR

Pinout Detail for Pmod B (Upper-Right)

JXADC12:PWR		JXADC6:PWR
JXADC11:GND		JXADC5:GND
JXADC10:N1		JXADC4:N2
JXADC9:M1		JXADC3:M2
JXADC8:M3		JXADC2:L3
JXADC7:K3		JXADC1:J3

Pmod Detail for XADC (Lower-Left)

JC1:K17		JC7:L17
JC2:M18		JC8:M19
JC3:N17		JC9:P17
JC4:P18		JC10:R18
JC5:GND		JC11:GND
JC6:PWR		JC12:PWR

Pinout Detail for Pmod C (Lower-Right)

Figure 2: Pinout Detail Schematic for Basys3 FPGA Board with location on Basys3 board

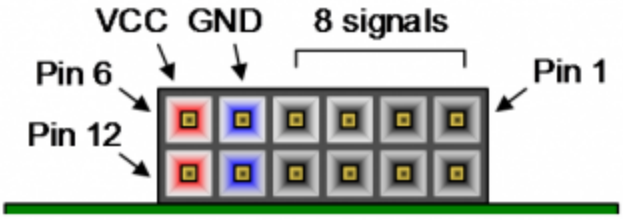


Figure 3: Generic Pmod for Basys 3

Basys3 configured as a "Digital Controller"

On the Canvas page is a file, "DigitalControllerTop.bin"/"DigitalControllerTop.bit" that will convert your Basys3 FPGA board into a discrete logic evaluation tool (see Appendix C, part III for the procedure to use this file). Your Digital Controller includes basic functions like Inputs (switches), Outputs (LEDs), a counter, and an adjustable rate clock with start/stop/step features.

The inputs and outputs utilize the PMOD connectors on the sides of the Basys3 as shown below:

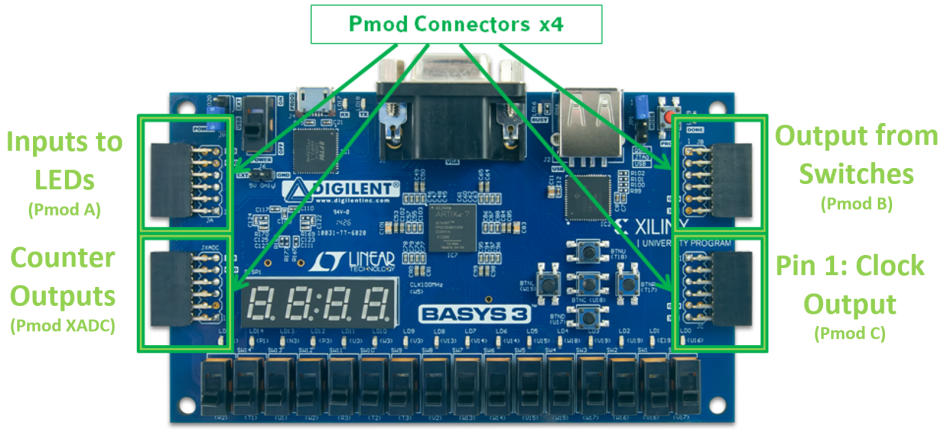
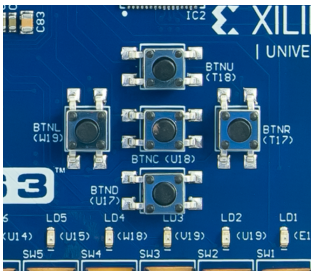
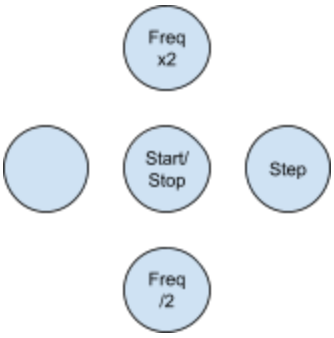


Figure 4: FPGA Digital Box Pin Definitions and General Functions

The cross of buttons, shown below, control the clock and counter outputs. NOTE: Every click of the "step" button toggles the clock. Since sequential machines generally, but not always, operate on only the rising edge of the clock, **the counter will advance once every two presses.** The clock rate will be displayed on the seven-segment display in the form 2^01 Hz.



Physical Basys3 Buttons

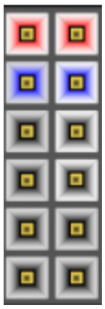


FPGA Digital Box Functions

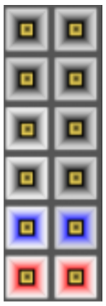
Figure 5: Buttons and functions when programed as an "FPGA Digital Controller"

Digital Controller Configuration

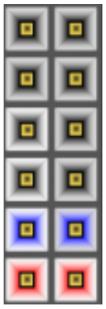
Inputs to LEDs (PMOD - A)

PWR		PWR
GND		GND
LD15		LD11
LD14		LD10
LD13		LD9
LD12		LD8

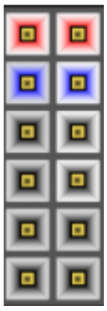
Outputs from Switches (PMOD - B)

SW0 / LD0		SW4 / LD4
SW1 / LD1		SW5 / LD5
SW2 / LD2		SW6 / LD6
SW3 / LD3		SW7 / LD7
GND		GND
PWR		PWR

Output from Clock (PMOD - C)

		Clock
GND		GND
PWR		PWR

Outputs from Counter (PMOD XADC)

PWR		PWR
GND		GND
		X1 Freq
		X2 Freq
		X4 Freq