

UNIVERSITY OF PENNSYLVANIA

ESE 668: MIXED SIGNAL CIRCUIT
AND MODELING

Final Project: ADC Design

Submitted by Nishant Sharma and Swetha Lakshmi Karthikeyan

CONTENTS

CONTENTS	1
Objective	3
Specification	3
Introduction:	3
Overview:	4
Design:	5
Hand Calculations	6
Schematics:	14
Test Schematics:	23
6-bit ADC test outputs:	32
6-bit ADC Power outputs:	34
Power Analysis:	35
METHODOLOGY:	35
REPORTED POWER:	35
DNL and INL:	36
6-bit ADC test output analysis/ Quality of results:	39
Reported Max Sampling Frequency:	41
Conclusion:	41
Scope for improvements:	41
Description of Distribution of Labor:	41
Extra Credit: SNDR, SFDR, New FOM w/measured ENOB:	42
Appendix	44

Objective

The aim of this project is to design a 6-bit pipelined ADC using 0.06 ami technology process on cadence satisfying the following base constraints:

- 5V supply voltage
- ENOB as 6 bits by pipelining the 1-bit flash ADC
- 1V Vpk with common mode of 2.5V
- Ideal reference voltage of 2.5V

Specification

- DNL ≤ 1
- INL ≤ 1

Introduction:

A pipelined ADC architecture offers a good trade-off between conversion rate, resolution and power consumption. It consists of several cascaded stages (each resolve $n -$ bit), timing circuits and digital correction block. The concurrent operation of all pipelined stages makes this architecture suitable to achieve very high conversion rates. The overall speed is determined by the speed of the single stage.

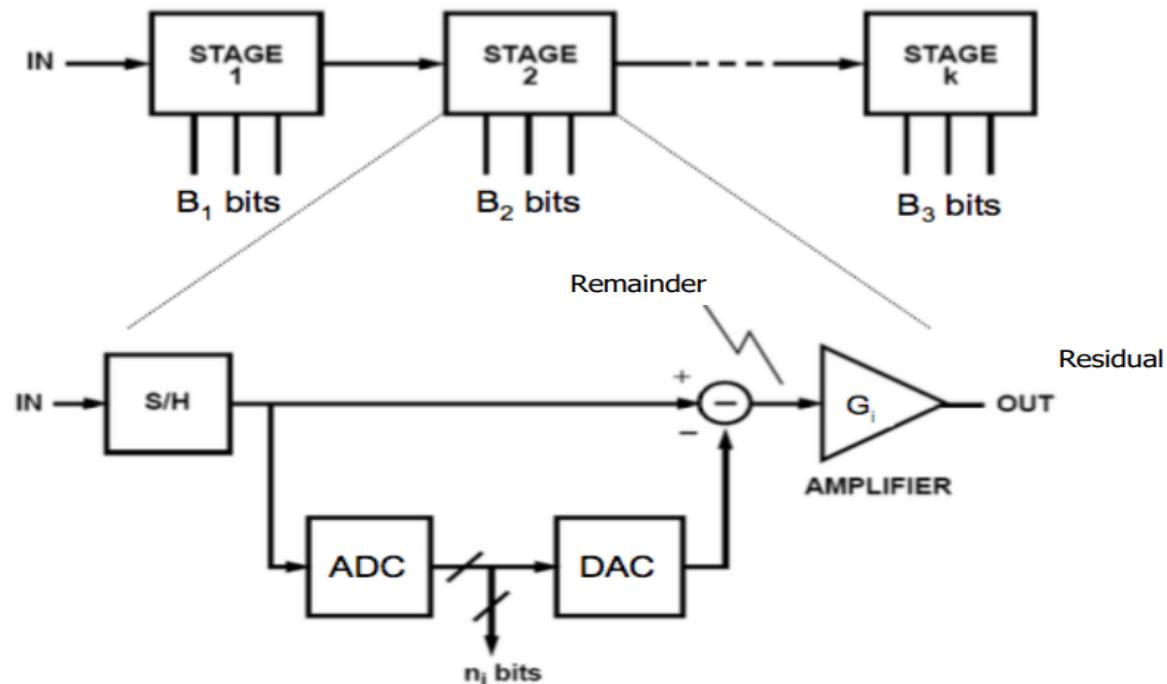


Fig: Pipelined ADC architecture cartoon representation.

Architecture:

First, the input signal v_{in} is captured by the sample and hold amplifier. Second, this signal is quantized by the subADC, which produces a digital output ($n -$ bit). This signal passes into the sub-DAC which converts it back to the analog signal. This analog signal is subtracted from the original sampled signal v_{in} . The residual signal goes into the opamp where it is amplified to the full scale range. Note when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput.

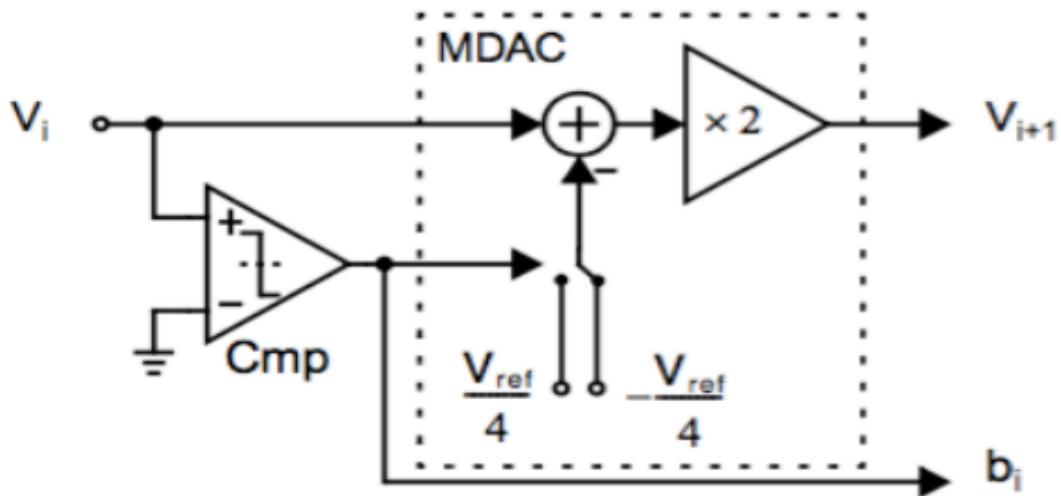


Fig: 1-bit flash sub-ADC.

Overview:

SAMPLE AND HOLD:

Track and Hold Amplifier(THA) is one of the most important parts of a data acquisition system. The THA stores the analog signal during an operation, usually analog to digital conversion, until the system can process the previous information. When the track-and-hold is in the track mode, the output follows the input with a small voltage offset. Analog to Digital converters are commonly made up of two stages. The first stage is a sampling circuit which holds a changing input signal constant at the output of the track and holds for a short time while the second stage, called the quantizing stage generates the digital output. When the THA is used with an ADC, the THA performance is critical to the overall dynamic performance of the ADC, and plays a major role in determining the Spurious Free Dynamic Range, Signal to Noise Ratio, etc., of the system.

LATCH-COMPARATOR:

A comparator is similar to an op amp. It has two inputs, inverting and non-inverting and an output. But it is specifically designed to compare the voltages between its two inputs. Therefore it operates in a non-linear fashion. The comparator operates open-loop, providing a two-state logic output voltage.

MDAC DIFFERENCE AMPLIFIER:

MDAC consists of a voltage divider, switching logic circuit, and a difference amplifier. A resistive voltage divider is designed to obtain desired reference voltages. The voltages are selected via a switching circuit. The output of the switching circuit is fed to the difference amplifier. The difference amplifier introduces a constant voltage gain.

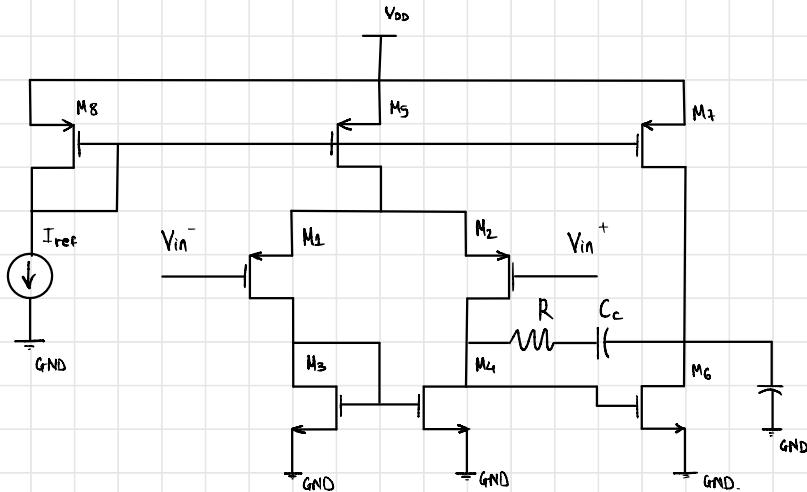
In this schematic, the analog input, V_{IN} , is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantifies it to one bit. The 1-bit output is then fed to a 1-bit latch-comparator, and the analog output is subtracted from the input. This "residue" is then gained up by a factor of two and fed to the next stage (Stage 2). This gained-up residue continues through the pipeline, providing one bit per stage until it reaches the 1-bit flash ADC, which resolves the last LSB bit. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to a DAC.

Design:

The designed 6-bit pipelined ADC is made up of sub-ADCs. 1-bit Flash ADCs are used as the sub-ADCs for the designed pipelined ADC.

- Pass transistors with wide switches were used in switched capacitor circuits to get better switching transfer characteristics.
- The slew rate of the opamp was increased to achieve sampling at the frequency of 10MHz by changing the feedback capacitor value.
- A preamplifier was designed to decrease the input offset voltage of the latch comparator. The offset was decreased to 182.51mV
- Voltage divider circuit and switching logic was designed to select MDAC reference voltage for the difference amplifier.
- Capacitor values were decided based on the desired gain value of the difference amplifier.
- Designed a 5 bit shift register using D-flip flops for adjusting delays at the out.

DESIGN STRATEGY

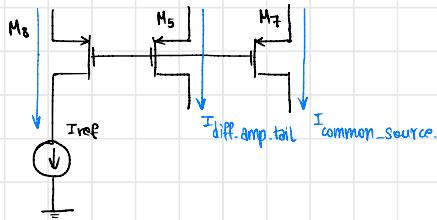


- CURRENT MIRROR: $[M_8, M_5, \& M_7]$
 - sum of currents in all branches is limited by the power specification
 - I_D of M_8 sets the reference current for the current mirror.
 - current in the differential amplifier branch & common source branch depends on the ratio of their W/L & $[W/L]_{M_8}$.
 - current in the differential amplifier branch & common source branch are divided proportionate to each stage's gain.
 - current in differential branch [I_D of M_5] is also designed according to the slew rate specification.
 - drop across M_5 controls the ICMR specification.
- DIFFERENTIAL AMPLIFIER: $[M_1, M_2, M_3, M_4]$
 - gain of the opamp: $g_m (r_{D2} || r_{O4}) \cdot g_m (r_{D6} || r_{O7})$.
 - therefore, we try in design $M_1, M_2, M_3, \& M_4$ according to the gain specification.
 - $M_3 \& M_4$ also controls ICMR specification.
- COMMON SOURCE: $[M_6]$
 - we try to design M_6 according to the gain specification.
- COMPENSATION CIRCUIT (C_c).
 - C_c controls the dominant pole and hence is designed by the phase margin & slew rate specifications.

OPAMP EQN:

DESIGN:

current mirror: transistor sizing:



— MOS parameters AMI 0.60 μ C5N

$$V_{t0} = 0.7068 \text{ V} \approx 0.8 \text{ V}$$

$$\begin{aligned} \mu_n &= 530 \text{ cm}^2/\text{V.s} & \mu_p &= 200 \text{ cm}^2/\text{V.s} \\ &= 0.053 \text{ m}^2/\text{V.s} & &= 0.02 \text{ m}^2/\text{V.s} \end{aligned}$$

$$t_{ox} = 14.1 \text{ nm}$$

$$\epsilon_{ox} = 3.9 \epsilon_0$$

$$= 3.9 (8.85 \times 10^{-12}) \text{ F/m}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{0.001447}{14.1} \text{ F/m}^2$$

$$\mu_n C_{ox} = 129.69 \mu \quad \mu_p C_{ox} = 48.94 \mu$$

Slew Rate: $I_{\text{diff.amp.tail}}$

$$C_c$$

Phase Margin: $\geq 60^\circ$

$$C_c \geq 0.22 C_L$$

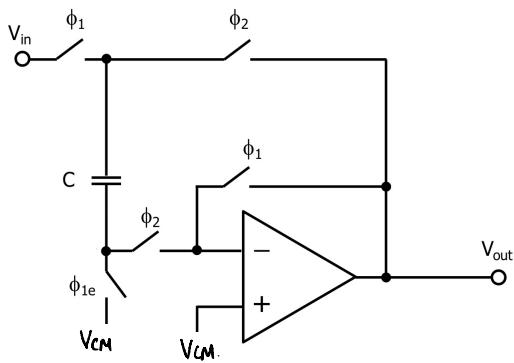
$$C_c \gtrsim 1 \text{ pF}$$

$$\text{gain} = g_{m1} (r_{02} \parallel r_{04}) \cdot g_{m6} (r_{06} \parallel r_{07})$$

i.e. gain depends on

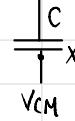
$$- g_{m1}, r_{02}, \text{ and } r_{04}$$

SHA Flip around.

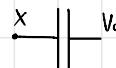


ϕ_1 :

V_{in}



ϕ_2 :



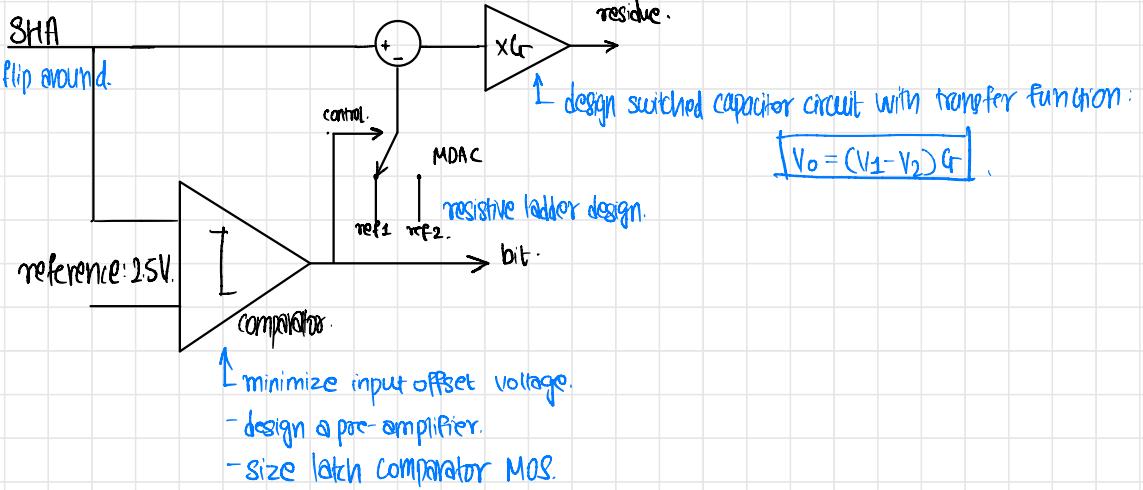
$$\phi_1: (V_{out} - V_{in})C - \Delta Q_C \quad \phi_2: -V_{out}C$$

equating ϕ_1 during $\phi_1 \neq \phi_2$.

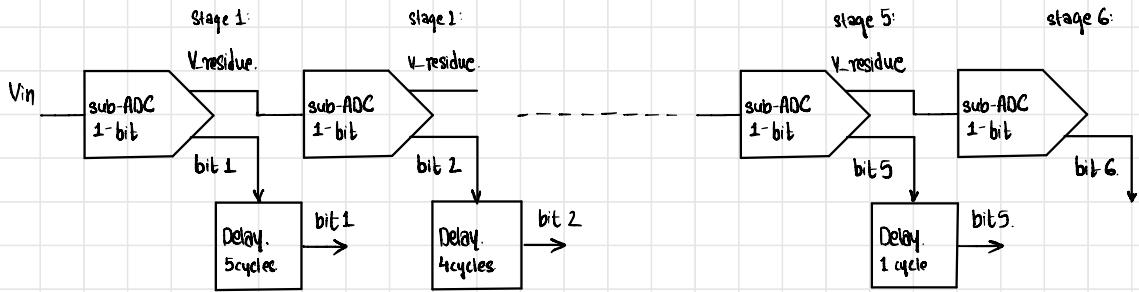
$$V_o = V_{in} + \frac{\Delta Q_C}{C}$$

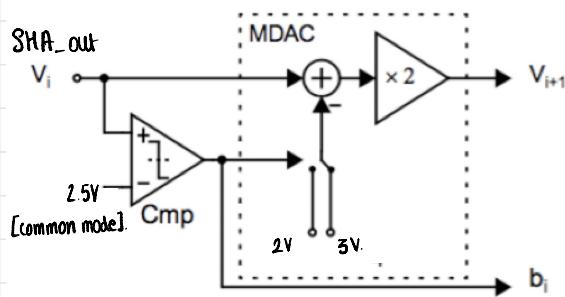
$$R_{on} = \text{output resistance of a MOS device} (r_D) = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{ds} - V_{th})}$$

Design of 1 bit Flash sub-ADC.



Design of 6-bit pipelined ADC.



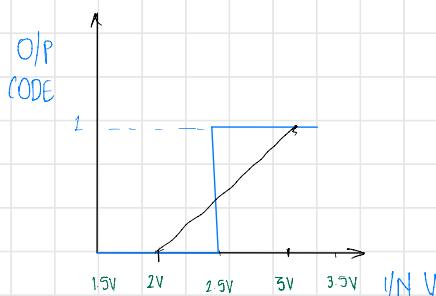


1 Bit Flash ADC design (calculation):

Given Full Scale Range: 1V peak.

$$V_{CM} = 2.5V$$

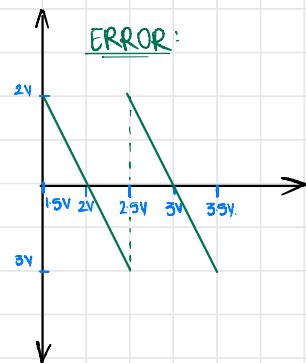
$$\therefore FSR = 1.5V \leq 3.5V$$

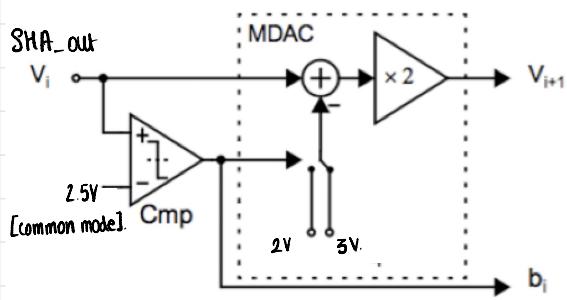


$$\text{then: } \frac{V_{CM} - FSR(\text{lower limit})}{2} \text{ to } \frac{FSR(\text{higher limit}) - V_{CM}}{2}$$

0 quantization error for 1 bit flash ADC at $2V \leq 3V$.

$$LSB = \frac{FSR}{2^N} = \frac{2V}{2^6 \text{ steps}} = \frac{2}{64 \text{ steps}} = 0.03125$$



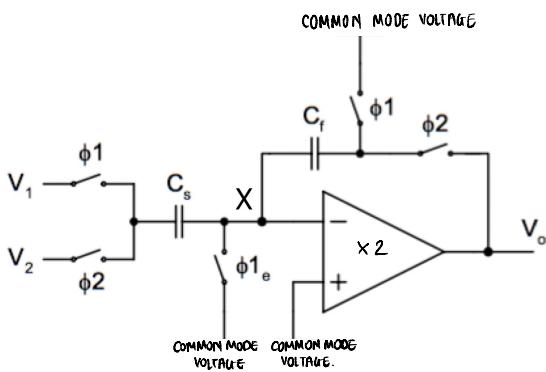


Residue Calculation of 1 bit flash sub-ADC stage

$$\text{Gain of difference amplifier} = 2^{\text{N-bits}}$$

$$= 2^1$$

$$= 2 \text{ V/V}$$



φ 1 :

$$Q_x = -V_1 C_S$$

equating Q_x during $\phi_1 \neq \phi_2$ because of charge conservation.

$$-V_1 C_S = -V_2 C_S - V_0 C_F$$

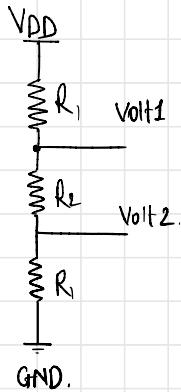
$$V_o = (V_1 - V_2) \frac{C_3}{C_F} + V_{CM} \quad \text{we want a gain of 2 hence, } C_3 = 2 C_F.$$

equivalent circuit during $\frac{V_d}{C_f}$

ϕ_2

$$Q_x = -V_2 C_S - V_0 C_F$$

MDAC calculation



$$V_{DD} \times \frac{R_1 + R_2}{2R_1 + R_2} = 3V \quad \frac{R_1 + R_2}{2R_1 + R_2} = \frac{3}{V_{DD}} \quad \text{--- (1)}$$

$$V_{DD} \times \frac{R_1}{2R_1 + R_2} = 2V \quad \frac{R_1}{2R_1 + R_2} = \frac{2}{V_{DD}} \quad \text{--- (2)}$$

Solving Eq. (1)

$$\Rightarrow R_1 = \frac{4}{5} R_1 + \frac{2}{5} R_2$$

$$\Rightarrow R_1 - \frac{4}{5} R_1 = \frac{2}{5} R_2$$

$$\Rightarrow \frac{1}{5} R_1 = \frac{2}{5} R_2$$

$$\Rightarrow \boxed{R_1 = 2R_2}$$

$$\text{let } R_2 = 500\Omega \quad \text{then } R_1 = 1k\Omega$$

COMPARATOR

$$T_{latch} = \frac{t_2 - t_1}{\ln \left[\frac{V_{DD2}}{V_{DD1}} \right]}$$

preamplifier - NMOS differential pair amplifier.

Figure of Merit (FOM)

i.) with ENOB = 6 bits.

$$FOM = \frac{\text{Power}}{f_s \cdot 2^{\text{ENOB}}}$$

$$= \frac{269.5 \text{ mW}}{10 \text{ M} \times 2^6}$$

$$= 4.21 \times 10^{-10} \text{ W/Hz}$$

EXTRA CREDIT:

ii.) with ENOB = 3.1 bits

$$FOM = \frac{269.5 \text{ mW}}{10 \text{ M} \times 2^{3.1}}$$

$$= 3.14 \times 10^{-9} \text{ W/Hz}$$

Schematics:

PASS TRANSISTOR:

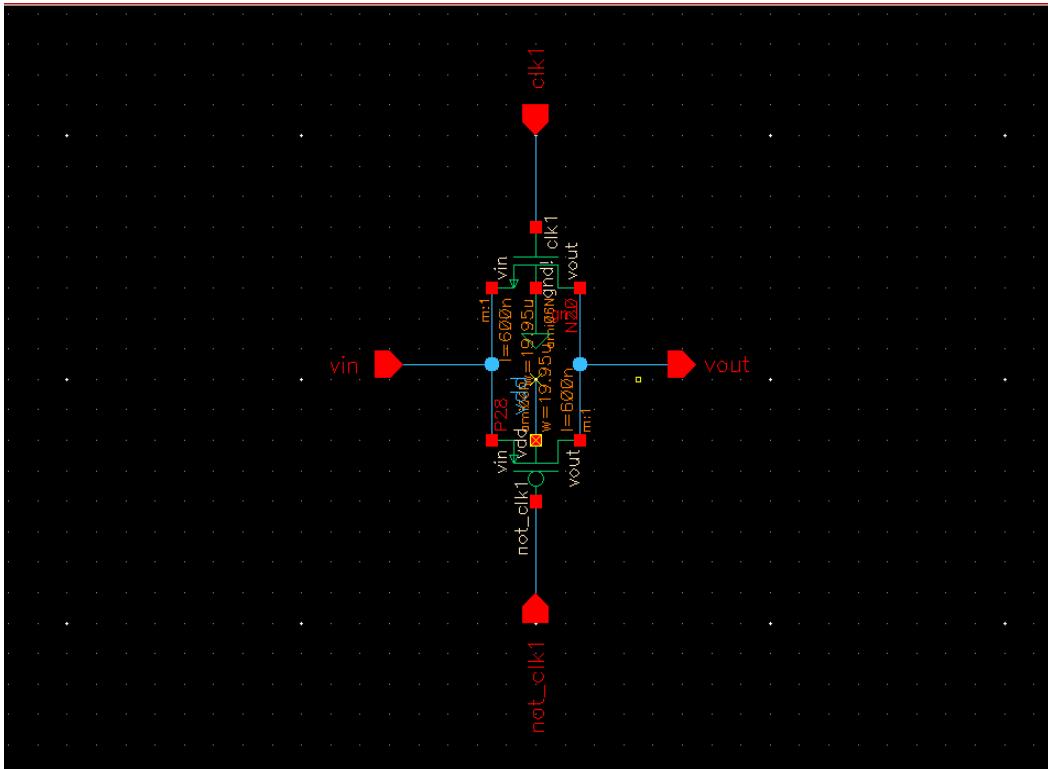


Fig: Pass transistor switch size schematic

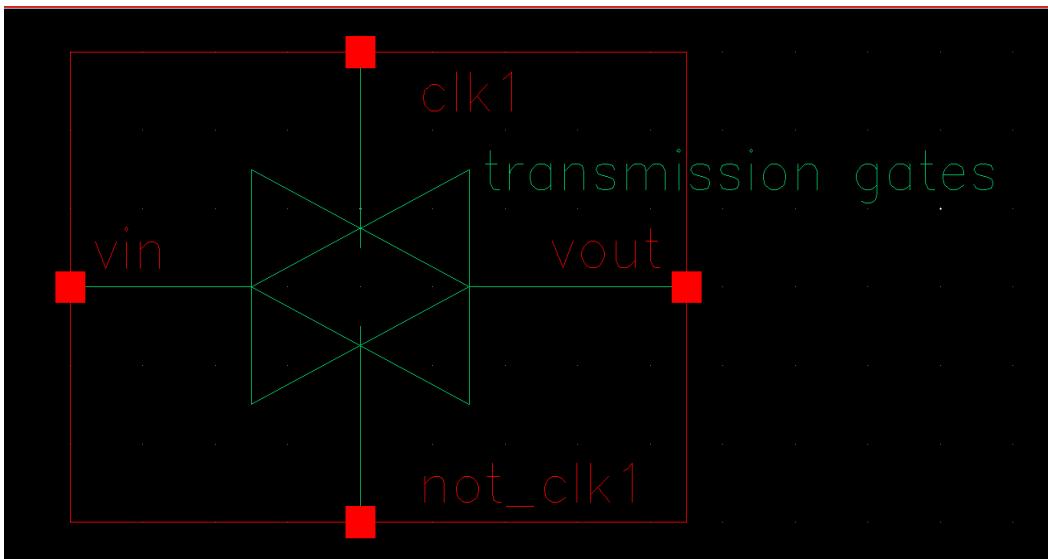


Fig: Pass transistor switch symbol

OPAMP:

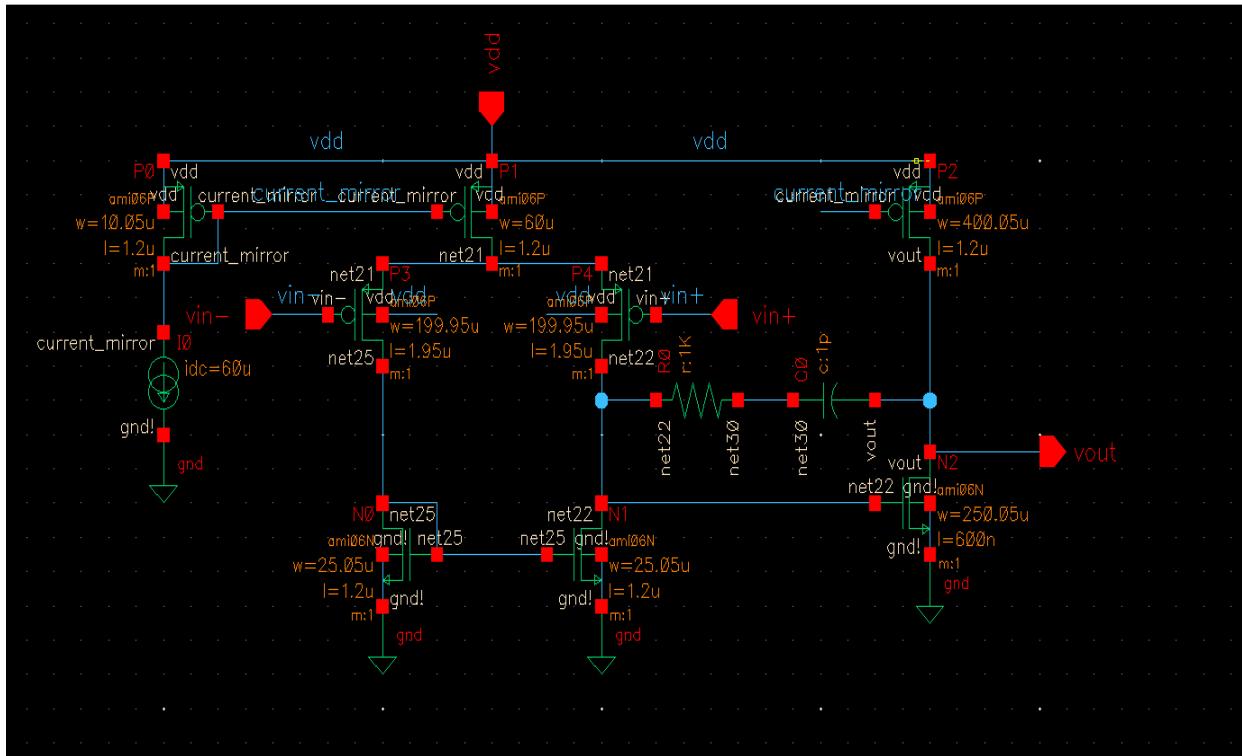


Fig: OPAMP size schematic

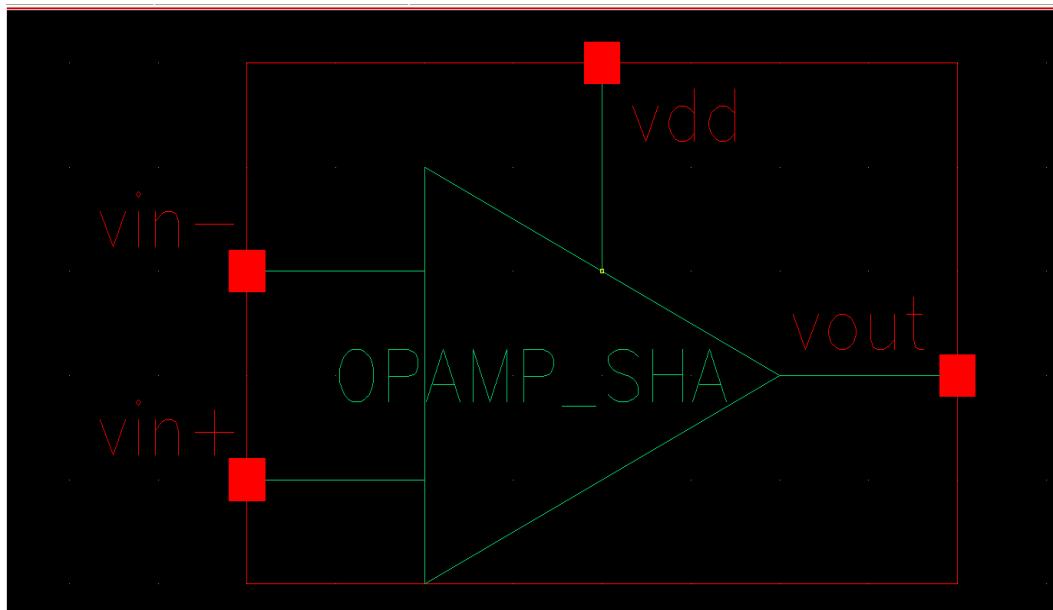


Fig: OPAMP symbol

SHA:

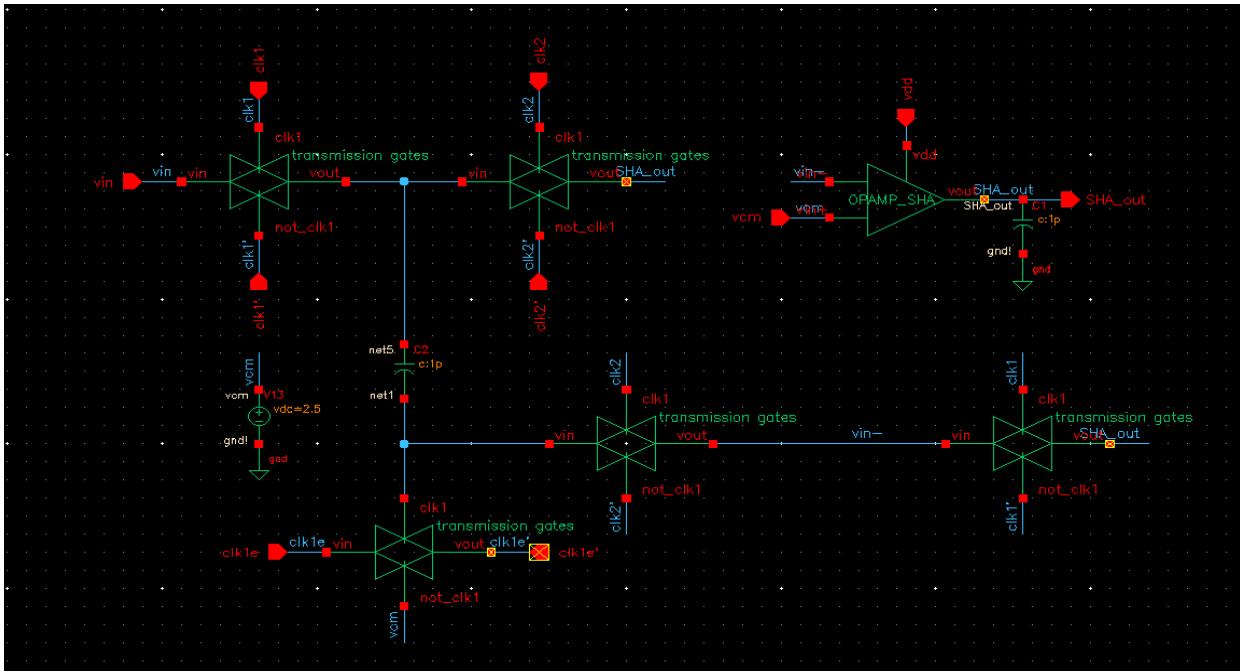


Fig: SHA flip around topology schematic

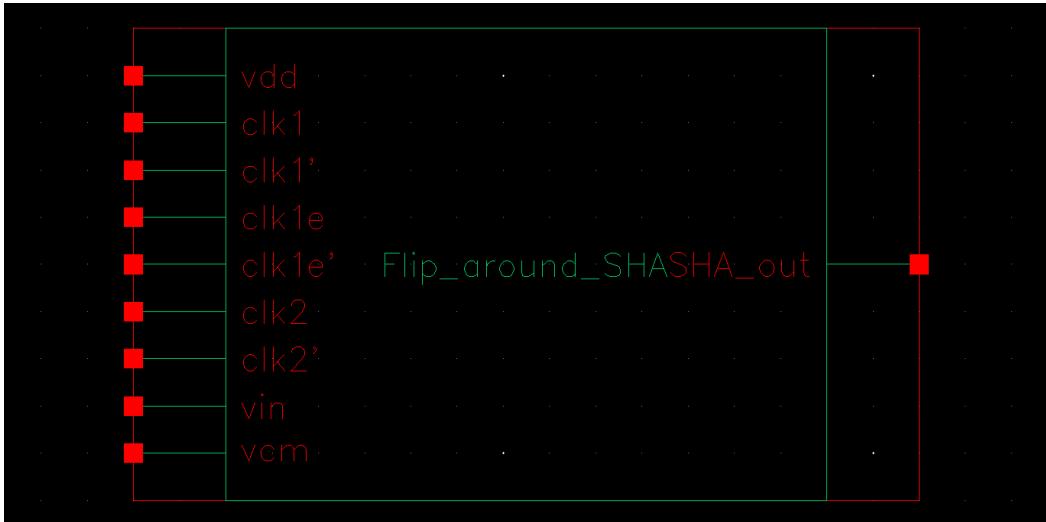


Fig: SHA symbol

COMPARATOR:

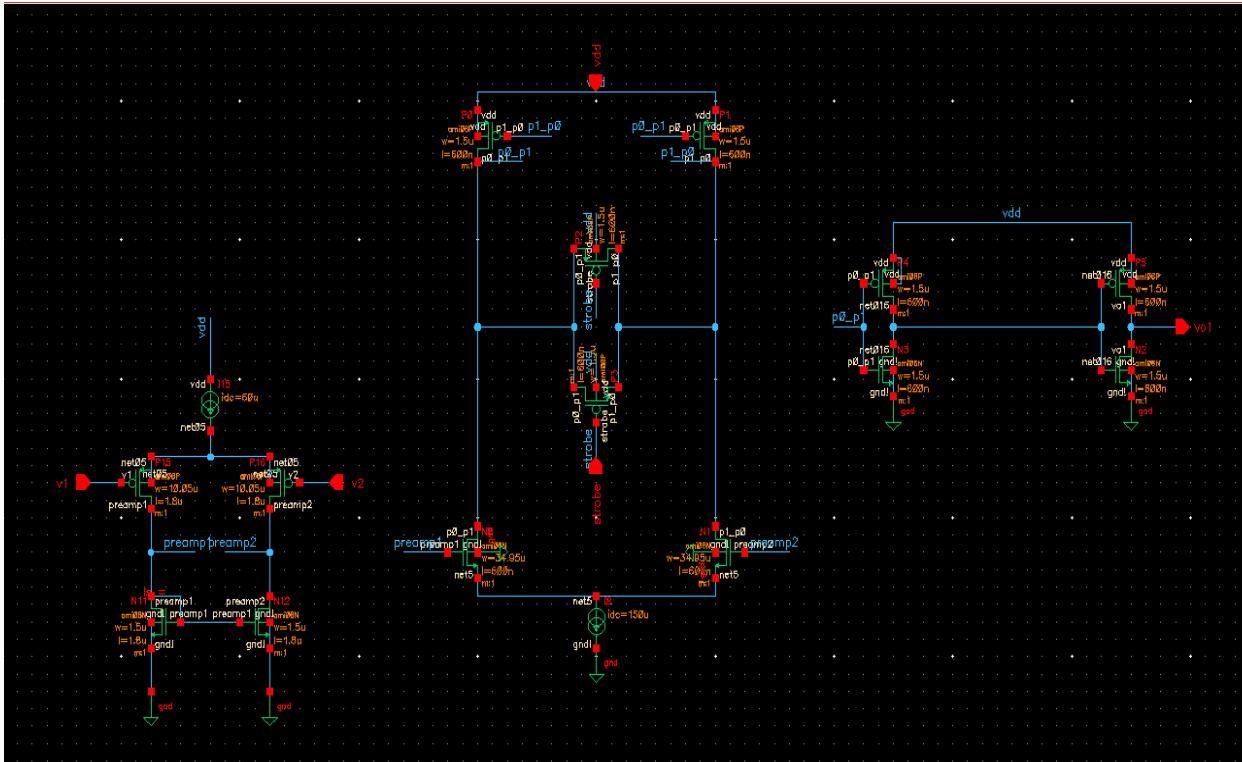


Fig: Latch Comparator size schematic

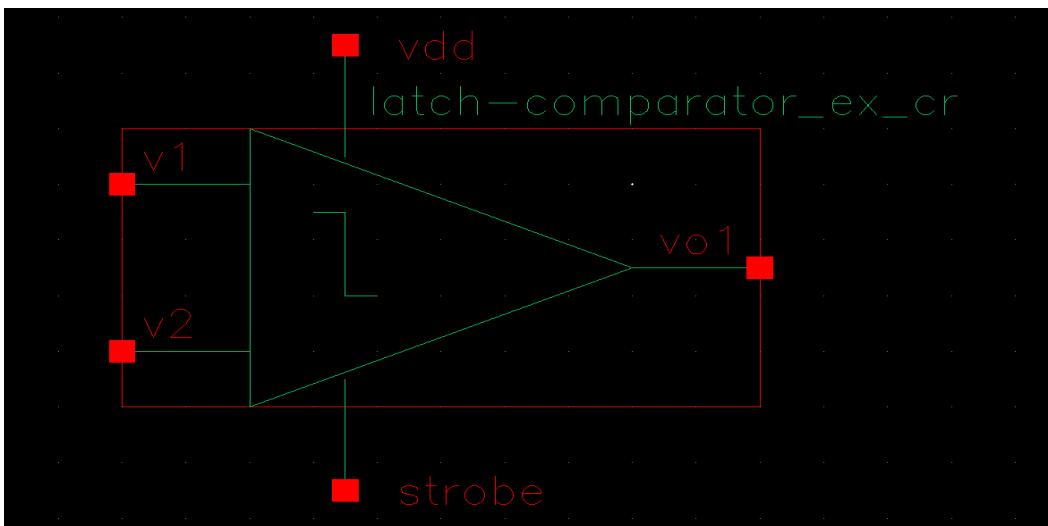


Fig: Comparator symbol

MDAC VOLTAGE DIVIDER SWITCH:

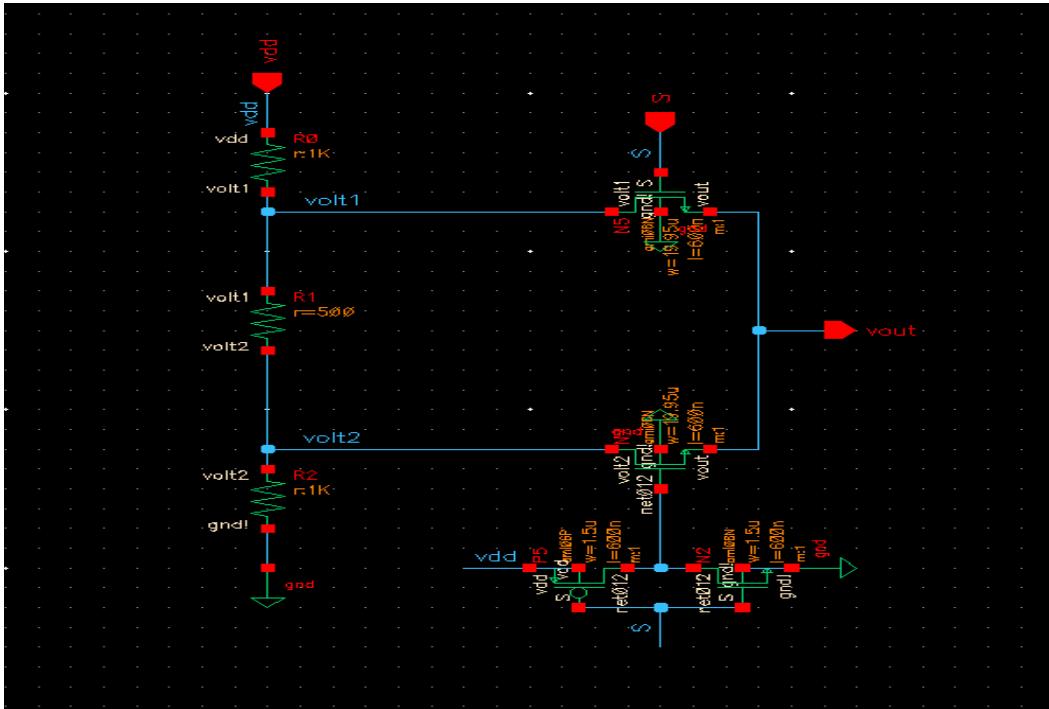


Fig: MDAC voltage divider and switch schematic

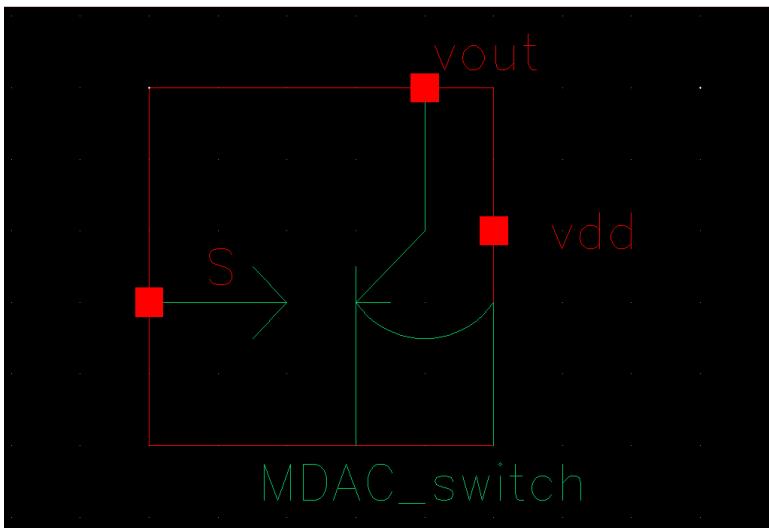


Fig: MDAC voltage divider and switch symbol

DIFFERENCE AMPLIFIER:

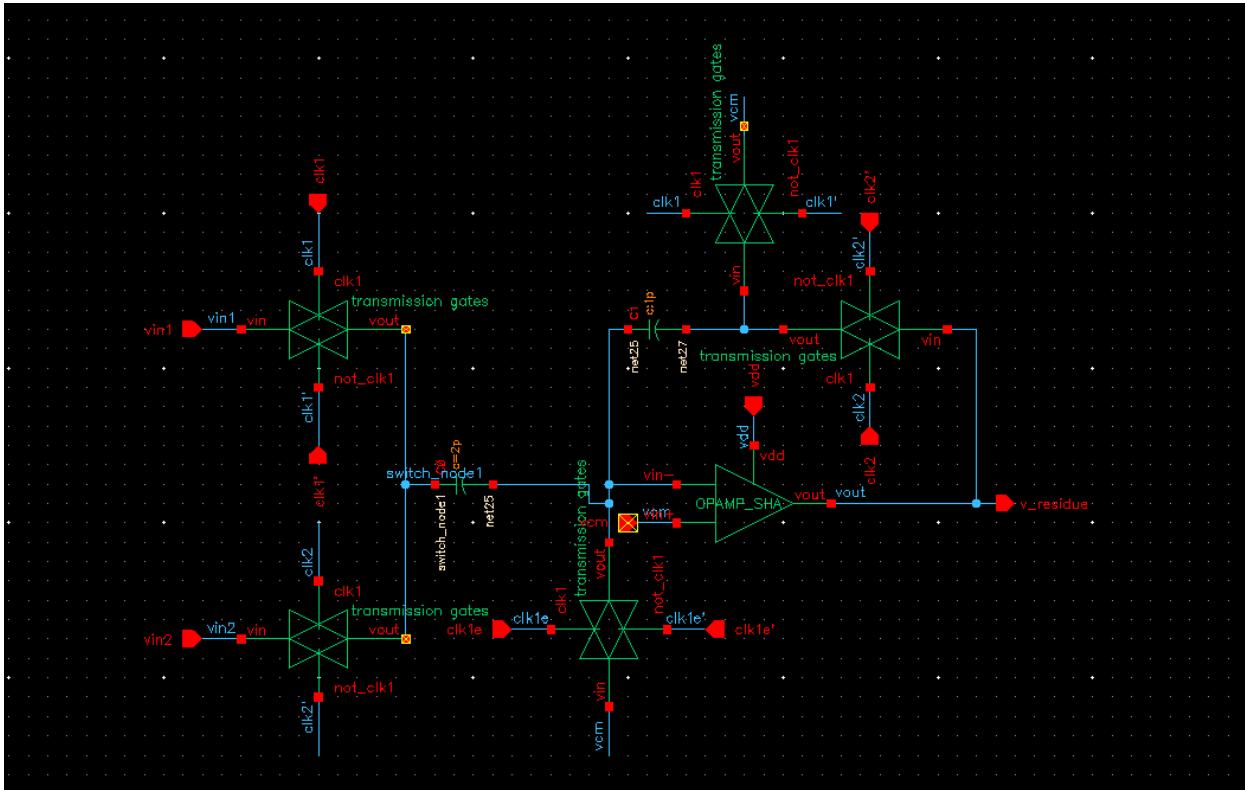


Fig: Difference amplifier schematic

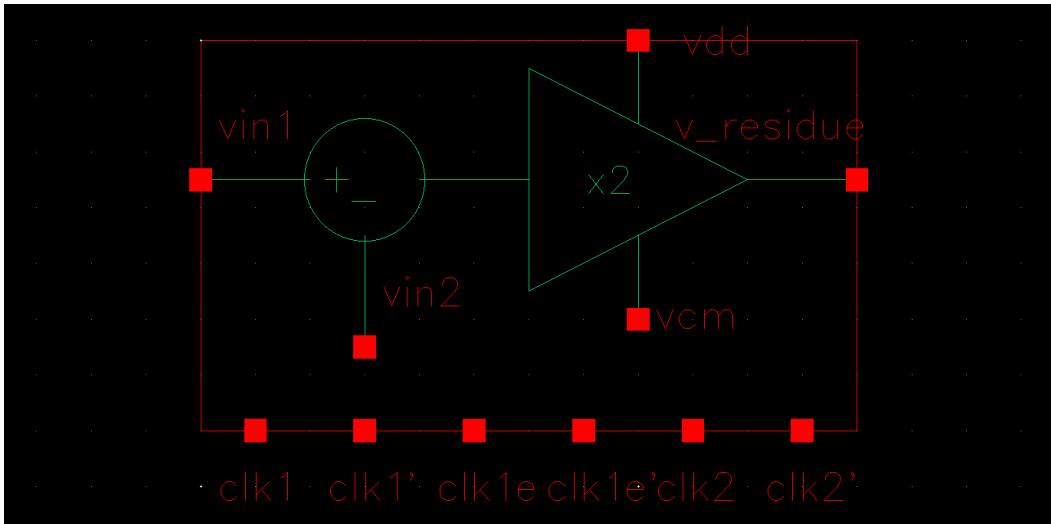


Fig: Difference amplifier symbol

1 BIT FLASH SUB-ADC:

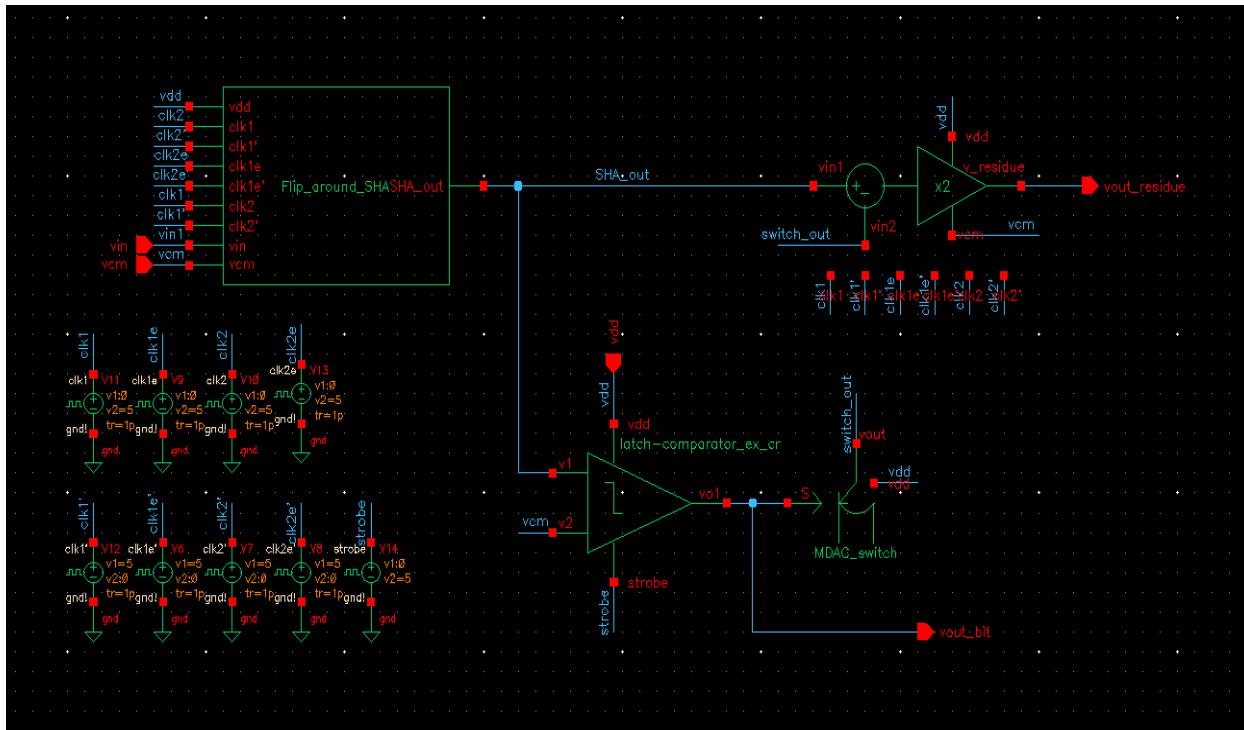


Fig: 1-bit Flash sub-ADC schematic

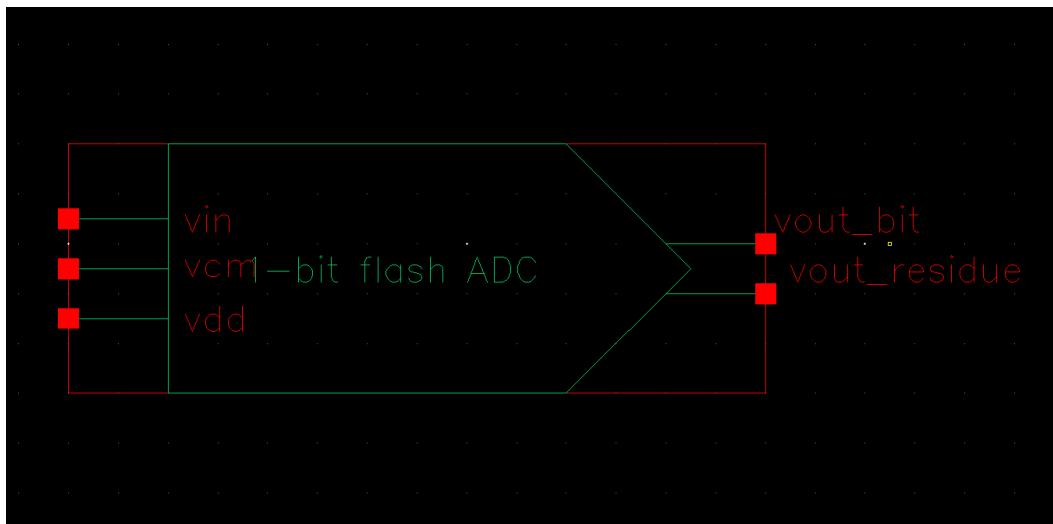


Fig: 1-bit Flash sub-ADC symbol

SHIFT REGISTER:

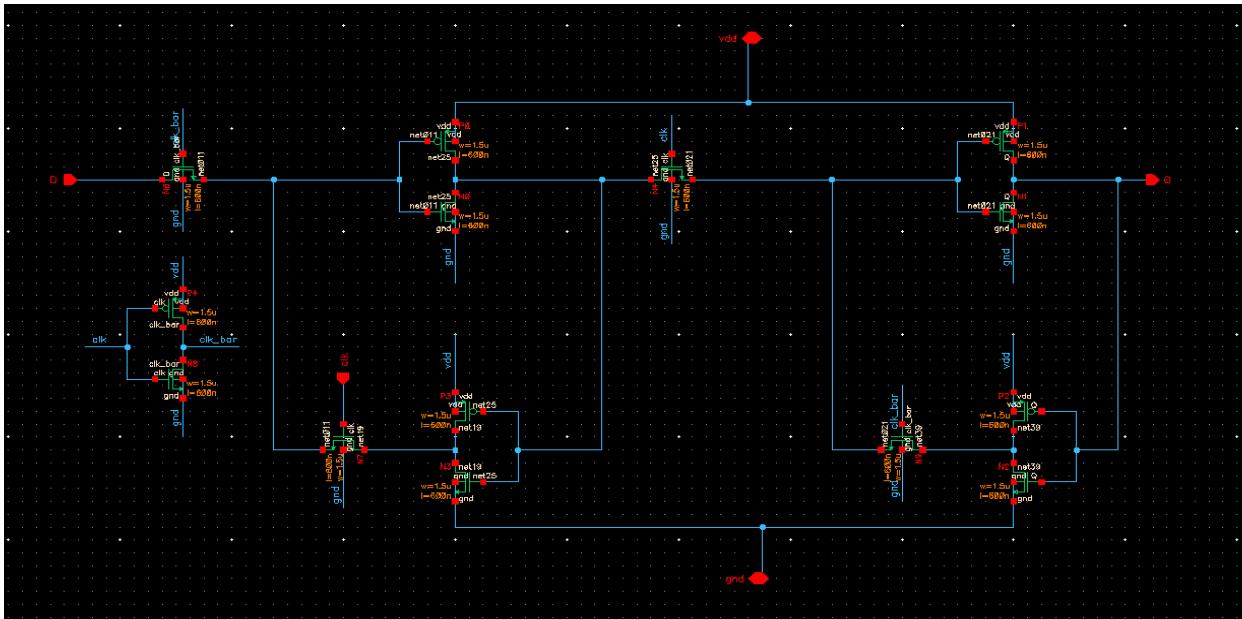


Fig: D Flip Flop schematic

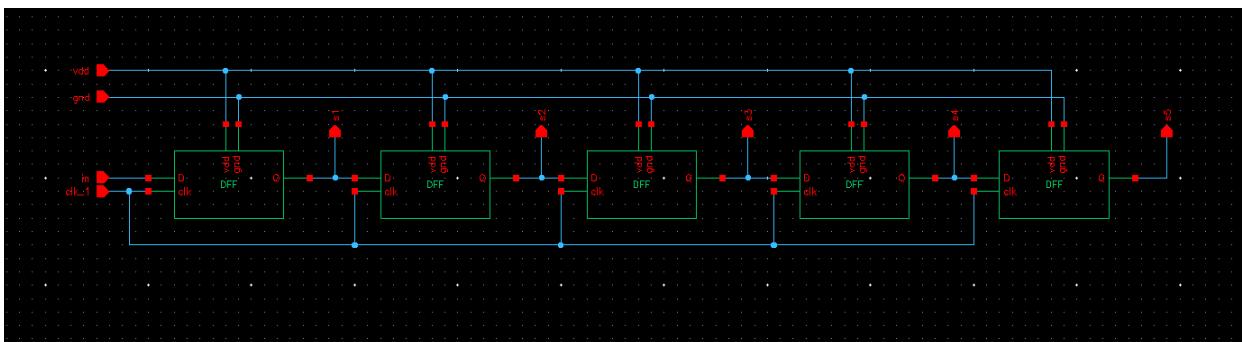


Fig: Shift Register schematic

6-bit pipelined ADC schematic description:

Six 1-bit Flash sub-ADCs are daisy chained to each other. The residue of prior stage is fed as the input of the next stage. The bit output of the sub-ADCs go to timing circuits where they are appropriately shifted to match the pipeline. A common clock is given to the timing circuit.

6-BIT PIPELINED ADC:

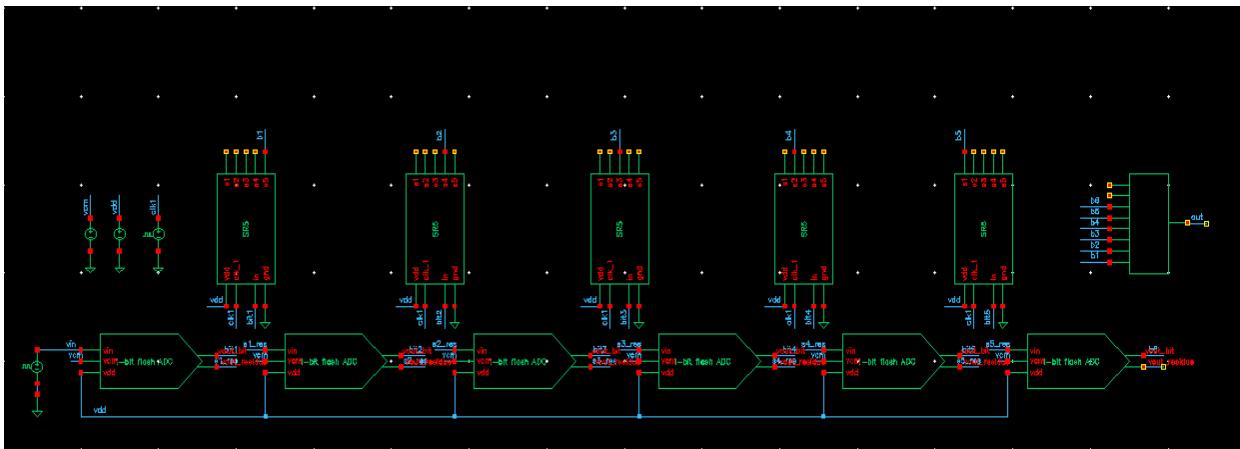


Fig: 6-bit pipelined ADC schematic

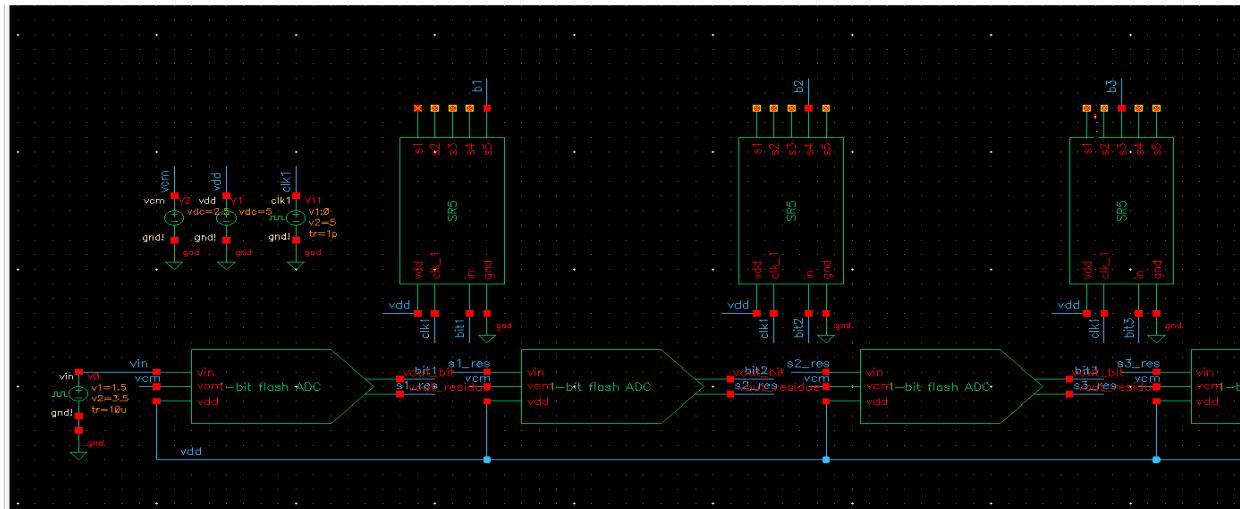


Fig: 6-bit pipelined ADC schematic zoomed in

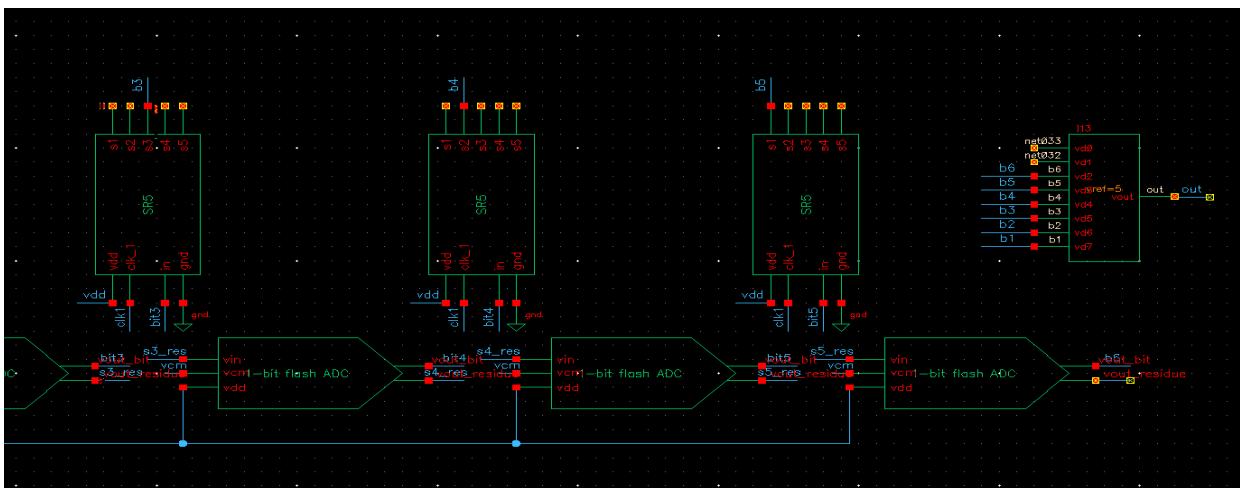


Fig: 6-bit pipelined ADC schematic zoomed in

Test Schematics:

Clocks:

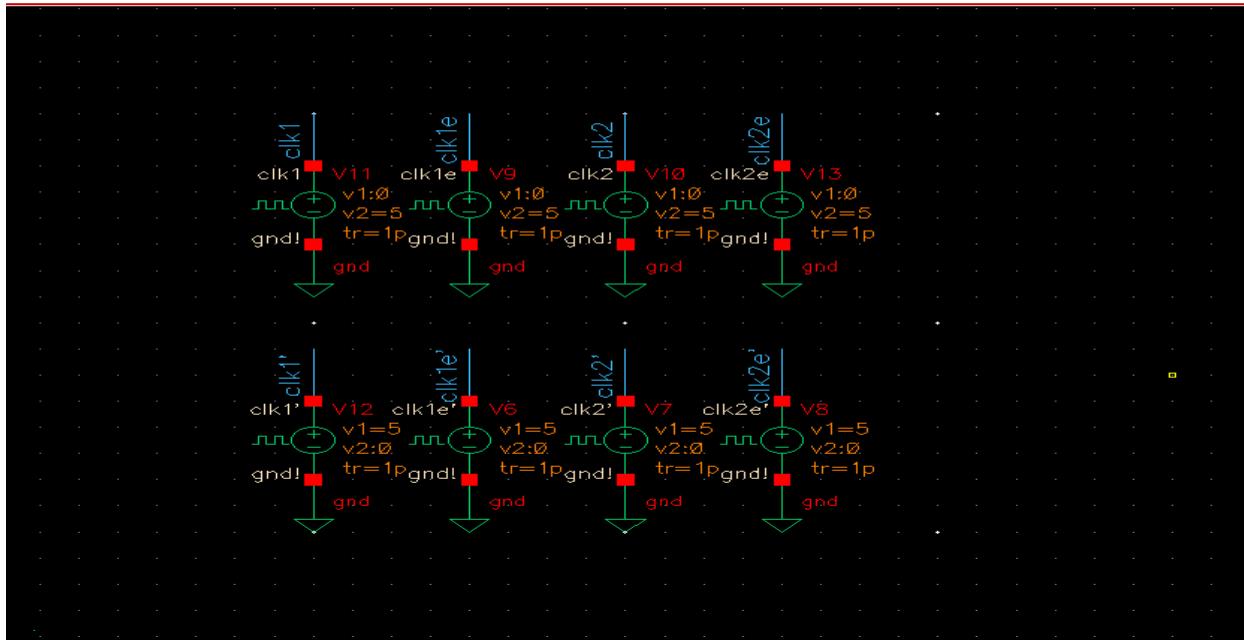


Fig: clocks

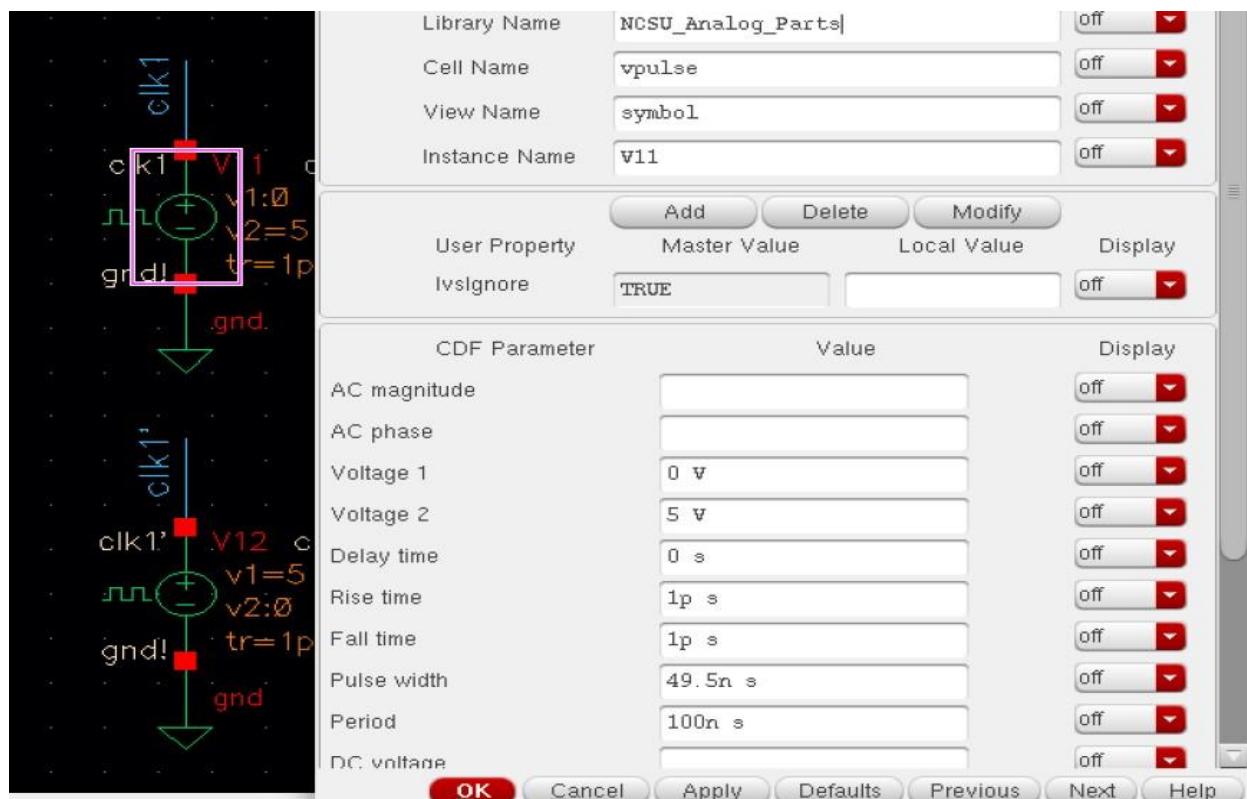


Fig: clock1

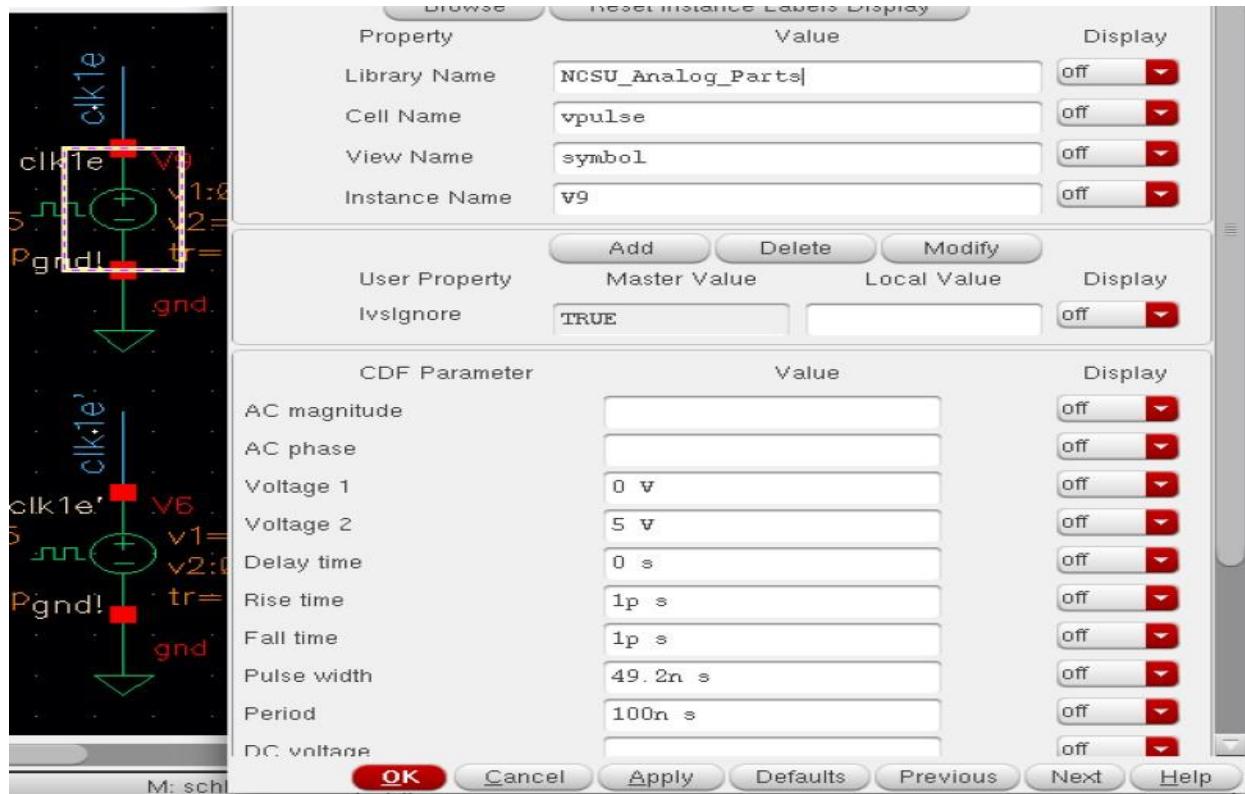


Fig: clock1e

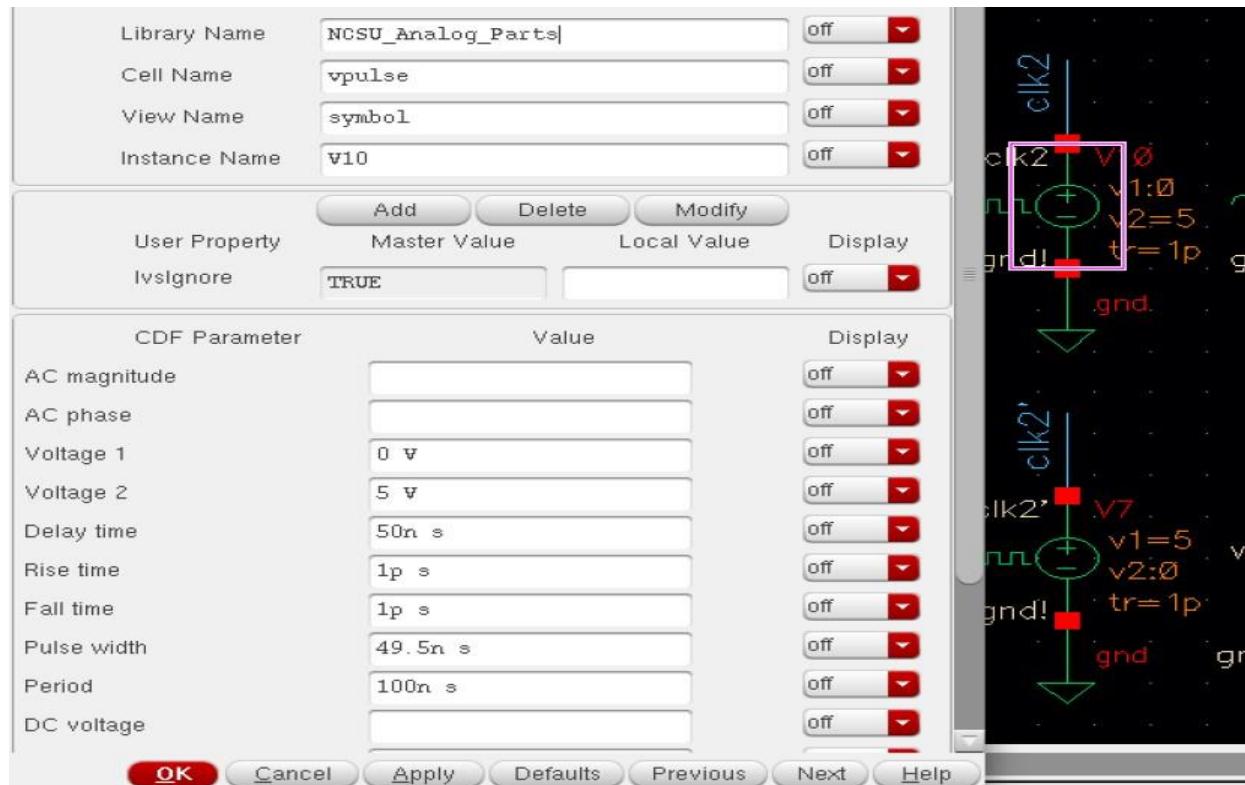


Fig: clock2

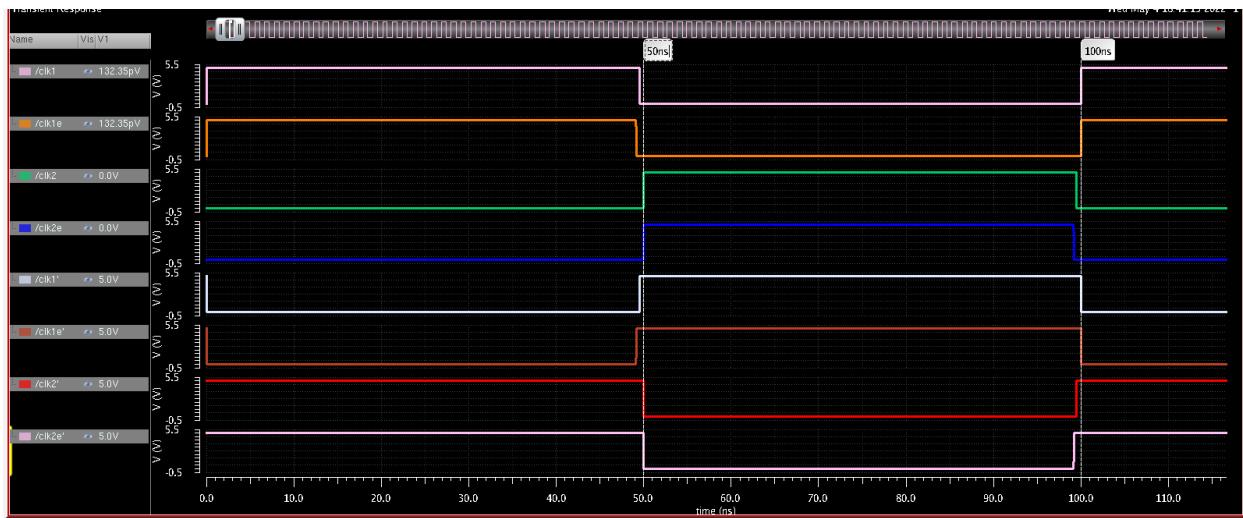


Fig: clocks output

SHA-Comparator

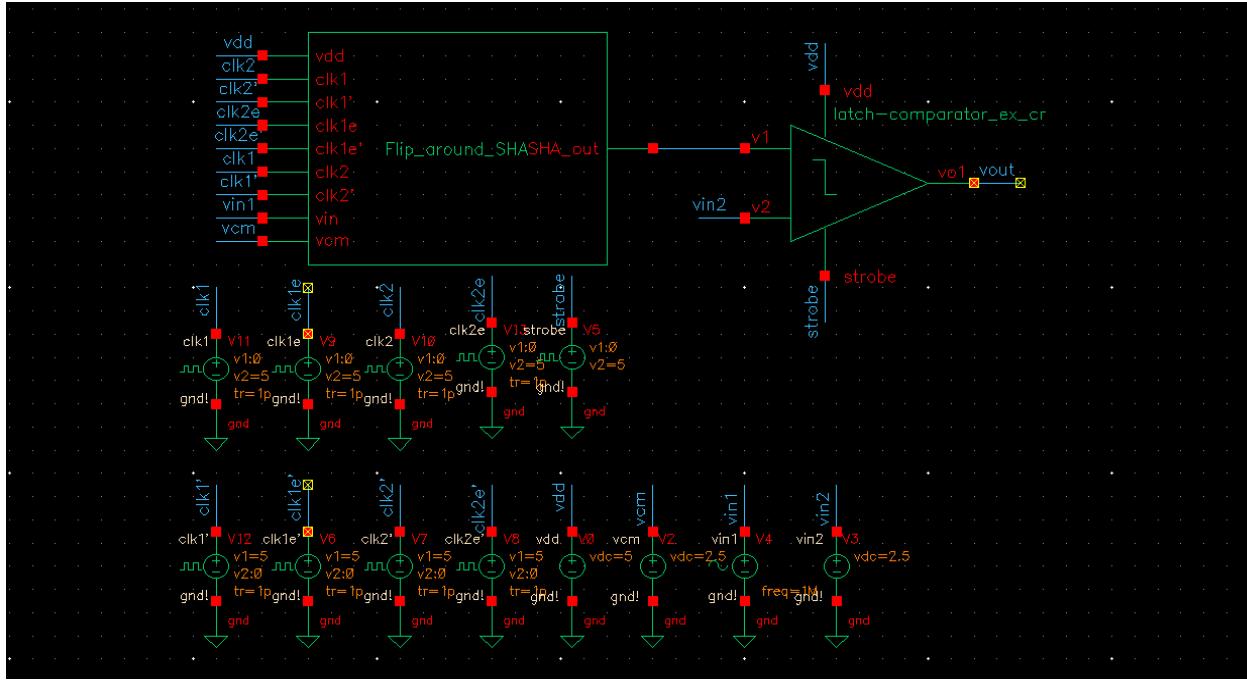


Fig: SHA-Comparator test schematic

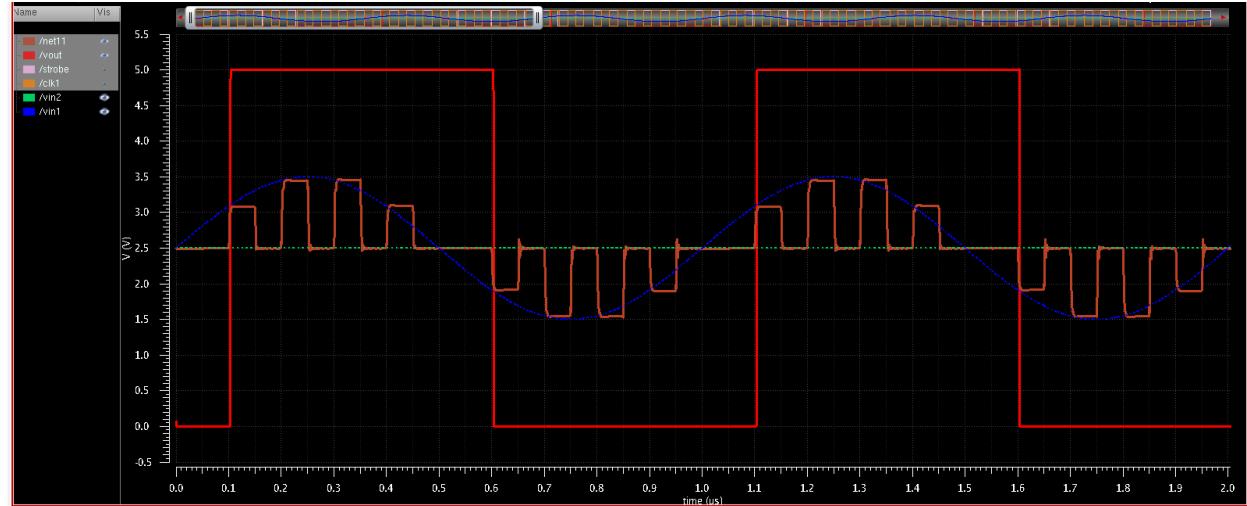


Fig: SHA-Comparator test output

Description:

To test the comparator, a sine wave (centered at 2.5V) is given as the input to the SHA circuit. The output of the SHA is given to the comparator. A common mode of 2.5V is given as the reference voltage to the comparator. The expected output of this schematic is that when the sampled signals are above 2.5V the comparator output should be the positive rail voltage. Conversely, when the samples are less than 2.5V, the comparator should output negative rail/ reference ground. The attached output shows that the desired behavior is achieved. The sine wave is sampled, and the comparator toggles correctly corresponding to the sample values.

MDAC test:

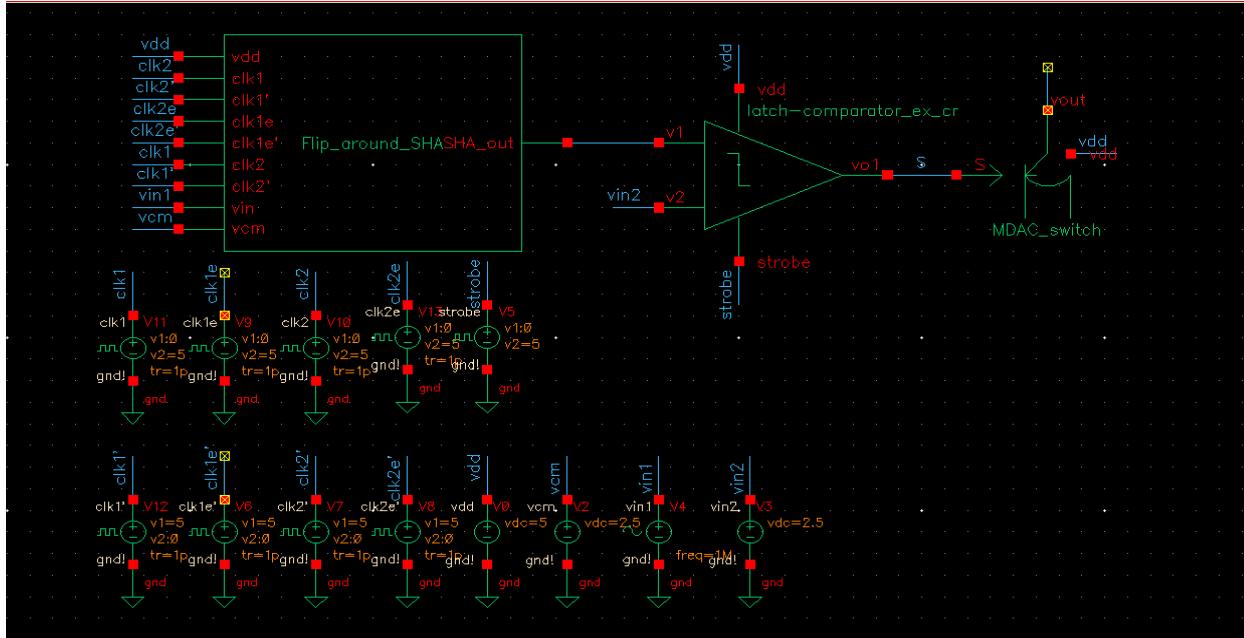
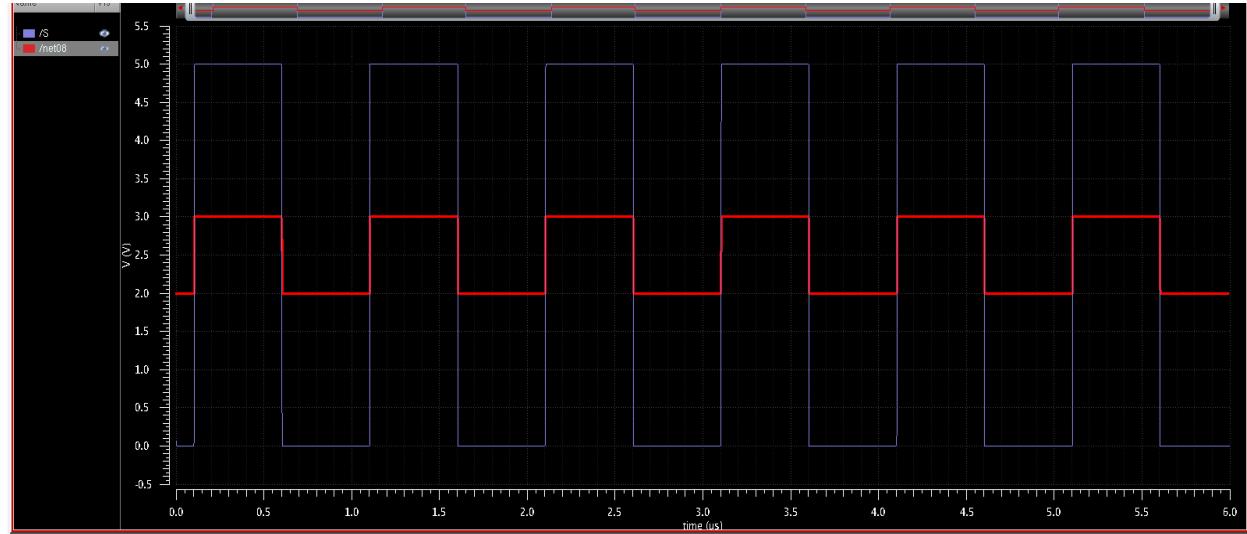


Fig: MDAC test schematic



Description:

The MDAC switching logic is supposed to be controlled by the output of the comparator. The MDAC switch is expected to toggle between two reference voltages generated by a resistive voltage divider. The MDAC switch toggles correctly between two reference voltages(3V and 2V) depending on the comparator output.

Difference Amplifier test:

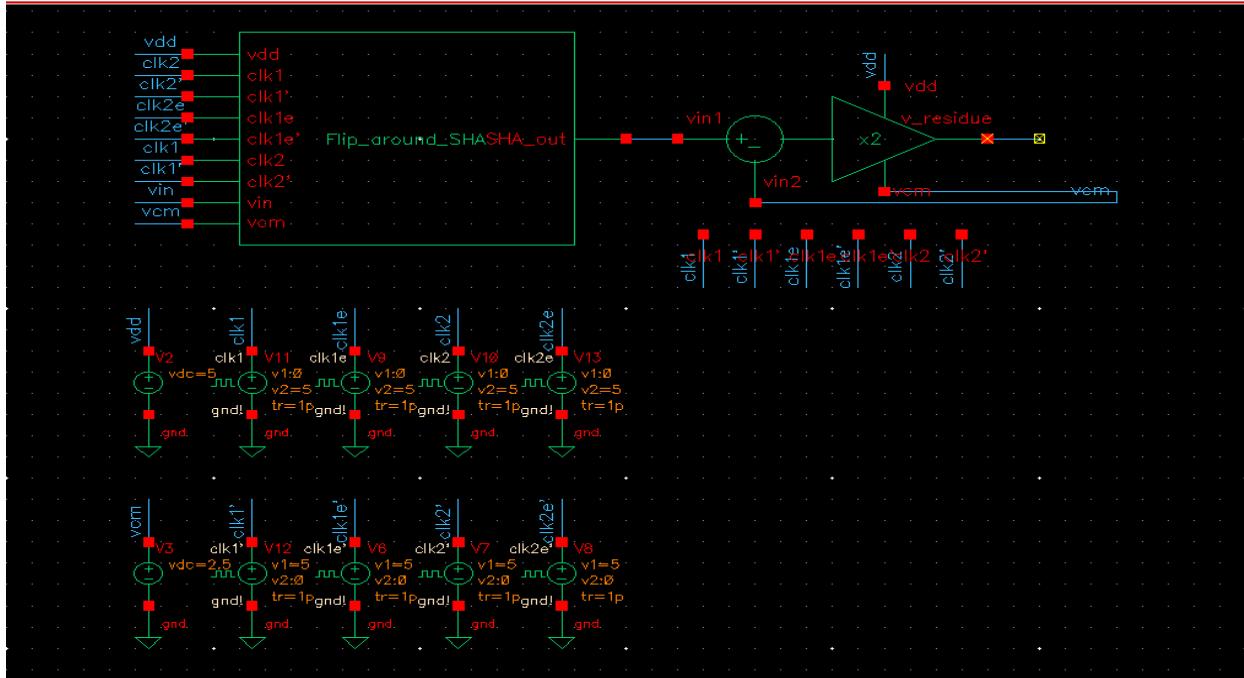


Fig: Difference amplifier test schematic

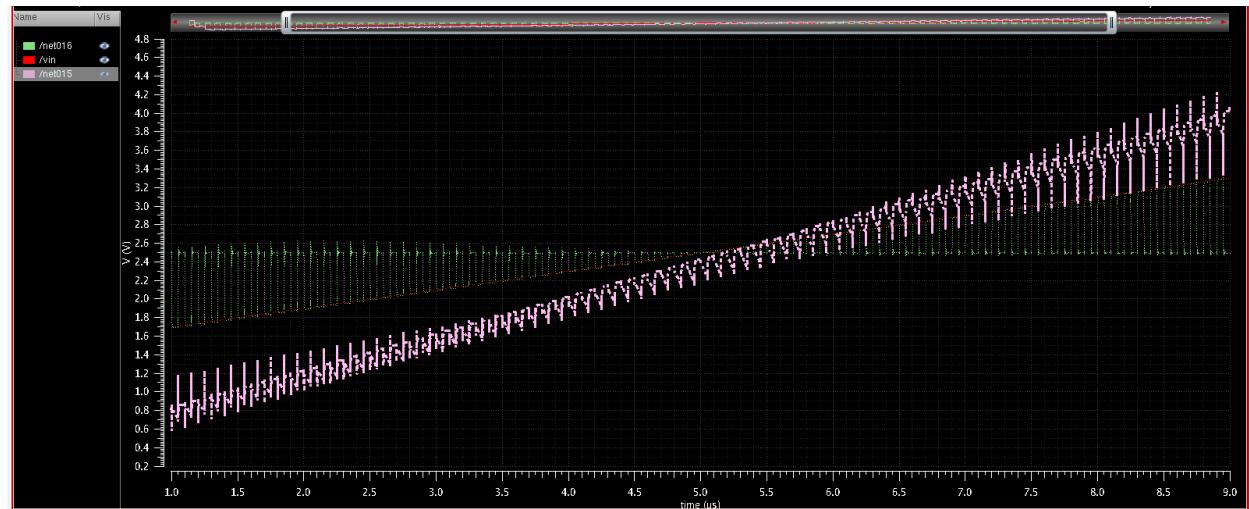


Fig: Difference amplifier test output

Description:

The output of the difference amplifier is the residue voltage that needs to propagate to the next stage. The difference amplifier is supposed to have a transfer function of $V_o = (V1 - V2) * 2 + 2.5V$. The difference amplifier is tested against a ramp voltage starting from 1.5V up till 3.5V. The signal in green is the output of the SHA/ input of the difference amplifier. The signal is light pink is the calculated residual voltage. The circuit is functioning correctly, which can be easily confirmed by checking its behavior at 2.5V input. That is when ramp voltage is equal to 2.5V, $(V1 - V2) = 0$ and the residue is at 2.5V.

1-bit Flash sub-ADC

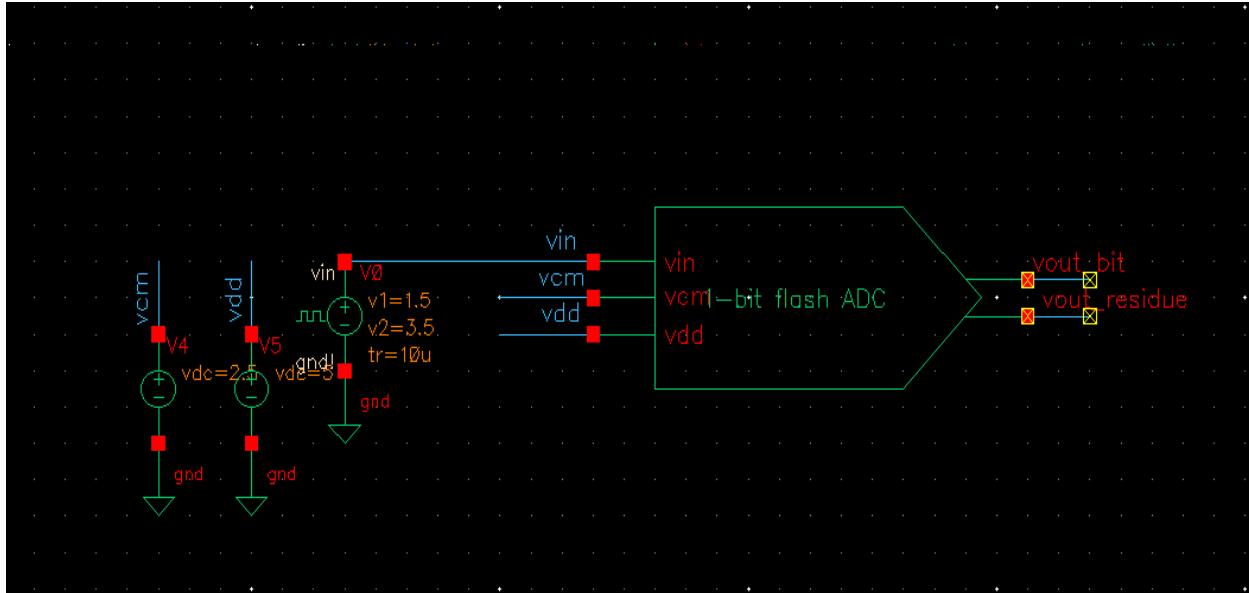


Fig: 1-bit Flash sub-ADC test schematic

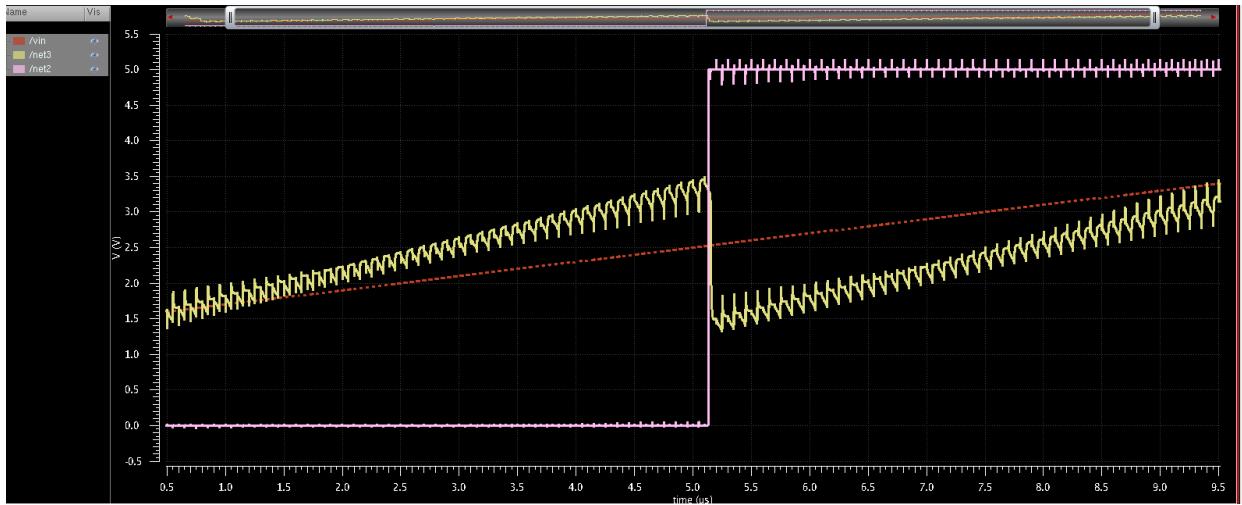


Fig: 1-bit Flash sub-ADC output

Description:

A slow moving ramp is given as the input to the 1-bit Flash sub-ADC (shown in dotted orange). The signal in light pink is the bit out from the 1-bit sub-ADC and the yellow signal is the calculated residue to be propagated to the next stage. When the output bit is low, the MDAC switch outputs 2V to the difference amplifier. That is, the difference amplifier subtracts the incoming signal from 2V and gives a gain of 2V/V. While, when the bit out is high the MDAC switch outputs 3V. The output is similar to the transfer function plotted while designing the 1-bit flash sub-ADC in the hand calculation section. Satisfactory performance is achieved.

6-bit pipelined ADC:

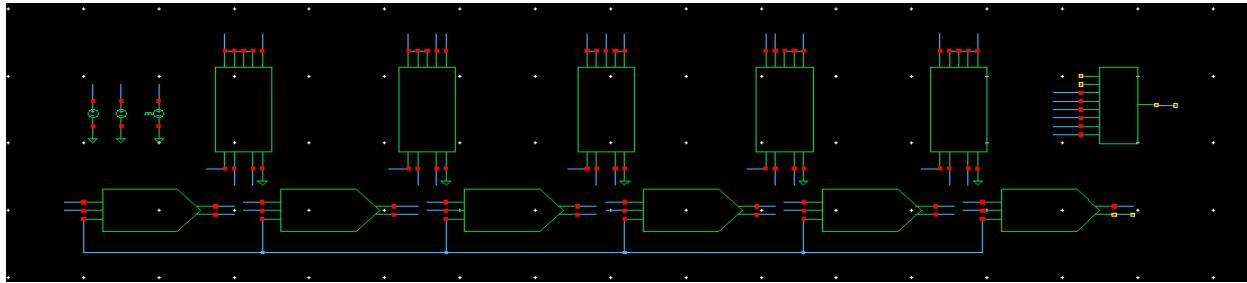


Fig: 6-bit schematic

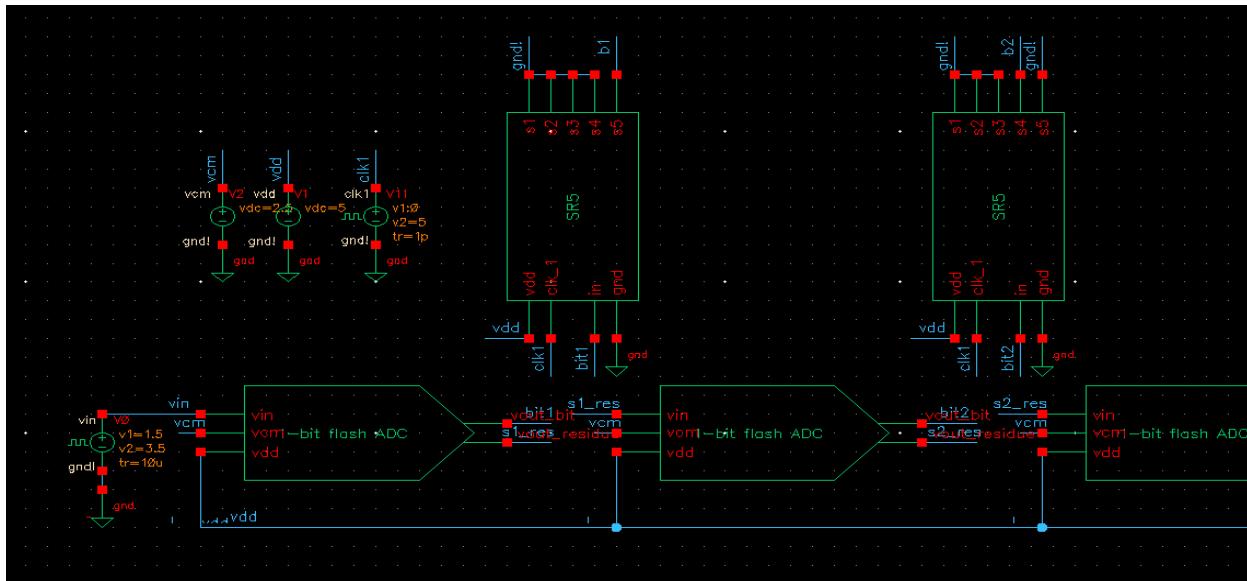


Fig: 6-bit ADC transient test schematic

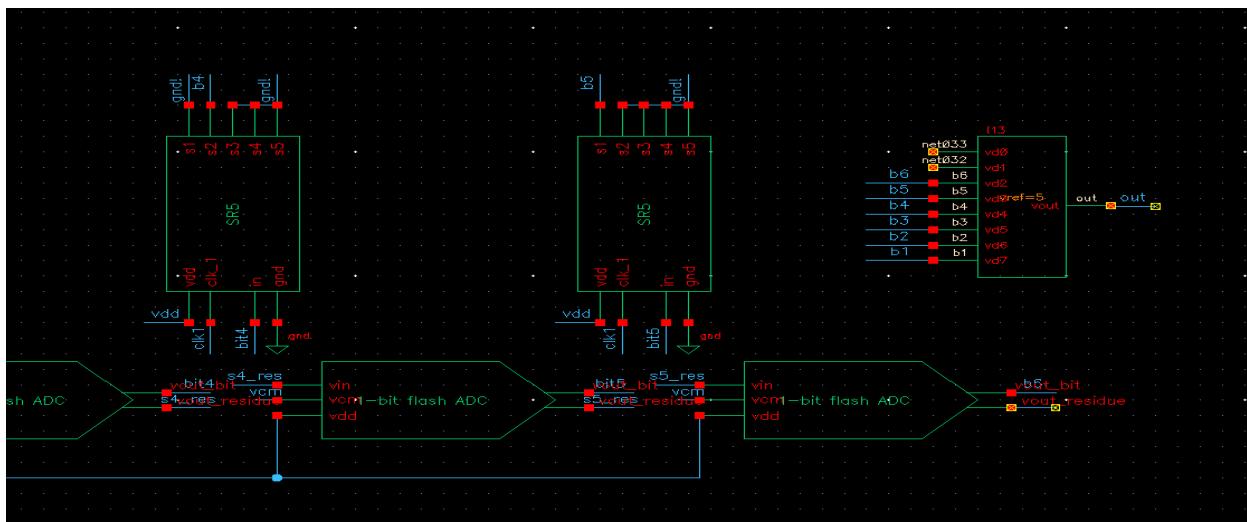


Fig: 6-bit ADC ideal DAC setup schematic

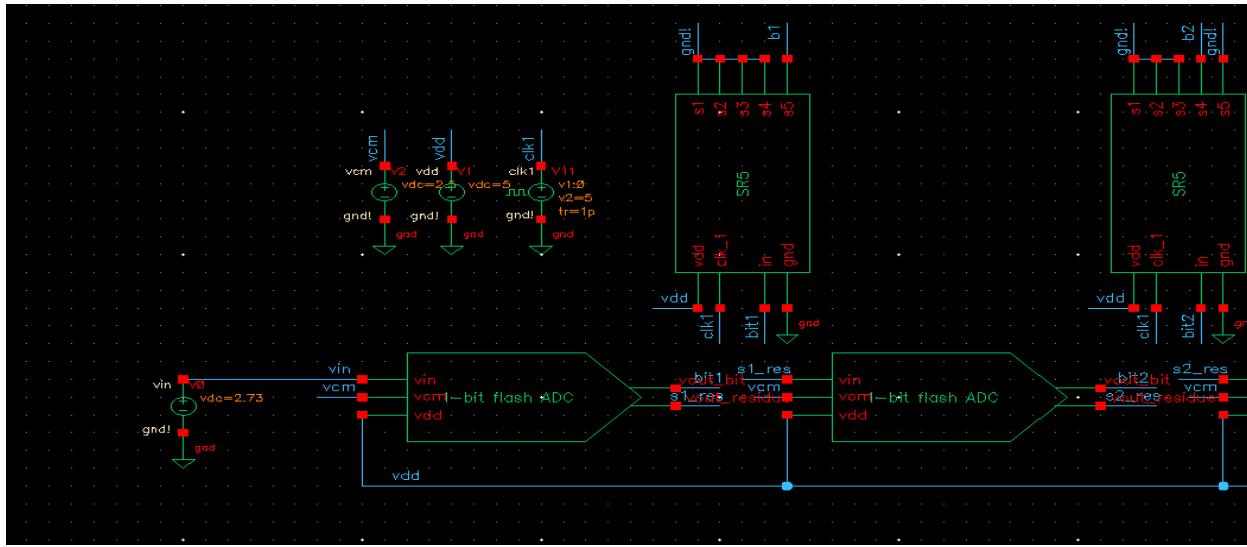


Fig: 6-bit ADC dc test schematic

Test schematic description:

Bit out from each stage is given to an ideal 8 bit DAC.

Transient test:

A slow moving ramp from 1.5V to 3.5V is given as the input to the 6-bit pipelined ADC. Output of the ideal DAC is plotted to check the resolution of the ADC. Bits are taken from each stage after time adjustment. Current at the node of V_{dd} is plotted to calculate the total power of the schematic.

Data acquisition: A strobeperiod inside the transient simulation setting of 15ns was used. A transient simulation of 505us was ran against a slow moving ramp of period 500us. Sampled points were exported as .csv files.

DC test:

DC input is given to the ADC to plot the dc/static power of the schematic.

6-bit ADC test outputs:

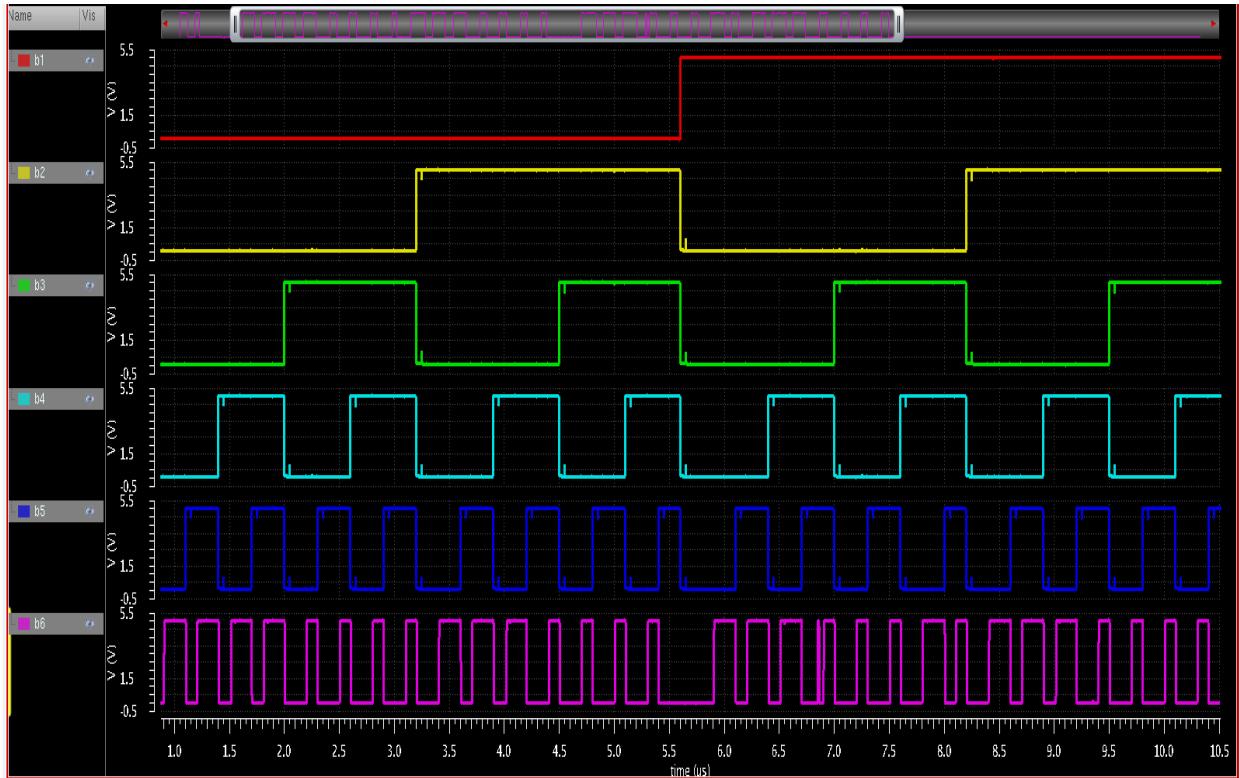


Fig: Bit output of 6-bit ADC



Fig: Transient output.

TRANSFER CHARACTERISTIC:

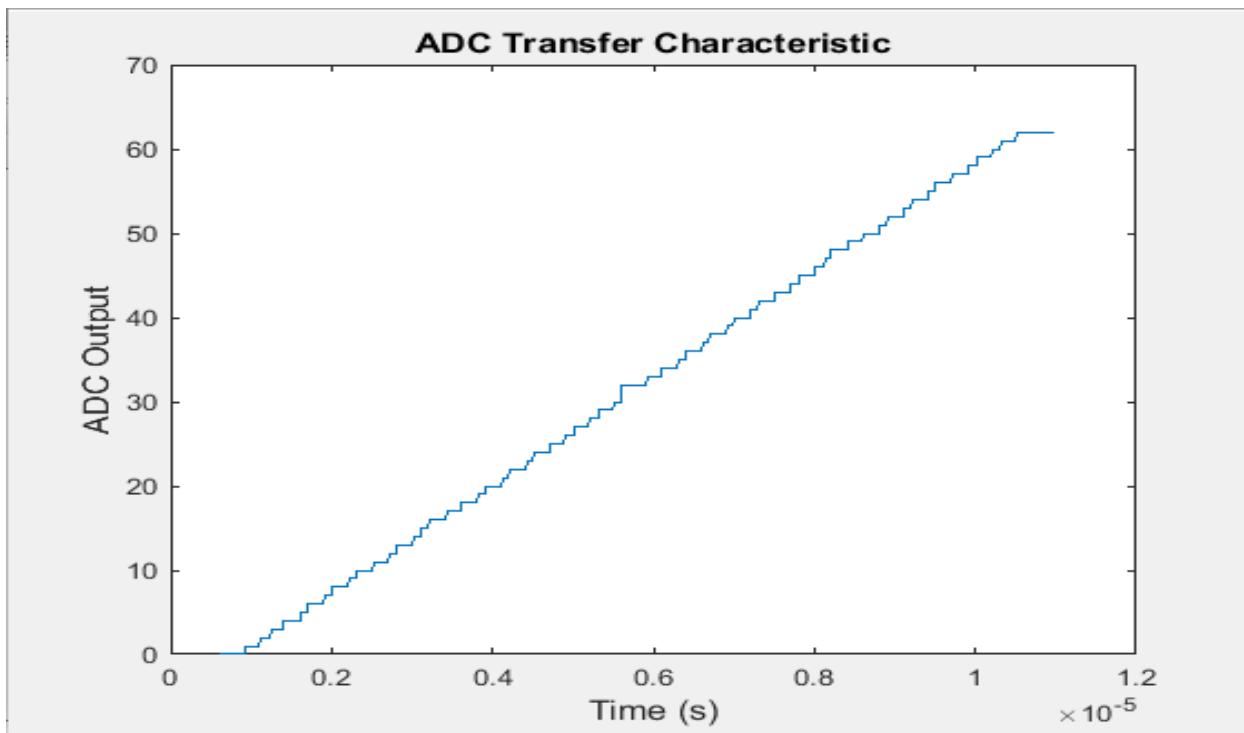


Fig: ADC transfer characteristics.

6-bit ADC Power outputs:

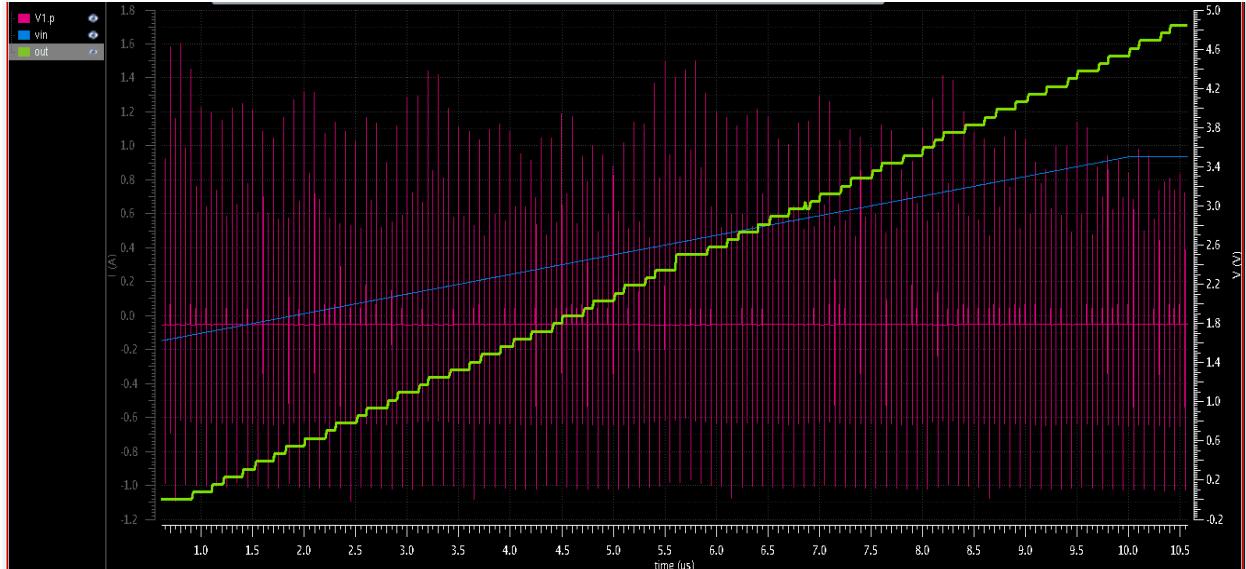


Fig: Current plot

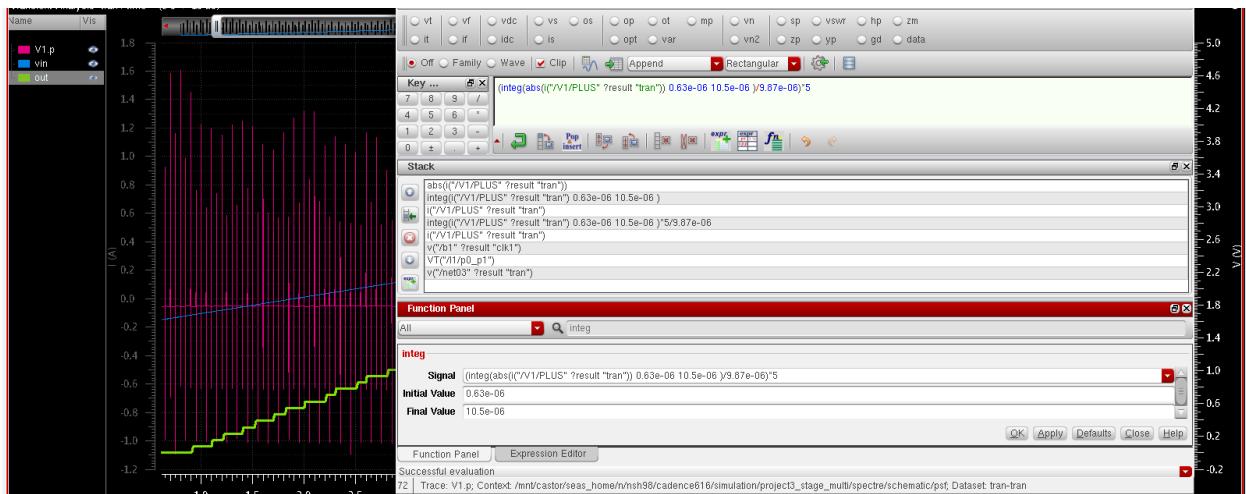


Fig: Calculator setting to calculate power

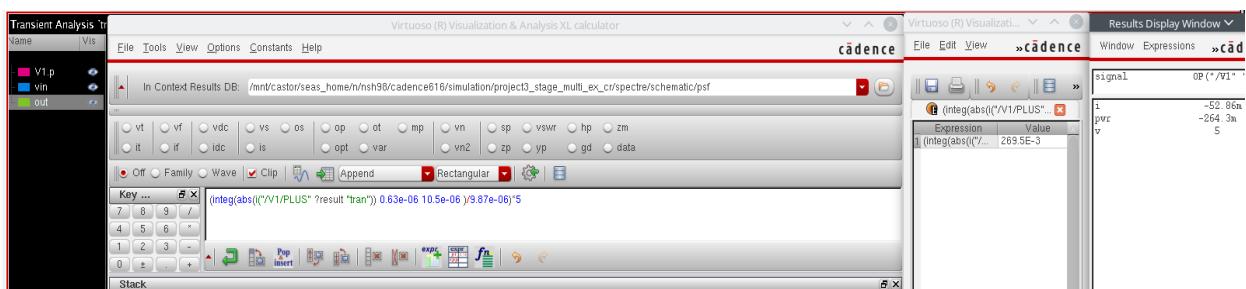


Fig: Calculator output and DC static power output

Power Analysis:

METHODOLOGY:

- Transient analysis was ran to plot the total current. Absolute value of the current was integrated over the transient period. The output was then multiplied by Vdd(5V) to get total power.
- DC simulation was performed after changing the input to a DC source. Then the power was plotted for Vdd.

REPORTED POWER:

- TOTAL POWER: 269.6mW
- STATIC POWER: 264.3mW
- DYNAMIC POWER: Total power-static power= $(269.5 - 264.3) \text{ mW}$
 $= (269.5 - 264.3) \text{ mW}$
 $= 5.2 \text{ mW}$

*Reported dynamic power makes little sense because most of the power is static. But the methodology to collect the result seems to be correct.

DNL and INL:

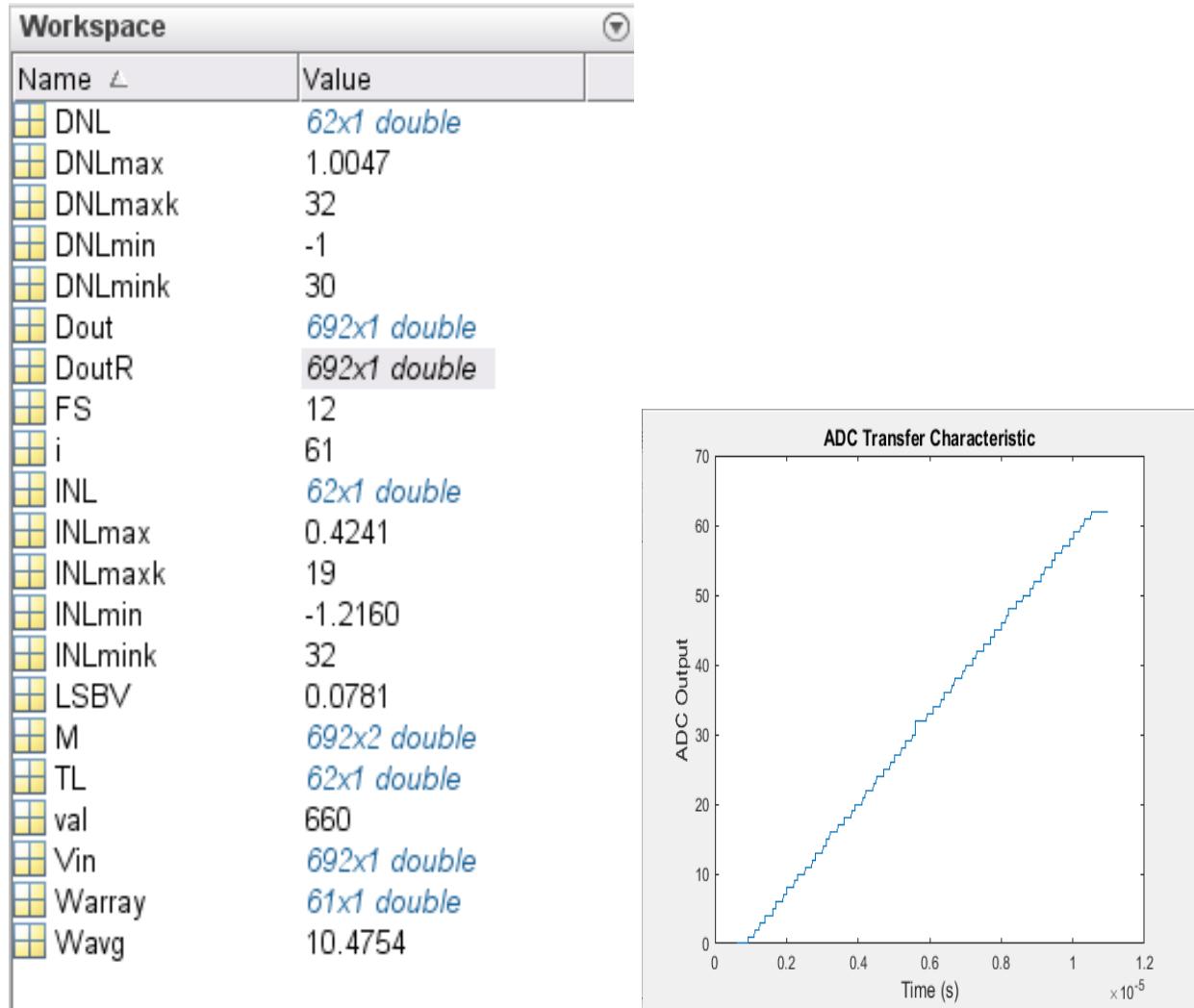


Fig: reported DNL and INL

REPORTED DNL+ = 1.0047

REPORTED DNL- = -1

REPORTED INL+ = 0.4241

REPORTED INL- = -1.2160

DNL:

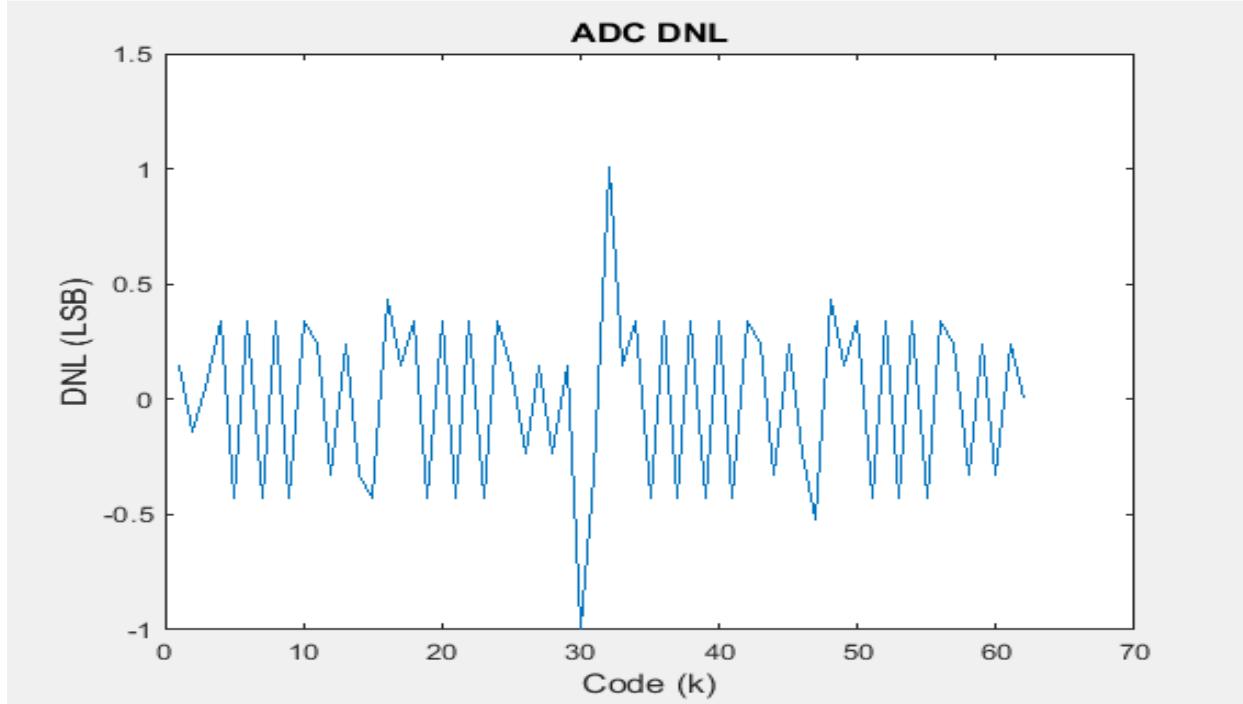


Fig: DNL plot

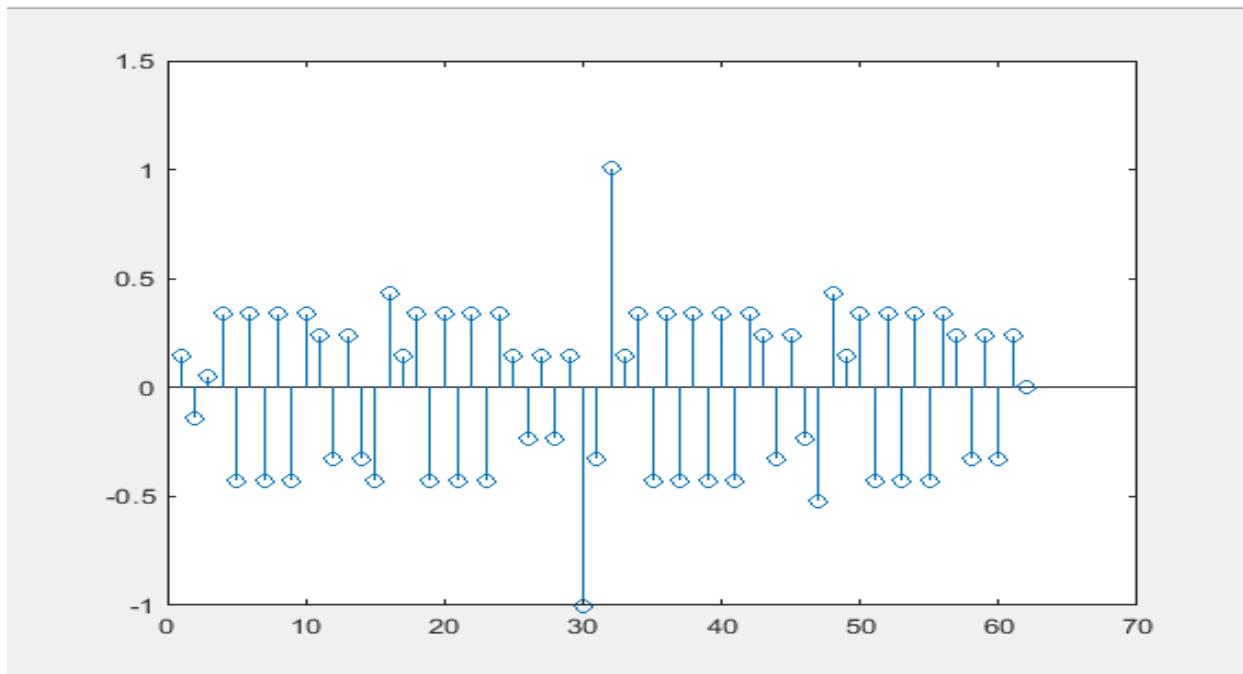


Fig: DNL stamp plot

INL:

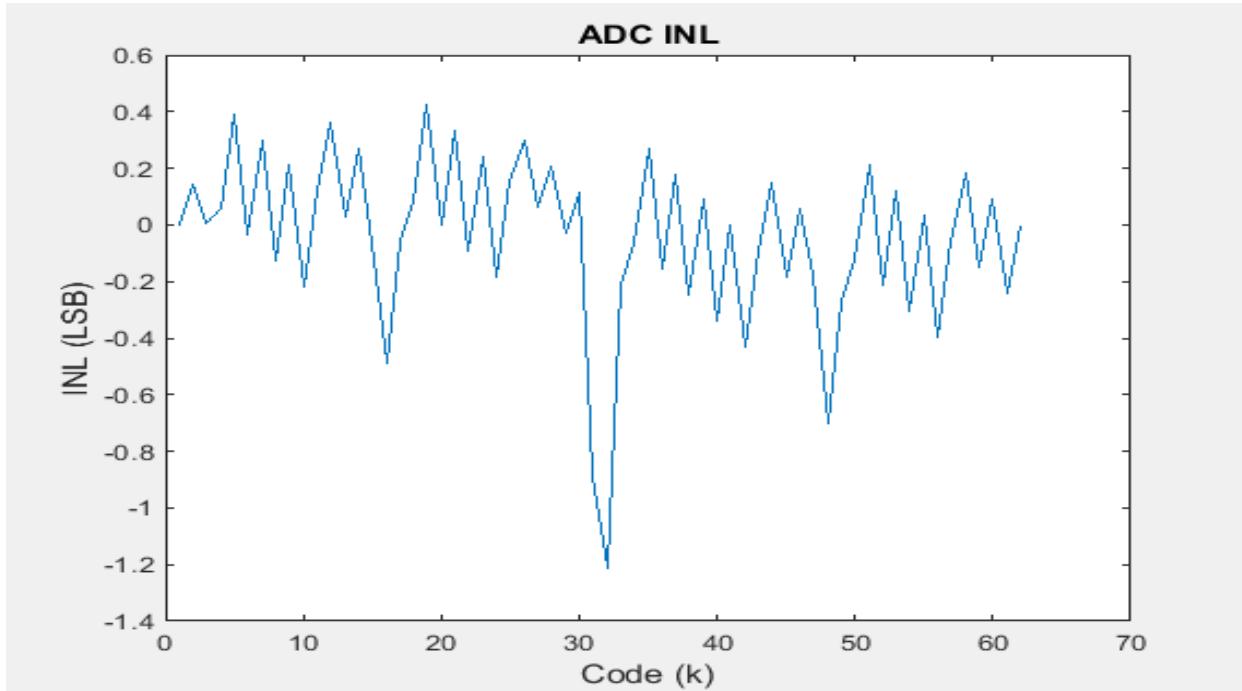


Fig: INL plot

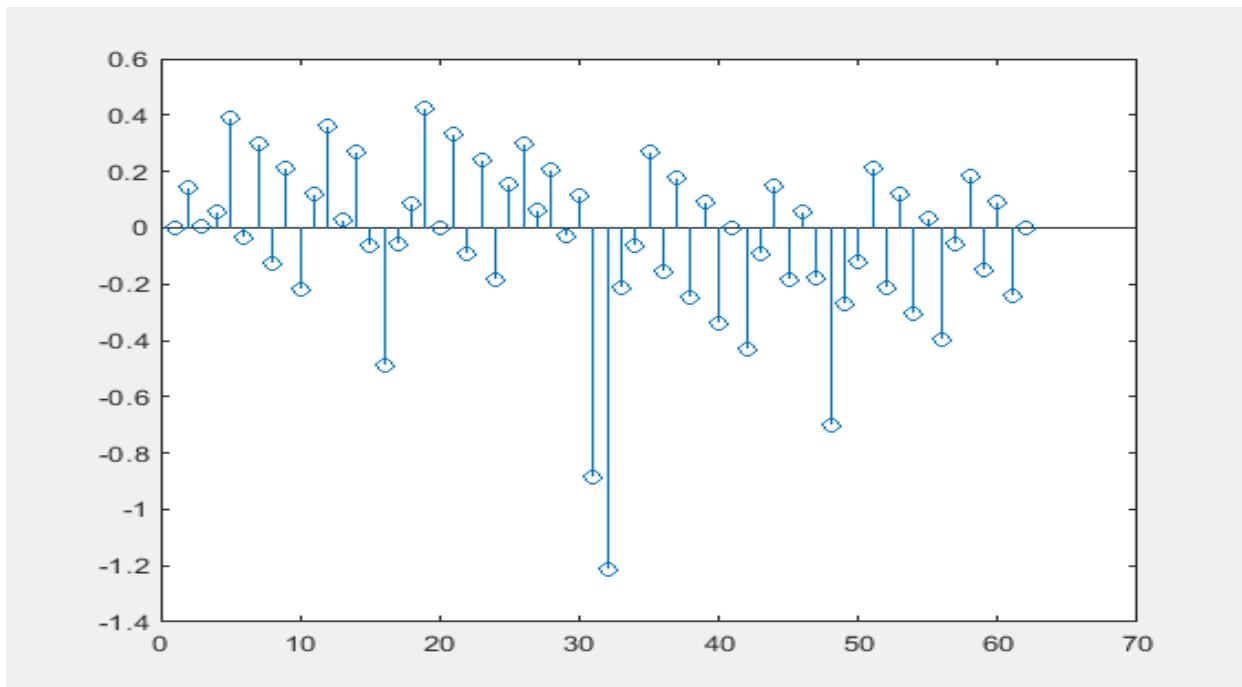


Fig: INL stamp plot

6-bit ADC test output analysis/ Quality of results:

62 distinct steps were achieved out of the designed 6-bits pipelined ADC. The code widths are unequal. The error is more near regions where the comparator changes values for bits. The most amount of error is near the most significant bit flip. Error near comparator flipping decreases with the bit significance.

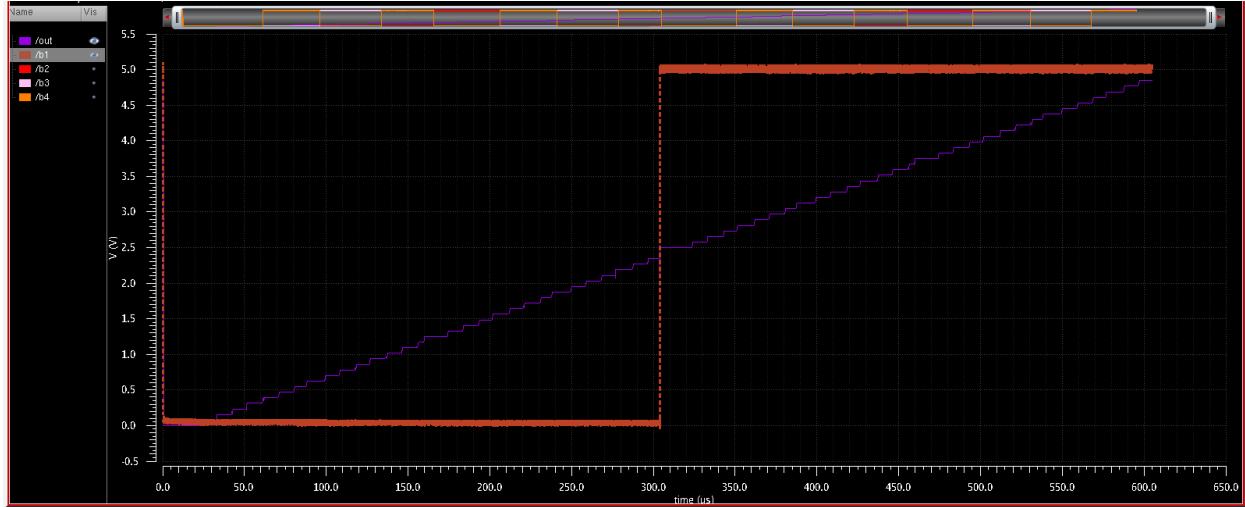


Fig: analysis of error

The largest error is where the MSB flips.

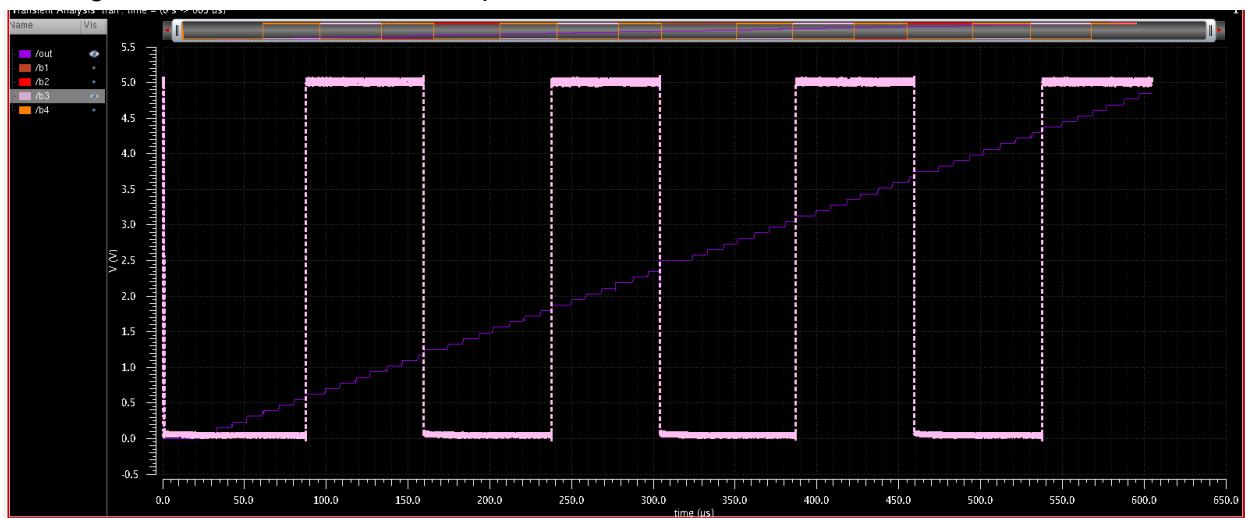


Fig: second largest error near second most significant bit.

A reason for this might be offset error in the designed 1-bit ADC.

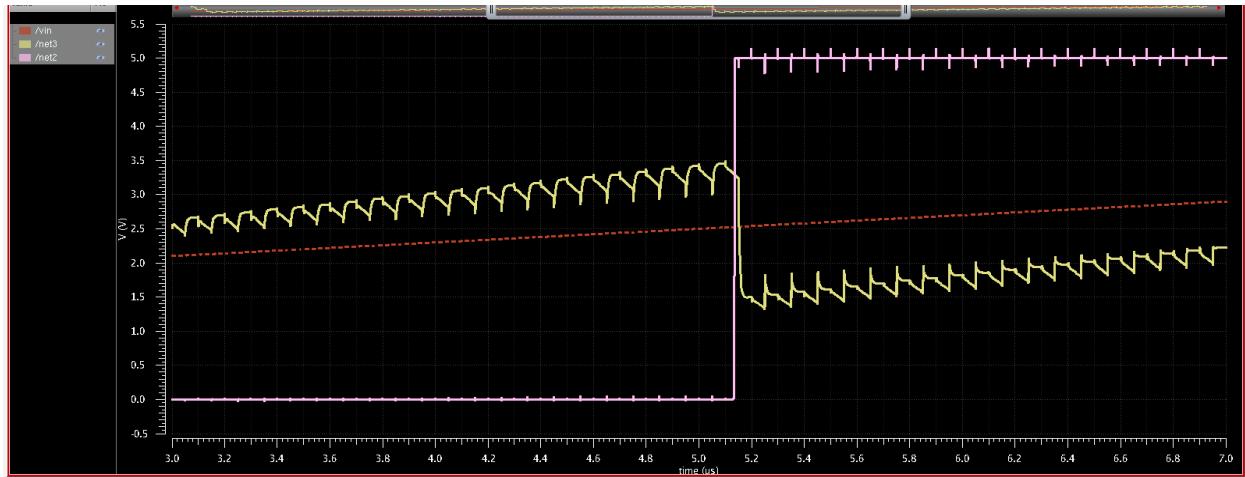


Fig: 1-bit Flash characteristics zoomed in

It is visible that the error characteristic does not exactly align with the comparator bit flip.

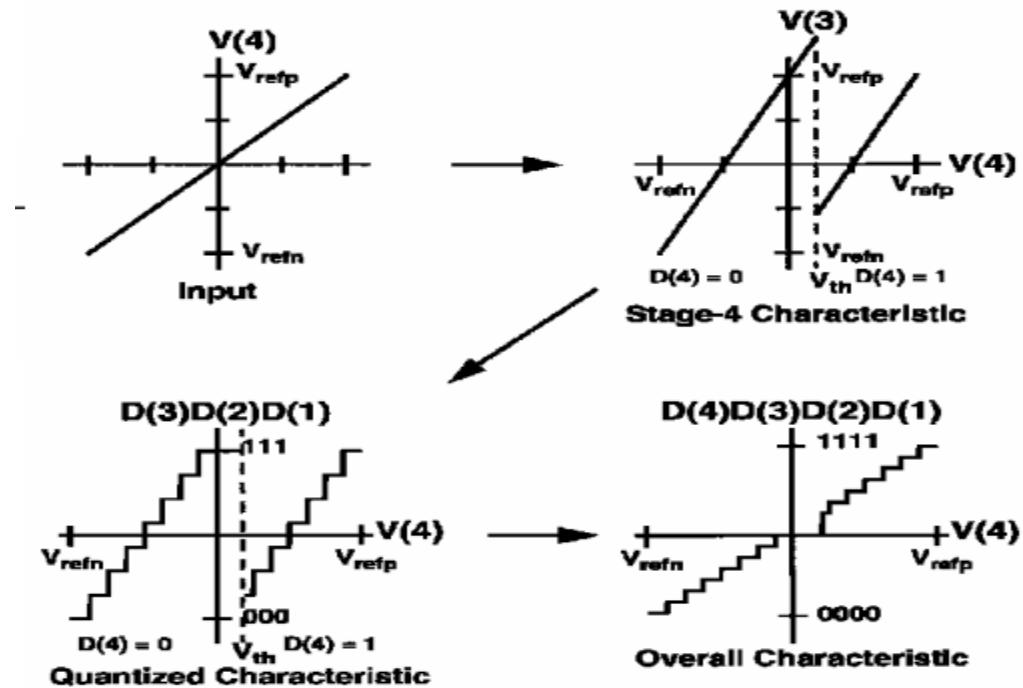


Fig: error explanation[1]

This behavior of 1-bit ADC seems to be the reason for the errors in the width sizes. Also, the output bits are unequal.

Reported Max Sampling Frequency:

REPORTED HIGHEST FREQUENCY: 10MHz

The OPAMP and THA circuit was optimized to sample at 10MHz. THA has a large error for 10MHz 2Vp-p voltage. If the frequency is increased over this the circuit is limited by the sample and hold circuit in the first place.

Conclusion:

The designed 6-bit pipelined ADC was able to generate 62 distinct step values. The reported DNL was 1.0047 and -1, reported INL was 0.4241 and -1.2160. The error was further investigated and the reason was cited[1]. The bit error is the result of offset error. The offset error was minimized by designing a preamplifier for the latch comparator. The imperfect SHA with a high settling error might also result in an improper latch characteristic since the input to latch is the output of SHA.

Another thing to notice is that the the switching in difference amplifier has a lot of spikes, meaning the switching is not perfect at 10MHz. Which might have also added no a non-ideal 1-bit characteristic.

Scope for improvements:

Latch comparator - offset .

Switch - SHA error can be reduced.

Description of Distribution of Labor:

NISHANT: Comparator pre-amplifier, Difference amplifier, 1-bit sub-ADC.

SWETHA: SHA circuit, MDAC switch, D flip flop, Shift register.

Collaborated on everything else.

Extra Credit: SNDR, SFDR, New FOM w/measured ENOB:

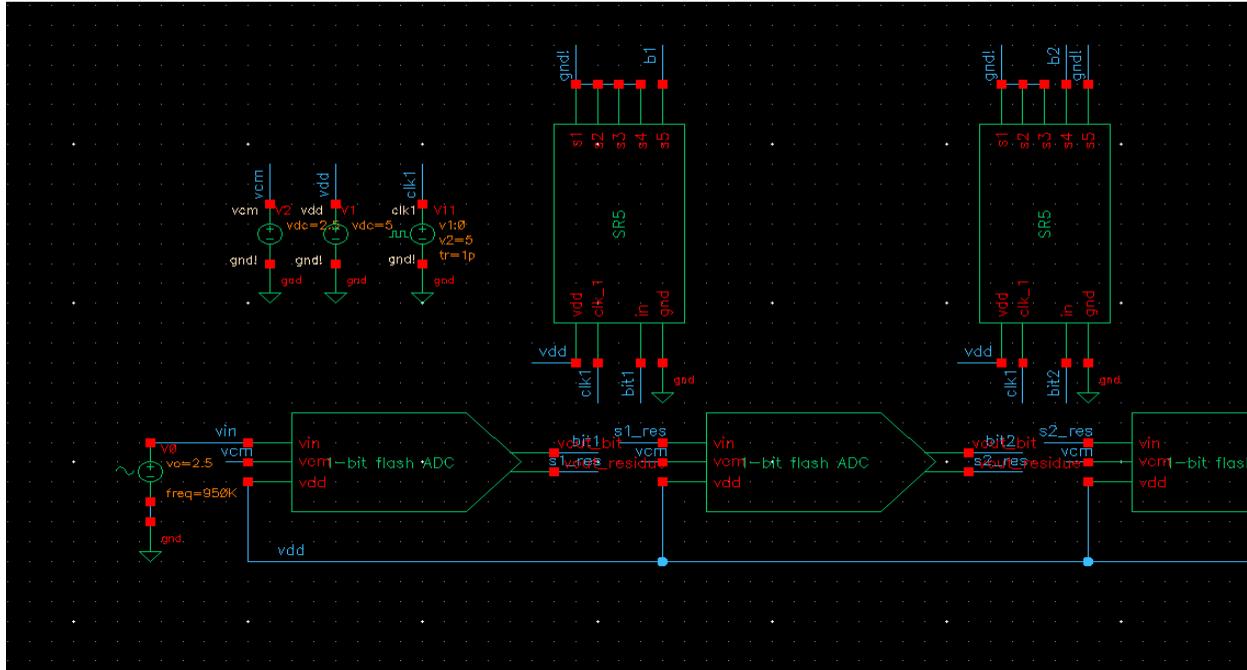


Fig: Extra credit test schematic

Description:

A sine wave of frequency 195Khz was given as an input to the ADC.

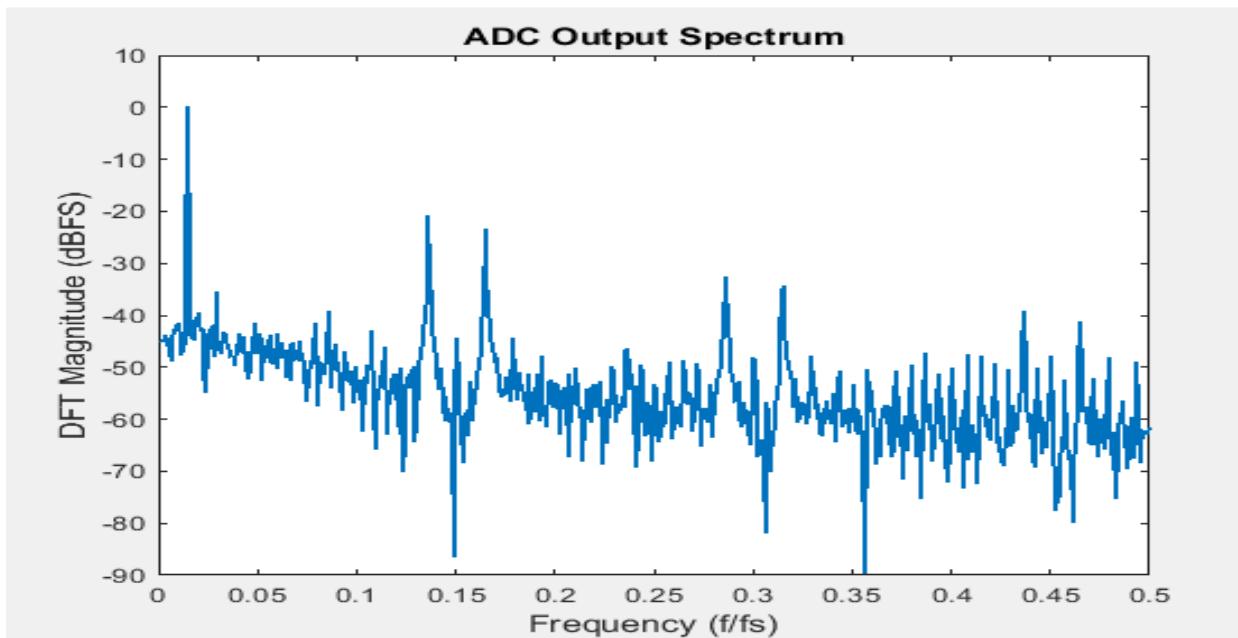


Fig: Output Spectrum

Name	Value
End	1375
ENO B	3.1925
f	<i>1x667 double</i>
FS	2.4220
N	1335
noise	<i>666x1 double</i>
s	<i>667x1 double</i>
sdBFS	<i>667x1 double</i>
SFDR	20.9790
sigbin	20
SNDR	16.3313
Start	41
time	<i>1667x1 double</i>
x	<i>1335x1 double</i>

Fig: Result: ENOB, SFDR, and SNDR

REPORTED RESULT:

ENO B: 3.19 bits

SFDR: 20.97

SNDR: 16.33

Appendix

[1] http://www.seas.ucla.edu/brweb/teaching/215D_S2012/PipeADCs.pdf

DNL INL MATLAB CODE:

```
clear all;
close all;
M= csvread("C:\Users\amrit\Downloads\matlab.csv",1,0); %read csv file
M=M(12:end,:);
LSBV=5/64; %Find LSB.

Dout= M(:,2);
DoutR=round(Dout/LSBV);%Calculate the digital level and round it to integer.
DoutR(2:4)=0;
Vin= M(:,1);

figure(1);
FS=12;
plot(Vin,DoutR);
xlabel('Time (s)', 'FontSize', FS);
ylabel('ADC Output', 'FontSize', FS);
title('ADC Transfer Characteristic', 'FontSize', FS);

TL= zeros(58,1);
for i=1:58
    val = find(DoutR == i,1);
    if(size(val,1) == 0)
        TL(i) = TL(i-1);
    else
        TL(i,1) = val;
    end
end
%
Wavg=(TL(58)-TL(1))/57;%Calculate average code width.
% Wavg=abs(Wavg);
Warray=diff(TL);%Calculate code width

%Calculate DNL.
DNL=zeros(58,1);
for i=1:57
    DNL(i)=(Warray(i)-Wavg)/Wavg;
end
```

```

%Calculate INL
INL=zeros(58,1);
for i=1:57
INL(i+1)=sum(DNL(1:i));
end

%Plot DNL and INL.
figure(2)
FS=12;
plot(DNL);
xlabel('Code (k)','FontSize',FS);
ylabel('DNL (LSB)','FontSize',FS);
title('ADC DNL','FontSize',FS);
figure(3)
plot(INL);
xlabel('Code (k)','FontSize',FS);
ylabel('INL (LSB)','FontSize',FS);
title('ADC INL','FontSize',FS);

%Find max/min DNL and INL.
DNLmax=max(DNL);
DNLmaxk=find(DNL==DNLmax);
INLmax=max(INL);
INLmaxk=find(INL==INLmax);
DNLmin=min(DNL);
DNLmink=find(DNL==DNLmin);
INLmin=min(INL);
INLmink=find(INL==INLmin);

```

EXTRA CREDIT MATLAB CODE:

```
clear all;
x=csvread("/home1/n/nsh98/sndr_sfdr.csv",1,0);%Import data.
%Start and End are set to make sure Cycle/N=fx/fs=95/1000=19/200 so that
%spectral leakage will not happen.
Start=41;
End=1375;
time=x(:,1);
x=x(:,2);
FS=(max(x(Start:End))-min(x(Start:End)))/2;%Calculate full scale.
x=x(Start:End);%Take 19 cycles with 200 points.
N=length(x);
figure()
plot(time(Start:End),x);
%Perform FFT
s=abs(fft(x));
s=s(1:N/2);
s(1)=0;%Eliminate the DC signal.
sdBFS=20*log10(2*s/N/FS);%Calculate magnitude in dBFS.
f=(0:N/2-1)/N;
%Plot output spectrum.
figure()
plot(f,sdBFS,'linewidth',2);
xlabel('Frequency (f/fs)', 'FontSize', 12);
ylabel('DFT Magnitude (dBFS)', 'FontSize', 12);
title('ADC Output Spectrum', 'FontSize', 12);
%Calculate SNDR and SFDR.
sigbin=find(s==max(s));
noise=vertcat(s(1:sigbin-1),s(sigbin+1:end));%Find noise.
SNDR=10*log10(s(sigbin)^2/sum(noise.^2));%Calculate SNDR.
SFDR=max(sdBFS)-max(sdBFS(sdBFS~=max(sdBFS)));%Calculate SFDR.
ENOB=(SFDR-1.76)/6.02;
```