

**UNIVERSITY OF PENNSYLVANIA**

**ESE 668: MIXED SIGNAL CIRCUIT AND MODELING**

**PROJECT 1  
OP AMP DESIGN**

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1. AIM: To design an OPAMP to meet the given specifications and simulate the circuit on cadence virtuoso.

**SPECIFICATIONS:**

- Total Power  $\leq 2 \text{ mW}$
- Slew Rate: SR  $\geq 20\text{V/us}$
- DC Gain  $\geq 75\text{dB}$
- Gain Bandwidth Product (GBW)  $\geq 25\text{MHz}$
- CMRR  $\geq 60 \text{ dB}$
- Input Common Mode Range (ICMR): ICMR  $\geq 0.5 \cdot V_{dd}$
- Phase Margin  $\geq 60^\circ$

**GIVEN:**

- Single ideal DC current source  $\leq 60\text{uA}$
- $V_{dd} \leq 5\text{V}$
- $C_L = 2\text{pF}$

## 2.THEORY:

### 2.1 CHAPTER 1: INTRODUCTION TO OP AMP

Operational amplifiers are linear devices that exhibit properties close to that of an ideal amplifier. For this reason op amps are widely used in applications such as an inverting amplifier, buffer, active rectifier, signal conditioning, and in mathematical operations such as addition, subtraction, integration, and differentiation.

#### IDEAL OP AMP CHARACTERISTICS:

- Infinite Differential Gain
- Zero Common Mode Gain
- Zero Offset Voltage
- Zero Bias Current
- Infinite Bandwidth

#### OP AMP INPUT ATTRIBUTES

- Infinite Impedance
- Zero Bias Current
- Respond to Differential Voltages
- Do Not Respond to Common Mode Voltages

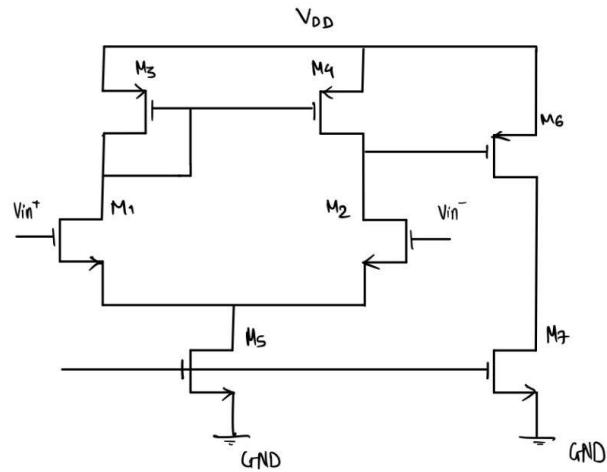
#### OP AMP OUTPUT ATTRIBUTES

- Zero Impedance

## 2.2 CHAPTER 2: OP AMP TOPOLOGIES

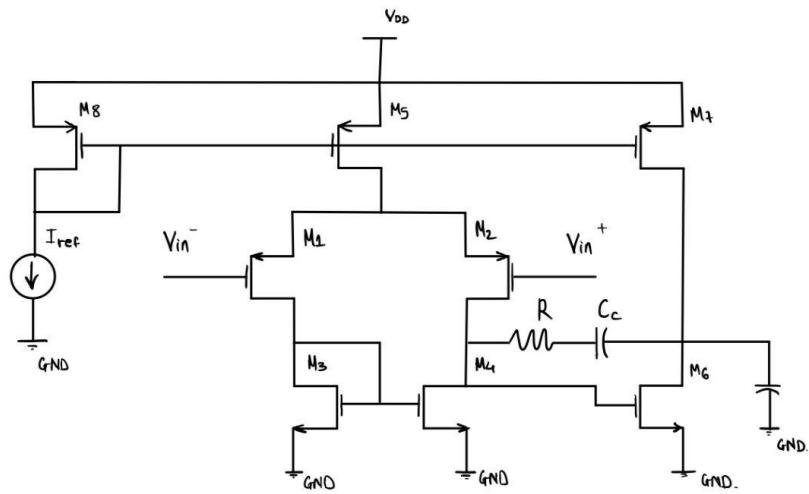
Topology 1: 2 stage op amp:

The most basic of op amps have 2 stages- a differential amplifier stage, followed by a gain stage- usually a common source amplifier.



Uncompensated 2-stage NMOS differential pair op amp

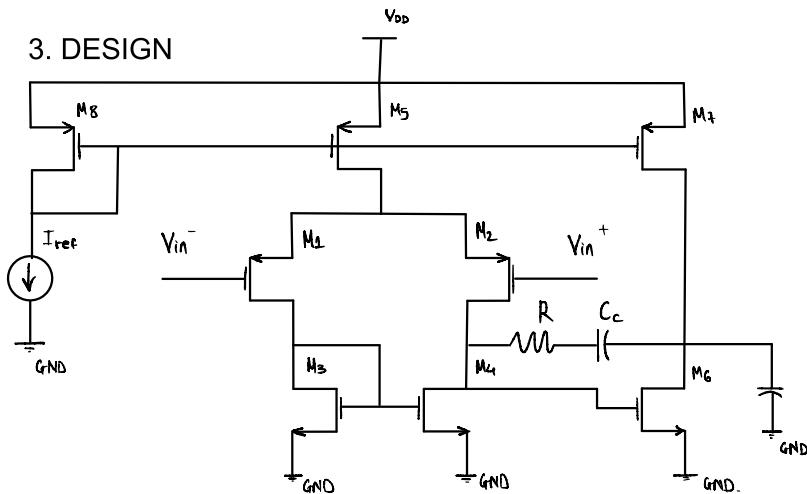
The circuit is unstable because the poles are very close to each other on the imaginary axis. To fix this we can add a piece of circuitry. A compensation capacitor is added to introduce a new dominant pole. The compensation capacitor is sized in such a way that the phase margin is above 45 degrees, ideally near 60 degrees. If the phase margin is above 60 degrees, nearing 90 degrees, the system is still stable though it increases the settling time and hence the system is slow.



2 stage PMOS-differential pair OPAMP

In addition to adding compensation circuitry(resistance and a capacitor) the NMOS differential pair is also replaced by a PMOS differential pair because PMOS transistors have better 1/F noise. Also, PMOS input stage results in a higher slew rate than an NMOS.

### 3. DESIGN



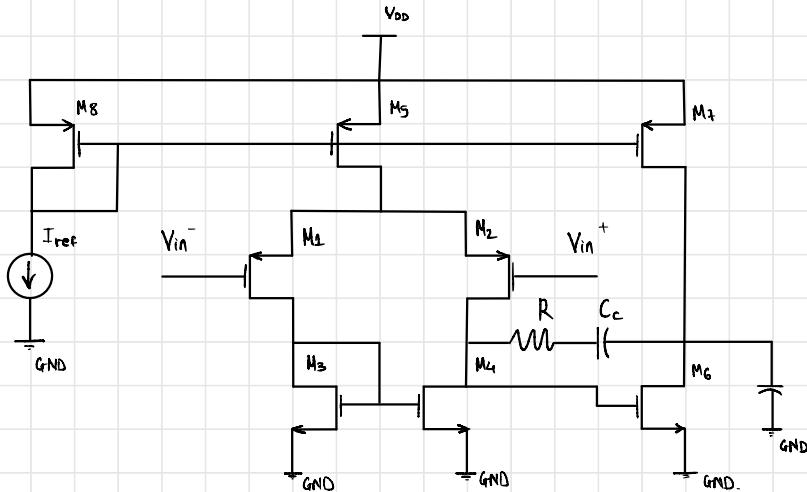
2 stage PMOS-differential pair OPAMP

Specifications:

Given:  $I_{ref} \leq 60\mu A$ ,  $V_{dd} \leq 5V$ ,  $\frac{1}{2} C_L = 2pF$

- Total power  $\leq 2mW$
- Stew Rate:  $SR \geq 20V/\mu s$ .
- DC gain  $\geq 75dB$
- Gain Bandwidth Product (GBW)  $\geq 25MHz$
- CMRR  $\geq 60dB$
- Input Common Mode Range (ICMR)  $\geq 0.5 V_{dd}$ .
- Phase Margin  $\geq 60^\circ$

# DESIGN STRATEGY



## - CURRENT MIRROR: $[M_8, M_5, \& M_7]$

- sum of currents in all branches is limited by the power specification.
- $I_D$  of  $M_8$  sets the reference current for the current mirror.
- current in the differential amplifier branch & common source branch depends on the ratio of their  $W/L$  &  $[W/L]_{M_8}$ .
- current in the differential amplifier branch & common source branch are divided proportionate to each stage's gain.
- current in differential branch [ $I_D$  of  $M_5$ ] is also designed according to the slew rate specification.
- drop across  $M_5$  controls the ICMR specification.

## - DIFFERENTIAL AMPLIFIER: $[M_1, M_2, M_3, M_4]$

- gain of the opamp:  $g_m (r_{D2} || r_{O4}) \cdot g_m (r_{D6} || r_{O7})$ .
- therefore, we try in design  $M_1, M_2, M_3, \& M_4$  according to the gain specification.
- $M_3 \& M_4$  also controls ICMR specification.

## - COMMON SOURCE: $[M_6]$

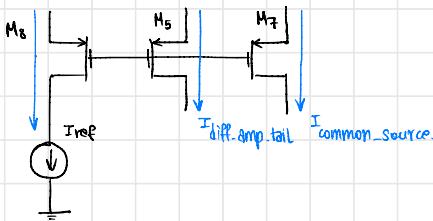
- we try to design  $M_6$  according to the gain specification.

## - COMPENSATION CIRCUIT ( $C_c$ )

- $C_c$  controls the dominant pole and hence is designed by the phase margin & slew rate specifications.

# DESIGN:

current mirror: transistor sizing:



— MOS parameters AMI 0.60  $\mu$  CSN

$$V_{t0} = 0.7068 \text{ V} \approx 0.8 \text{ V}$$

$$\begin{aligned} \mu_n &= 530 \text{ cm}^2/\text{V.s} & \mu_p &= 200 \text{ cm}^2/\text{V.s} \\ &= 0.053 \text{ m}^2/\text{V.s} & &= 0.02 \text{ m}^2/\text{V.s} \end{aligned}$$

$$box = 14.1 \text{ nm}$$

$$\epsilon_{ox} = 3.9 \text{ fF}$$

$$= 3.9 (8.85 \times 10^{-12}) / \text{m}$$

$$C_{ox} = \frac{\epsilon_{ox}}{box} = \frac{0.002447 \text{ F/m}^2}{14.1 \text{ nm}}$$

$$\mu_n C_{ox} = 129.69 \mu \quad f_p C_{ox} = 48.94 \mu$$

Phase Margin:  $\geq 60^\circ$

$$\text{power} \leq 2 \text{ mW} \quad \text{Slew Rate: } \geq 20 \text{ V/ps}$$

$$20 \text{ V/ps} \leq I_{\text{diff.amp.tail}}$$

$$\text{power} = V \cdot I$$

$$C_c$$

$$C_c \geq 0.22 C_L$$

then for 20 V/ps SR

$$C_c \geq 0.44 \text{ pF}$$

$$I_{\text{diff.amp.tail}} \geq 20 \text{ pA}$$

$$\text{power} \leq V_{DD} \cdot I_{\text{budget}} \quad \text{where } I_{\text{budget}} = I_{\text{ref}} + I_{\text{diff.amp}} + I_{\text{common-source}}$$

$$2 \text{ mW} \leq 5 \cdot I_{\text{budget}}$$

$$C_c \approx 1 \text{ pF}$$

then if  $I_{\text{ref}} = 20 \mu\text{A}$

$$\text{let } I_{\text{diff.amp.tail}} = 2 \times I_{\text{ref}}$$

$$I_{\text{budget}} \geq 400 \mu\text{A} \quad \text{— where } I_{\text{ref}} = 20 \mu\text{A}, I_{\text{diff.amp.tail}} = 40 \mu\text{A}, \text{then } I_{\text{common-source}} \leq 360 \mu\text{A}.$$

$$A_v \geq 75 \text{ dB} \approx 6000 \text{ V/V} \quad \boxed{A_v = A_{v1} \cdot A_{v2}}$$

\* there are 2 gain stages in the OPAMP. The differential amplifier has less gain compared to the common source stage.

Hence, the current budget is divided such that the first stage has less current compared to the second stage.

$$\text{Q. } I_{\text{ref}} = \frac{1}{2} I_{\text{diff.amp.tail}}$$

$$1 - \eta_L \approx 0.16$$

$$\text{if } \left[ \frac{W}{L} \right]_{M8} = \frac{10 \mu}{1.2 \mu} \quad \text{then} \quad \left[ \frac{W}{L} \right]_{M5} = \frac{20 \mu}{1.2 \mu}$$

$$\eta_L = 1 - 0.16$$

## differential amplifier transistor sizing

$$\text{gain} = g m_2 (r_0 2 || r_0 4), g m_6 (r_0 6 || r_0 7)$$

i.e. gain depends on  
-  $gm_1, rD_2, g, rD_4$

taking  $H\pi_3$  topology as the base.

to increase gain we increase  
 $q_m$ ,  $nO_2$ ,  $\frac{1}{2} n_4$

increase in  $L$  increases  $\tau_0$  of the transistor.

$$- L = 1.8 \text{ p. for } M_1, M_2, M_3, \text{ & } M_4.$$

$$- I \propto W/L$$

- to compensate  $W$  is to be increased as well.

- we also try to increase  $g_{m1}$

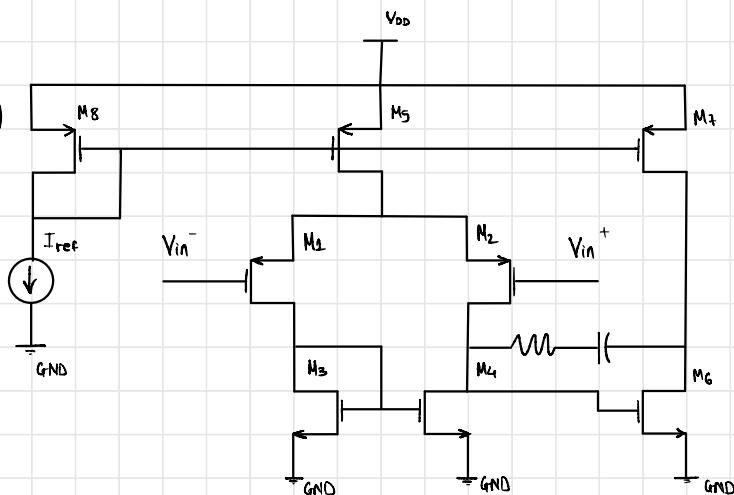
$$- qm_1 = 2\pi [GB] c$$

$$- q_{M1} = 2\pi [30M] (> 1 \text{ pF})$$

$$- q_m > 254.5 \mu \text{ at } C = 1.35 \mu F$$

$$- \text{ gm} = \sqrt{2 \cdot \text{ No Cox} \cdot \frac{W}{L} \cdot \text{ ID}}$$

$$-\begin{bmatrix} W \\ L \end{bmatrix}_1 = \frac{g m_1^2}{2 \mu p \cos ID} = \frac{(350 \mu)^2}{2 \times 49 \mu \times 204} \approx 62.5$$



$$ICMR \geq 0.5V_{DD}$$

$$ICMR \geq 0.5(5)$$

$$ICMR \geq 2.5.$$

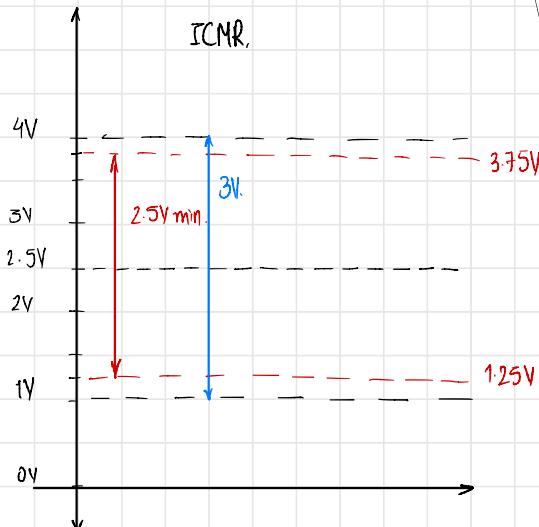
$$I_{D3} = \frac{1}{2} \mu n C_{Ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

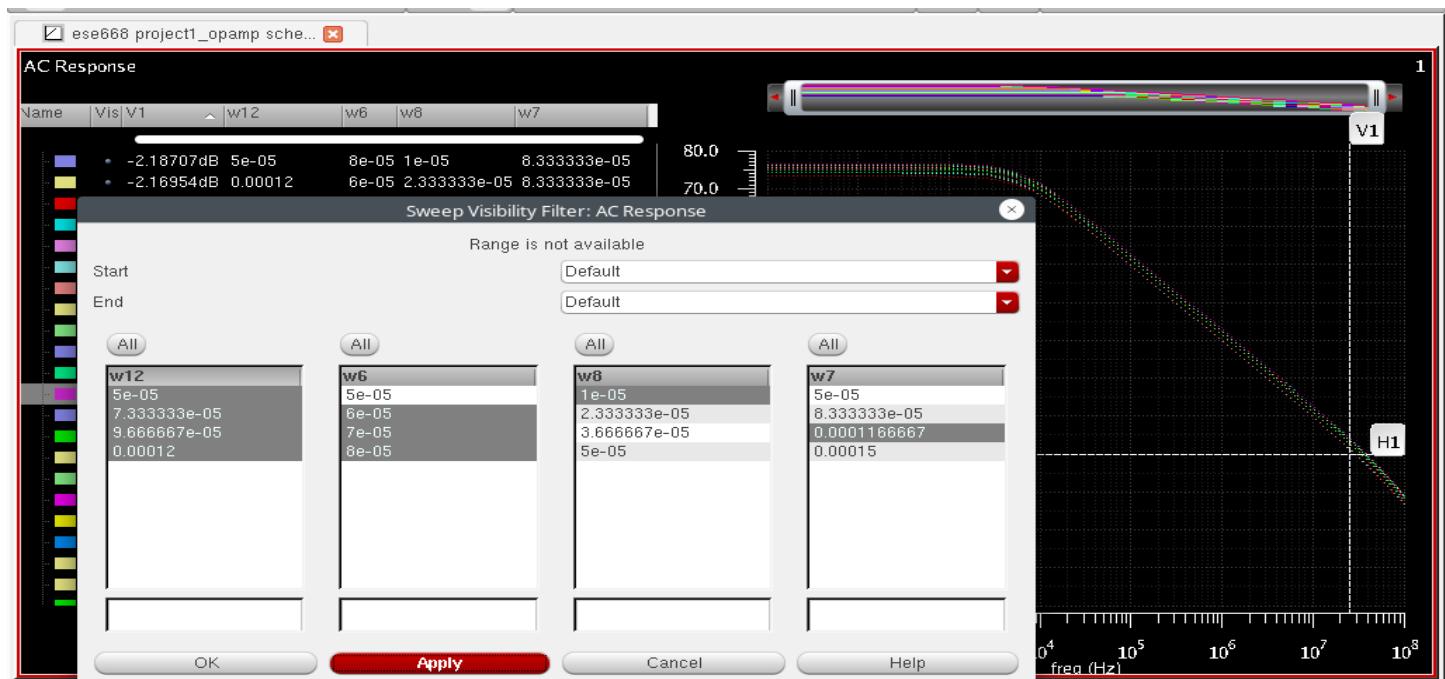
$$\left[ \frac{W}{L} \right]_3 > \frac{2I_{D3}}{\mu n C_{Ox}} \frac{1}{(V_{GS} - V_{TH})^2}$$

$$\left[ \frac{W}{L} \right]_3 > \frac{2[20\mu]}{130\mu} \frac{1}{(1-0.8)^2}$$

$$\left[ \frac{W}{L} \right]_3 > 7.7$$

$$\left[ \frac{W}{L} \right]_3 \approx 11.$$

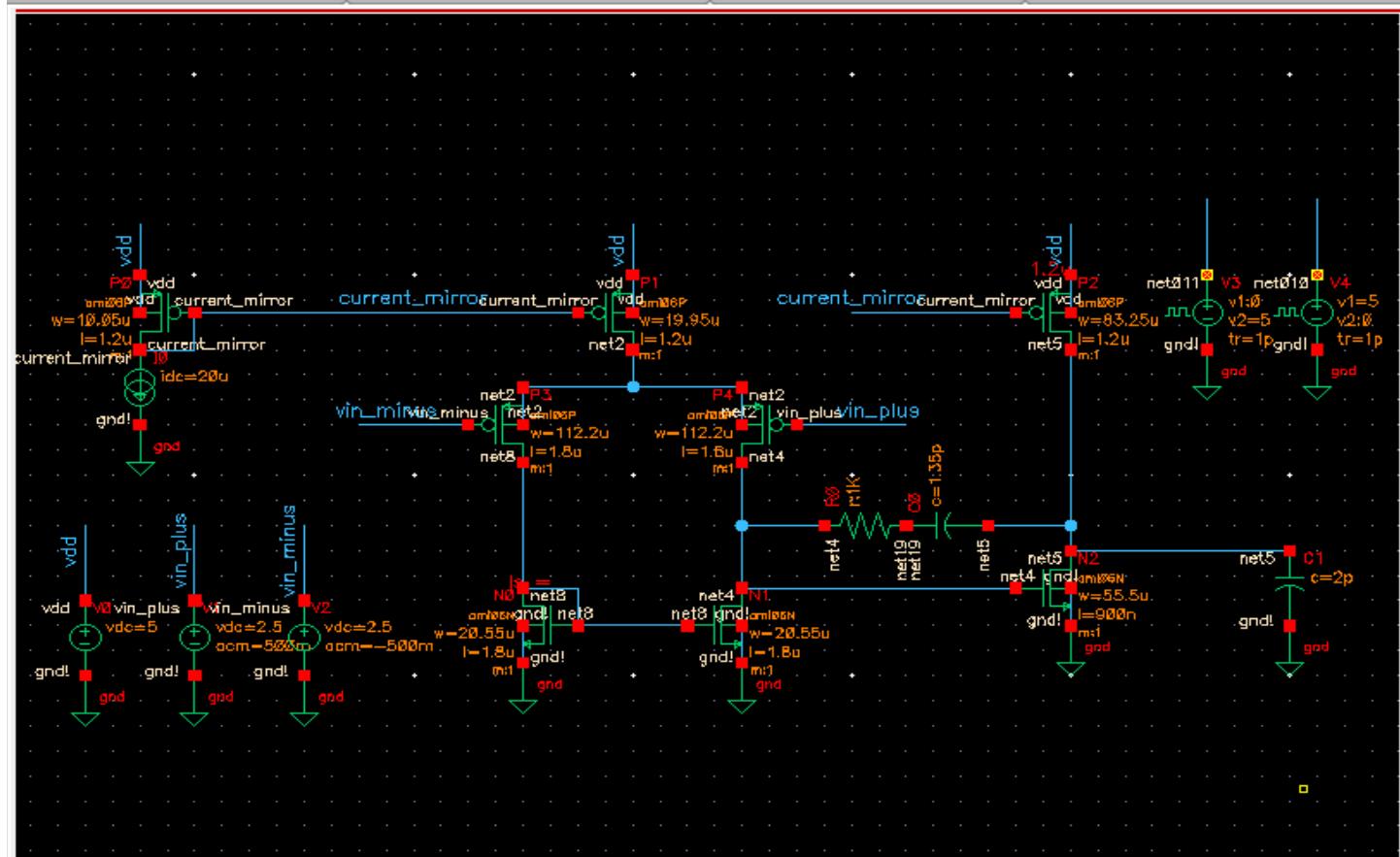




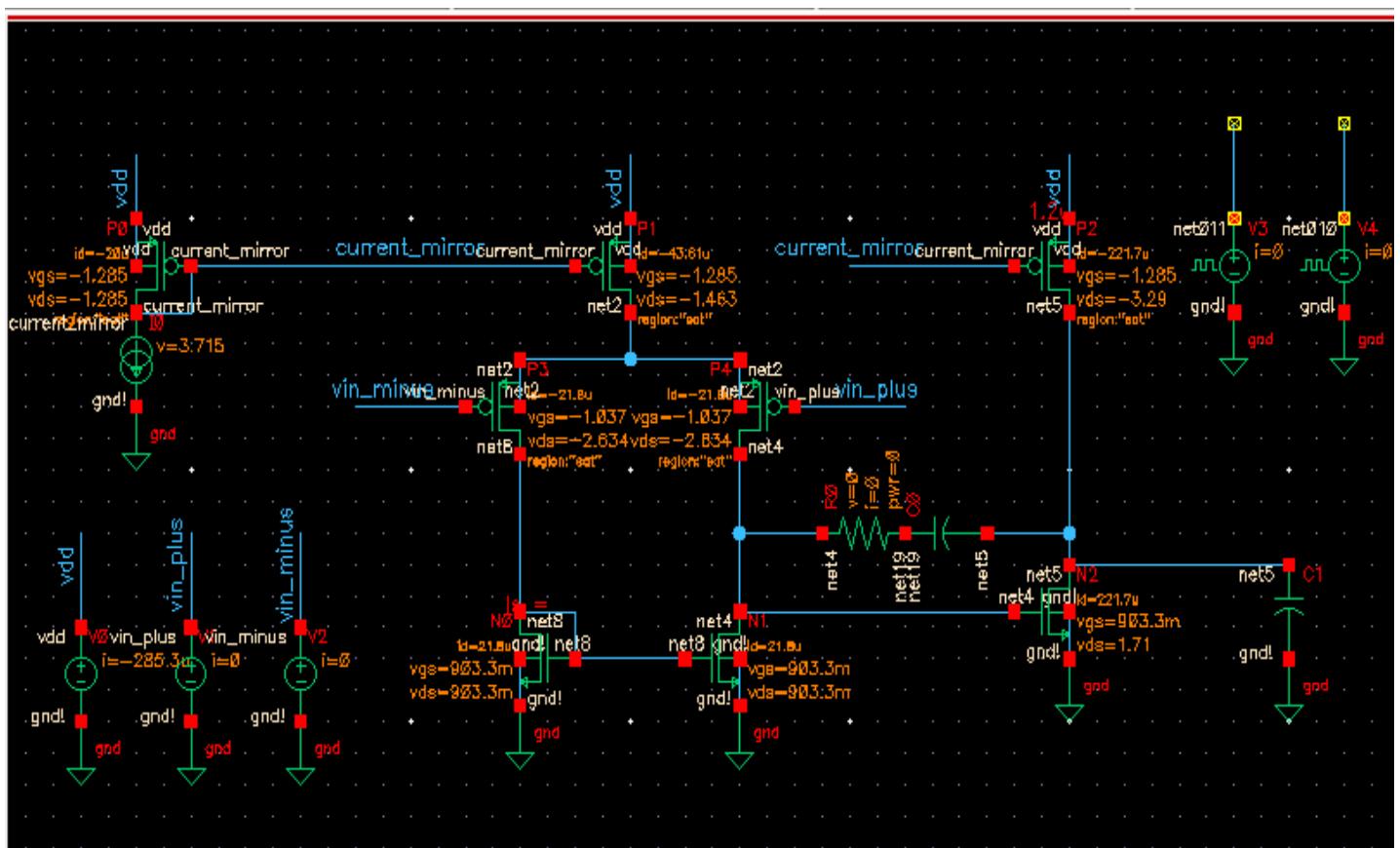
Parametric sweep\*

\*parametric sweep to get optimised results after hand calculations.

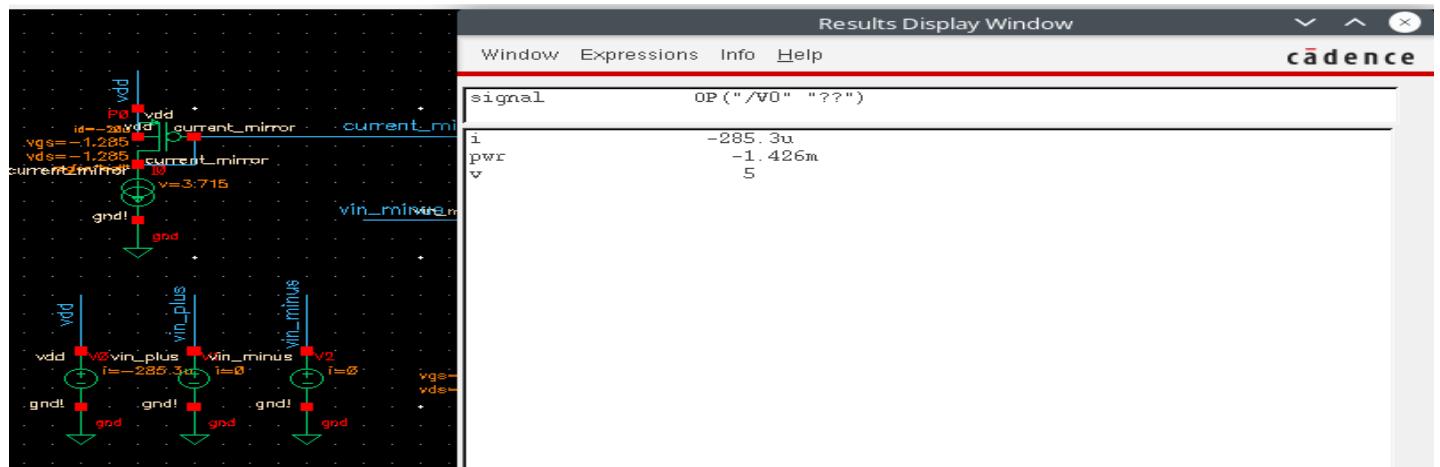
## 4. OBSERVATION



Sized schematic.



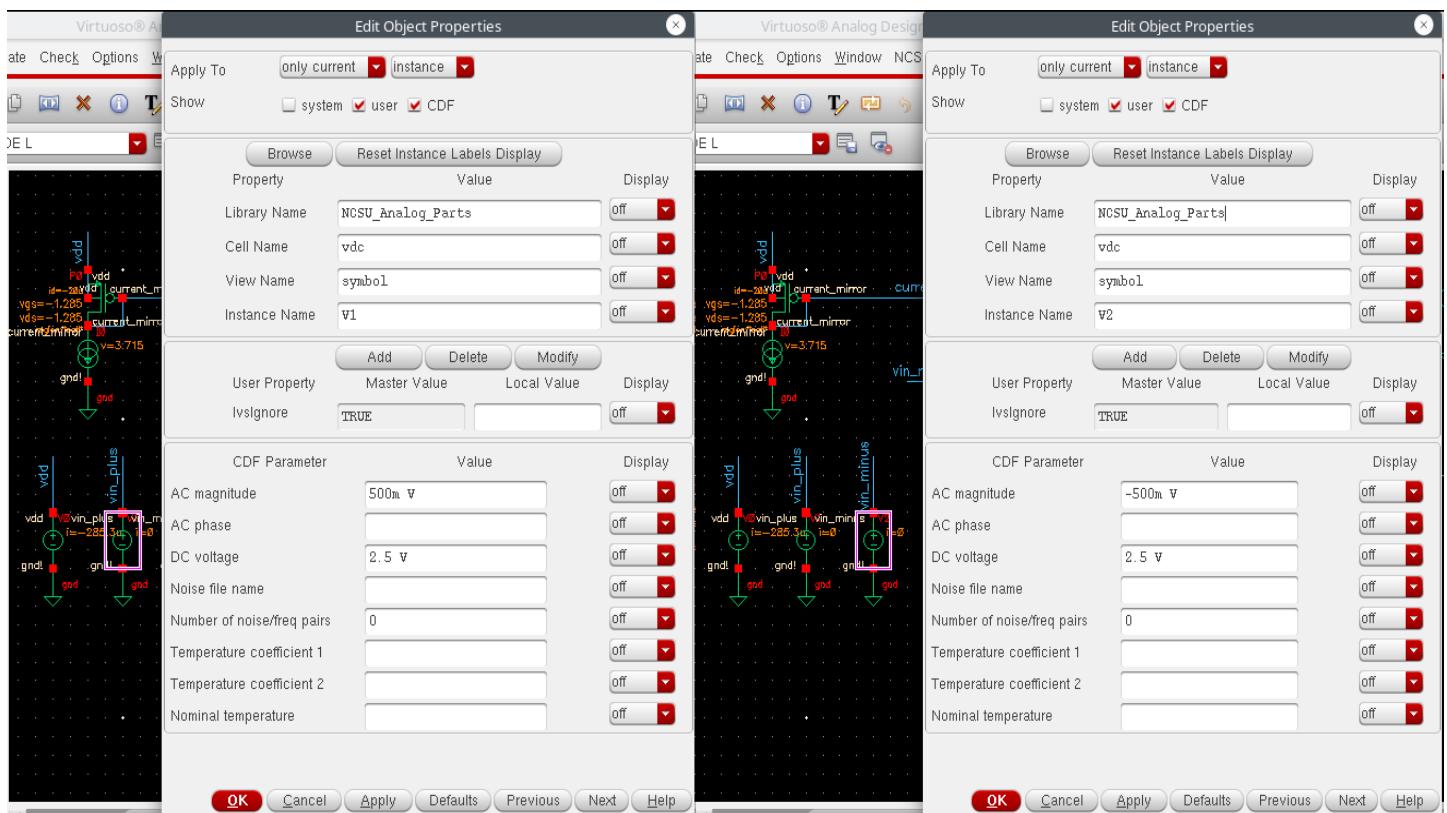
DC simulation- DC operating points.



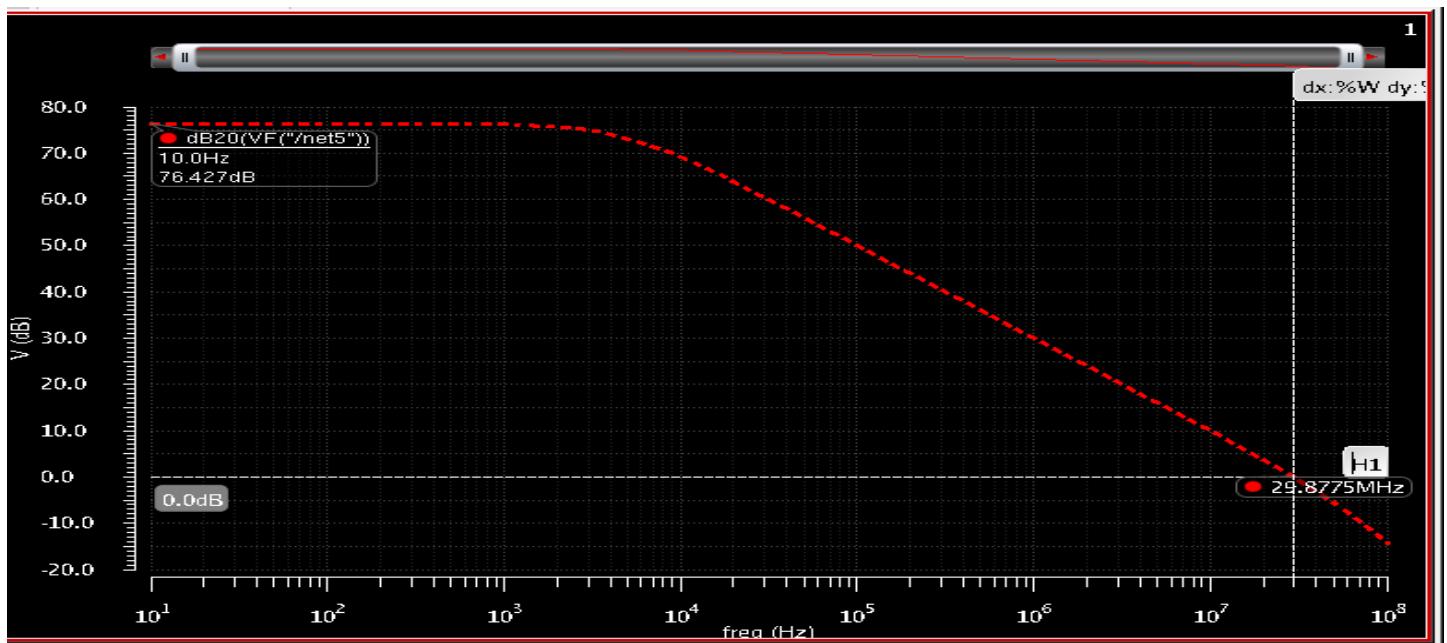
Specification: power observation\*

REPORTED POWER: 1.426mW

\*DC analysis: print DC operating points: Vdd(Vdc voltage source)



AC simulation test set up(dialogue box corresponds to supply highlighted in pink)

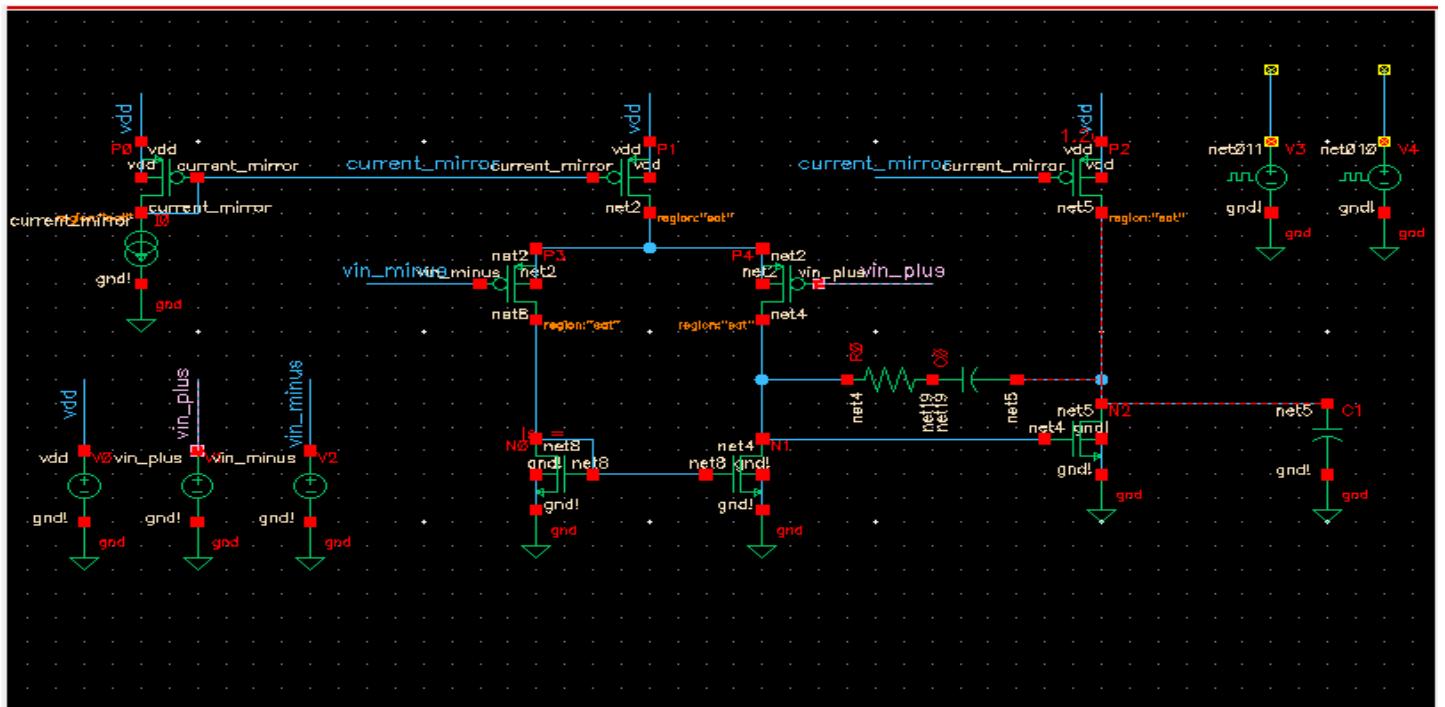


Specification: DC gain and GBW\*

REPORTED DC GAIN: 76.427dB

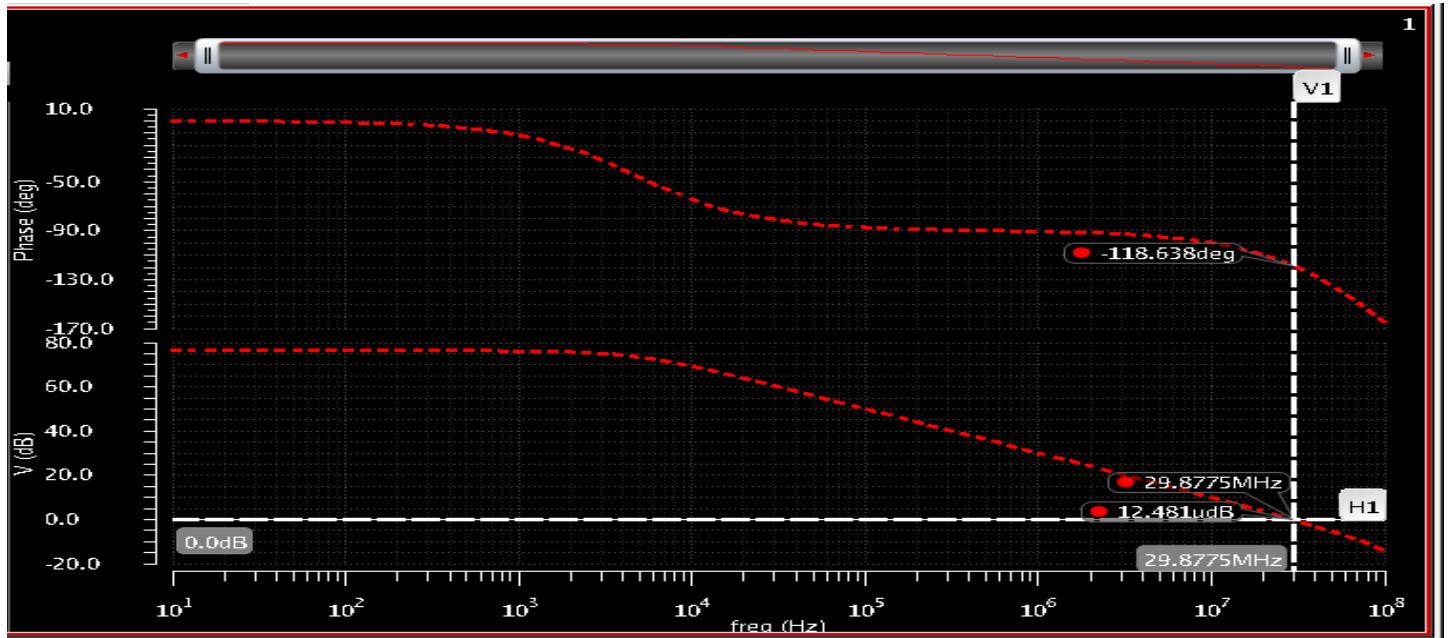
REPORTED GBW: 29.8775MHz

\*copy gain plot in new window to save it.



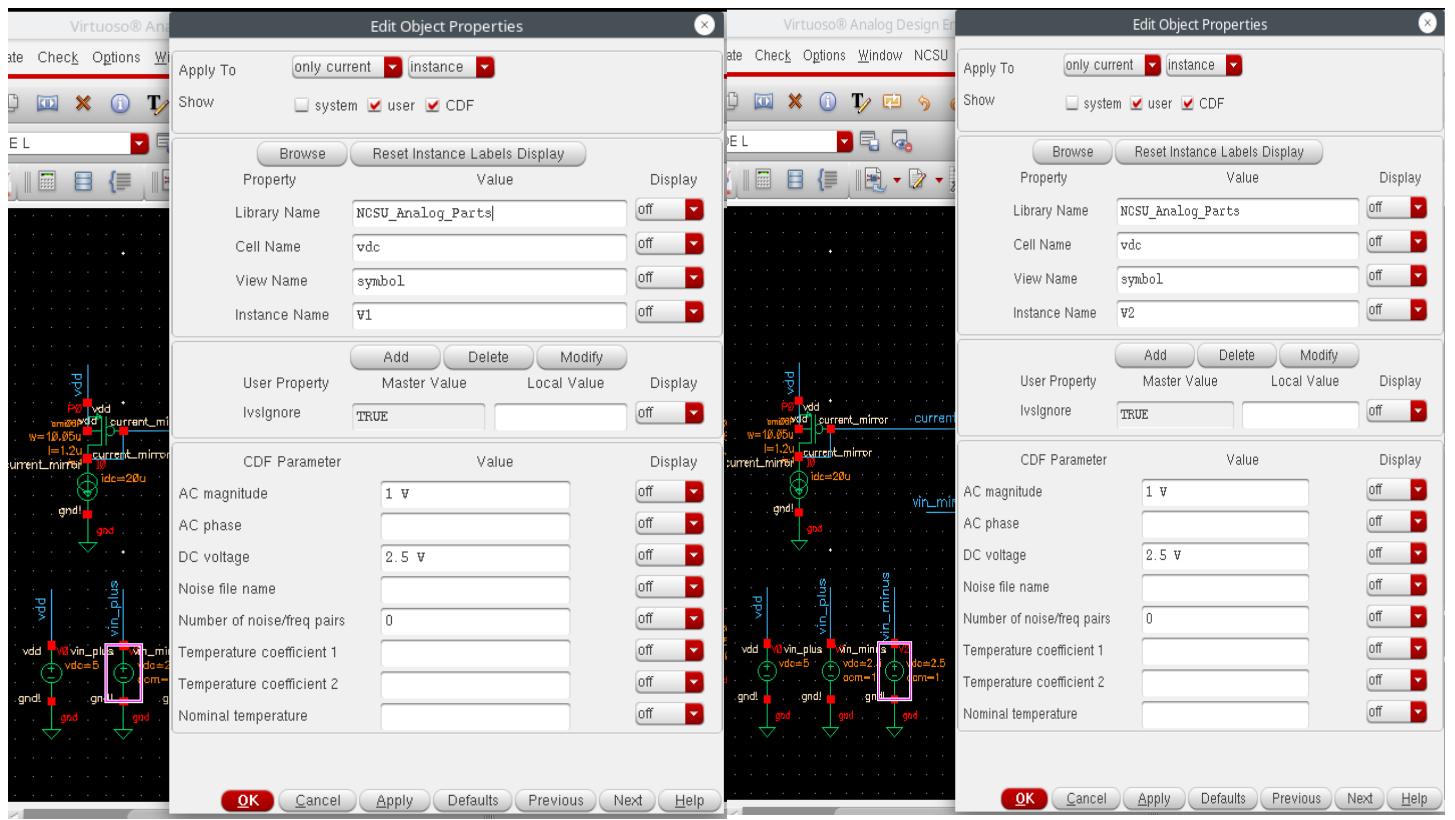
Test probe for phase margin(selected nets are highlighted)

- ac simulation: direct plot: gain and phase
- delete the gain plot and copy the previously saved gain plot.

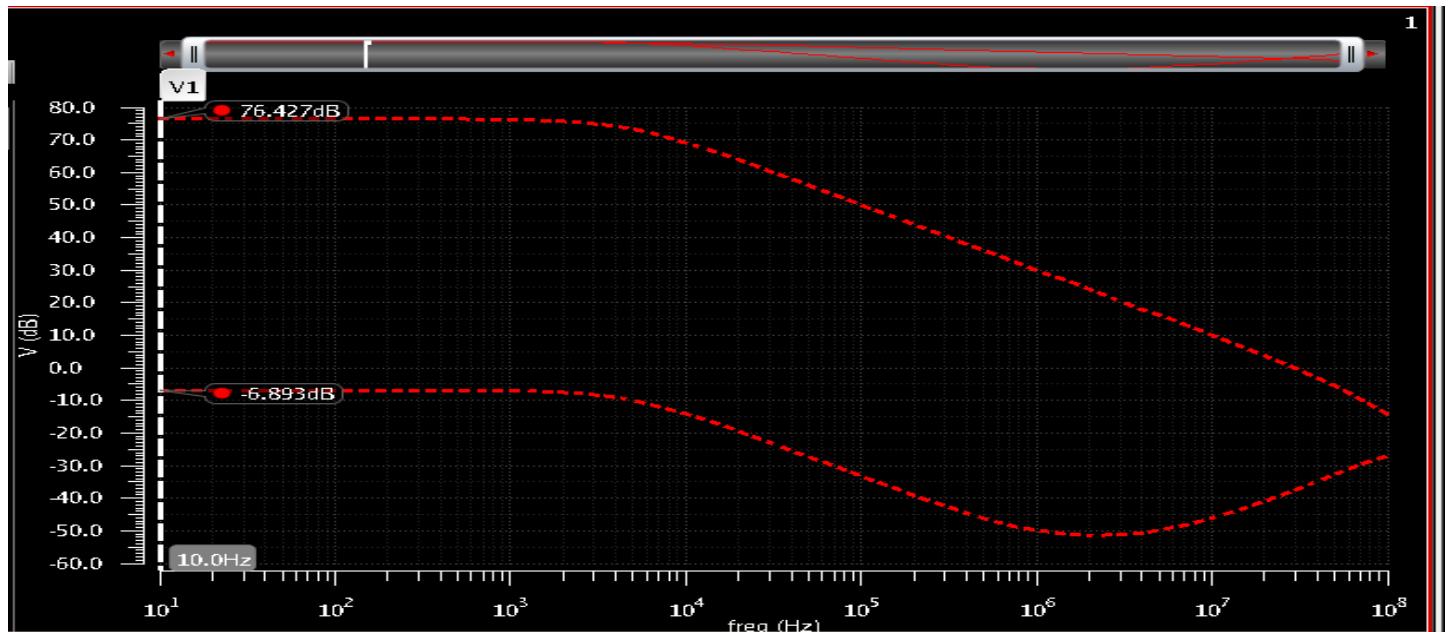


Specification: phase margin

REPORTED PHASE MARGIN:  $180 - 118.628 = 61.362$  degrees.

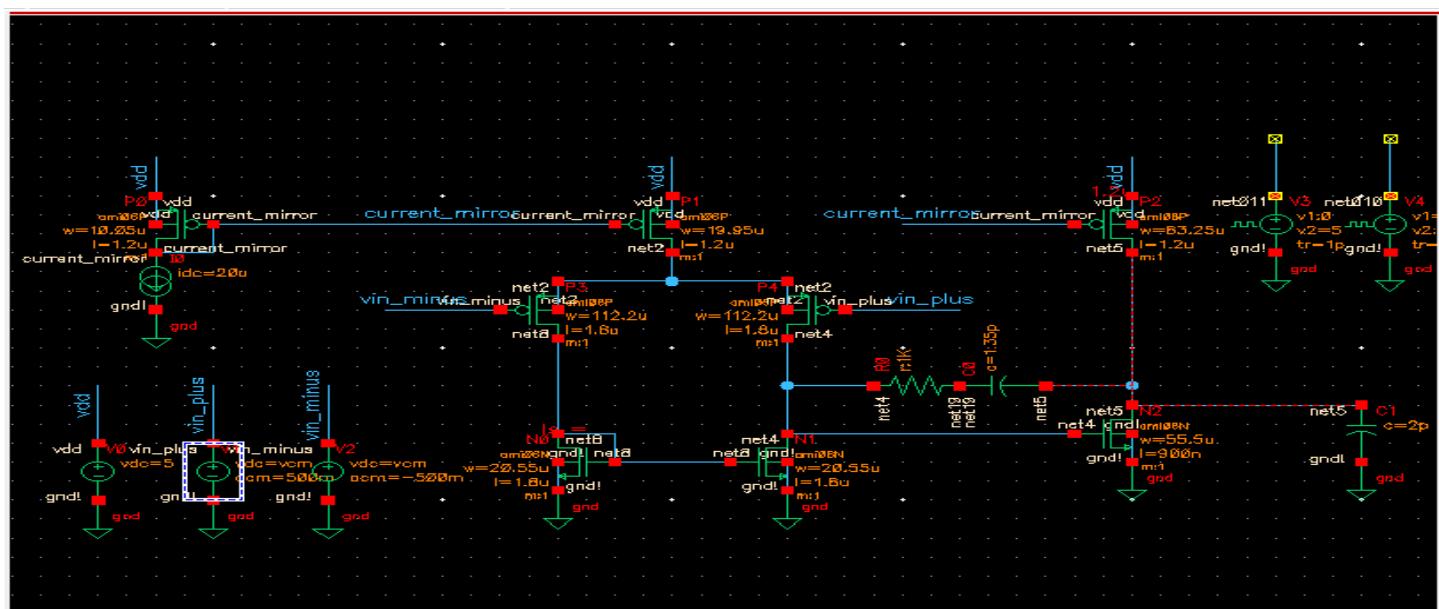


Test set up for CMRR

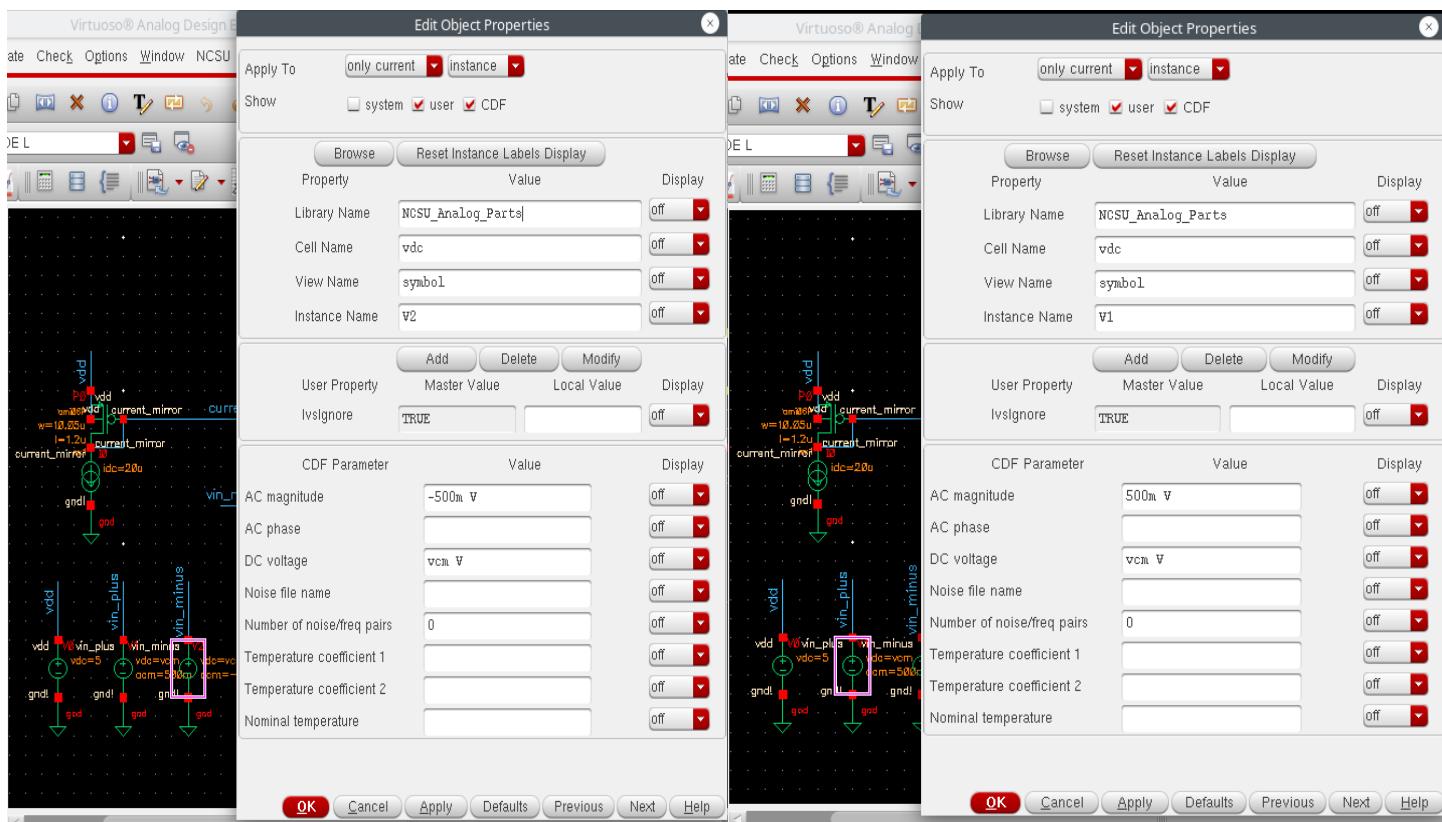


Specification: CMRR

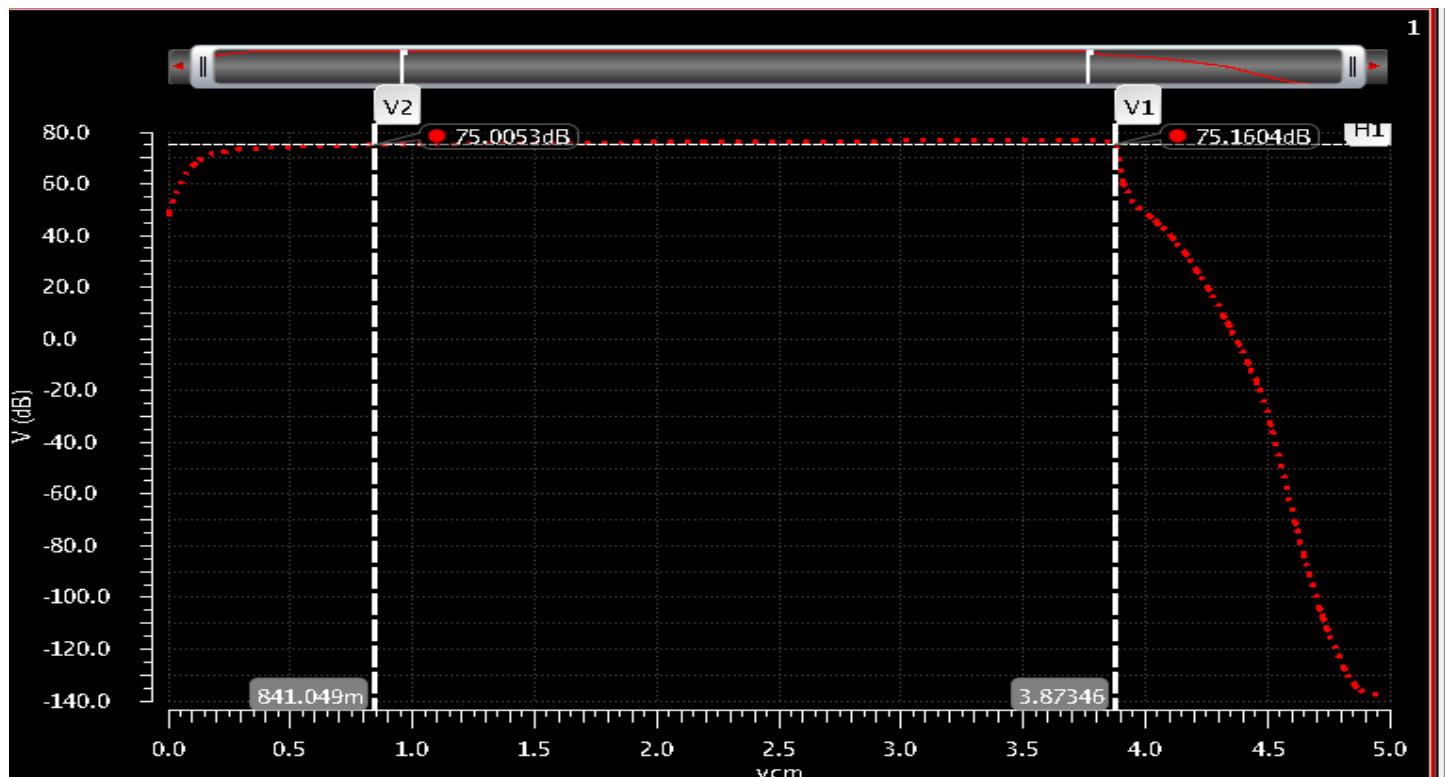
REPORTED CMRR: 83.32dB



Test schematic for ICMR (Vdc= vcm for supply V1 and V2)

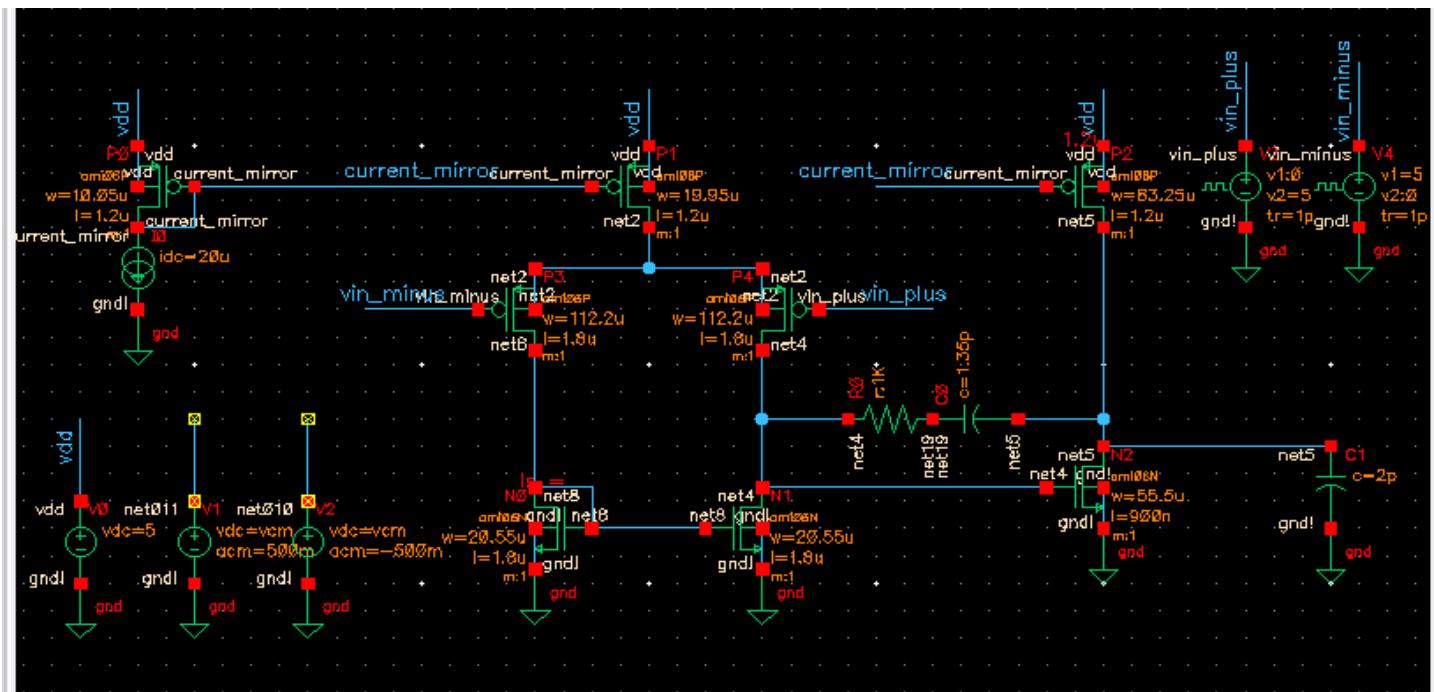


Test setup for ICMR



Specification: ICMR

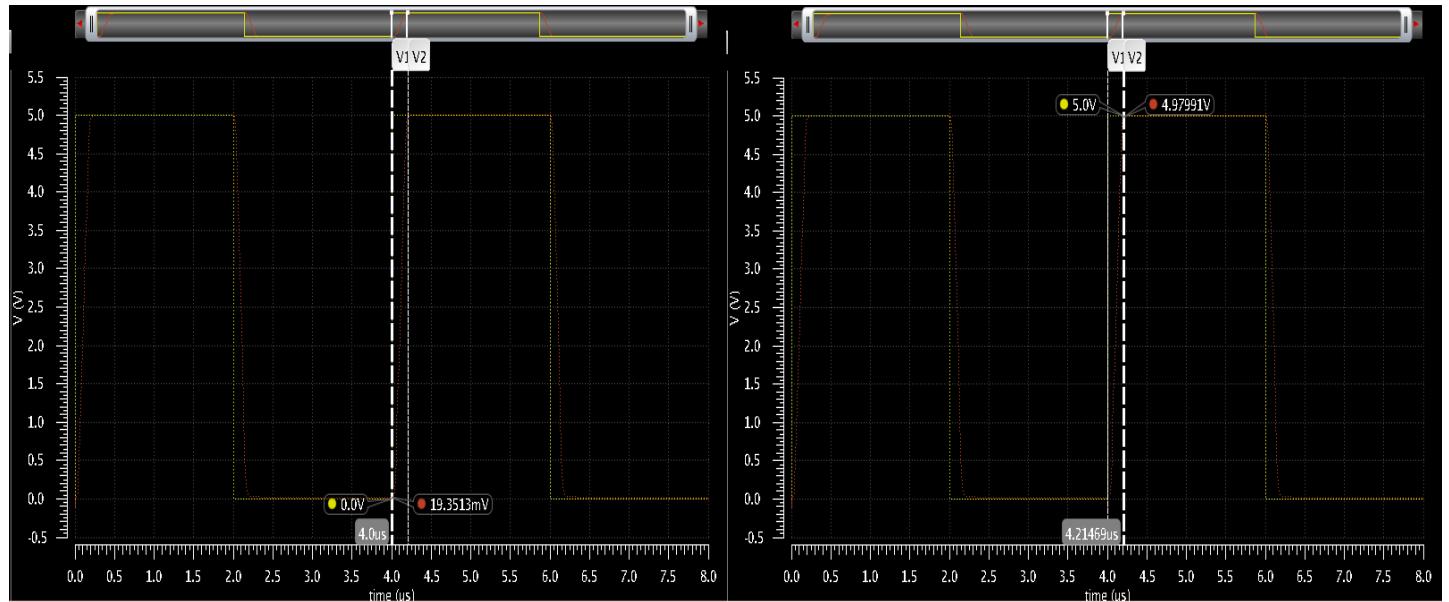
REPORTED ICMR: 3.032411V



## Slew rate test schematic



## Slew rate test input



Specification: slew rate observation

REPORTED SLEW RATE: 23.66V/us

Slew Rate: rate of rise for the output signal.

$$SR = \frac{4.99 - 19.35m}{(4 - 4.21)\mu s}$$

$$= 23.66 \text{ V}/\mu\text{s}$$

## 5. CONCLUSION:

SR. NO.	PARAMETER	DESIGN SPECIFICATION	ACHIEVED SPECIFICATION
1	Total Power	$\leq 2 \text{ mW}$	1.426mW
2	Slew Rate	$\geq 20\text{V/us}$	23.66V/us
3	DC Gain	$\geq 75\text{dB}$	76.427dB
4	Gain Bandwidth Product	$\geq 25\text{MHz}$	29.8775MHz
5	CMRR	$\geq 60\text{dB}$	83.32dB
6	ICMR	$\geq 2.5\text{V}$	3.032411V
7	Phase Margin	$\geq 60^\circ$	61.362°