EE312: Project

Embedded System

November 1, 2021

Implement the following functions using single precision floating point representation in Verilog.

$$
\begin{aligned}
f(x) &= \frac{1}{x} \\
f(x) &= \sqrt{x} \\
f(x) &= e^{-x} \\
f(x) &= e^{x} \\
f(x) &= ln(x) \\
f(x) &= 2^{x^2} \\
sinh(x) &= \frac{e^{x} - e^{-x}}{2} \\
cosh(x) &= \frac{1 + e^{-2x}}{2e^{-x}} \\
tanh(x) &= \frac{e^{2x} - 1}{e^{2x} + 1}
\end{aligned}
$$

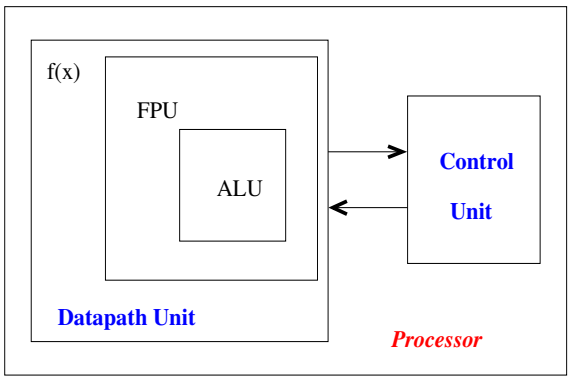

Figure 1: Block Diagram

Implementation guidelines:

- All functions must be implemented using blocks designed in earlier lab.
- ALU designed in earlier lab should be used to implement Floating Point Unit (FPU) for single precision floating point adder/subtractor,multiplier and divider operation.
- Above defined functions 1-8 must be implemented using FPU.
- Input to the processor should be clk, 8 bit data x and 4 bit input to select function number(0-8).The processor should return value of f(x).
- You can choose how and what signals control unit send and receives from other blocks.

Report must consist of the following : RTL Schematic,Behavioural Simulation,Post synthesis simulation,Synthesis report.

Zip all the source files and test bench (verilog files) along with the report and mail it to corresponding TA.