Embedded Systems Group Project

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1. Objective

- Implement the following functions using single precision floating point representation in Verilog.:
  - $\frac{1}{x}$
  - $\sqrt{x}$
  - e^{-x}
  - e^{x}
  - $\tanh(x)$
  - $\ln(x)$
  - 2^{x^2}
  - $\sinh(x)$
  - $\cosh(x)$

2. Verilog Coding Tasks

Parameters:

```
parameter [3:0] f0 = 4'b0000,   //if select is 0000 then we 1 / x
                f1 = 4'b0001,   //if select is 0001 then we sqrt(x)
                f2 = 4'b0010,   //if select is 0010 then we e^-x
                f3 = 4'b0011,   //if select is 0011 then we e^x
                f4 = 4'b0100,   //if select is 0100 then we ln(x)
                f5 = 4'b0101,   //if select is 0101 then we 2^(x^2)
                f6 = 4'b0110,   //if select is 0110 then we sinh(x)
                f7 = 4'b0111,   //if select is 0111 then we cosh(x)
                f8 = 4'b1000;   //if select is 1000 then we tanh(x)
```

Parameters for the select Function

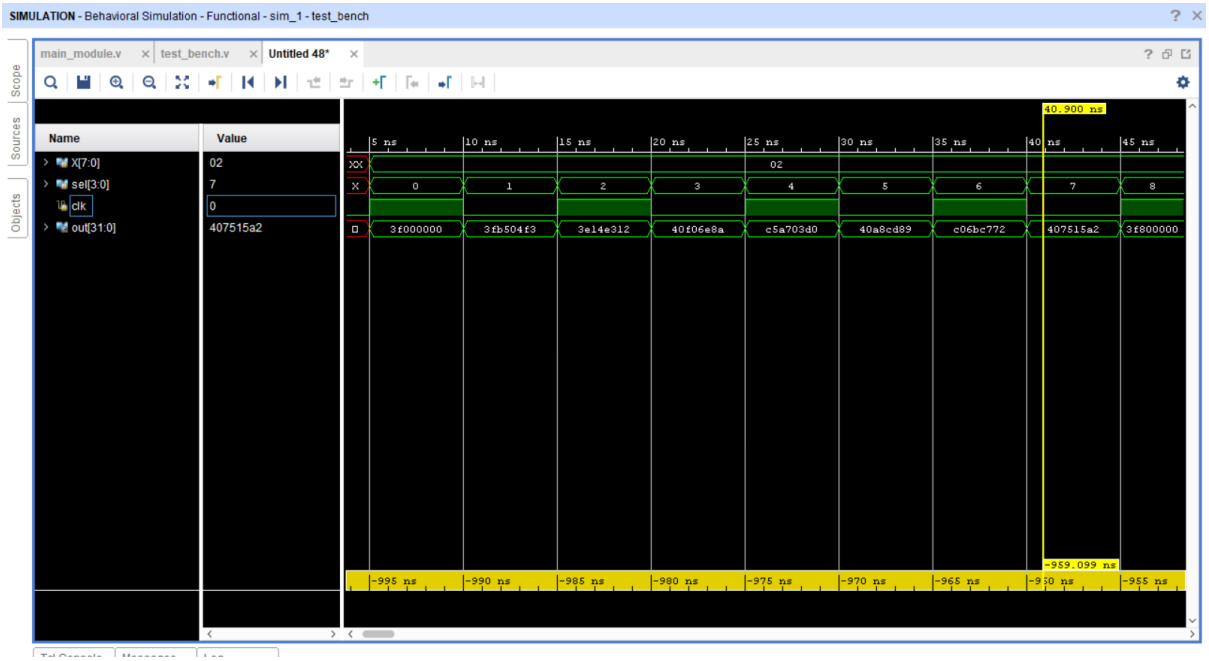
```
assign ADD = !outputcode[1] & !outputcode[0];
assign SUB = !outputcode[1] & outputcode[0];
assign DIV = outputcode[1] & !outputcode[0];
assign MUL = outputcode[1] & outputcode[0];
```

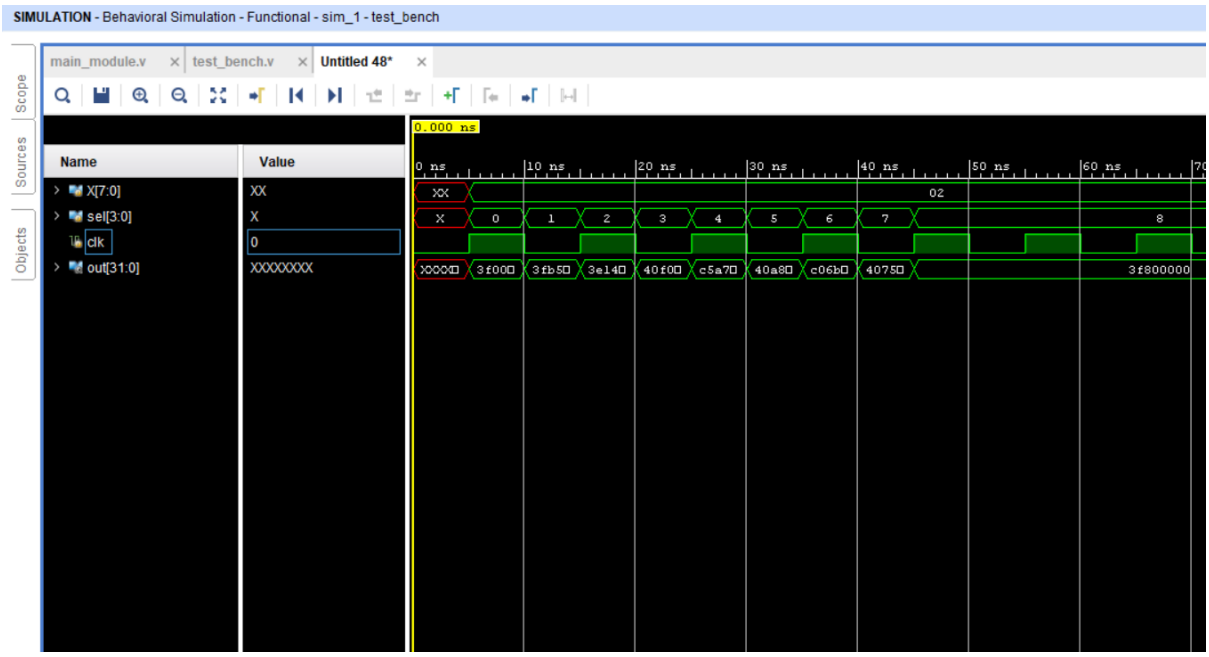
Parameters to select operation in FPU

Testbench:

```
// Group Project - Test Bench
module test_bench;
//All inputs
reg [7:0] X;            //This is the input X
reg [3:0] sel;          //This is for selecting function
reg clk;

//Outputs
wire [31:0] out;         //This is output in 32-bit IEEE-754 format


//Instantiating the main module
main_module M1 (clk, X, sel, out);

initial begin
    clk = 1'b0;
end

always begin
    #5 clk = ~clk;
end

initial begin
    #5 sel = 4'b0000;  X = 8'b00000010;
    #5 sel = 4'b0001;  X = 8'b00000010;
    #5 sel = 4'b0010;  X = 8'b00000010;
    #5 sel = 4'b0011;  X = 8'b00000010;
    #5 sel = 4'b0100;  X = 8'b00000010;
    #5 sel = 4'b0101;  X = 8'b00000010;
    #5 sel = 4'b0110;  X = 8'b00000010;
    #5 sel = 4'b0111;  X = 8'b00000010;
    #5 sel = 4'b1000;   X = 8'b00000010;
end

endmodule
```

Output Waveform (Behavioural):





Synthesis Report:

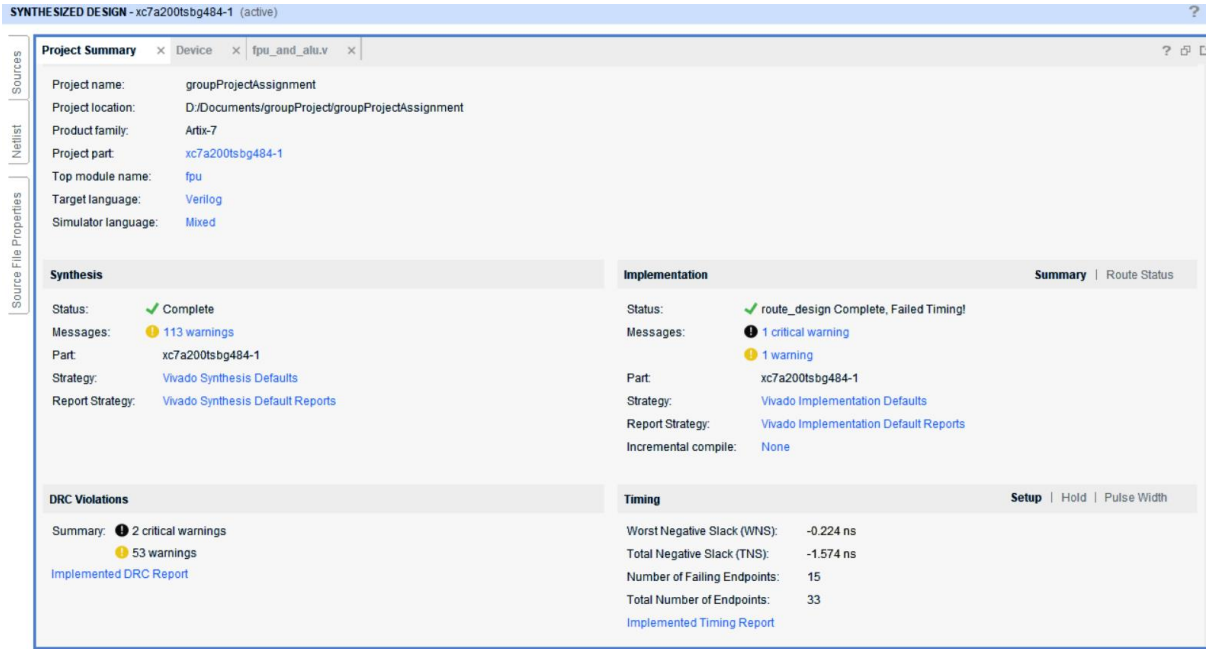
Utilization — Post-Synthesis | Post-Implementation — Graph | Table

Resource	Estimation	Available	Utilization %
LUT	2711	134600	2.01
FF	190	269200	0.07
DSP	14	740	1.89
IO	99	285	34.74
BUFG	12	32	37.50

Power — Summary | On-Chip

Total On-Chip Power:	**0.2 W**
Junction Temperature:	**25.7 °C**
Thermal Margin:	59.3 °C (17.6 W)
Effective ϑJA:	3.3 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report



Post Synthesis Functional simulation output waveform:

Implementation Report:

Utilization — Post-Synthesis | **Post-Implementation** — Graph | **Table**

Resource	Utilization	Available	Utilization %
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Power — **Summary** | On-Chip

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Implemented Power Report

SYNTHESIZED DESIGN - xc7a200tsbg484-1 (active)

Sources | Netlist | Source File Properties

Project Summary | Device | fpu_and_alu.v

Project name:	groupProjectAssignment
Project location:	D:/Documents/groupProject/groupProjectAssignment
Product family:	Artix-7
Project part:	xc7a200tsbg484-1
Top module name:	fpu
Target language:	Verilog
Simulator language:	Mixed

Synthesis

Status:	✓ Complete
Messages:	113 warnings
Part:	xc7a200tsbg484-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports

Implementation — **Summary** | Route Status

Status:	✓ route_design Complete, Failed Timing!
Messages:	1 critical warning
	1 warning
Part:	xc7a200tsbg484-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental compile:	None

DRC Violations

Summary: 2 critical warnings
53 warnings

Implemented DRC Report

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	-0.224 ns
Total Negative Slack (TNS):	-1.574 ns
Number of Failing Endpoints:	15
Total Number of Endpoints:	33

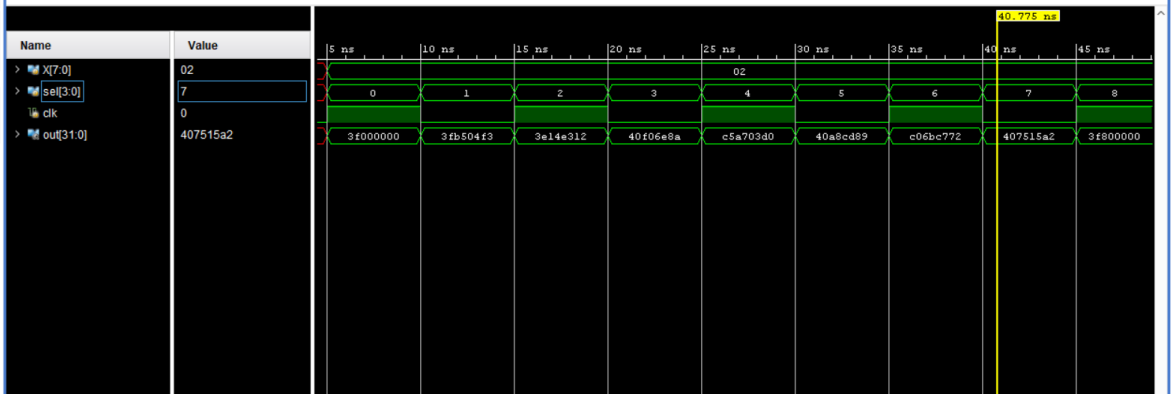
Implemented Timing Report

Post Implementation Functional simulation output waveform:

SIMULATION — Post-Synthesis Simulation - Functional - sim_1 - test_bench | **Post-Implementation Simulation - Functional - sim_1 - test_bench**

Scope | Sources | Objects

fpu_and_alu.v | Untitled 2



Power Report:

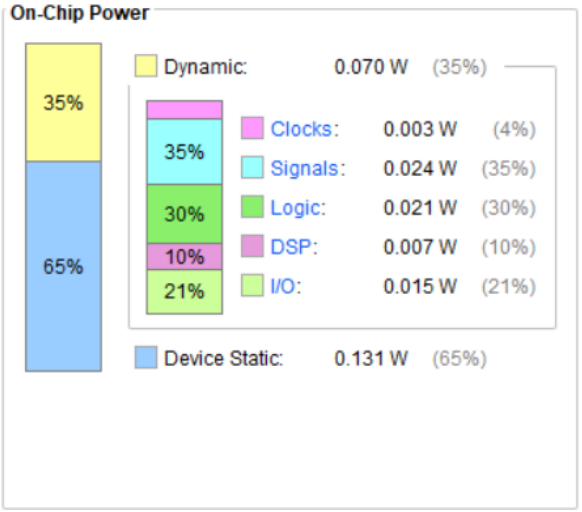
Reports | Design Runs | **Power** ×

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.201 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.7°C**
Thermal Margin:	59.3°C (17.6 W)
Effective ϑJA:	3.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



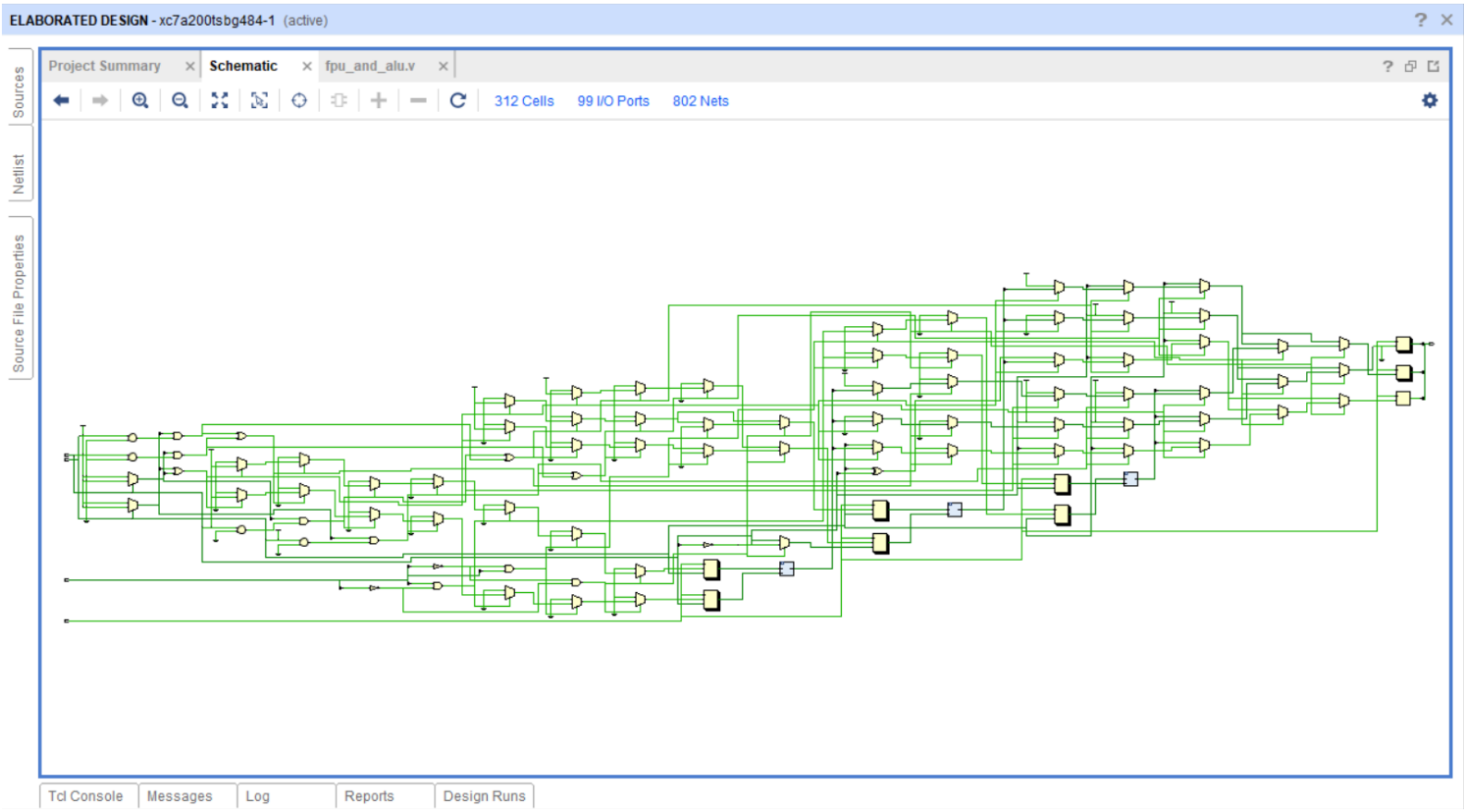
Timing Report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.224 ns	Worst Hold Slack (WHS):	0.366 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	-1.574 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	15	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	33	Total Number of Endpoints:	33	Total Number of Endpoints:	191

Timing constraints are not met.

RTL-Analysis Diagram



Click Here for Zoomed RTL-diagram

Click Here For Post-synthesis utilization Report

Click Here for Post-Implementation utilization Report

Click Here For Vivado Synthesis Report

3. Conclusions

- We have successfully designed and coded for the FPU and the ALU
- We have successfully implemented all the functions
- We have successfully acquired the Synthesis reports, implementation reports, and timing reports.