# 4-Bit Arithmetic Logic Unit

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In Digital Circuits, A **Binary Adder-Subtractor** is can do both the addition and subtraction of binary numbers in one circuit itself. The operation is performed depending on the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit).

## Functional Description

### Operation Table

| A (4 bits) | B (4 bits) | op (1 bit) | Operation | R (4 bits) | C_out (1 bit) |
|---|---|---|---|---|---|
| A (binary) | B (binary) | 0 | Addition (A + B) | Sum (4-bit) | Carry (overflow) |
| A (binary) | B (binary) | 1 | Subtraction (A - B) | Difference (4-bit) | Borrow (overflow) |

### Addition (Control = 0)

- The 4-bit binary numbers AAAA and BBBB are added.
- If the sum exceeds 4 bits (i.e., it requires a 5th bit), C_out will be set to 1.

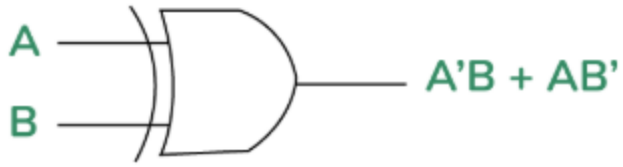
### Subtraction (Control = 1)

- The 4-bit binary number BBBB is complemented (using 2's complement method) and added to AAAA.
- B' = NOT(B) + 1 (2’s complement of B)
- The 4-bit result is stored in R, and if a borrow occurs, C_out will be set to 1

**XOR gate operation**
* If one input is high it produce invert of the other input.
* If one input is low it produce same of the other input.

**2's complement**
* It represent a positive number as it is and negative number by its corresponding 2s-complement so we can use the same circuit to perform addition and subtraction.

XOR Gate




Truth Table

| A (Input 1) | B (Input 2) | X = A'B + AB' |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**2's complement**
* It represent a positive number as it is and negative number by its corresponding 2s-compleme so we can use the same circuit to perform addition and subtraction.

## Internal Design

1. **Full Adders**
    - The ALU has 4 **1-bit Full Adders** connected serially.
    - Each bit position ($A_0$, $A_1$, $A_2$, $A_3$) and ($B_0$, $B_1$, $B_2$, $B_3$) are processed one by one.
2. **Operation Control**
    - The operation selector (**op**) determines if addition or subtraction is to be performed.
    - To perform subtraction, BBBB is XOR-ed with **op** to invert the bits of BBBB when op=1op = 1op=1, and a **1** is added to achieve 2's complement subtraction.
    - For addition, the bits of BBBB remain unchanged.
    - **B' = B XOR op** (this acts like a NOT gate on BBB when op=1op = 1op=1).

3. **Carry/Borrow Handling**
    - The carry out (**C_out**) is set when overflow occurs in addition or borrow occurs in subtraction.

## Circuit Design

Logic Circuit Design for the 4-bit ALU includes:

1. XOR gates to modify BBB based on the operation (B' = B XOR control).
2. Full Adders using and,or and ex-or gates to compute the sum of AAAA and B′B'B′B’.
3. Switches to select between addition and subtraction.
4. Overflow/Borrow Detection is done via C_out from the last stage.
5. 7 segment Display to show the inputs and outputs.