Vending Machine Project Using Verilog

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1. Introduction

This project presents the design and implementation of a sequential circuit-based vending machine using a Mealy Finite State Machine (FSM). The vending machine dispenses three different products based on user input and returns change if excess money is inserted. The vending machine accepts monetary inputs (Rs 5, Rs 10, and Rs 20) and dispenses products; a bag of chips priced at Rs 10, a chocolate bar at Rs 15, and a soda at Rs 20. The system operates based on a finite state machine (FSM) approach to ensure proper functionality and user interaction using Verilog in Xilinx Vivado.

2. System Design

2.1 Finite State Machines (FSM)

A finite state machine is an abstract computational model used to design synchronous sequential circuits. It consists of defined states, inputs, outputs, and transition logic. FSMs can be categorized into:

Moore Finite State Machine : The output depends only on the present state.

Mealy Finite State Machine : The output depends on both the present state and the present input.

The vending machine in this project is implemented using a **Mealy FSM** due to its dependency on both the current state and the inserted money.

2.2 Inputs and Outputs

The vending machine is designed to dispense three different products with specific prices:

- **Lays Chips** – Rs. 10
- **Chocolate Bar** – Rs. 15
- **Soda** – Rs. 20

The vending machine accepts the following denominations:

- Rs. 5
- Rs. 10
- Rs. 20

Inputs:

- `clk`: Clock signal.
- `rst`: Reset signal.
- `money[1:0]`: Binary encoded money input (Rs 10, Rs 5, Rs 20).
- `product_select[1:0]`: Product selection (Rs 10, Rs 15, Rs 20 products).

Outputs:

- `product_dispensed`: Indicates when a product is dispensed.
- `change[1:0]`: Returns appropriate change if necessary.

2.3 Finite State Machine (FSM) Description

The vending machine follows a sequential state transition based on the amount inserted and product selection:

- **S0 (Initial State):** No money inserted.
- **S1 (Rs 5 Received):** System waits for additional money.
- **S2 (Rs 10 Received):** A product may be dispensed based on selection.
- **S3 (Rs 15 Received):** Higher-priced products can be selected.
- **S4 (Rs 20 Received):** The most expensive product can be dispensed, and change may be returned.

3. Implementation

3.1 Verilog Code for Vending Machine

The vending machine is implemented using a sequential logic FSM in Verilog. The state transitions and product dispensing logic are handled efficiently.

3.2 Testbench for Verification

A testbench is written to simulate various cases:

- Inserting different denominations and selecting products.
- Checking for correct change return.
- Ensuring the machine transitions correctly between states.

4. Simulation and Analysis

4.1 Waveform Analysis

Using Xilinx Vivado, the simulation results are observed:

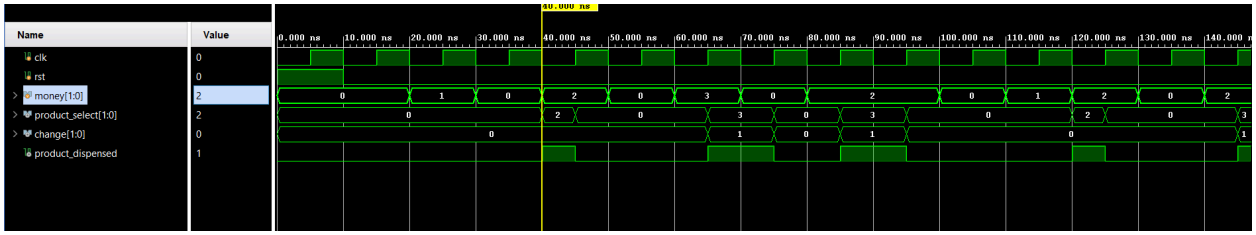

Fig.1. Output waveform/Behavioral Simulation

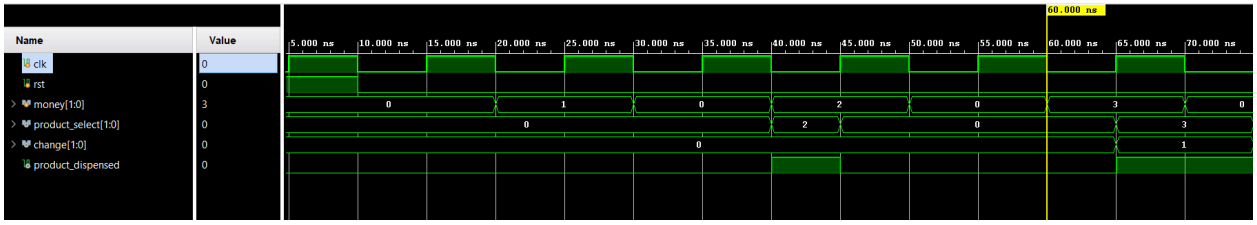

Fig.2. Output waveform, cursor at 70ns

Outputs/Observation :

- `change[1:0] = 1` → Change of Rs. 5 is calculated but not yet fully processed.
- `product_dispensed = 1` → The vending machine has dispensed the selected product.
- The user inserted Rs. 20 (`money = 3`).
- The selected product i.e. chocolate bar costs Rs. 15 (`product_select = 3`).
- The vending machine dispenses the product (`product_dispensed = 1`).
- Since Rs. 20 was given for a Rs. 15 product, **Rs. 5 change** is calculated and registered (`change = 1`).
- The system successfully processes the transaction and prepares to return the change.

At **60 ns**, the vending machine successfully processes a Rs. 20 input for a Rs. 15 product selection. The product is dispensed, and Rs. 5 change is calculated, which is expected to be fully processed in the next cycle.

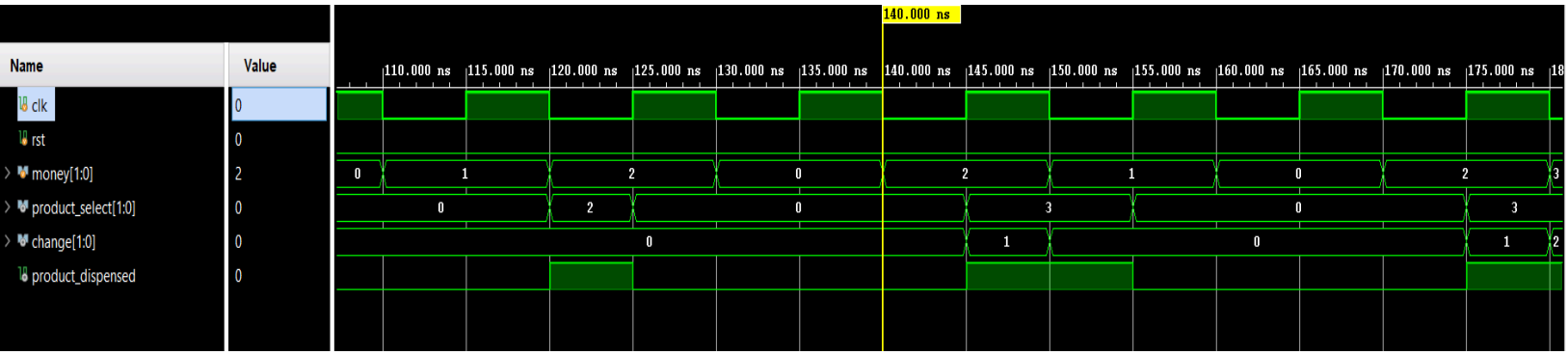

Fig.3. Output waveform, cursor at 140ns

At **140 ns**, the vending machine processes Rs. 10 input for a Rs. 5 product selection. The product is successfully dispensed, and Rs. 5 change is returned to the user, confirming the correct operation of the vending machine.

4.2 Functional Verification

The simulation confirms that the vending machine operates as intended:

- Correct state transitions.
- Proper product dispensing based on inserted money.
- Accurate change return handling.

5. Conclusion

This project successfully demonstrates the design and implementation of a vending machine using Verilog in Xilinx Vivado. The FSM-based approach ensures efficient money handling, product selection, and change return. Future enhancements can include adding more products, handling invalid inputs, and implementing a display system.

6. Future Enhancements

- Integration with FPGA hardware for real-world deployment.
- LCD display to show transaction details.
- Support for more denominations and product variations.

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