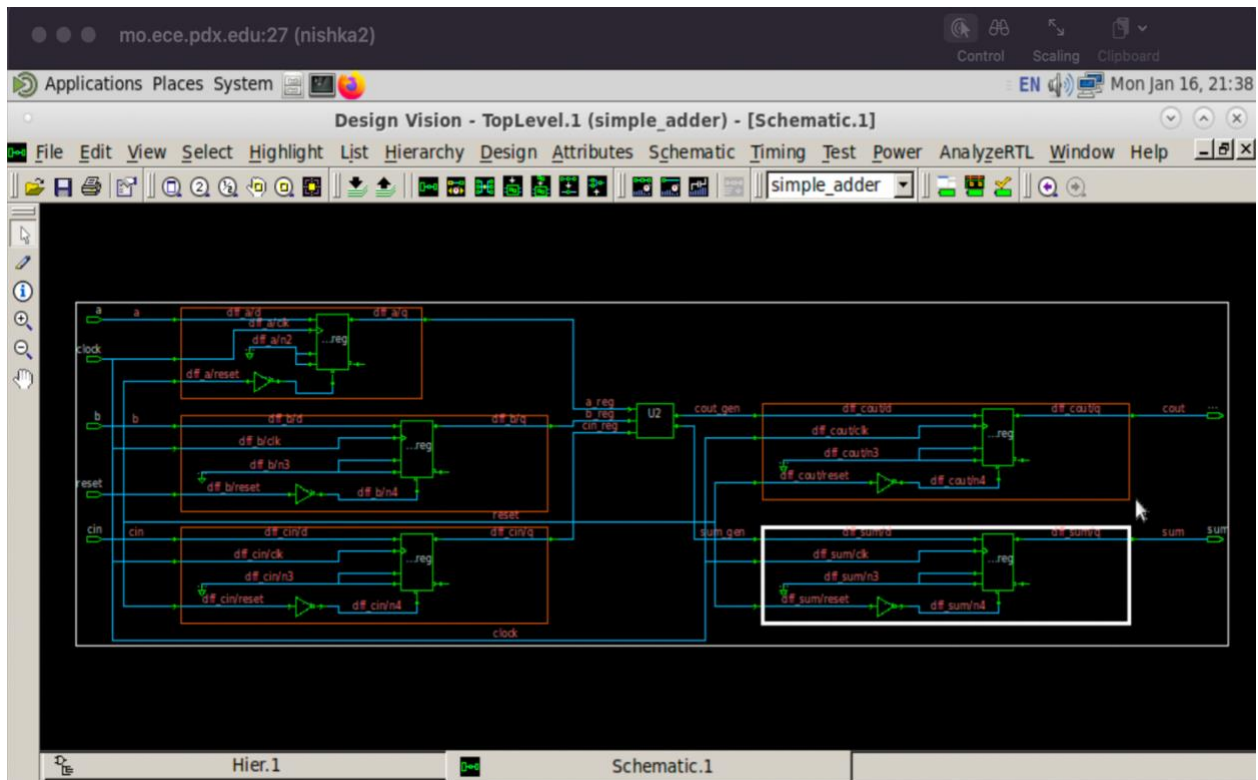
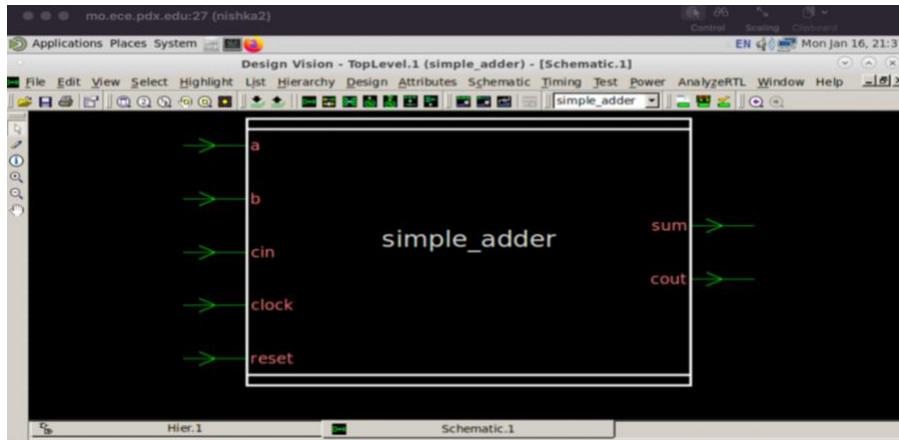


**ASIC 481/581 – Lab1**  
**Nishka Sathisha**

**HW\_LAB\_1\_A:**

**Schematic Circuit of Simple Adder:**



# ASIC 481/581 – Lab1

## Nishka Sathisha

### Timing report:

```
mo.ece.pdx.edu:27 (nishka2)
Applications Places System
Mate Terminal
File Edit View Search Terminal Help

*****
Report : timing
-path full
-delay max
-max_paths 1
Design : simple_adder
Version: P-2019.03-SP1-1
Date   : Mon Jan 16 21:38:57 2023
*****

Operating Conditions: ss0p95v125c  Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed

Startpoint: dff_a/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Endpoint: dff_sum/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

Des/Clust/Port  Wire Load Model  Library
-----
simple_adder    ForQA          saed32rvt_ss0p95v125c

Point          Incr      Path
-----
clock CLK (rise edge)          0.00      0.00
clock network delay (ideal)    0.00      0.00
dff_a/q_reg/CLK (S0FFARX1_RVT) 0.00      0.00 r
dff_a/q_reg/Q (S0FFARX1_RVT)   0.20      0.20 f
dff_a/q (dff 4)                0.00      0.20 f
U2/S (FAD0X1_RVT)              0.15      0.35 r
dff_sum/d (dff 0)              0.00      0.35 r
dff_sum/q_reg/D (S0FFARX1_RVT) 0.00      0.35 r
data arrival time              0.35

clock CLK (rise edge)          0.50      0.50
clock network delay (ideal)    0.00      0.50
```

```
mo.ece.pdx.edu:27 (nishka2)
Applications Places System
Mate Terminal
File Edit View Search Terminal Help

Wire Load Model Mode: enclosed

Startpoint: dff_a/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Endpoint: dff_sum/q_reg
(rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

Des/Clust/Port  Wire Load Model  Library
-----
simple_adder    ForQA          saed32rvt_ss0p95v125c

Point          Incr      Path
-----
clock CLK (rise edge)          0.00      0.00
clock network delay (ideal)    0.00      0.00
dff_a/q_reg/CLK (S0FFARX1_RVT) 0.00      0.00 r
dff_a/q_reg/Q (S0FFARX1_RVT)   0.20      0.20 f
dff_a/q (dff 4)                0.00      0.20 f
U2/S (FAD0X1_RVT)              0.15      0.35 r
dff_sum/d (dff 0)              0.00      0.35 r
dff_sum/q_reg/D (S0FFARX1_RVT) 0.00      0.35 r
data arrival time              0.35

clock CLK (rise edge)          0.50      0.50
clock network delay (ideal)    0.00      0.50
dff_sum/q_reg/CLK (S0FFARX1_RVT) 0.00      0.50 r
library setup time             -0.12      0.38
data required time              0.38

-----
data required time              0.38
data arrival time              -0.35
-----
slack (MET)                    0.03

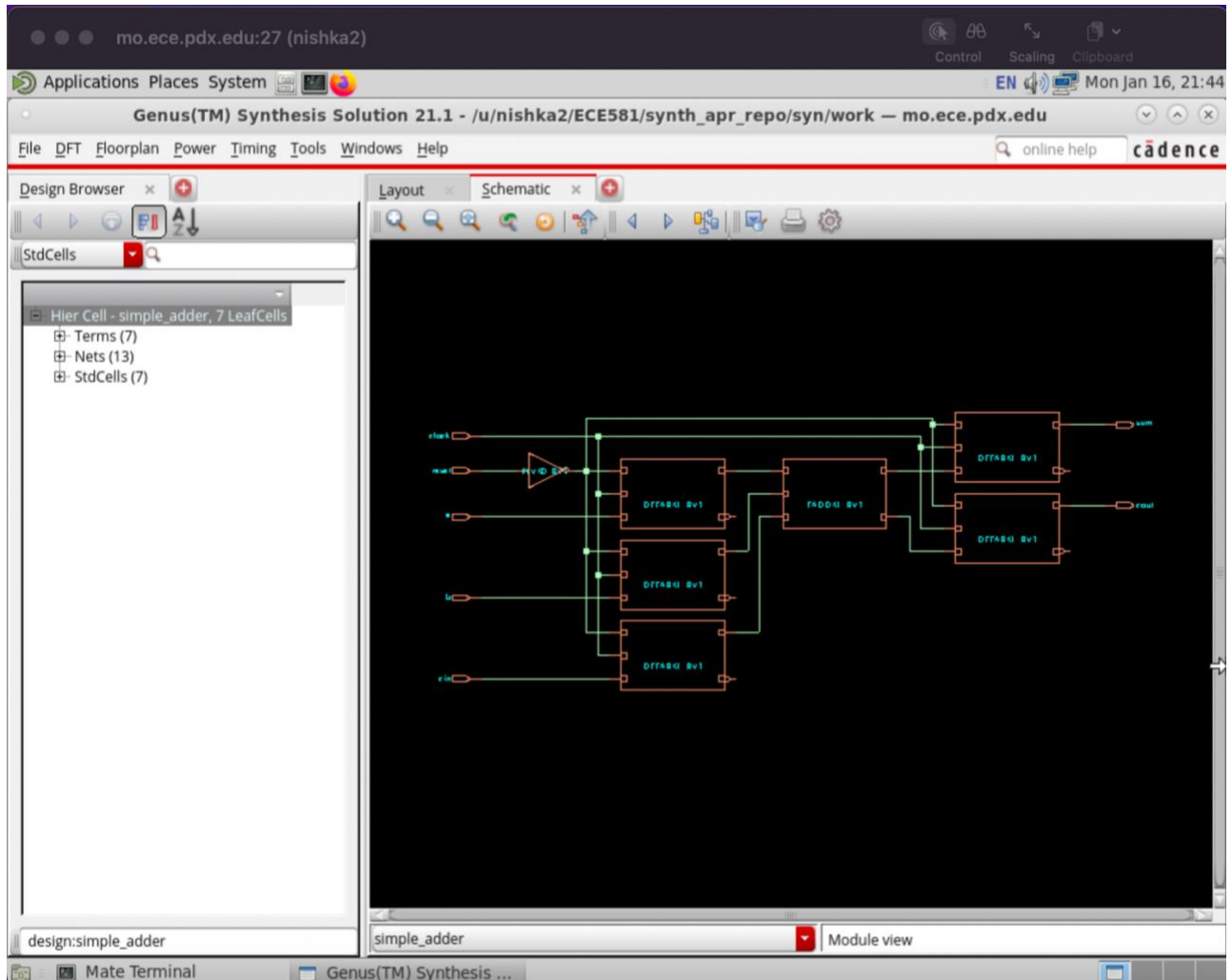
c shell>
```

## ASIC 481/581 – Lab1

Nishka Sathisha

### HW\_LAB\_1\_B:

#### Schematic circuit in Genus



**ASIC 481/581 – Lab1**  
**Nishka Sathisha**

**Timing report in Genus:**

```
mo.ece.pdx.edu:27 (nishka2)
Applications Places System
Mate Terminal
File Edit View Search Terminal Help

=====
Generated by:      Genus(TM) Synthesis Solution 21.12-s068_1
Generated on:      Jan 16 2023 09:47:46 pm
Module:            simple adder
Operating conditions: _nominal_ (balanced_tree)
Wireload mode:     enclosed
Area mode:         timing library
=====

Path 1: MET (62 ps) Late External Delay Assertion at pin cout
Group: CLK
Startpoint: (R) dff_cout_q_reg/CLK
Clock: (R) CLK
Endpoint: (R) cout
Clock: (R) CLK

      Capture      Launch
Clock Edge:+      500      0
Src Latency:+      0      0
Net Latency:+      0 (I)    0 (I)
Arrival:=         500      0

Output Delay:-     250
Required Time:=    250
Launch Clock:-     0
Data Path:-        188
Slack:=            62

Exceptions/Constraints:
output_delay        250        ou_del_2_1

#-----
# Delay Arrival    Cell      Flags    Timing Point
# (ps) (ps)
#-----
#
0      0 (arrival) - dff_cout_q_reg/CLK
188    188 DFFARX1_RVT - dff_cout_q_reg/Q
0      188 (port) <<< cout
```

**Comparison Table:**

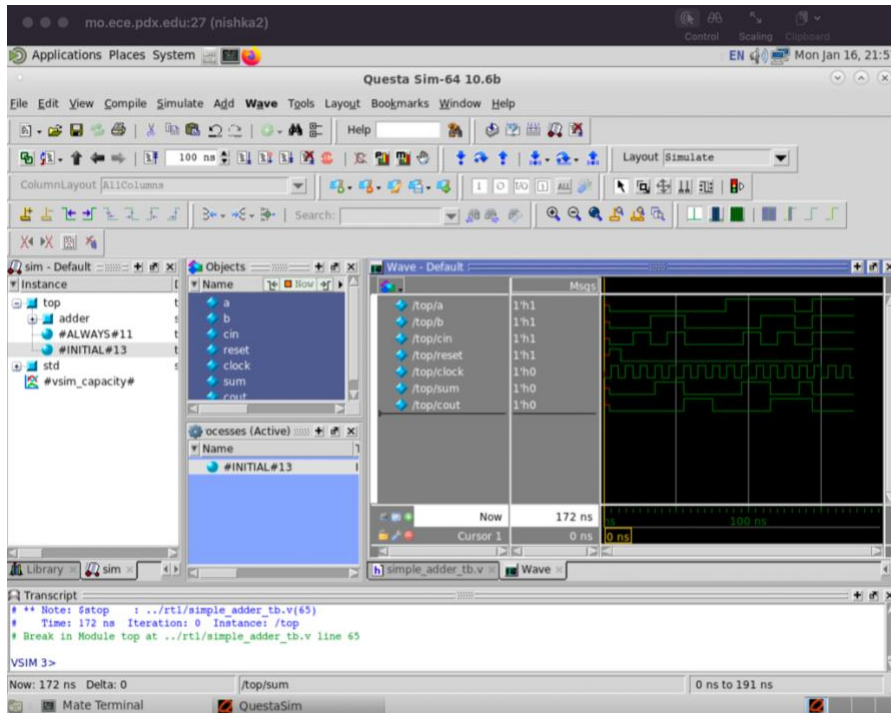
CONSTRAINTS	DC	GENUS
Cell count	11	7
Combinational cell count	6	2
Sequential cell count	5	5
Cell Area	56.928257	41.680
WNS	0	0
TNS	0	0
Violation Count	0	0

## ASIC 481/581 – Lab1

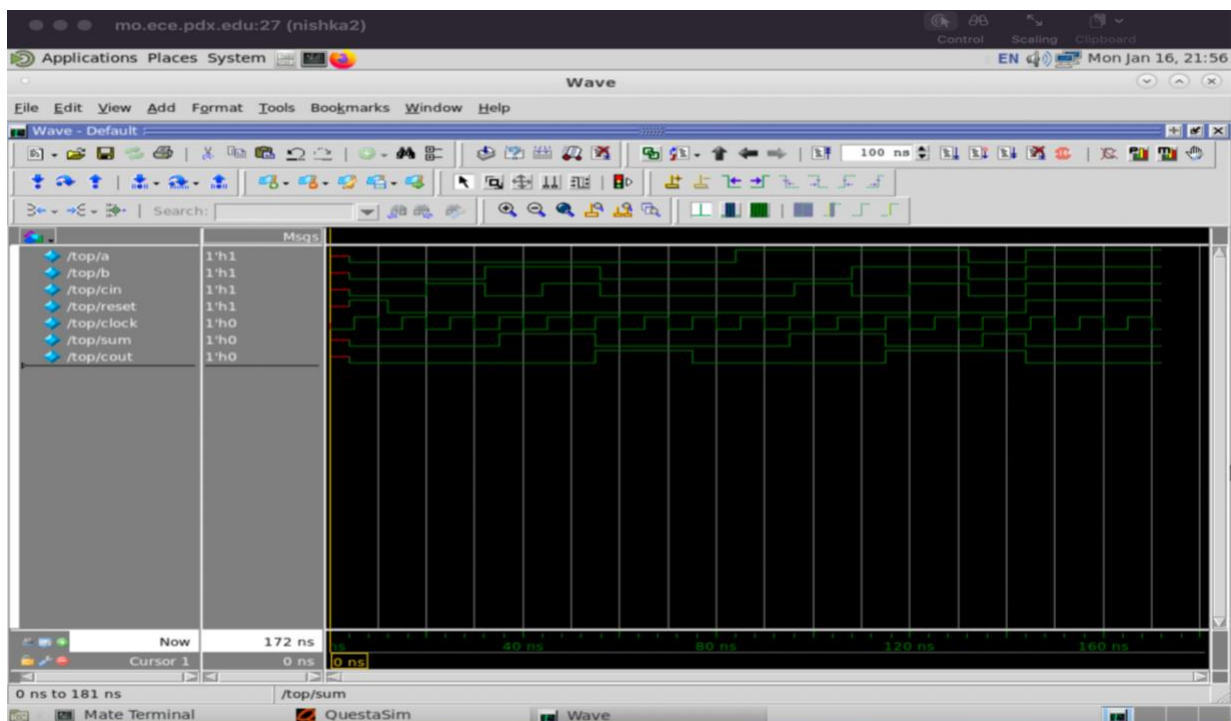
Nishka Sathisha

HW\_LAB\_1\_C:

FE RTL WAVEFORM



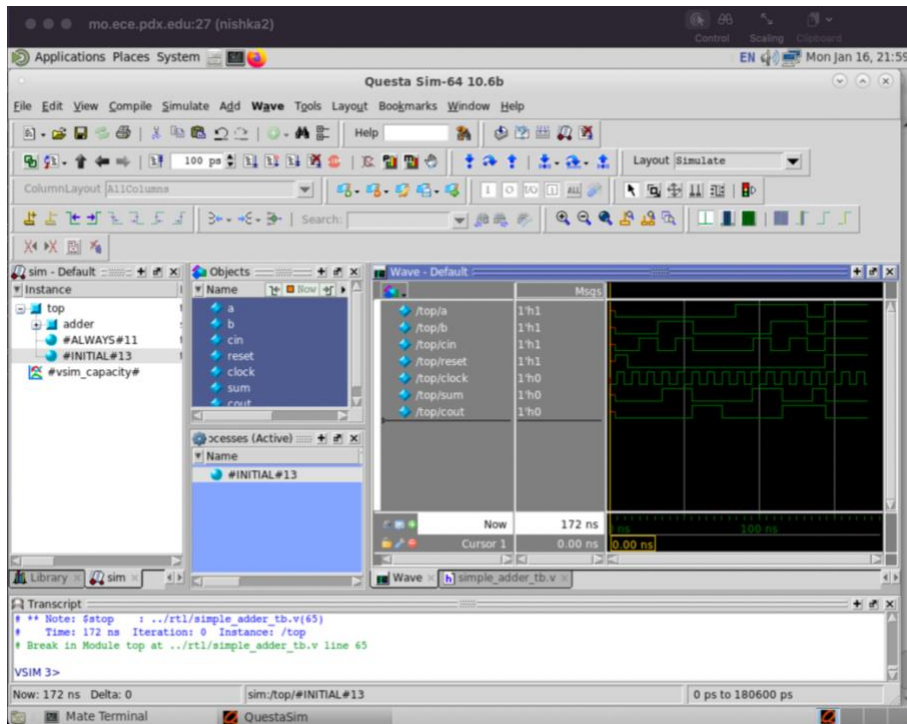
ZOOMED VIEW:



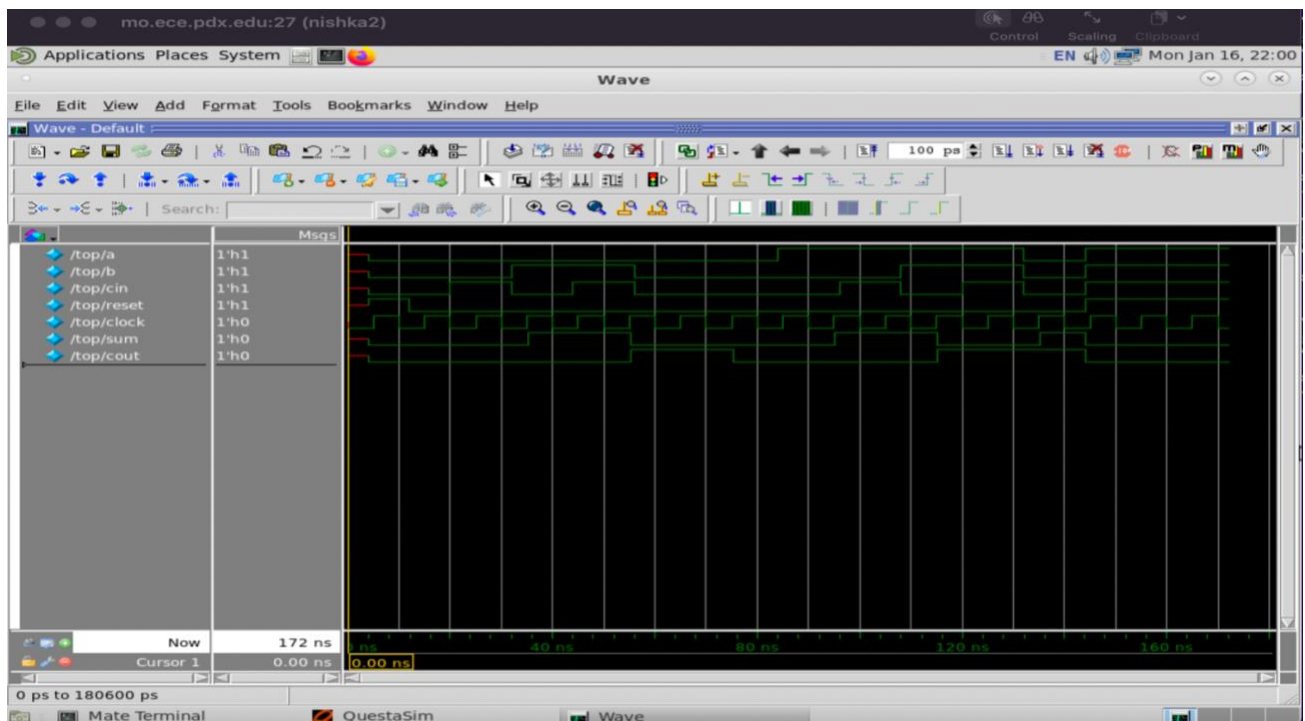
# ASIC 481/581 – Lab1

## Nishka Sathisha

### BE Netlist Waveform



### Zoomed view



## ASIC 481/581 – Lab1

Nishka Sathisha

### Comparison statement FE RTL Netlist vs BE RTL Netlist

The waveforms are same for both FE and BE and hence the RTL and generated netlist have similar functionality.

### Questa Commands:

**vlib:** The vlib command creates a design library

**vmap:** The vmap command defines a design defines a mapping between a logical library name and a directory

**vlog:** The vlog compiler invokes the Verilog compiler and compiles all the Verilog files

**vsim:** The vsim command invokes the VHDL/Questa simulator

### HW\_LAB\_1\_D:

### LEC equivalency

The screenshot shows the Cadence Conformal(R) Logic Equivalence Checking tool interface. The top menu bar includes File, Compare, Tools, Custom, Preferences, Window, and Help. The current mode is set to LEC. The interface is divided into two main panes: Golden and Revised.

**Golden Design Tree:**

- simple\_adder
  - 7 primitives
  - dff\_a(dff)
  - dff\_b(dff)
  - dff\_cin(dff)
  - dff\_cout(dff)
  - dff\_sum(dff)

**Revised Design Tree:**

- simple\_adder
  - U2(FADDX1\_RVT)
  - dff\_a(dff\_4)
  - dff\_b(dff\_3)
  - dff\_cin(dff\_2)
  - dff\_cout(dff\_1)
  - dff\_sum(dff\_0)

**Comparison Table:**

```
// Mapping key points ...
Mapped points: SYSTEM class
-----
Mapped points  PI    PO    DFF    Total
-----
Golden         5     2     5     12
-----
Revised        5     2     5     12
-----

0
// Command: add_compared_points -all
// 7 compared points added to compare list
0
// Command: compare
-----
Compared points  PO    DFF    Total
-----
Equivalent       2     5     7
-----

0
```

The bottom status bar indicates "Compare done!" and "100% completed".

## ASIC 481/581 – Lab1

Nishka Sathisha

### LEC Command description:

**Lec -tclmode:** Lec tool is invoked in tclmode

**Lec -dofile:** Lec tool is invoked and commands in dofile is executed

**read\_design:** This reads the RTL or netlist, or the library files required for the lec run

**set\_system\_mode:** Used to switch system modes

**add\_compared\_points:** Used to specify which mapped points the conformal compares.

**Compare:** This compares the points added in the list and checks whether the key points are equivalent or not.

**HW\_LAB\_1\_E:**

<https://github.com/nishkasathisha/Lab1>