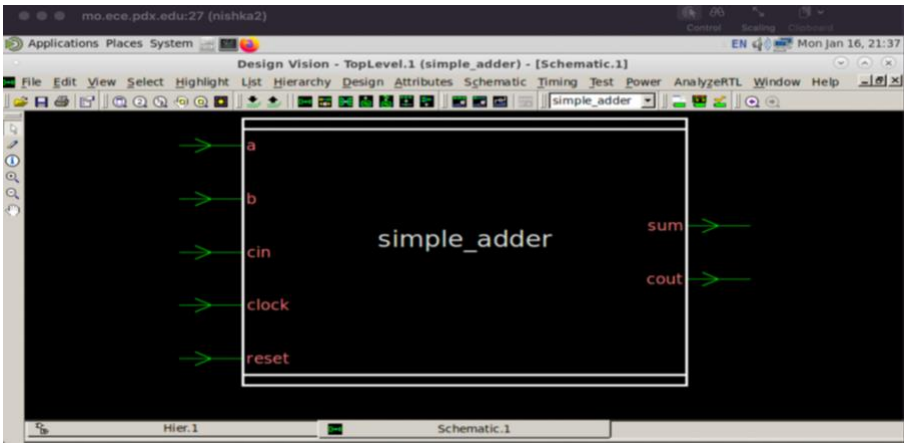
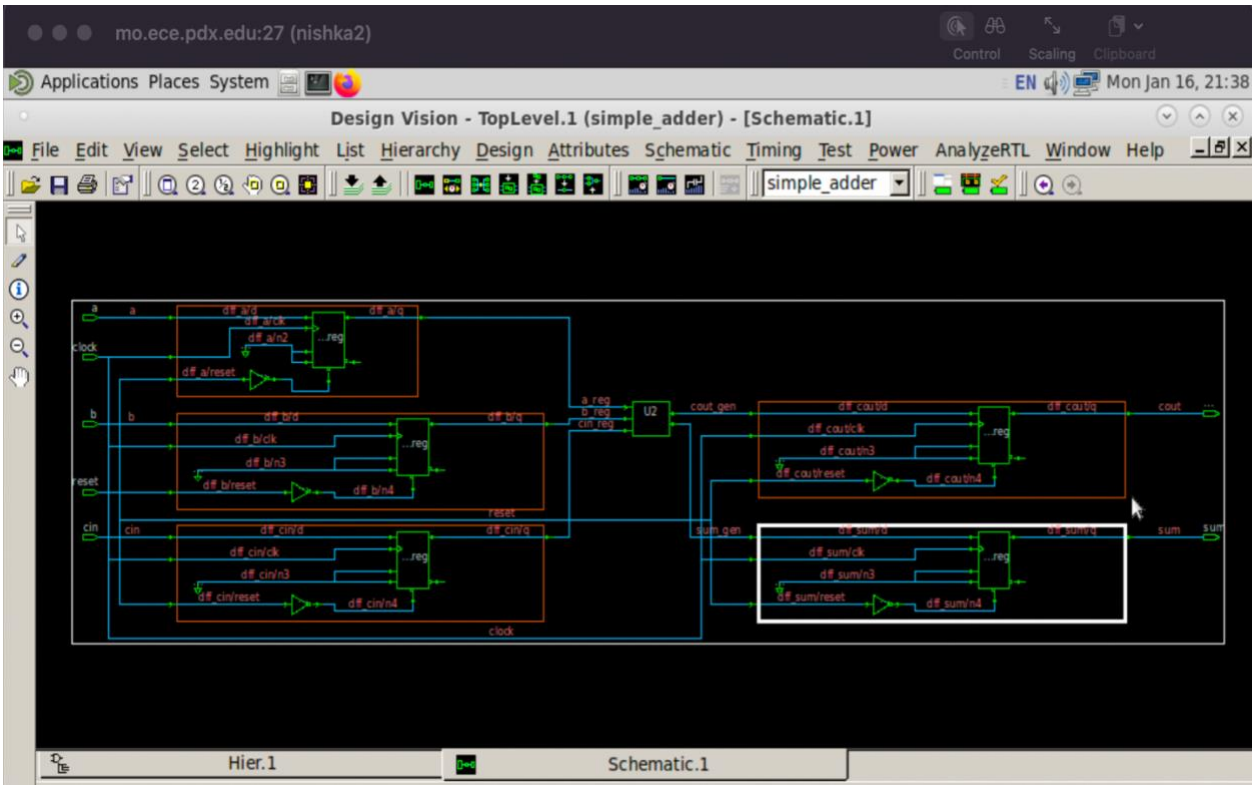
ASIC 481/581 – Lab1

Nishka Sathisha

HW_LAB_1_A:

Schematic Circuit of Simple Adder:





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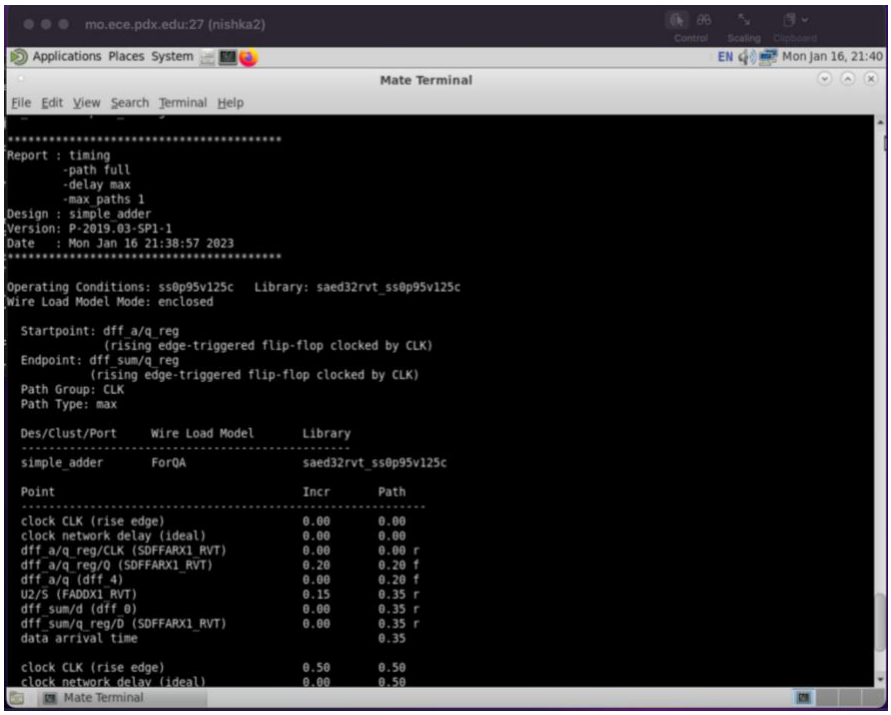
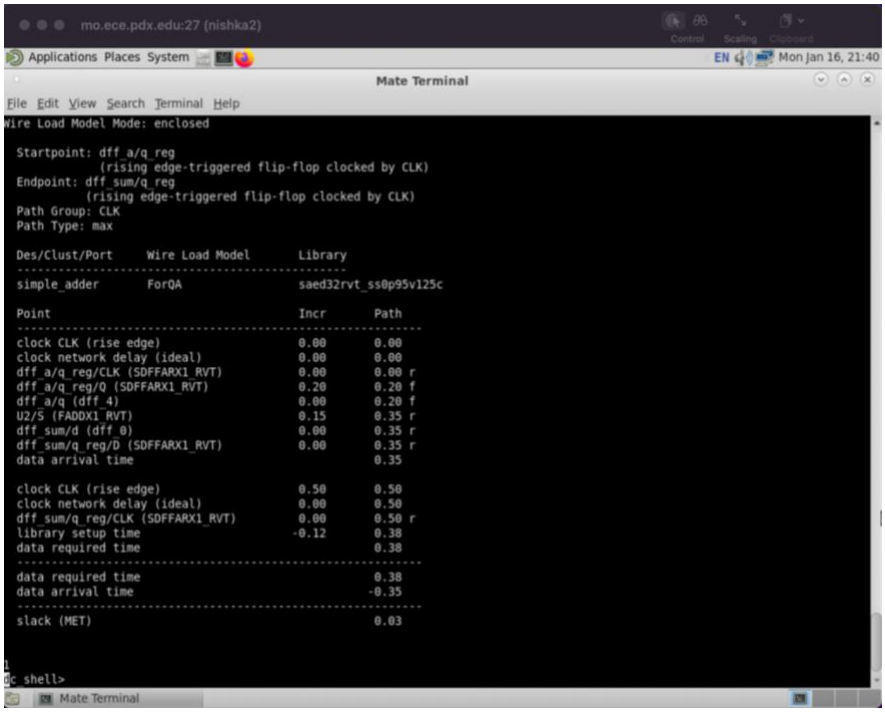
Timing report:





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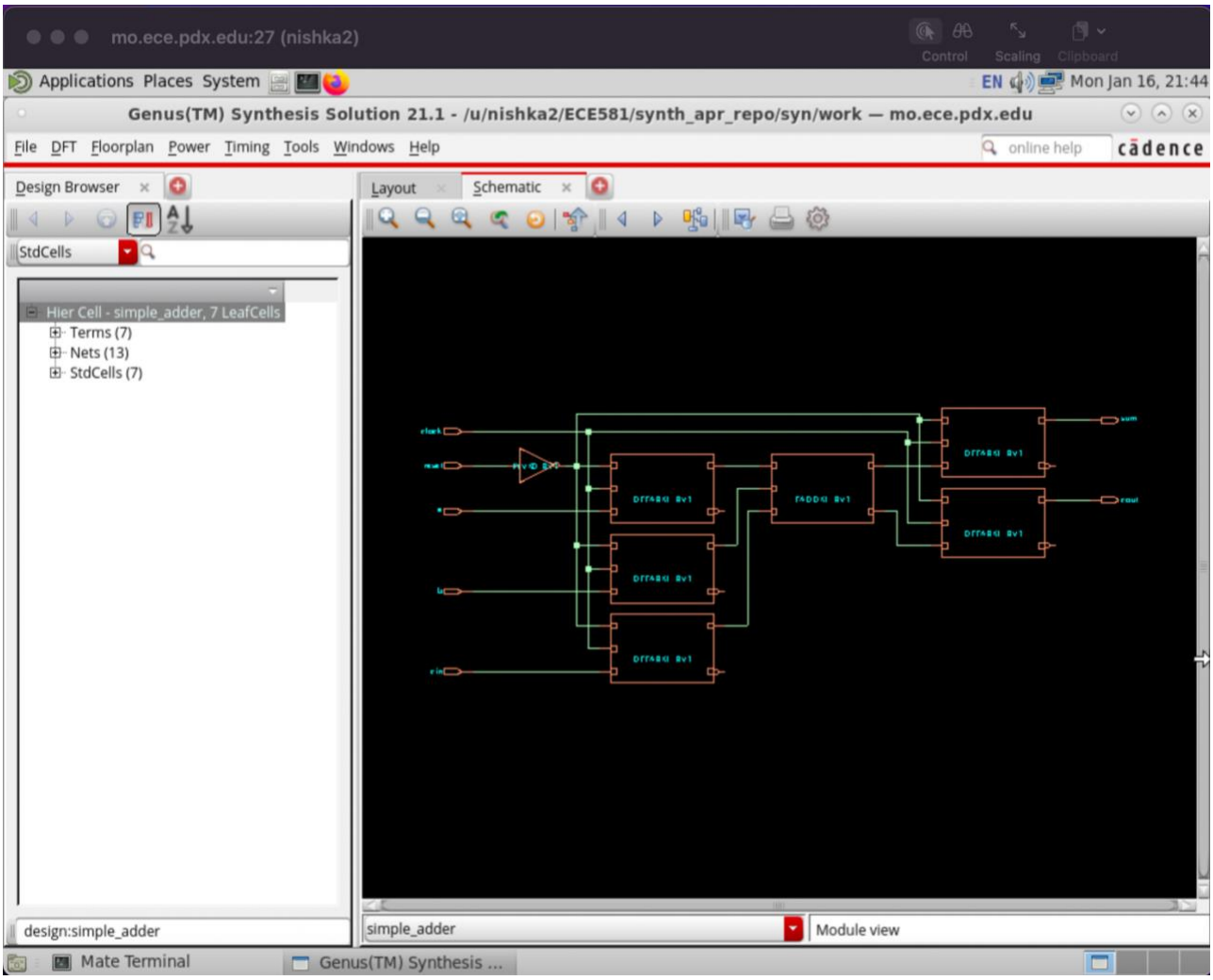
HW_LAB_1_B:

Schematic circuit in Genus



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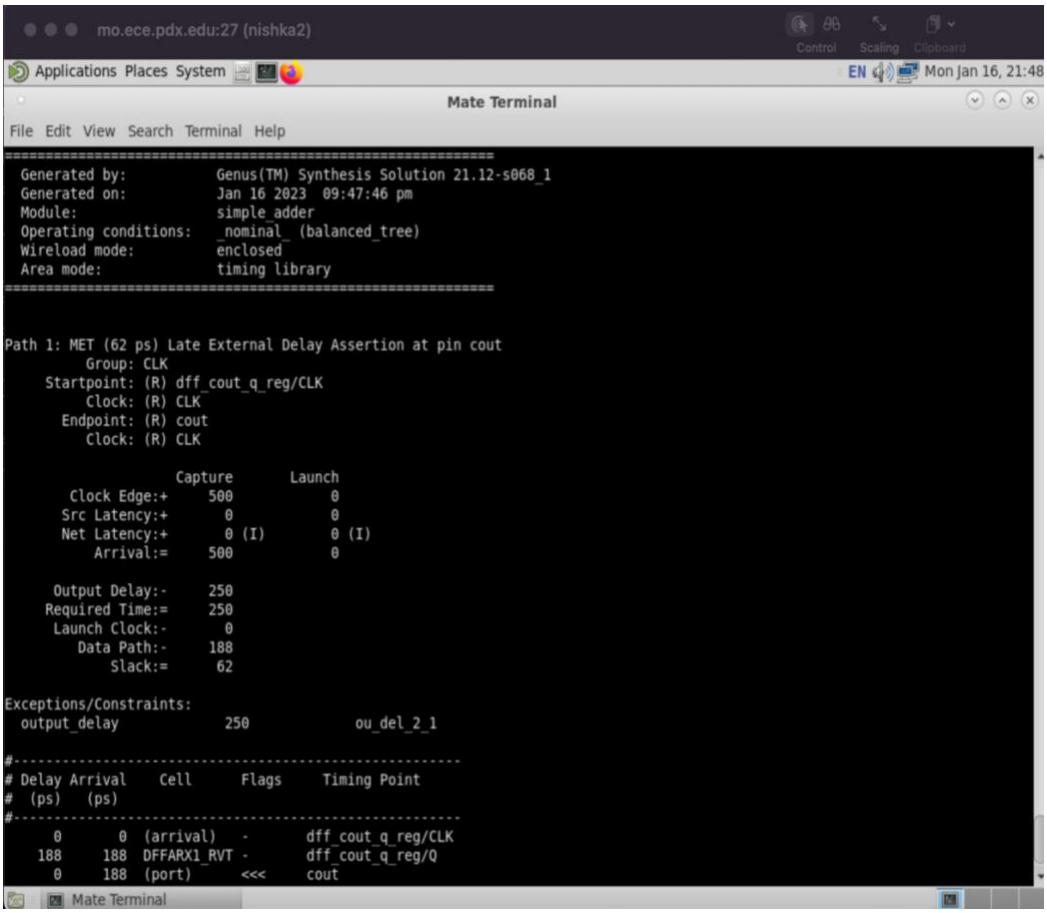
Timing report in Genus:



Comparison Table:

CONSTRAINTS	DC	GENUS
Cell count	11	7
Combinational cell count	6	2
Sequential cell count	5	5
Cell Area	56.928257	41.680
WNS	0	0
TNS	0	0
Violation Count	0	0

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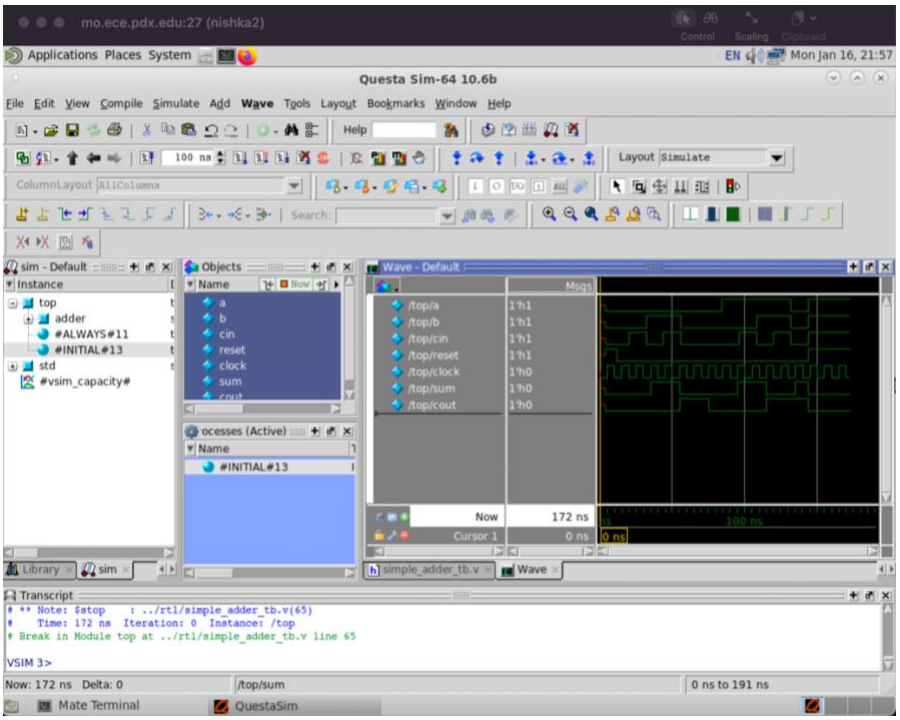
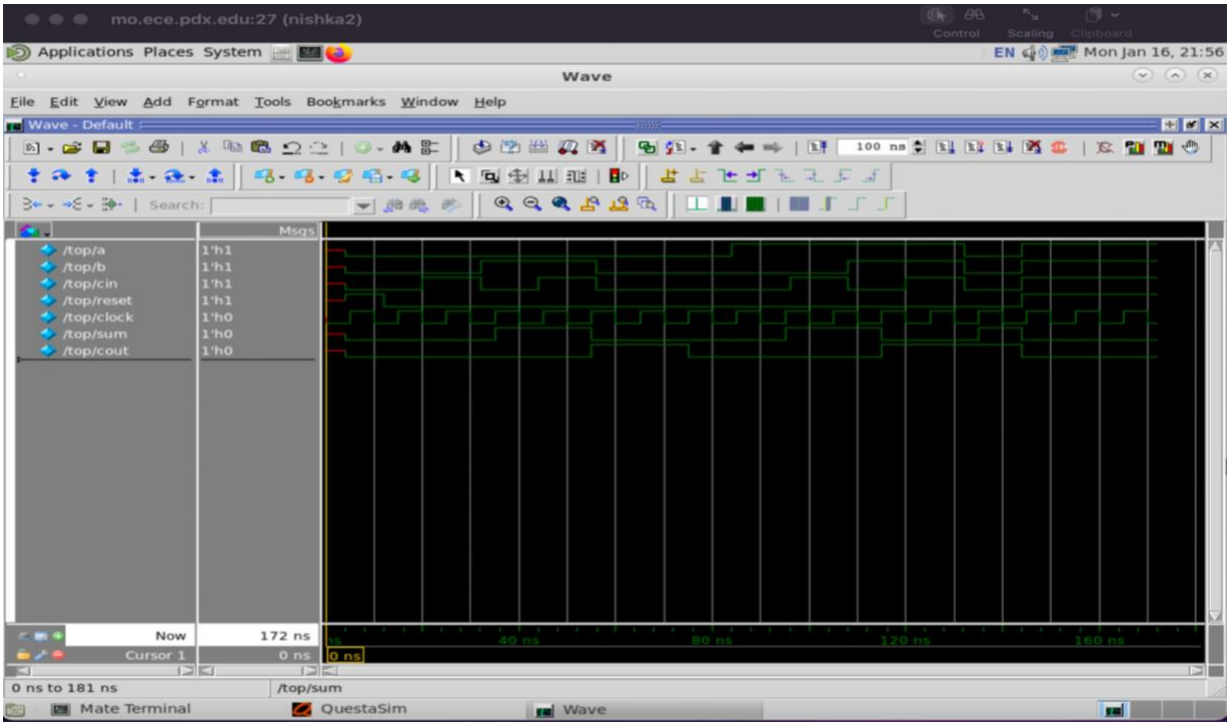
HW_LAB_1_C:

FE RTL WAVEFORM



ZOOMED VIEW:



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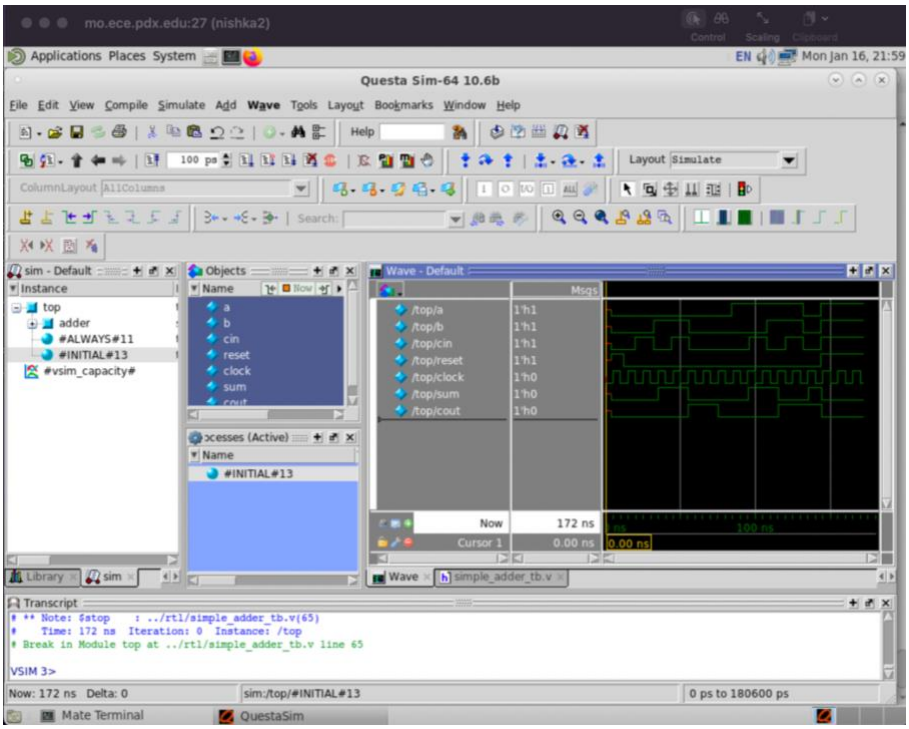
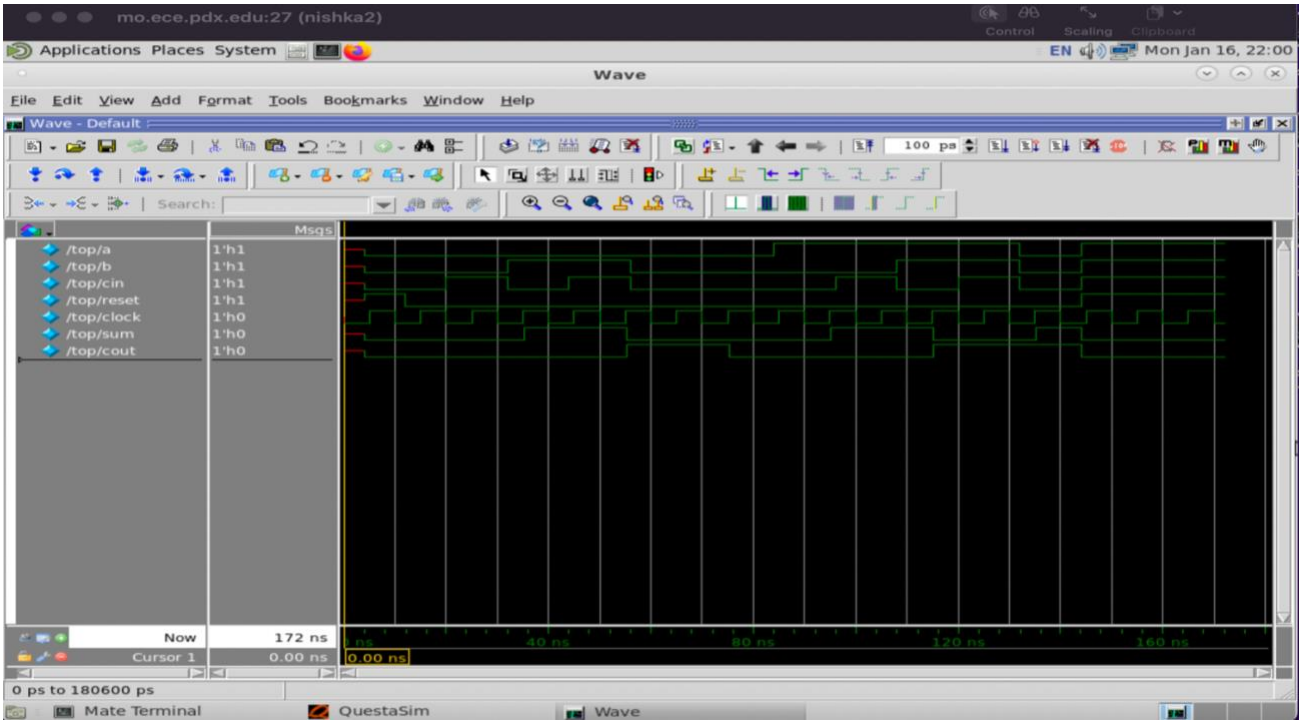
BE Netlist Waveform



Zoomed view



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Comparison statement FE RTL Netlist vs BE RTL Netlist

The waveforms are same for both FE and BE and hence the RTL and generated netlist have similar functionality.

Questa Commands:

vlib: The vlib command creates a design library

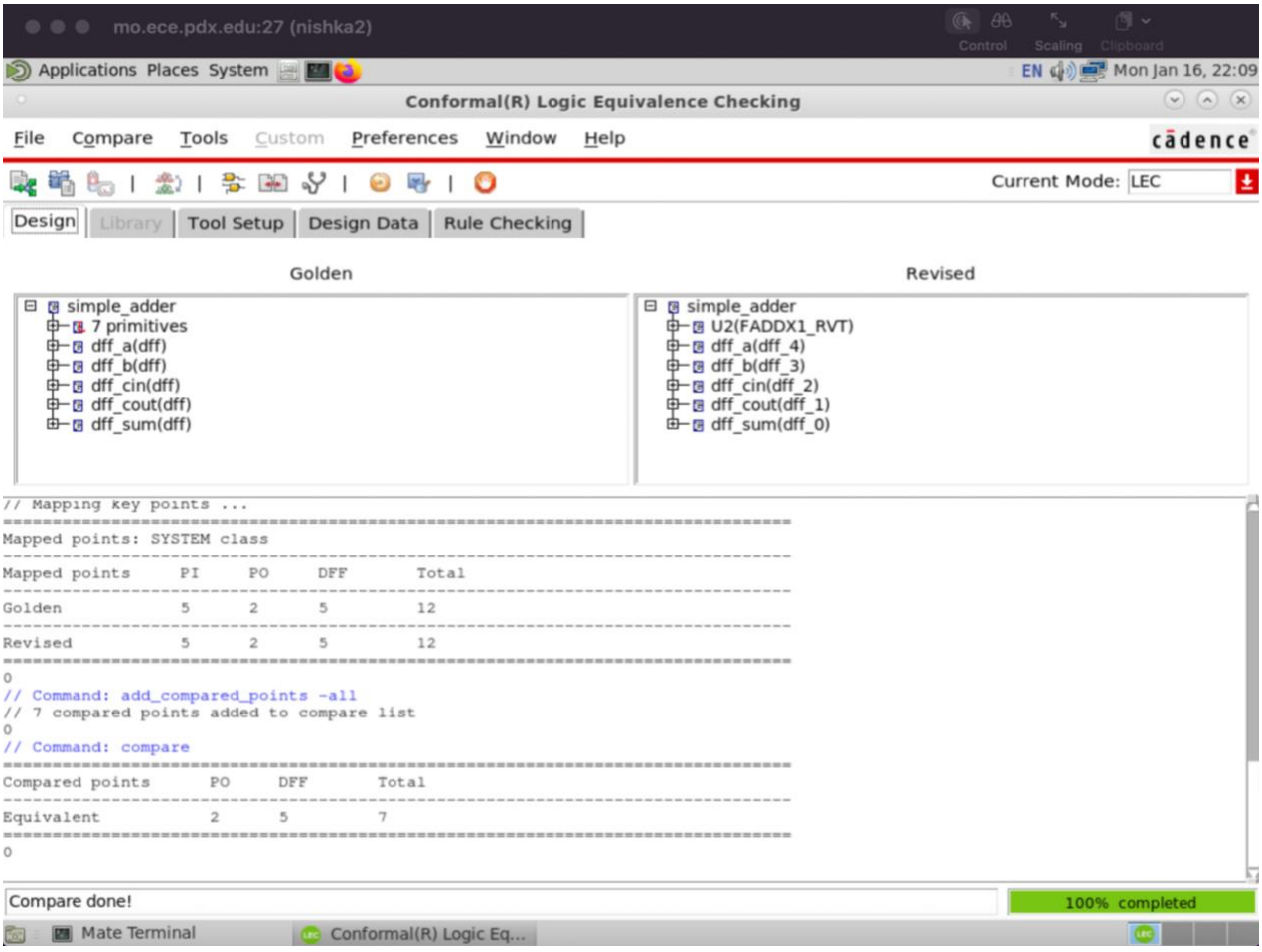
vmap: The vmap command defines a design defines a mapping between a logical library name and a directory

vlog: The vlog compiler invokes the Verilog compiler and compiles all the Verilog files

vsim: The vsim command invokes the VHDL/Questa simulator

HW_LAB_1_D:

LEC equivalency



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LEC Command description:

Lec -tclmode: Lec tool is invoked in tclmode
Lec -dofile: Lec tool is invoked and commands in dofile is executed
read_design: This reads the RTL or netlist, or the library files required for the lec run
set_system_mode: Used to switch system modes
add_compared_points: Used to specify which mapped points the conformal compares.
Compare: This compares the points added in the list and checks whether the key points are equivalent or not.

HW_LAB_1_E:

https://github.com/nishkasathisha/Lab1