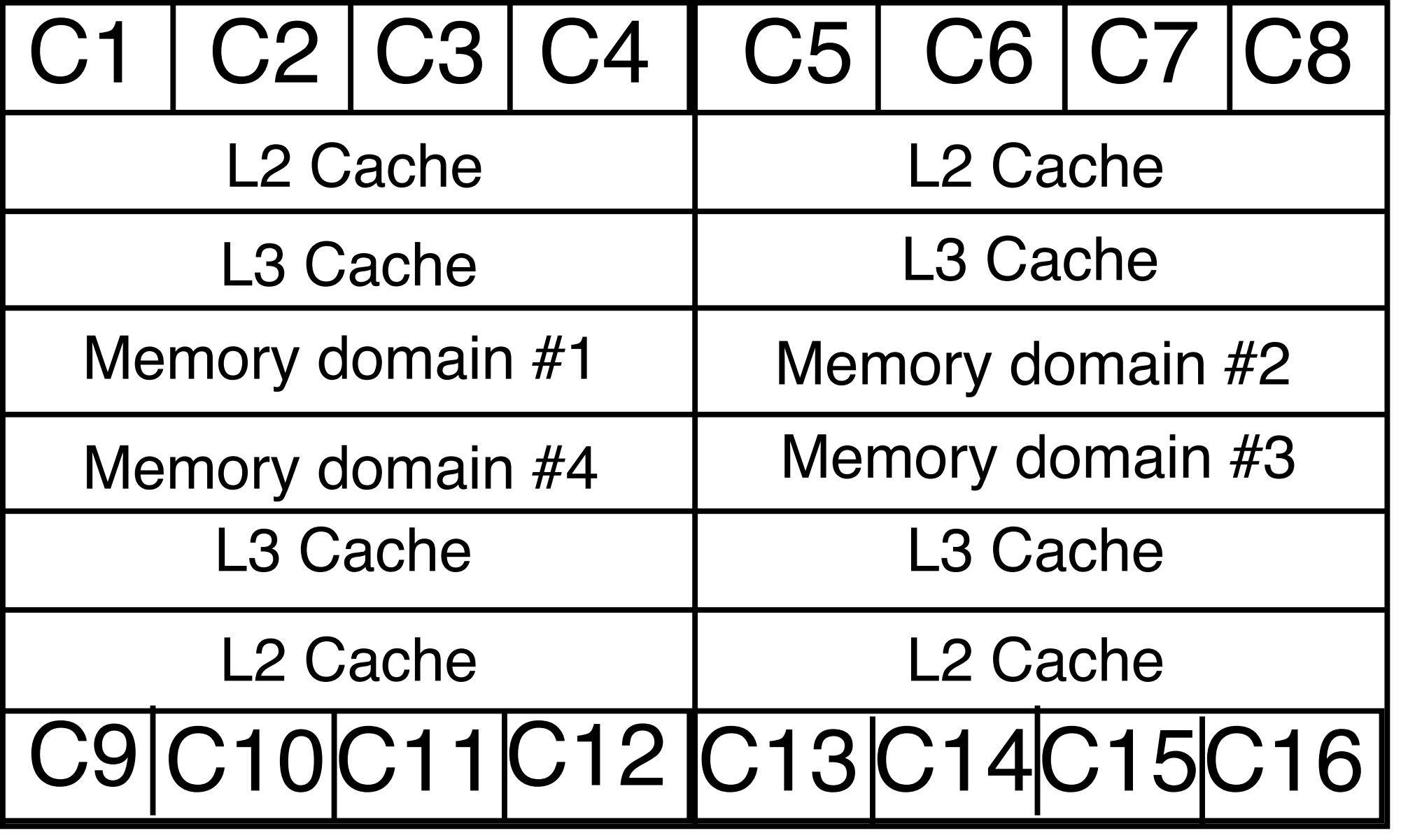
C1
C2
C3
C4
C5
C6
C7
C8
L2 Cache
L2 Cache
L3 Cache
L3 Cache
Memory domain #1
Memory domain #2
Memory domain #4
Memory domain #3
L3 Cache
L3 Cache
L2 Cache
L2 Cache
C9
C10
C11
C12
C13
C14
C15
C16