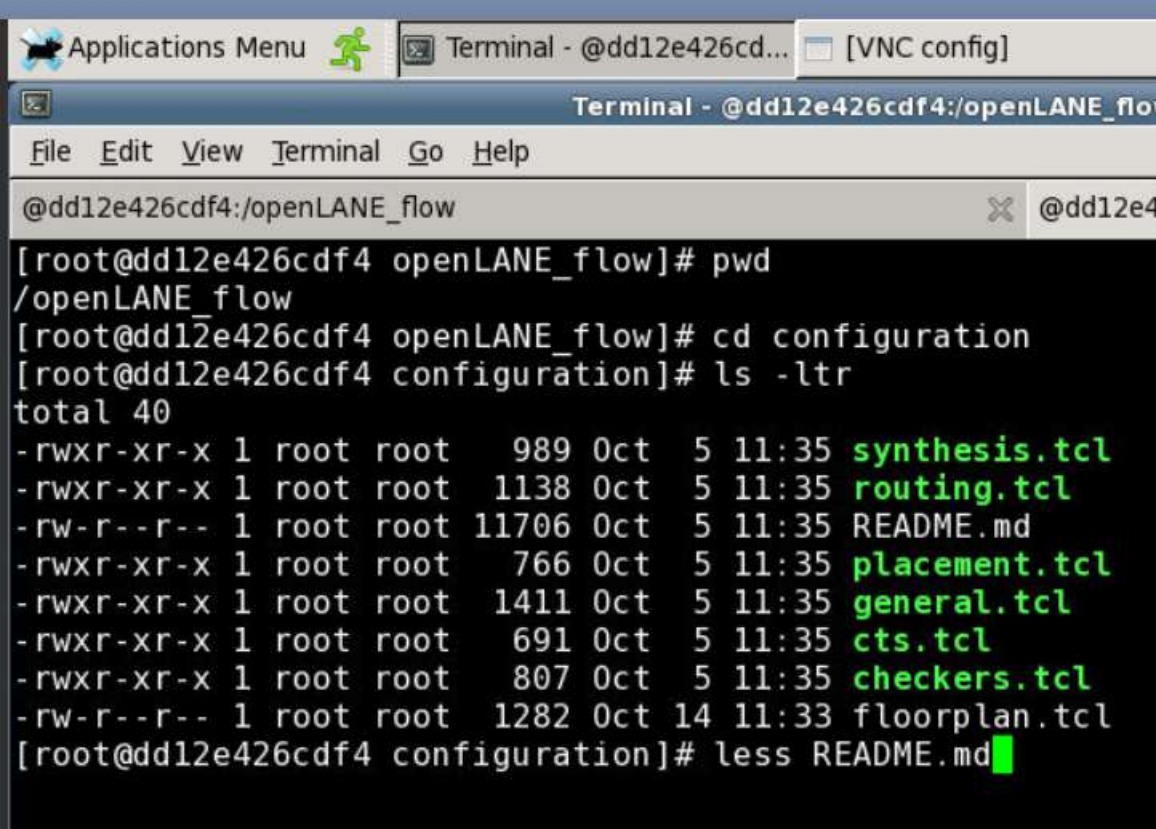

Applications Menu
Terminal - @dd12e426cd...
[VNC config]
Terminal - @dd12e426cdf4:/openLANE_flo
File Edit View Terminal Go Help
@dd12e426cdf4:/openLANE_flow
@dd12e4
[root@dd12e426cdf4 openLANE_flow]# pwd
/openLANE_flow
[root@dd12e426cdf4 openLANE_flow]# cd configuration
[root@dd12e426cdf4 configuration]# ls -ltr
total 40
-rwxr-xr-x 1 root root 989 Oct 5 11:35 synthesis.tcl
-rwxr-xr-x 1 root root 1138 Oct 5 11:35 routing.tcl
-rw-r--r-- 1 root root 11706 Oct 5 11:35 README.md
-rwxr-xr-x 1 root root 766 Oct 5 11:35 placement.tcl
-rwxr-xr-x 1 root root 1411 Oct 5 11:35 general.tcl
-rwxr-xr-x 1 root root 691 Oct 5 11:35 cts.tcl
-rwxr-xr-x 1 root root 807 Oct 5 11:35 checkers.tcl
-rw-r--r-- 1 root root 1282 Oct 14 11:33 floorplan.tcl
[root@dd12e426cdf4 configuration]# less README.md

File Edit View Terminal Go Help

@dd12e426cdf4:/openLANE_flow | @dd12e426cdf4:/openLANE_flow/configuration

```
# Variables information

This page describes configuration variables and their default values.

## Required variables

| Variable      | Description                                                    |
|---------------|----------------------------------------------------------------|
| `DESIGN_NAME`    | The name of the top level module of the design         |
| `VERILOG_FILES`  | The path of the design's verilog files |
| `CLOCK_PERIOD`   | The clock period for the design in ns        |
| `CLOCK_NET` | The name of the Net input to root clock buffer. |
| `CLOCK_PORT`     | The name of the design's clock port    |

## Optional variables

These variables are optional that can be specified in the design configuration file.

### Synthesis

| Variable      | Description                                                            |
|---------------|------------------------------------------------------------------------|
| `LIB_SYNTH` | The library used for synthesis by yosys. <br> (Default: `./pdks/ef-skywater-s8/EFS8A/libs.ref/liberty/efs8hd/efs8hd_tt_1.80v_25C.lib`)|
| `SYNTH_DRIVING_CELL`  | The cell to drive the input ports. <br>(Default: `efs8hd_inv_8`)|
| `SYNTH_DRIVING_CELL_PIN`  | The name of the SYNTH_DRIVING_CELL output pin. <br>(Default: `Y`)|
| `SYNTH_CAP_LOAD` | The capacitive load on the output ports in femtofarads. <br> (Default: `17.65` ff)|
| `SYNTH_MAX_FANOUT`  | The max load that the output ports can drive. <br> (Default: `5` cells) |
| `SYNTH_MAX_TRANS` | The max transition time (slew) from high to low or low to high on cell inputs in ns. Used in synthesis <br> (Default: Calculated at runtime as `10%` of the provided clock period)
|
| `SYNTH_STRATEGY` | Strategies for ab[illegible]nology mapping <br> Possible values are 0, 1 (delay), 2, and 3 (area)<br>
README.md
```

File Edit View Terminal Go Help

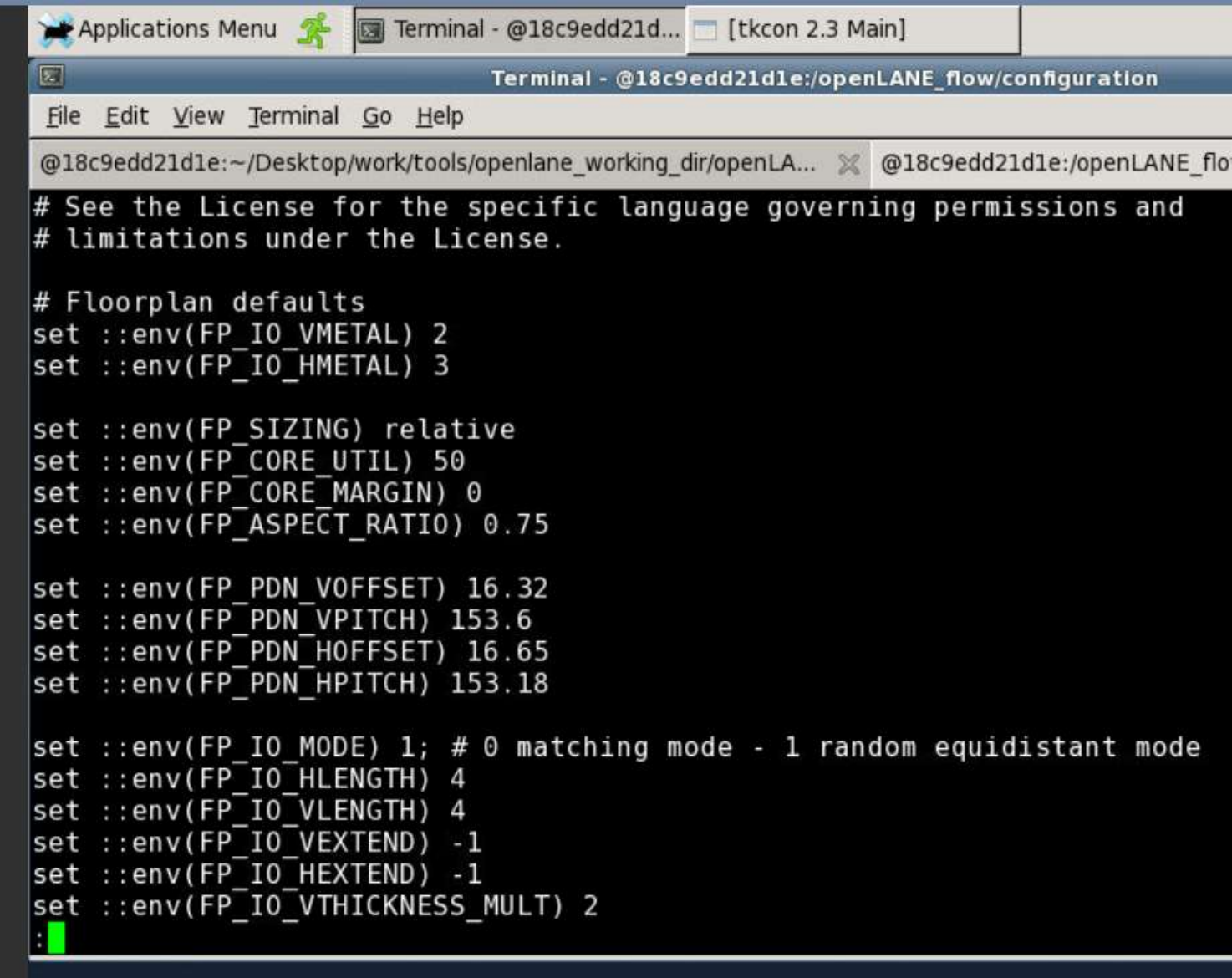
@dd12e426cdf4:/openLANE_flow @dd12e426cdf4:/openLANE_flow/cor

```
# Copyright 2020 Efabless Corporation
#
# Licensed under the Apache License, Version 2.0 (the "License");
# you may not use this file except in compliance with the License.
# You may obtain a copy of the License at
#
#      http://www.apache.org/licenses/LICENSE-2.0
#
# Unless required by applicable law or agreed to in writing, software
# distributed under the License is distributed on an "AS IS" BASIS,
# WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
# See the License for the specific language governing permissions and
# limitations under the License.

# Floorplan defaults
set ::env(FP_IO_VMETAL) 2
set ::env(FP_IO_HMETAL) 3

set ::env(FP_SIZING) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 0.75

set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18

set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 2
floorplan.tcl
```

File Edit View Terminal Go Help

@dd12e426cdf4:/openLANE_flow | @dd12e426cdf4:/

```
set ::env(GLB_RT_ADJUSTMENT) 0.1
set ::env(SYNTH_STRATEGY) 2

#Routing
set ::env(ROUTING_STRATEGY) 0
# Regression
set ::env(FP_CORE_UTIL) 50
set ::env(PL_TARGET_DENSITY) 0.60
set ::env(SYNTH_STRATEGY) 2
set ::env(SYNTH_MAX_FANOUT) 6
set ::env(CLOCK_PERIOD) "10.000"
sky130A_sky130_fd_sc_hd_config.tcl (END)
```


Applications Menu
Terminal - @18c9edd21d...
[tkcon 2.3 Main]
Terminal - @18c9edd21d1e:/openLANE_flow/configuration
File Edit View Terminal Go Help
@18c9edd21d1e:~/Desktop/work/tools/openlane_working_dir/openLA...
@18c9edd21d1e:/openLANE_flo
See the License for the specific language governing permissions and
limitations under the License.
Floorplan defaults
set ::env(FP_IO_VMETAL) 2
set ::env(FP_IO_HMETAL) 3
set ::env(FP_SIZING) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 0.75
set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18
set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 2
:

File Edit View Terminal Go Help

@dd12e426cdf4:/openLANE_flow | @dd12e426cdf4:/openLANE_flow/configuration | @dd12e426cdf4:/openLANE_flow/designs/pic...

```
The LEF parser will ignore this statement.
To avoid this warning in the future, remove this statement from the LEF file with version 5.6 or lat
er. See file /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/merged_unpadded.lef at line 61852
.

Notice 0: Warning: WARNING (LEFPARS-2036): SOURCE statement is obsolete in version 5.6 and later.
The LEF parser will ignore this statement.
To avoid this warning in the future, remove this statement from the LEF file with version 5.6 or lat
er. See file /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/merged_unpadded.lef at line 61950
.

Notice 0:     Created 11 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 437 library cells
Notice 0: Finished LEF file:  /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/merged_unpadded.
lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/floorplan/ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17323 components and 96161 component-terminals.
Notice 0:     Created 17425 nets and 61476 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/floorplan/ioPlace
r.def
Running tapcell...
Step 1: Cut rows...
[INFO] Macro blocks found: 0
[INFO] #Original rows: 288
[INFO] #Cut rows: 0
Step 2: Insert endcaps...
[INFO] #Endcaps inserted: 576
Step 3: Insert tapcells...
[INFO] #Tapcells inserted: 10728
Running tapcell... Done!
```

```
[root@dd12e426cdf4 configuration]# cd ../
[root@dd12e426cdf4 openLANE_flow]# cd designs
[root@dd12e426cdf4 designs]# cd picorv32a
[root@dd12e426cdf4 picorv32a]# ls -ltr
total 12
drwxr-xr-x 2 root root 4096 Oct  5 11:35 src
-rwxr-xr-x 1 root root  267 Oct  5 11:35 sky130A_sky130_fd_sc_hd_config.tcl
-rwxr-xr-x 1 root root  439 Oct  5 11:35 config.tcl
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# less sky130A_sky130_fd_sc_hd_config.tcl
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# leafpad
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# cd runs
[root@dd12e426cdf4 runs]# ls -ltr
total 4
drwxr-xr-x 6 root root 4096 Oct 17 09:32 17-10_09-25
[root@dd12e426cdf4 runs]#
```

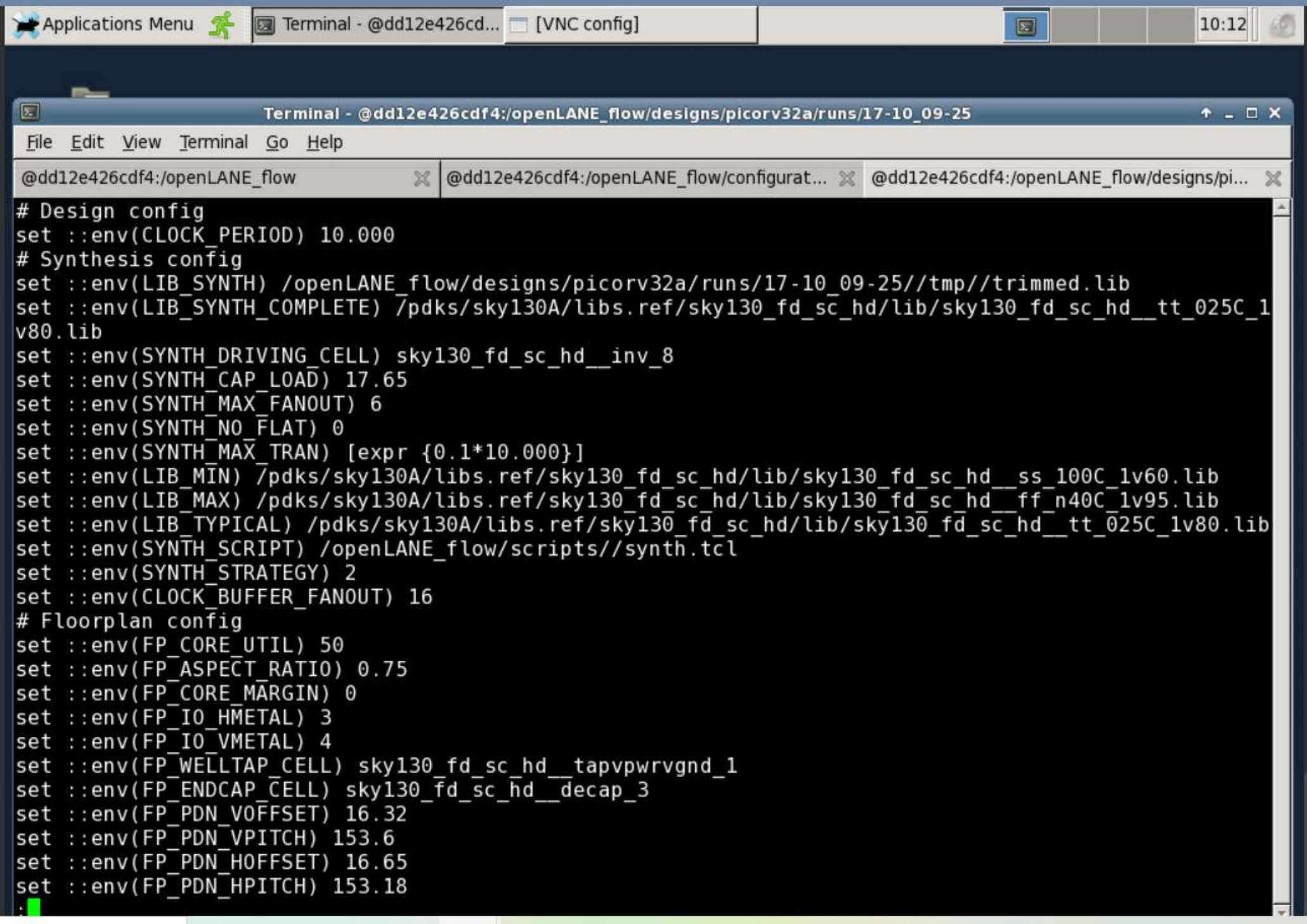
```
[root@dd12e426cdf4 picorv32a]# less config.tcl
[root@dd12e426cdf4 picorv32a]# cd runs
[root@dd12e426cdf4 runs]# ls -ltr
total 4
drwxr-xr-x 6 root root 4096 Oct 17 09:32 17-10_09-25
[root@dd12e426cdf4 runs]# cd 17-10_09-25
[root@dd12e426cdf4 17-10_09-25]# ls -ltr
total 24
drwxr-xr-x 9 root root 4096 Oct 17 09:26 tmp
drwxr-xr-x 9 root root 4096 Oct 17 09:26 results
drwxr-xr-x 9 root root 4096 Oct 17 09:26 reports
drwxr-xr-x 9 root root 4096 Oct 17 09:26 logs
-rw-r--r-- 1 root root 1922 Oct 17 09:32 cmds.log
-rw-r--r-- 1 root root 2939 Oct 17 09:32 config.tcl
[root@dd12e426cdf4 17-10_09-25]# cd logs/floorplan/
[root@dd12e426cdf4 floorplan]# ls -ltr
total 452
-rw-r--r-- 1 root root 146886 Oct 17 09:32 verilog2def.openroad.log
-rw-r--r-- 1 root root     12 Oct 17 09:32 verilog2def_openroad_runtime.txt
-rw-r--r-- 1 root root 147779 Oct 17 09:32 ioPlacer.log
-rw-r--r-- 1 root root     11 Oct 17 09:32 ioPlacer_runtime.txt
-rw-r--r-- 1 root root 151455 Oct 17 09:32 tapcell.log
-rw-r--r-- 1 root root     12 Oct 17 09:32 tapcell_runtime.txt
[root@dd12e426cdf4 floorplan]#
```

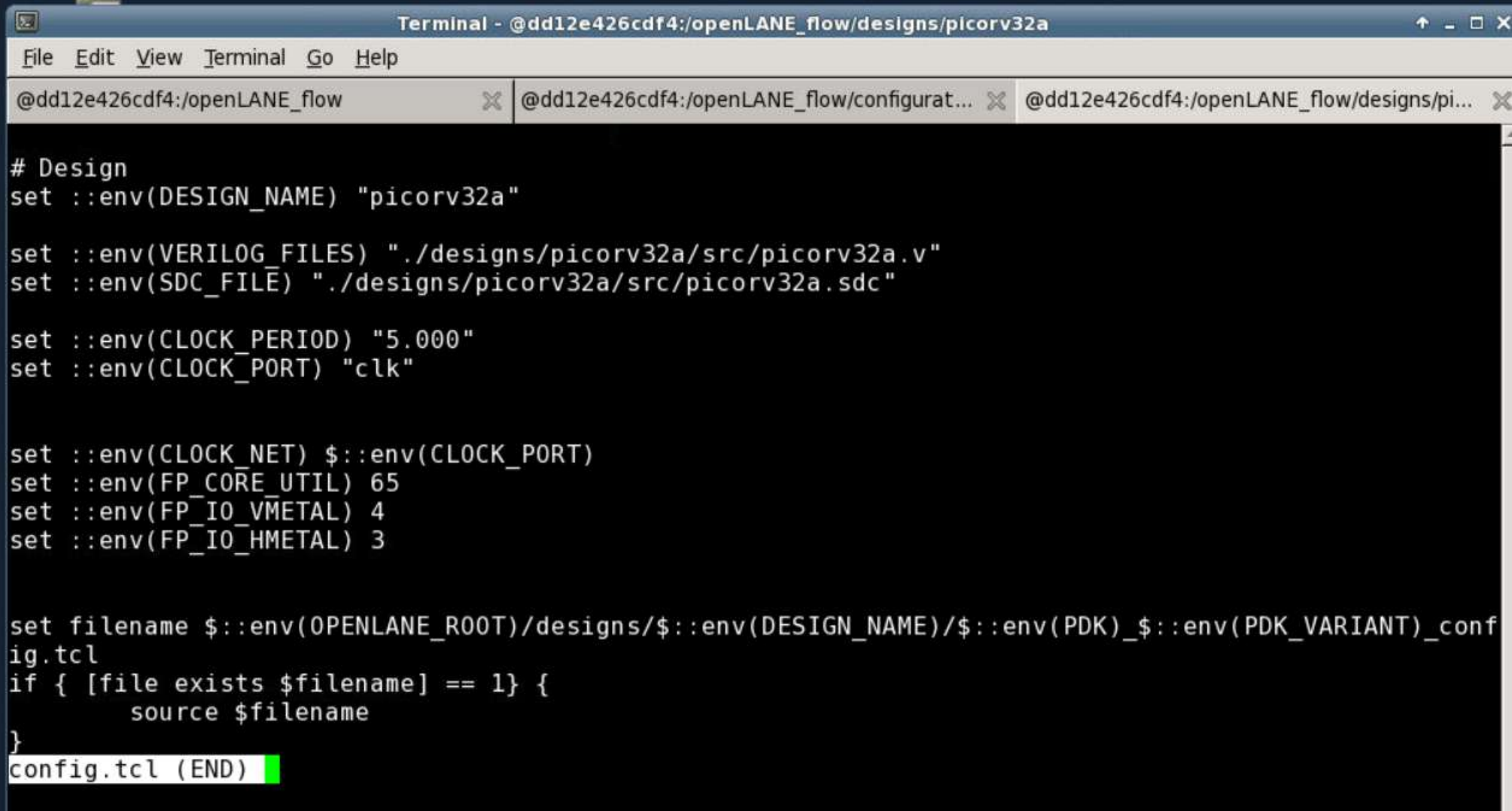
Terminal - @dd12e426cdf4:/openLANE_flow/designs/picorv32a/runs/17-10_09-25/logs/floorplan

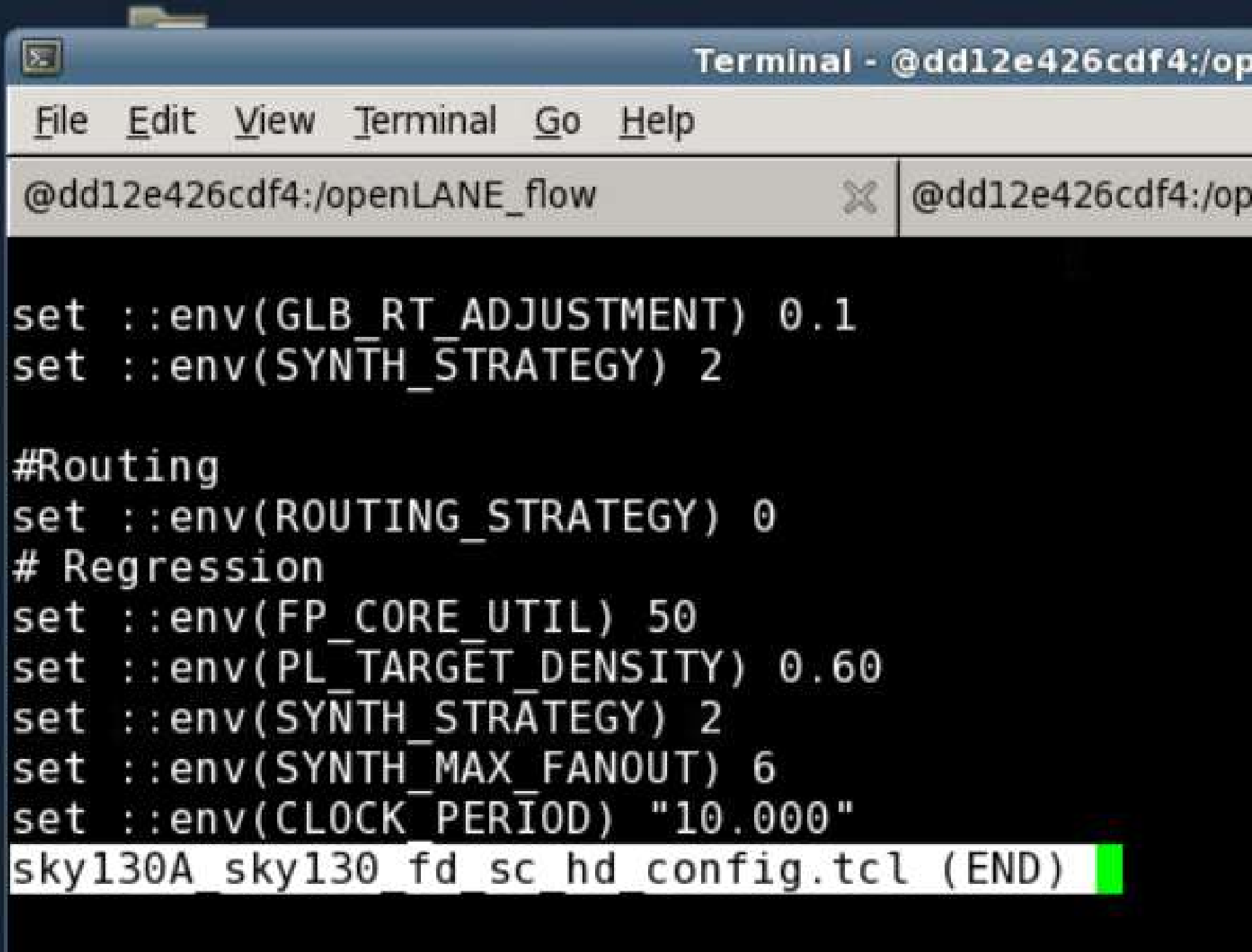
File Edit View Terminal Go Help

@dd12e426cdf4:/openLANE_flow | @dd12e426cdf4:/openLANE_flow/configuration | @dd12e426cdf4:/openLANE_flow/designs/pic...

```
The LEF parser will ignore this statement.
To avoid this warning in the future, remove this statement from the LEF file with version 5.6 or lat
er. See file /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/merged.lef at line 61950.

Notice 0:     Created 11 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 437 library cells
Notice 0: Finished LEF file:  /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/floorplan/verilog2def_openro
ad.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17323 components and 96161 component-terminals.
Notice 0:     Created 17425 nets and 61476 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/17-10_09-25/tmp/floorplan/verilog
2def_openroad.def
[INFO]: Vertical Metal Layer: 5
[INFO]: Horizontal Metal Layer: 4
WARNING: force pin spread option has no effect when using random pin placement
 > Running IO placement
 * Num of slots          4668
 * Num of I/O            409
 * Num of I/O w/sink     374
 * Num of I/O w/o sink   35
 * Slots Per Section     200
 * Slots Increase Factor 0.01
 * Usage Per Section     0.8
 * Usage Increase Factor 0.01
 * Force Pin Spread      1

WARNING: running random pin placement
```


Applications Menu
Terminal - @dd12e426cd...
[VNC config]
10:12
Terminal - @dd12e426cdf4:/openLANE_flow/designs/picorv32a/runs/17-10_09-25
File Edit View Terminal Go Help
@dd12e426cdf4:/openLANE_flow
@dd12e426cdf4:/openLANE_flow/configurat...
@dd12e426cdf4:/openLANE_flow/designs/pi...
Design config
set ::env(CLOCK_PERIOD) 10.000
Synthesis config
set ::env(LIB_SYNTH) /openLANE_flow/designs/picorv32a/runs/17-10_09-25//tmp//trimmed.lib
set ::env(LIB_SYNTH_COMPLETE) /pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1
v80.lib
set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd__inv_8
set ::env(SYNTH_CAP_LOAD) 17.65
set ::env(SYNTH_MAX_FANOUT) 6
set ::env(SYNTH_NO_FLAT) 0
set ::env(SYNTH_MAX_TRAN) [expr {0.1*10.000}]
set ::env(LIB_MIN) /pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib
set ::env(LIB_MAX) /pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib
set ::env(LIB_TYPICAL) /pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
set ::env(SYNTH_SCRIPT) /openLANE_flow/scripts//synth.tcl
set ::env(SYNTH_STRATEGY) 2
set ::env(CLOCK_BUFFER_FANOUT) 16
Floorplan config
set ::env(FP_CORE_UTIL) 50
set ::env(FP_ASPECT_RATIO) 0.75
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_IO_HMETAL) 3
set ::env(FP_IO_VMETAL) 4
set ::env(FP_WELLTAP_CELL) sky130_fd_sc_hd__tapvpwrvgnd_1
set ::env(FP_ENDCAP_CELL) sky130_fd_sc_hd__decap_3
set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18


Terminal - @dd12e426cdf4:/openLANE_flow/designs/picorv32a
File Edit View Terminal Go Help
@dd12e426cdf4:/openLANE_flow
@dd12e426cdf4:/openLANE_flow/configurat...
@dd12e426cdf4:/openLANE_flow/designs/pi...
Design
set ::env(DESIGN_NAME) "picorv32a"
set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"
set ::env(CLOCK_PERIOD) "5.000"
set ::env(CLOCK_PORT) "clk"
set ::env(CLOCK_NET) $::env(CLOCK_PORT)
set ::env(FP_CORE_UTIL) 65
set ::env(FP_IO_VMETAL) 4
set ::env(FP_IO_HMETAL) 3
set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(PDK_VARIANT)_conf
ig.tcl
if { [file exists $filename] == 1} {
source $filename
}
config.tcl (END)


Terminal - @dd12e426cdf4:/op
File Edit View Terminal Go Help
@dd12e426cdf4:/openLANE_flow
@dd12e426cdf4:/op
set ::env(GLB_RT_ADJUSTMENT) 0.1
set ::env(SYNTH_STRATEGY) 2
#Routing
set ::env(ROUTING_STRATEGY) 0
Regression
set ::env(FP_CORE_UTIL) 50
set ::env(PL_TARGET_DENSITY) 0.60
set ::env(SYNTH_STRATEGY) 2
set ::env(SYNTH_MAX_FANOUT) 6
set ::env(CLOCK_PERIOD) "10.000"
sky130A_sky130_fd_sc_hd_config.tcl (END)

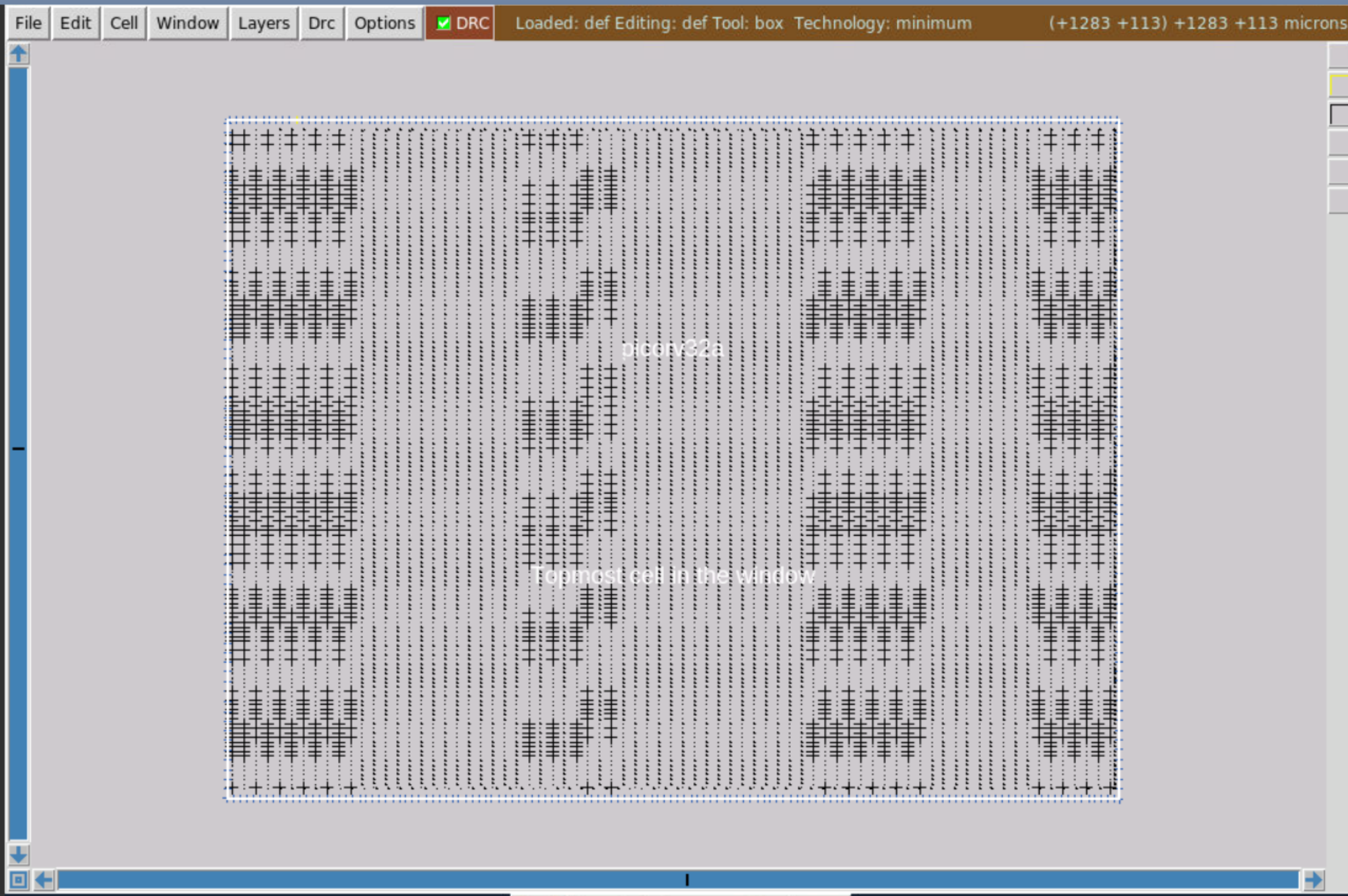
Terminal - @dd12e426cdf4:/openLANE_flow/designs/picorv32a/runs/

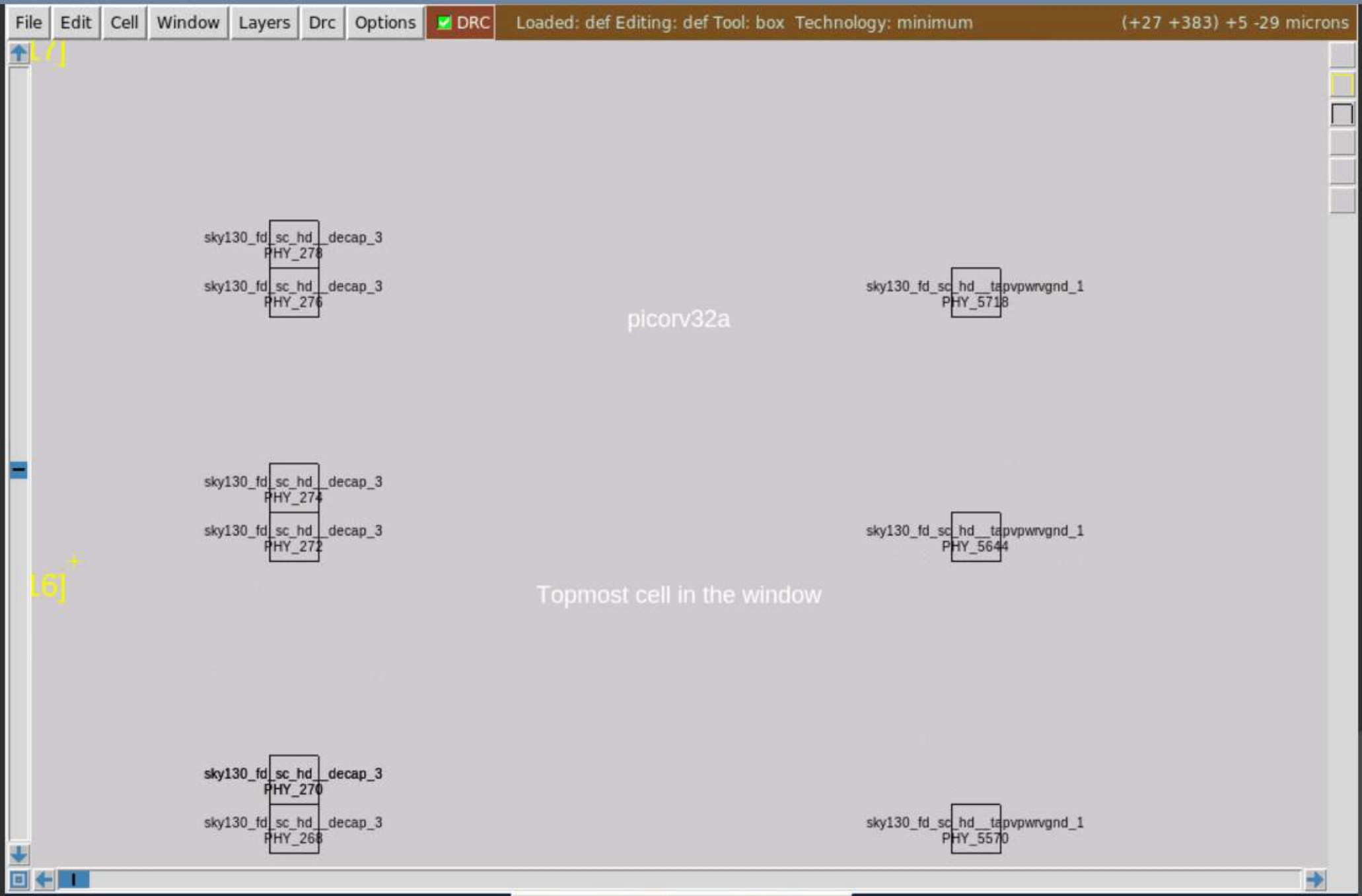
File Edit View Terminal Go Help

@dd12e426cdf4:/openLANE_flow | @dd12e426cdf4:/openLANE_flow/configu

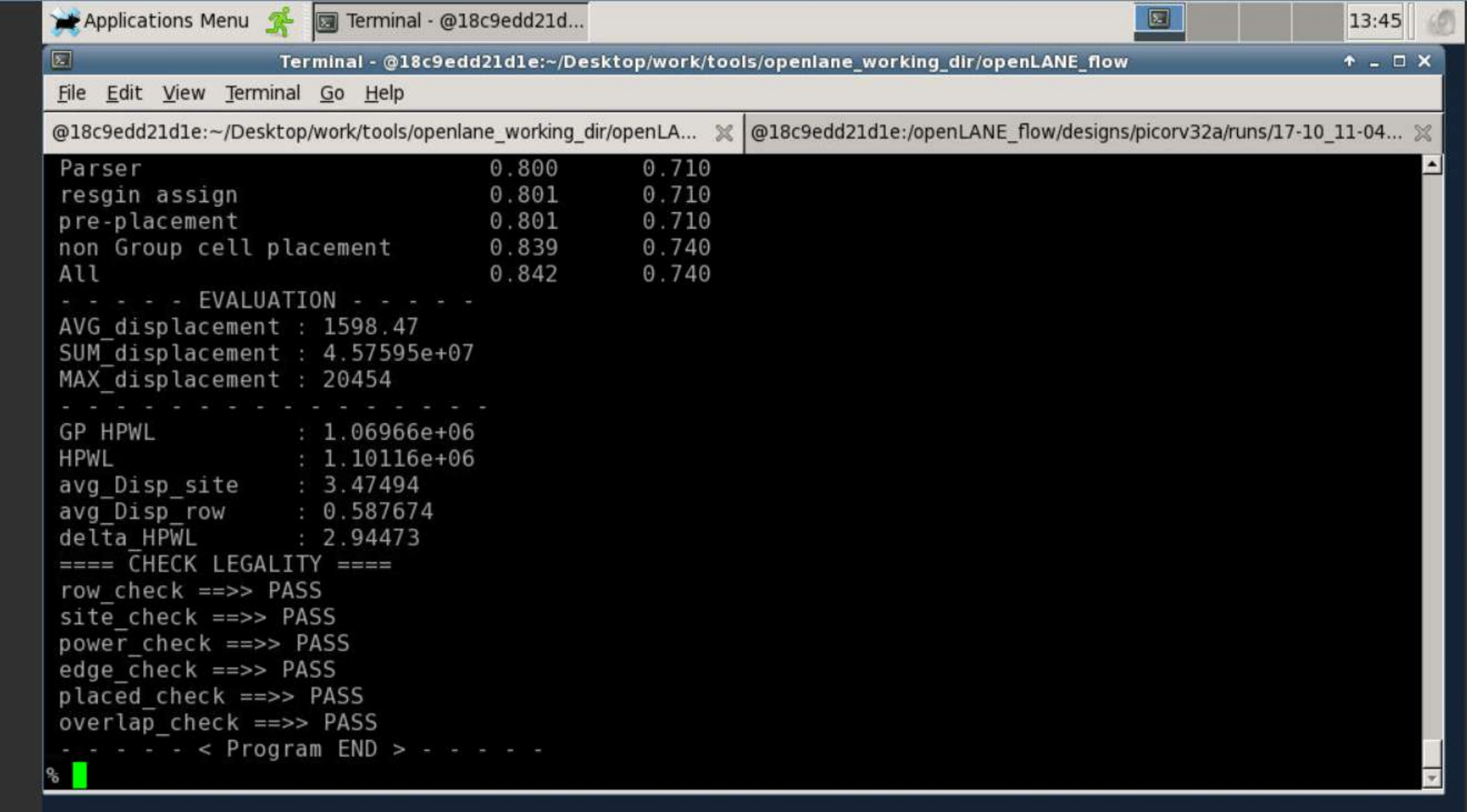
```
VERSION 5.8 ;
NAMESCASESENSITIVE ON ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;
DESIGN picorv32a ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 1057235 806405 ) ;
ROW ROW_0 unithd 5520 10880 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_1 unithd 5520 13600 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_2 unithd 5520 16320 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_3 unithd 5520 19040 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_4 unithd 5520 21760 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_5 unithd 5520 24480 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_6 unithd 5520 27200 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_7 unithd 5520 29920 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_8 unithd 5520 32640 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_9 unithd 5520 35360 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_10 unithd 5520 38080 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_11 unithd 5520 40800 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_12 unithd 5520 43520 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_13 unithd 5520 46240 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_14 unithd 5520 48960 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_15 unithd 5520 51680 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_16 unithd 5520 54400 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_17 unithd 5520 57120 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_18 unithd 5520 59840 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_19 unithd 5520 62560 N DO 2274 BY 1 STEP 460 0 ;
ROW ROW_20 unithd 5520 65280 FS DO 2274 BY 1 STEP 460 0 ;
ROW ROW_21 unithd 5520 68000 N DO 2274 BY 1 STEP 460 0 ;
picorv32a.floorplan.def
```

```
[root@18c9edd21d1e 17-10_11-04]# cd logs/floorplan/
[root@18c9edd21d1e floorplan]# ls -ltr
total 452
-rw-r--r-- 1 root root 146886 Oct 17 11:24 verilog2def.openroad.log
-rw-r--r-- 1 root root     12 Oct 17 11:24 verilog2def_openroad_runtime.txt
-rw-r--r-- 1 root root 147779 Oct 17 11:24 ioPlacer.log
-rw-r--r-- 1 root root     11 Oct 17 11:24 ioPlacer_runtime.txt
-rw-r--r-- 1 root root 151455 Oct 17 11:24 tapcell.log
-rw-r--r-- 1 root root     12 Oct 17 11:24 tapcell_runtime.txt
[root@18c9edd21d1e floorplan]# cd ../
[root@18c9edd21d1e logs]# cd ../
[root@18c9edd21d1e 17-10_11-04]# cd results/floorplan/
[root@18c9edd21d1e floorplan]# ls -ltr
total 2992
-rw-r--r-- 1 root root 3061515 Oct 17 11:24 picorv32a.floorplan.def
[root@18c9edd21d1e floorplan]# cd picorv32a.floorplan.def
bash: cd: picorv32a.floorplan.def: Not a directory
[root@18c9edd21d1e floorplan]# less picorv32a.floorplan.def
[root@18c9edd21d1e floorplan]# magic -T /openlane_working_dir/pdks/skywater130A/libs.tech/magic/sky
130A.tech lef read ../../tmp/merged.lef read def picorv32a.floorplan.def &
[1] 10453
[root@18c9edd21d1e floorplan]#
```


File
Edit
Cell
Window
Layers
Drc
Options
DRC
Loaded: def Editing: def Tool: box Technology: minimum
(+1283 +113) +1283 +113 microns
picorv32a
Topmost cell in the window


File
Edit
Cell
Window
Layers
Drc
Options
DRC
Loaded: def Editing: def Tool: box Technology: minimum
(+27 +383) +5 -29 microns
sky130_fd_sc_hd__decap_3
PHY_278
sky130_fd_sc_hd__decap_3
PHY_276
sky130_fd_sc_hd__tapvpwrvgnd_1
PHY_5718
picorv32a
sky130_fd_sc_hd__decap_3
PHY_274
sky130_fd_sc_hd__decap_3
PHY_272
sky130_fd_sc_hd__tapvpwrvgnd_1
PHY_5644
Topmost cell in the window
sky130_fd_sc_hd__decap_3
PHY_270
sky130_fd_sc_hd__decap_3
PHY_268
sky130_fd_sc_hd__tapvpwrvgnd_1
PHY_5570


File
Edit
Cell
Window
Layers
Drc
Options
DRC
Loaded: def Editing: def Tool: box Technology: minimum
(+2 +0) +2 +0 microns
mem_rdata[26]


Applications Menu
Terminal - @18c9edd21d...
13:45
Terminal - @18c9edd21d1e:~/Desktop/work/tools/openlane_working_dir/openLANE_flow
File Edit View Terminal Go Help
@18c9edd21d1e:~/Desktop/work/tools/openlane_working_dir/openLA...
@18c9edd21d1e:/openLANE_flow/designs/picorv32a/runs/17-10_11-04...
Parser 0.800 0.710
resgin assign 0.801 0.710
pre-placement 0.801 0.710
non Group cell placement 0.839 0.740
All 0.842 0.740
- - - - - EVALUATION - - - - -
AVG_displacement : 1598.47
SUM_displacement : 4.57595e+07
MAX_displacement : 20454
- - - - - - - - - - - - - - - - - -
GP HPWL : 1.06966e+06
HPWL : 1.10116e+06
avg_Disp_site : 3.47494
avg_Disp_row : 0.587674
delta_HPWL : 2.94473
==== CHECK LEGALITY ====
row_check ==>> PASS
site_check ==>> PASS
power_check ==>> PASS
edge_check ==>> PASS
placed_check ==>> PASS
overlap_check ==>> PASS
- - - - - < Program END > - - - - -
%