`timescale 1ns / 1ps

/\*\*

\* counter: a generic clearable up-counter

\*/

module counter

#(parameter WIDTH=64)

(

input clk,

input ce,

input arst\_n,

output reg [WIDTH-1:0] q

);

// some child

clock\_buffer #(WIDTH) buffer\_inst (

.clk(clk),

.ce(ce),

.reset(arst\_n)

);

// Simple gated up-counter with async clear

always @(posedge clk or negedge arst\_n) begin

if (arst\_n == 1'b0) begin

q <= {WIDTH {1'b0}};

end

else begin

q <= q;

if (ce == 1'b1) begin

q <= q + 1;

end

end

end

endmodule